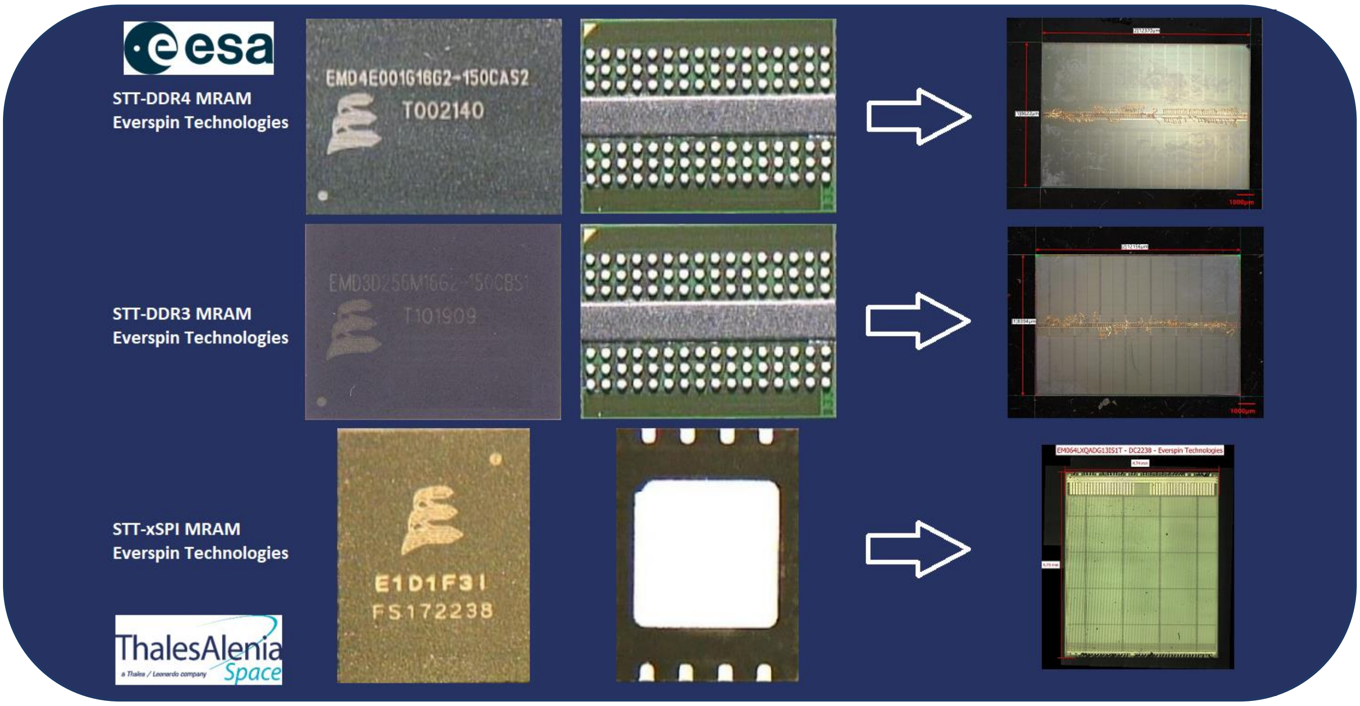
→ DISCOVERY



Evaluation of Spintransfer Torque DDR MRAM in Space Environment

Executive Summary Report

Activity type : Early Technology Development

OSIP NEW IDEAS FOR THE USE OF COMMERCIAL OFF THE SHELF (COTS) COMPONENTS CAMPAIGN

Affiliation(s): Thales Alenia Space France (Prime), Alter Technology TUV Nord France SAS (Sub 1), TRAD – Test et Radiations (Sub 2)

Activity summary:

The “Evaluation of Spintransfer Torque DDR MRAM in Space Environment” takes place in the OSIP “New ideas for the use of Commercial Off The Shelf (COTS) components” campaign as an Early Technology Development of ESA. The aim is to evaluate the Spin-transfer Torque DDR Magnetic Random Access Memory (MRAM) from EVERSPIN in radiation environment in both SEE (Single Event Effect) and TID (Total Ionizing Dose) since having such MRAM available for Space Application could be a real benefit for improving the performances of future designs since these memories are 256Mb and 1Gb MRAM whereas available HiRel MRAM reach only 64Mb.

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1 Introduction

1.1 Scope and purpose

MRAM (Magnetic Random Access Memory) technology is very interesting for space use since:

- MRAM could replace both non-volatile memories (EEPROM, NOR & NAND Flash, …) and volatile memories due to its fast writes (SRAM or even DRAM…)
- MRAM technology has a very high endurance (>1e10 cycles when Flash and EEPROM technologies are limited to about 10 000 or 100 000 cycles)
- MRAM technology is known to have a good withstanding in TID, to have a memory cell SEU immune and some MRAM from EVERSPIN technologies are already SEL immune.

All MRAM evaluated here are in Spin-Transfer Torque technology (STT-MRAM) using deep-submicron nodes.
This Everspin’s newest MRAM technology use the spin torque transfer property, which is the manipulation of the spin of electrons with a polarizing current, to establish the desired magnetic state of the free layer to program, or write, the bits in the memory array.
STT-MRAM provides a significant reduction in switching energy compared to Toggle MRAM, and is highly scalable, enabling higher density memory products. This third generation of MRAM technology uses a Perpendicular MTJ (Magnetic-Tunnel Junction).
These products perform like a persistent DRAM but with no refresh required.

1.2 Project summary

In this project, the following EVERSPIN STT-DDR MRAM have been evaluated :

Type	Manufacturer	Part Number	Size	Evaluated in
STT-DDR3 MRAM	EVERSPIN Technologies	EMD3D256M16G2-150CBS1	256Mb	TID
STT-DDR4 MRAM	EVERSPIN Technologies	EMD4E001G16G2-150CAS2	1Gb	SEE and TID
STT-xSPI MRAM	EVERSPIN Technologies	EM064LXQADG13IS1T	64Mb	SEE

1.3 Reference documents

Reference	Title and revision
RD[1]	ESCC Basic specification No. 25100 Issue 2 of October 2014
RD[2]	ESCC Basic specification No. 22900 Issue 5 of June 2016
RD[3]	Datasheet: EMD4E011GAS2, Rev. 1.2 by Everspin Technologies dated August 2020
RD[4]	Datasheet: EMD3D256MxxBS1, Rev 1.3 by Everspin Technologies dated October 2018
RD[5]	Datasheet: EMxxLX v2.9, by Everspin Technologies dated december 2022
RD[6]	TRAD_TI_EMD4E001G_XXX1_ASI_PC_2203, rev2 by TRAD dated March 2024
RD[7]	TRAD_TI_EM064LXQADG13_2238_ASI_AAY_2306, rev1 by TRAD dated December 2023
RD[8]	HRX/TID/02079 Issue 01 by ALTER Technology dated December 2023
RD[9]	HRX/TID/02080 Issue 01 by ALTER Technology dated December 2023

2 Methodology and Results

2.1 Methodology

2.1.1 SEE testing

SEE testing has been performed at RADEF Heavy ion test facility.
With respect to reference documents RD[1]; RD[3] and RD[5], runs were performed:

- Up to a fluence of 1E+7 cm-2 with only SEL monitoring.
- Up to a fluence of 1E+6 cm-2 for the SEU, MBU, Burst and SEFI detection.

2.1.1.1 *STT-DDR4 MRAM*

Part designation	EMD4E001G16G2-150CAS2
Manufacturer	Everspin Technologies
Part Function	1Gb Non-Volatile ST-DDR4 Spin-transfer Torque MRAM
Package	FBGA-96
Date Code	2140 (T002140 / Lot number : E290T62S302)
Number of tested parts	2 irradiated samples

2.1.1.2 STT-xSPI MRAM

Part designation	EM064LXQADG13IS1T
Manufacturer	Everspin Technologies
Part Function	Expanded Serial Peripheral Interface (xSPI) Industrial STT-MRAM Persistent Memory
Package	8-Lead DFN
Date Code	2238 / Trace F91J69S701
Number of tested parts	3 irradiated samples

2.1.1.3 Type of events

The SEU/Burst/SEFI detection is ensured by the FPGA, driven by the remote computer. The memory is continuously read back and data are compared to the expected data set contained in the FPGA. There are three types of events recorded during this test:

- **SEU:** Any mismatch of data reading with expected data is at first considered to be a SEU and the data is sent to the computer. A counter is incremented accordingly. This process is repeated from address 0 to the last address of the memory. An SEU is an isolated upset in the data array of a memory. At normal flux under beam (until 5000 part./s.cm²), the number of SEUs induced by heavy ions in the memory should not exceed a few events (less than 10 events).

- **MBU:** An MBU is detected when several bits change from state 0 to 1 or from state 1 to 0 in a single word.
- **Burst:** If the SEU/MBU error counter reach more than 10 events and less than 500 events of SEU before the last address is reached, then a Burst is considered.
- **SEFI:** If the error counter reach more than 500 events of SEU before the last address is reached, then a SEFI is considered and a power cycle is applied to the memory.

2.1.2 TID testing

With respect to reference documents RD[2]; RD[3] and RD[4], TID testing has been performed at GAMRAY facility in Toulouse (France). In this irradiation facility, a Cobalt 60 source is used with the possibility to vary the dose rate by simply adjusting the distance to the source.
During the dose exposures, devices under test have been irradiated in an ambient temperature of 24°C ±6°C.
During annealing step at 100°C±5°C, the temperature was controlled and monitored by using an external monitoring system.
A total ionizing dose verification test has been performed with an accumulated dose of about 49 krad(Si) at a dose rate of 221 rad(Si)/hour

2.1.2.1 STT-DDR4 MRAM

Part designation	EMD4E001G16G2-150CAS2
Manufacturer	Everspin Technologies
Part Function	1Gb Non-Volatile ST-DDR4 Spin-transfer Torque MRAM
Package	FBGA-96
Date Code	2140 (T002140 / Lot number : E290T62S302)
Number of tested parts	6 irradiated samples (3 ON + 3 OFF + 1 control sample)

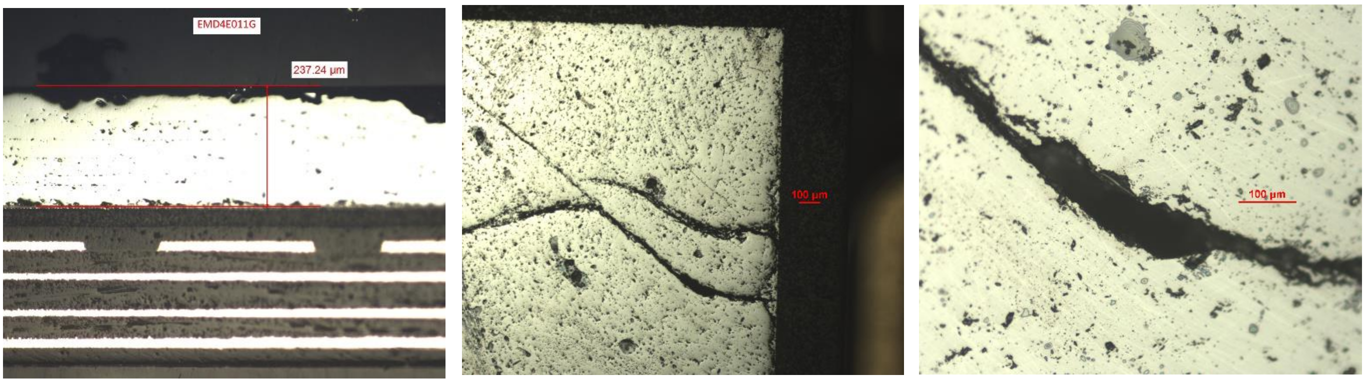
2.1.2.2 STT-DDR3 MRAM

Part designation	EMD3D256M16G2-150CBS1
Manufacturer	Everspin Technologies
Part Function	256Mb Non-Volatile ST-DDR3 Spin-transfer Torque MRAM
Package	FBGA-96
Date Code	1909 (T101909 / Lot number : C21876S601)
Number of tested parts	6 irradiated samples (3 ON + 3 OFF + 1 control sample)

2.2 Results

2.2.1 Sample preparation

Since STT-DDR4 MRAM is a flip chip die in FBGA-96 package. Both delidding and backlapping was necessary to ease the SEE testing. Unfortunately, TRAD has not achieved to keep the components function after delidding and backlapping. As soon as the backlapping start, the die is beginning to break in the corner. So the STT-DDR4 MRAM have just been delidded and a high-range cocktail under vacuum has been used



2.2.2 SEE results

2.2.2.1 STT-DDR4 MRAM

<u>In SEL test configuration :</u>
No SEL was observed with LET of 39.48 MeV.cm²/mg, Krypton heavy ion.

<u>In SEU_READ test configuration :</u>
SEU were observed with a minimum LET of 1.4 MeV.cm²/mg, Oxygen heavy ion.
No lower LET was tested during this test campaign.

MBU were observed with a minimum LET of 23.6 MeV.cm²/mg, Iron heavy ion.
No MBU was observed with LET of 1.4 MeV.cm²/mg, Oxygen heavy ion.

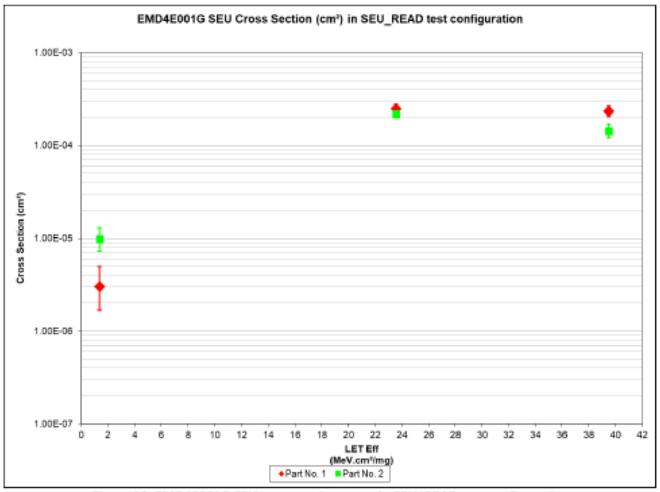


Figure 12: EMD4E001G SEU cross section curve in SEU_READ test configuration

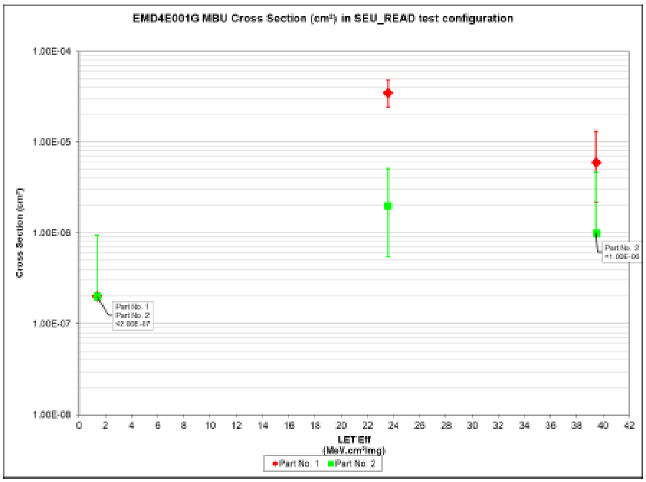


Figure 16: EMD4E001G MBU cross section curve in SEU_READ test configuration

Burst were observed with a minimum LET of 1.4 MeV.cm²/mg, Oxygen heavy ion.
No lower LET was tested during this test campaign.

SEFI were observed with a minimum LET of 1.4 MeV.cm²/mg, Oxygen heavy ion.
No lower LET was tested during this test campaign.

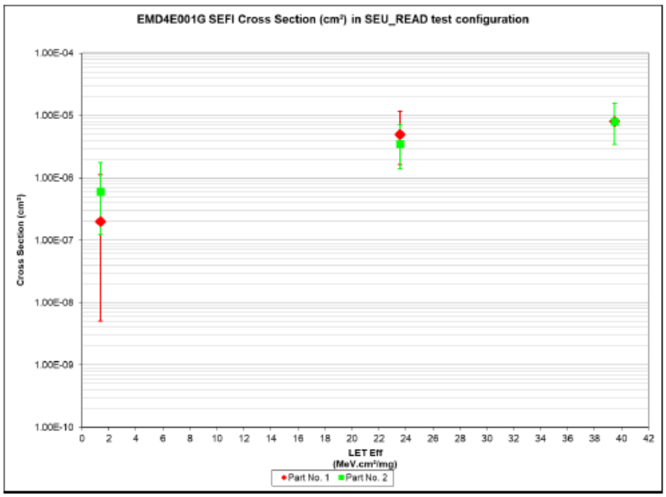


Figure 18: EMD4E001G SEFI cross section curve in SEU_READ test configuration

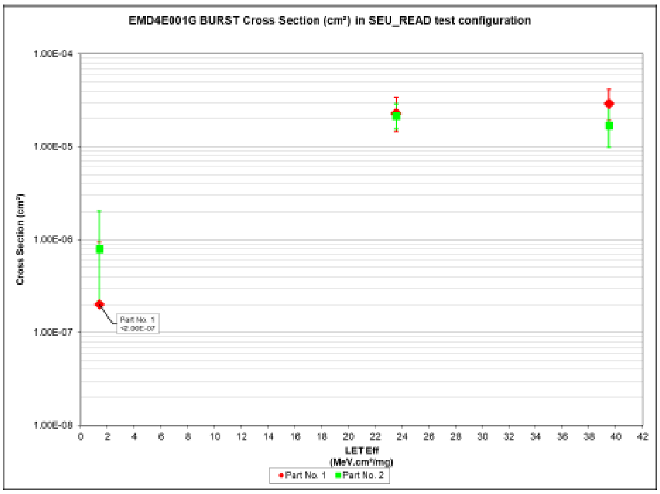


Figure 20: EMD4E001G Burst cross section curve in SEU_READ test configuration

<u>In SEU_WRITE test configuration :</u>

SEU were observed with a minimum LET of 1.4 MeV.cm²/mg, Oxygen heavy ion.
No lower LET was tested during this test campaign.

MBU were observed with a minimum LET of 23.6 MeV.cm²/mg, Iron heavy ion.
No MBU was observed with LET of 1.4 MeV.cm²/mg, Oxygen heavy ion.

Burst were observed with a minimum LET of 1.4 MeV.cm²/mg, Oxygen heavy ion.
No lower LET was tested during this test campaign.

SEFI were observed with a minimum LET of 1.4 MeV.cm²/mg, Oxygen heavy ion.
No lower LET was tested during this test campaign.

Details results are on RD[6]

2.2.2.2 STT-xSPI MRAM

<u>In SEL test configuration</u>

SEL were observed with a minimum LET of 28.96 MeV.cm²/mg, Krypton heavy ion.
No SEL was observed with LET of 15.45 MeV.cm²/mg, Iron heavy ion.

The worst amplitude SEL observed on VCC occurred during run No. 10 on part No. 2.

Run No.	10
Part No.	2
Test configuration	SEL
Type event	SEL
Ion LET (MeV.cm²/mg)	60.29
Relative amplitude	159 mA

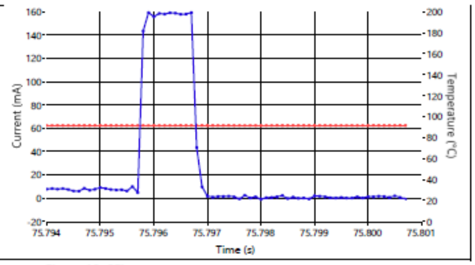


Figure 13: SEL worst case

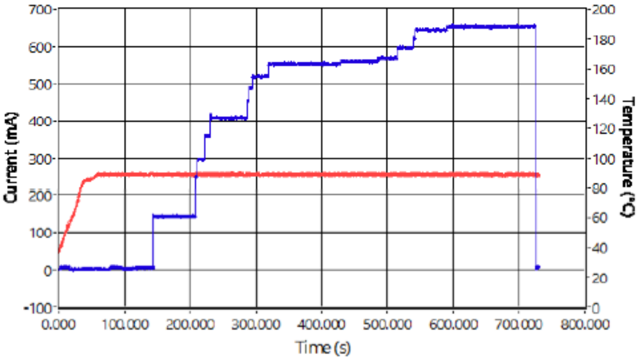


Figure 14: Current consumption monitoring during destructive test run

In SEU_READ test configuration

SEU were observed with a minimum LET of 8.05 MeV.cm²/mg, Argon heavy ion.
No lower LET was tested during this test campaign.

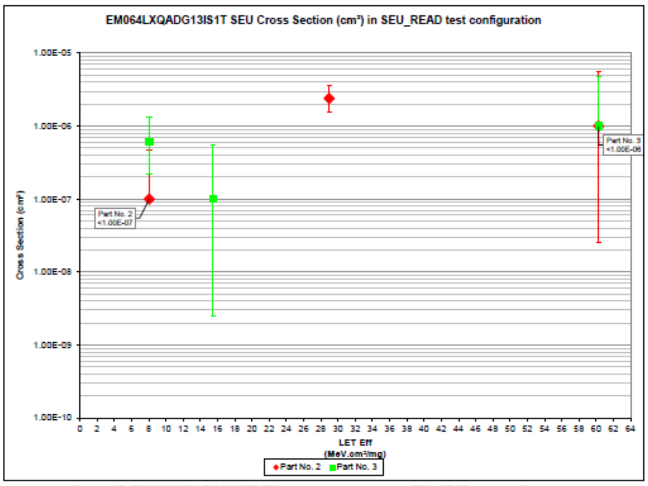


Figure 15: EM064LXQADG13IS1T SEU cross section curve in SEU_READ test configuration

No MBU was observed with a maximum LET of 60.29 MeV.cm²/mg, Xenon heavy ion.

BURST were observed with a minimum LET of 8.05 MeV.cm²/mg, Argon heavy ion.
No lower LET was tested during this test campaign.

SEFI were observed with a minimum LET of 8.05 MeV.cm²/mg, Argon heavy ion.
No lower LET was tested during this test campaign.

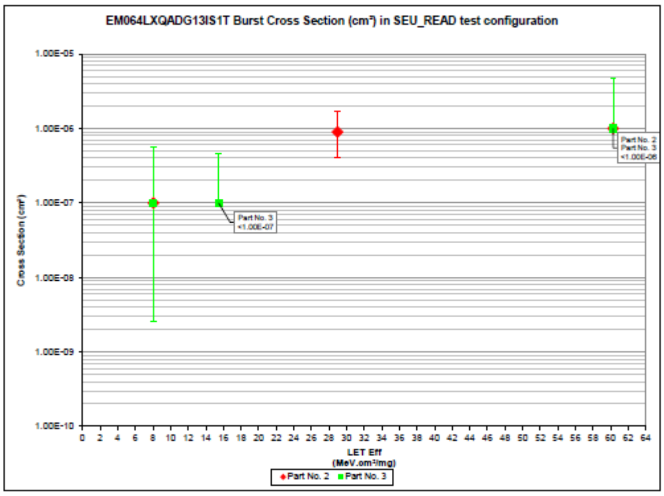


Figure 17: EM064LXQADG13IS1T Burst cross section curve in SEU_READ test configuration

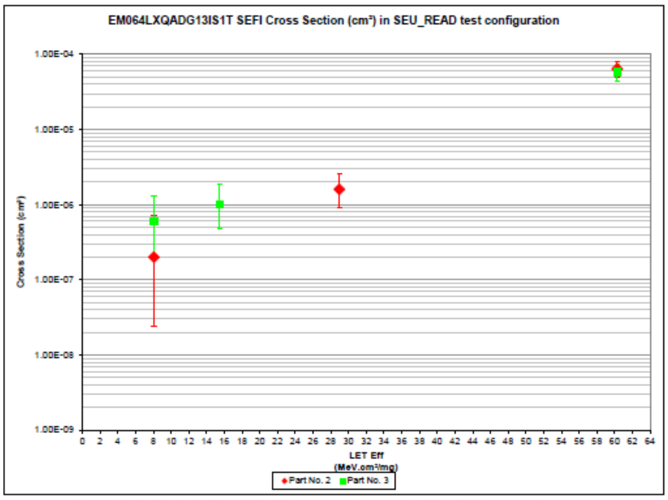


Figure 18: EM064LXQADG13IS1T SEFI cross section curve in SEU_READ test configuration

Details results are on RD[7]

2.2.3 TID results

2.2.3.1 STT-DDR4 MRAM

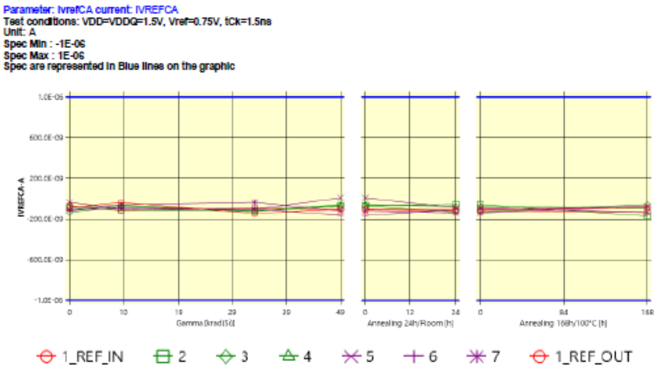
6 samples plus one control sample were used during testing. They were exposed to radiation using a dose rate of 221 rad(Si)/hour at room temperature with an accumulated dose of about 49 krad(Si).
All parameters remained within specification limits all along testing.

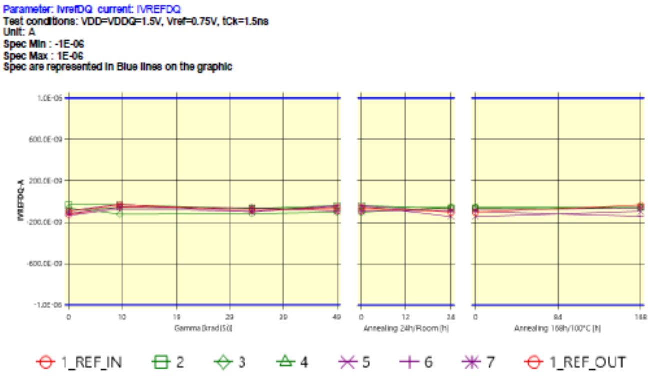
Details results are on RD[8]

2.2.3.2 STT-DDR3 MRAM

6 samples plus one control sample were used during testing. They were exposed to radiation using a dose rate of 221 rad(Si)/hour at room temperature with an accumulated dose of about 49 krad(Si).

All parameters remained within specification limits all along testing.





Details results are on RD[9]

3 Conclusions and perspectives

3.1 Conclusions

This project has allowed to evaluate in radiation the STT MRAM form EVERSPIN Technologies with the main conclusions :

- No destructive events on both MRAM tested (STT-DDR4 MRAM and STT-xSPI MRAM)
- SEU, MBU, SEFI and burst events detected on STT-DDR4 MRAM and STT-xSPI MRAM
- No drift in TID up to 49krad on the both MRAM tested (STT-DDR4 MRAM and STT-DDR3 MRAM)

3.2 Perspectives

Additional campaigns could be performed to evaluate deeper these parts :

  - TID campaign for the STT xSPI MRAM
  - Heavy ions campaign with additional samples and higher energy for the STT-DDR4 MRAM
  - Heavy ions campaign to define and try potential mitigation techniques if needed

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