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Executive Summary Report

GEROS-ISS REDUCED

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1. INTRODUCTION & SCOPE

This Executive Summary Report document summarises the new architecture for reduced GEROS-ISS in the frame of GEROS-ISS Cost reduction Exercise (ESA contract No 400012034017/NL/FE.

It is done with the contributions from TRYO Aerospace (CAL/LNA and BFN) and RUAG GmbH (SPU and POD units).

2. DOCUMENTATION AND NOMENCLATURE

2.1. APPLICABLE DOCUMENTS

AD	TITLE	REFERENCE
AD-1	GEROS-ISS Cost Reduction Exercise RFP	ESA RFP3-14901/17/NL/FE
AD-2	Statement of Work	ESA-TECER-SOW-004454
AD-3	Final Data Pack GEROS-ISS Phase A	ESA No 4000112188/14/NL/MV

2.2. REFERENCE DOCUMENTS

RD	TITLE	REFERENCE
RD-1	PROPOSED GEROS-ISS PAYLOAD SIMPLIFICATION	03 Feb 2017
RD-2	GEROS-ISS SRD	Isssue:2.4, 10/09/2015
RD-3	Mapping of Applications onto Operational Modes	
RD-4	ESA ACTIONS TC-1	
RD-5	“Cookie”: A Satellite Concept for GNSS Remote Sensing Constellations	
RD-6	SPU Simplification	P-11461-TN-00004-RSA
RD-7	CAL/LNA and BFN cost reduction analysis	GEROS-ANL-0001-TA-03
RD-8	SPU simplification	P-11461-TN-00004-RSA_2
RD-9	SPU cost estimation	P-11461-REP-00002-RSA_2
RD-10	Antenna simplification	rGEROS-ASE-TN-0003_Iss01

3. GEROS-ISS REDUCED PAYLOAD OVERVIEW

3.1. PAYLOAD CONCEPT AND FUNCTIONALITIES

The main goal of GEROS-ISS is to demonstrate the capabilities of GNSS remote sensing to derive geophysical parameters of ocean, ice and land surfaces, which are associated with geophysical research with special focus on relevant climate change phenomena.

To reach the mission objectives GEROS-ISS payload must be capable of receiving multiple GNSS direct and reflected signals coming from different directions within a wide angular range. In addition, the signals have to be received with a sufficiently high antenna gain so as to guarantee range performance, crucial for the first priority mission objective, altimetry. The type of antenna which can fulfil all these requirements is a beamforming antenna. Such an antenna consists of a number of elements whose output signals are split, phase shifted and combined to form multiple and simultaneous high gain beams pointing towards the desired directions.

The single and common front-end (GAB) which is used for all scientific objectives is complemented by several on-board signal processors within the back-end unit (SPU). Since GAB enables different processing techniques, including interferometric reflectometry, the antenna must consists of 2 arrays, mounted back-to-back, with CAL/LNA modules in-between. The SPU shall receive pairs of beams to be cross-correlated pursuing the applications objectives.

The GEROS-ISS payload is also mechanically designed to be an integrated payload attached to the Upper Limb Balcony (ULB) of the Columbus External Payload Facility (CEPF) part of the International Space Station (ISS).

The original GEROS-ISS characteristics are gathered in RD-07. During the last months, additional work has been done on the GEROS-ISS payload aiming at reducing the total cost while keeping the main performances of the original GEROS-ISS up to its maximum extend. The payload concept described in the following paragraphs corresponds to the outcome of this cost reduction exercise. Reduced GEROS-ISS concept is able to manage 2 beam pairs at CL1 frequency band and 2 beams pairs at CL5 frequency band to track at least 2 satellites and associated reflections. This beam configuration allows to perform applications such as altimetry, scatterometry, grazing altimetry and radio occultation to each of these 2 tracked GNSS satellites.

Figure 3-1 depicts a very basic functional block diagram of the designed GEROS-ISS reduced payload.

One of the main advantages of the GEROS-ISS payload is its ability to work with an extensive number of GNSS systems and their corresponding augmentation systems, increasing the opportunities of obtaining data from the experiment. This important feature has been kept.

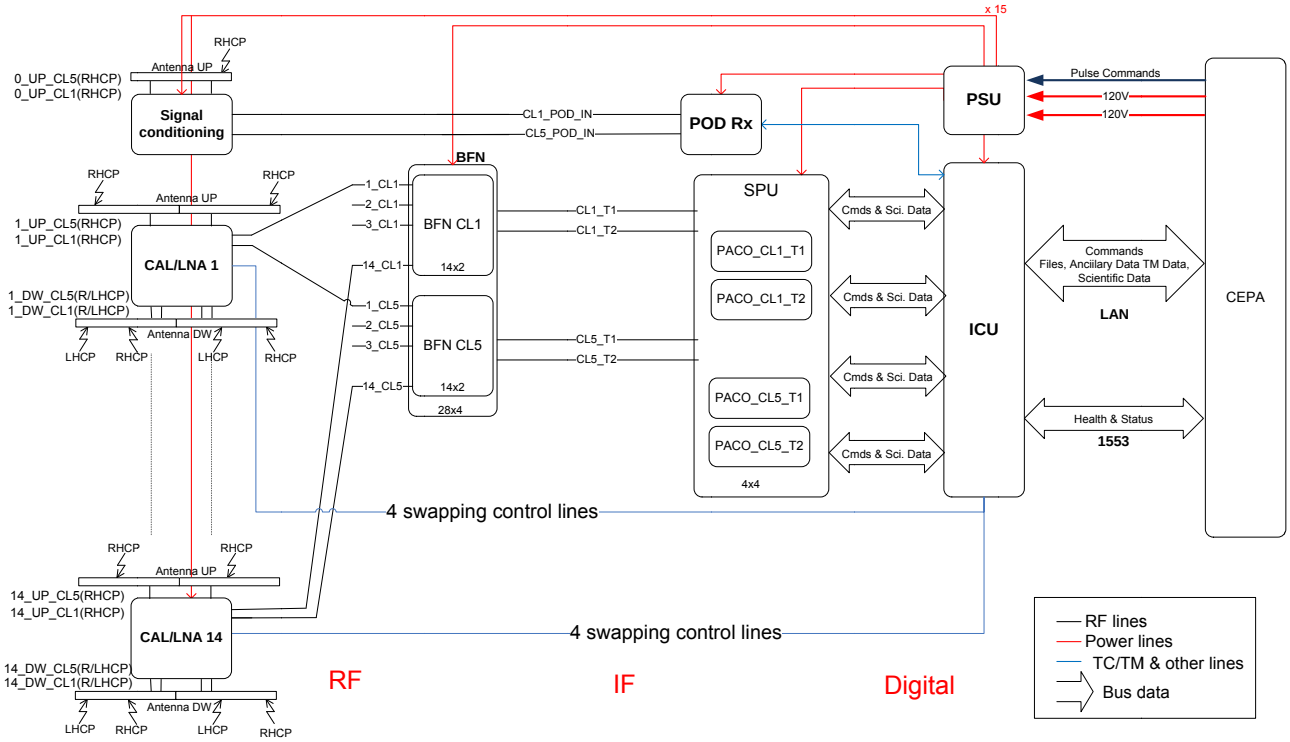

Figure 3-1 Reduced GEROS-ISS Architecture

3.2. REDUCED GEROS-ISS

From the previous GEROS-ISS concept, the payload has been simplified in different ways assuming some minor reduction on performance and on mission capabilities. See RD-1.

H/W REDUCTION	JUSTIFICATION
Number of antenna patches reduced from 30 to 28	It has been proven that an array with 14 subarrays of 2 elements each has sufficient performance for the reduced GEROS-ISS applications Additionally, the up-looking central patch is used for the POD – this does not change Thus, in total there are (14x2)+ (14x2) + 1 = 57 antenna patches.
Reduction of CAL/LNA units from 30 to 14	This comes from grouping the patches in 14 subarrays instead of considering independent elements.
Removal of the reception of the up-looking LHCP signal	This signal was originally used for scatterometry. As scatterometry is not a primary object of the mission, the contributors considering LHCP in the uplooking signal have been removed. This signal is not used for any other application.

Number of outputs in the CAL/LNA reduced from 6 to 2	• The applications products are obtained sequentially and not in parallel as in the original GEROS-ISS concept. • Polarimetric RO is no longer required. • Switching of the polarization in the down-looking antenna and the semi-swapping technique at CAL/LNA level support this reduction. Therefore 1 output per frequency results in 2 outputs per CAL/LNA.
Digital internal control of the CAL/LNAs removed	The control of the CAL/LNAs has been simplified since now a CAL/LNA has only a SP4T switch that selects the input signal among the 3 available {up-looking RHCP, down-looking RHCP, down-looking LHCP} plus a 50 Ohm load for calibration. The number of lines required to control the internal switching have been extremely removed and so the need of a bus commanding implementation plus the digital decoding.
BFN Input reduction from 180 lines to 28	As we are managing 14 CAL/LNAs with only 1 output per frequency each, the input signals to the BFN are now 14X2 = 28
BFN output reduction from 22 to 4	2 satellites are being tracked in 2 different frequencies, resulting in 2 outputs of the BFN. The semi-swapping technique implementation allows as well for this reduction
Number of PACOS reduced by a factor of 3. Four PACOS are required.	The satellites that can tracked in parallel have been reduced from 4 to 2. Polarimetric Radio-Occultation is not required Semi-swapping technique
Number of ADC reduced from 22 to 4	The satellites that can tracked in parallel have been reduced from 4 to 2. Polarimetric Radio-Occultation is not required Semi-swapping technique

Table 3.1 Summary of HW reductions

As the BFN is massively reduced, it will be considered as one unit containing CL1 and CL5 frequencies instead of separate BFN blocks.

The same applies for the SPU, in which one unit will be considered containing 4 SPUs ADCs and 4 PACOS.

The semi-swapping technique will be explained below, since it has been identified as key for the hardware reduction.

3.2.1. SEMI-SWAPPING TECHNIQUE

The semi-swapping operation is illustrated in Figure 3-2 for a geometry such that the swapping time quasi-equals the relative delay between the reflected and the direct signals. The system control the swapping time in order correlate the direct and reflected signal. The RF switched are commanded to select the up-looking or the down-looking antenna. Also the un-swapping network internal to PACO changes the configuration to route the down-looking antenna signal straight into the correlator and the up-looking antenna signal to the delay line. Half the time the signals will be valid to the input of the correlator, and half the time can be discarded.

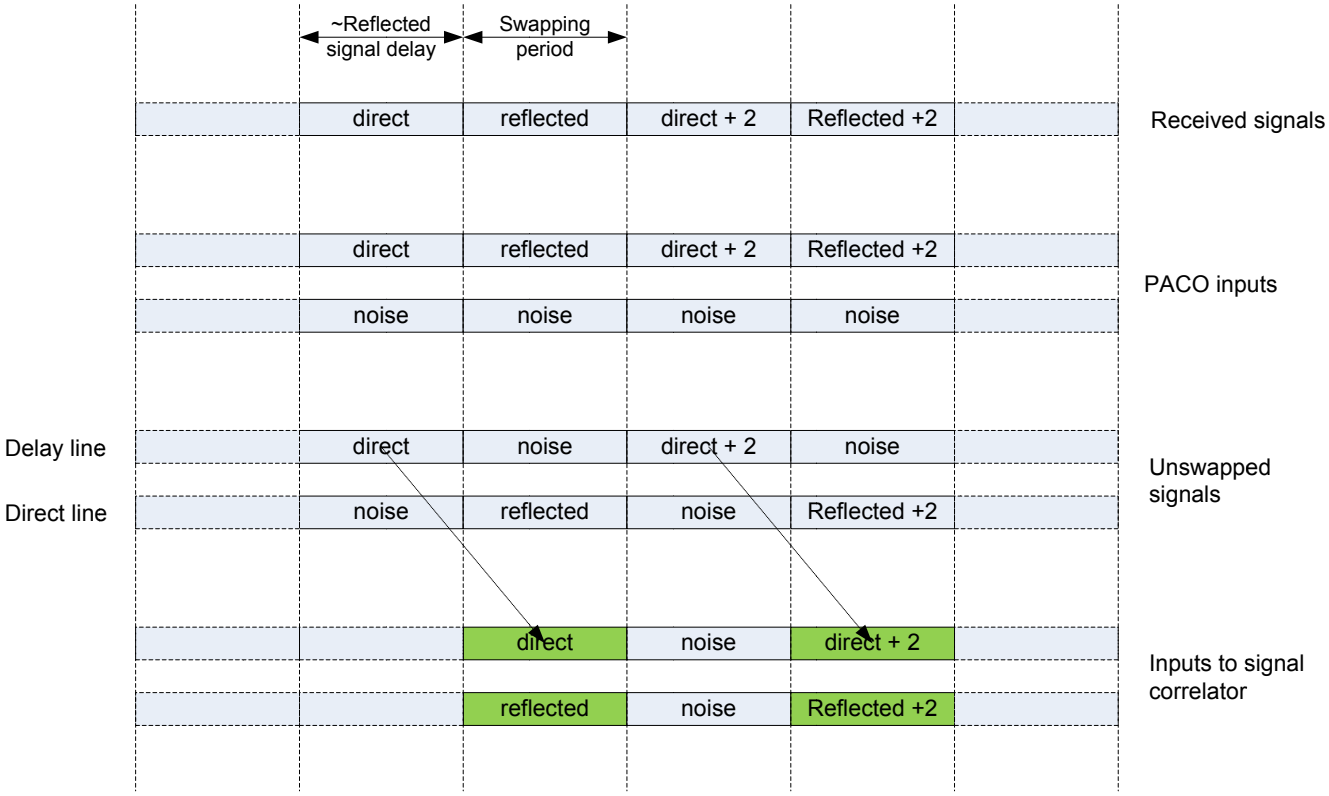

Figure 3-2 GEROS-ISS semi-swapping technique

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3.3. REDUCED PAYLOAD DESCRIPTION

When it comes to the antenna, the up-looking and down-looking antennas have a mechanical tilt of 20º so that the unobstructed field of view towards the Earth is maximized and to minimize the degradation due to the roll-off of the 2-element sub-array pattern. The up-looking side of the GAB antenna contains RHCP polarization whereas the down-looking side of the GAB antenna contains both LHCP and RHCP polarizations. GEROS antenna is an array of 29 patch elements in a hexagonal array lattice with a separation of 178 mm between patches, organized in 14 subarrays of 2 elements each The central element in the up-looking array is used for the POD receiver and the central element of the down-looking is used by a retro-reflector allowing laser ranging, so actually the array has 28 active elements. The radiating elements of the antenna array are stacked circular patches using as substrate an air-like foam.

Inside a subarray, the output of the 2 elements are internally combined, so that 1 output is obtained per pairs of elements. Every up-looking subarray of GAB is paired with its corresponding down-looking subarray by means of a CAL/LNA unit. The main components inside the CAL/LNA are the low noise amplifiers (LNA), necessary to ensure optimal signal to noise ratio, as well as the relevant parts needed for the amplitude calibration system (CAL). For the second function, 50Ω loads are employed. Several stages of notch filters are added for X, Ku, S and UHF bands rejection through the RF paths. RF amplifiers to boost the signal to the required levels are used just before the sharp cavity filters that conform the RF signal to the required mask and provide the signal to the BFN as clean as possible. A switch allows for the selection of the desired signal or the 50 Ohm load. The RF network scheme is duplicated for F1 and F5 and each frequency circuit is based on 3 RF inputs (up-looking RHCP and down-looking RHCP and LHCP) and 1 RF outputs or RF chains (LNA + Amplifier + Filters). Figure 3-3 shows a functional diagram block of the CAL/LNA, which is identical for CL1 and CL5.

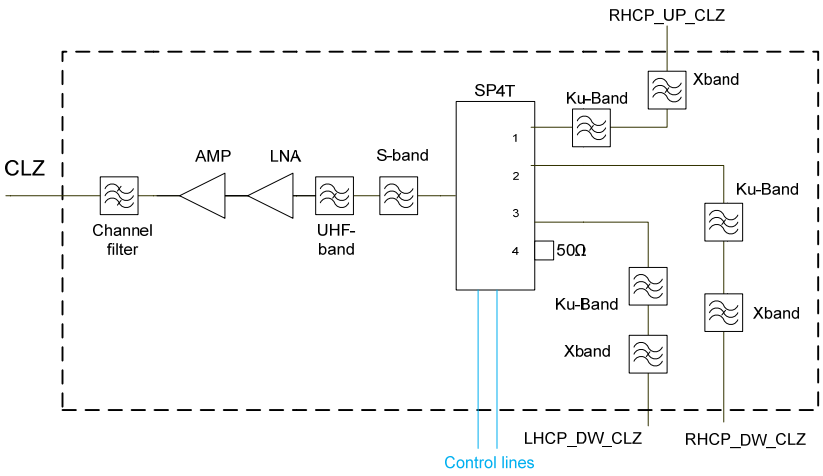


Figure 3-3: CAL/LNA Functional Diagram (One frequency, Z = {1, 5})

Just after the CAL/LNAs, the beamforming network is placed. The BFN is based on 2 BFN modules, each devoted to one frequency. Each BFN module delivers 2 different beam outputs, aiming at tracking in total 2 satellites. The architecture is based on a succession of several stages:

1) MCM that splits the signal in 2 to track 2 satellites and applies the beams-forming though phase shifters,
2) a set of RF combiners to single signal and
3) RF to IF down-converter. The beamforming configuration is externally controlled by RS422 data links.

Figure 3-4 shows a functional diagram block of the BFN, which is identical for CL1 and CL5.

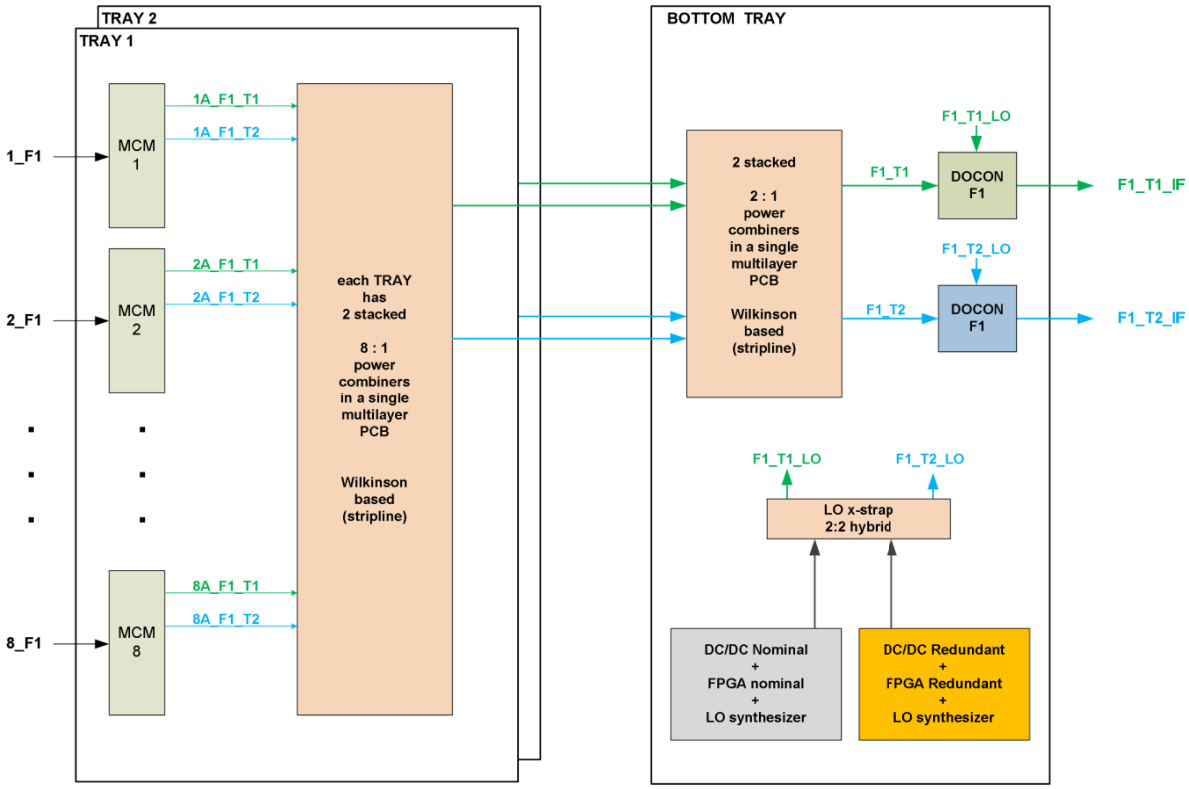


Figure 3-4: BFN Functional diagram

The beams at intermediate frequency are connected to the processing unit, the SPU. This module is based on ADC chips and correlators formerly implemented in ASIC technology (called PACO) which are controlled by Spacewire links. The correaltors are able to perform different processing techniques for GNSS reflectometry, scatterometry and radio occultation. Each correlator can compensate the physical delay and the Doppler frequency differences between the signals to be processed (i.e. for altimetry application the up and down signals). The coherent and non-coherent integration times are also configurable via the Spacewire interface. A functional diagram of PACO can be seen in Figure 3-5.

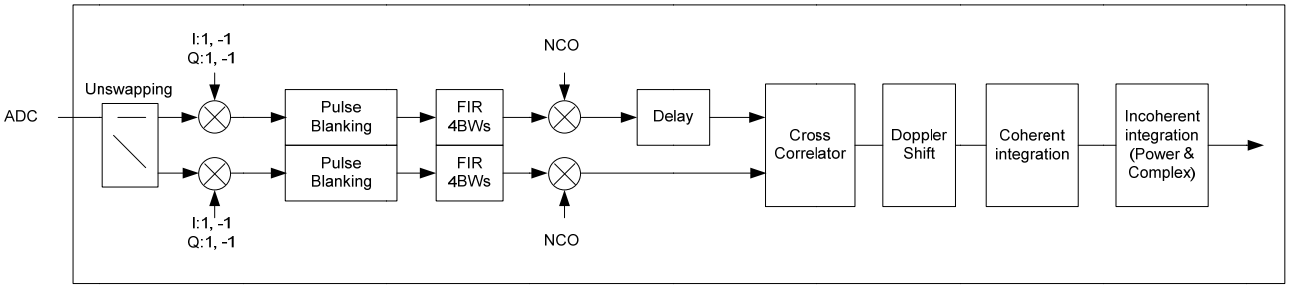


Figure 3-5: PACO Functional Diagram

The Instrument Control Unit (ICU) is in charge of the control of the overall instrument, data handling, data storage and interfacing towards the ISS. It is the operational brain of the whole instrument. So it is in charge of the payload preparation and synchronization for an event observation. The ICU manages the beams pointing, the CAL/LNAs switching and the operation of the SPU, providing to PACOs with data as Doppler settings, coherent and incoherent integration parameters, desired output waveform, etc.

For the synchronization of the whole instrument the ICU generates and distributes the master clock to the whole instrument as needed.

Other generic ICU activities are also performed, such as FDIR, thermal control, power supply unit management, interface towards the ISS and time management.

It is basically composed of a microprocessor system, where the software runs, a memory module, a payload housekeeping signals acquisitions module and hardware interfaces towards the rest of the payload modules and ISS.

The PSU is the power distribution subsystem that conditions and distributes the required power to the subsystems for all mission phases and payload modes. The unit must be compatible with the electrical/power interfaces of C3-1 Dragon and CEPF.

A COTS POD receiver subsystem is included in the payload which:

- provides the on-board time reference to all the payload, including the PPS signal
- provides the position of the payload to the ICU
- delivers observables that are considered as Level 0 data products and
- it is used in the geo-location of the power-delay waveforms in the level 1B product.

The signal received from the central element of the up-looking array will be conditioned by an LNA to adapt the level to the input of the POD rx.

The last element to be mentioned is the Laser Retro-Reflector (LRR) that is placed in the central element of the down-looking array and it is used in the validation of the POD solution obtained using the POD receiver.

3.4. ELECTRICAL ARCHITECTURE

Figure 3-6 depicts the electrical architecture of the concept for GEROS-ISS reduced payload. All elements receive power supply from the PSU. TM/TC interfaces between units are based on Space-wire for ICU-POD and ICU-SPU and on RS422 buses for ICU-BFNs and ICU-CAL/LNAs.

In order to control the front-end units RS485-422 type buses are conceived. For the CAL/LNAs the RS422 signals are conceived to be directly the switching commands. Each line can be shared by several receivers due to the fact that all the CAL/LNAs will switch identically and at the same time. Two drivers per control line is foreseen, each controlling 7 or 8 CAL/LNAs.

The BFN TC link (BFNTC) is based on three “point to multipoint” signals (multidrop configuration): data, clock and strobe. For the TM link function dedicated lines are added to avoid any bus conflict and the associated line arbitration control. Telemetry shall be transmitted when strobe signal is active. The data will contain the last received command which is currently active after the strobe signal edge. Further details on the BFN TC link are shown in Figure 3-7 and for the TM link in Figure 3-8.

The non-RF internal interfaces within the GEROS-ISS system are listed below:

- 4 Spw lines for TM/TC between ICU and 4 PACOs
- 2 Clock signal from ICU to each PSU board
- 2 Reset signal from ICU to each PSU board
- Switching control lines, bi-level RS422 based, between ICU and CAL/LNAs
- BFN TC link, digital communication based on RS422, between ICU and BFN
- TM/TC SpW link between ICU and POD
- Reference PPS from the POD to the ICU
- 2 Primary power lines from the COLUMBUS module
- Secondary power lines between PSU and all other GEROS-ISS equipments
- TBD analog telemetries (secondary voltages, thermistors, relay status)

The RF interfaces between BFNs and SPUs have been drastically simplified from the original GEROS-ISS concept. The final connection between entities is shown in Figure 3-9. One single frequency beam is directly connected to a single ADC and later to a single PACO. Each has now only one input connected.

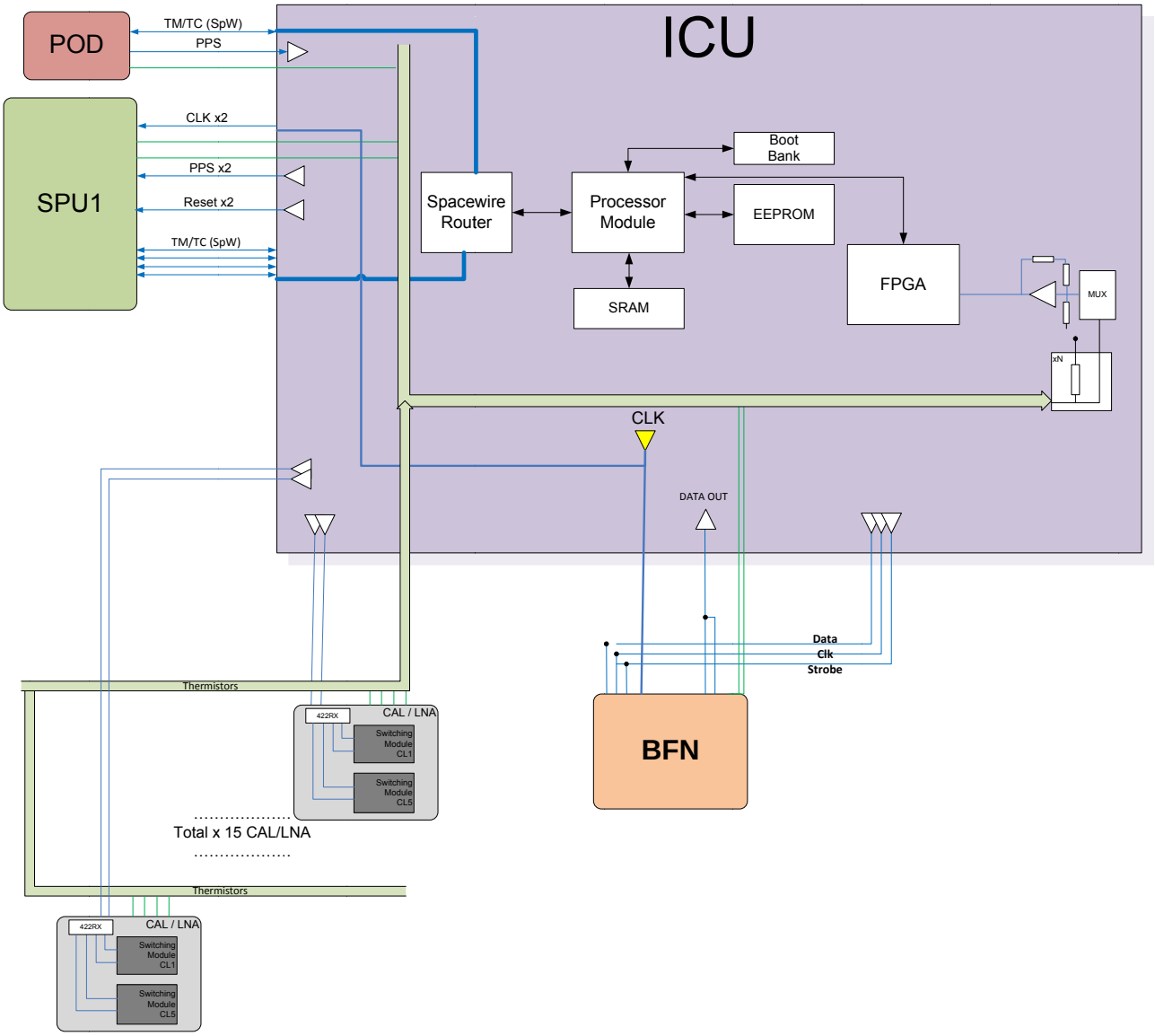


Figure 3-6 Electrical Architecture

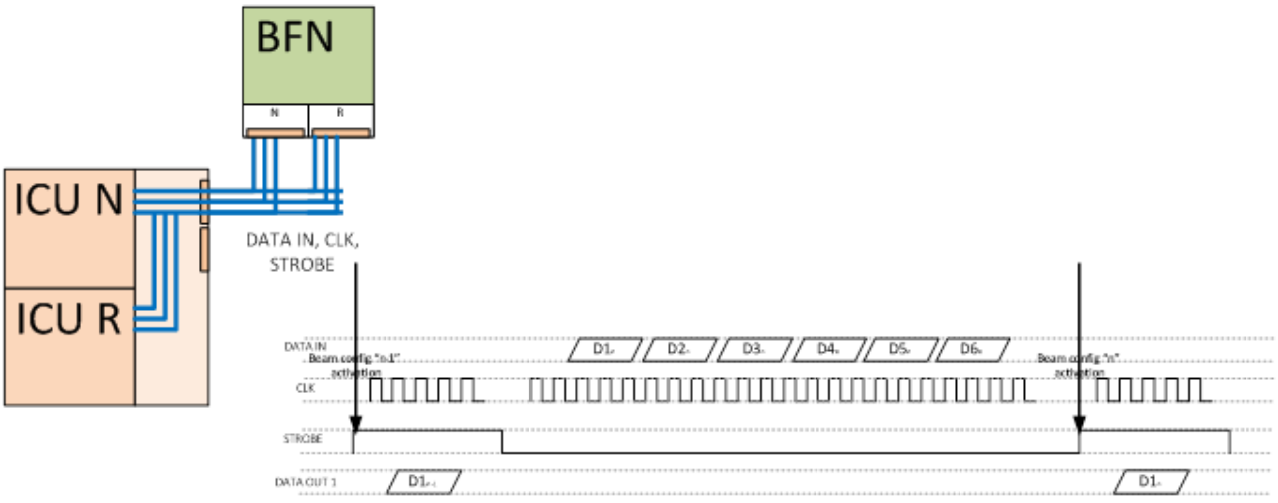


Figure 3-7 BFN TC link

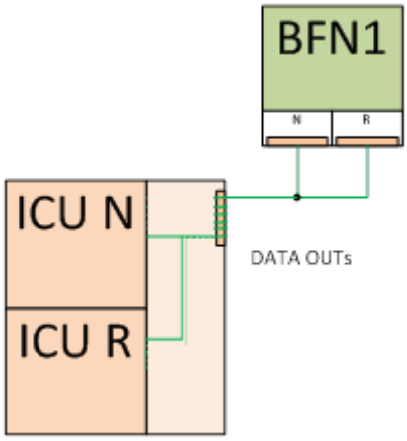


Figure 3-8 BFN TM link

The control of SPU is basically the PACOs control. Each PACO has one Spacewire interface that will be used by the ICU to control all PACO internal parameters and configurations. Same Spacewire interface is used for housekeeping and scientific telemetry.

3.4.1. BFN-SPU INTERFACE

Each PACO is physically connected only to one RF path via 1 ADC internal to the SPU.

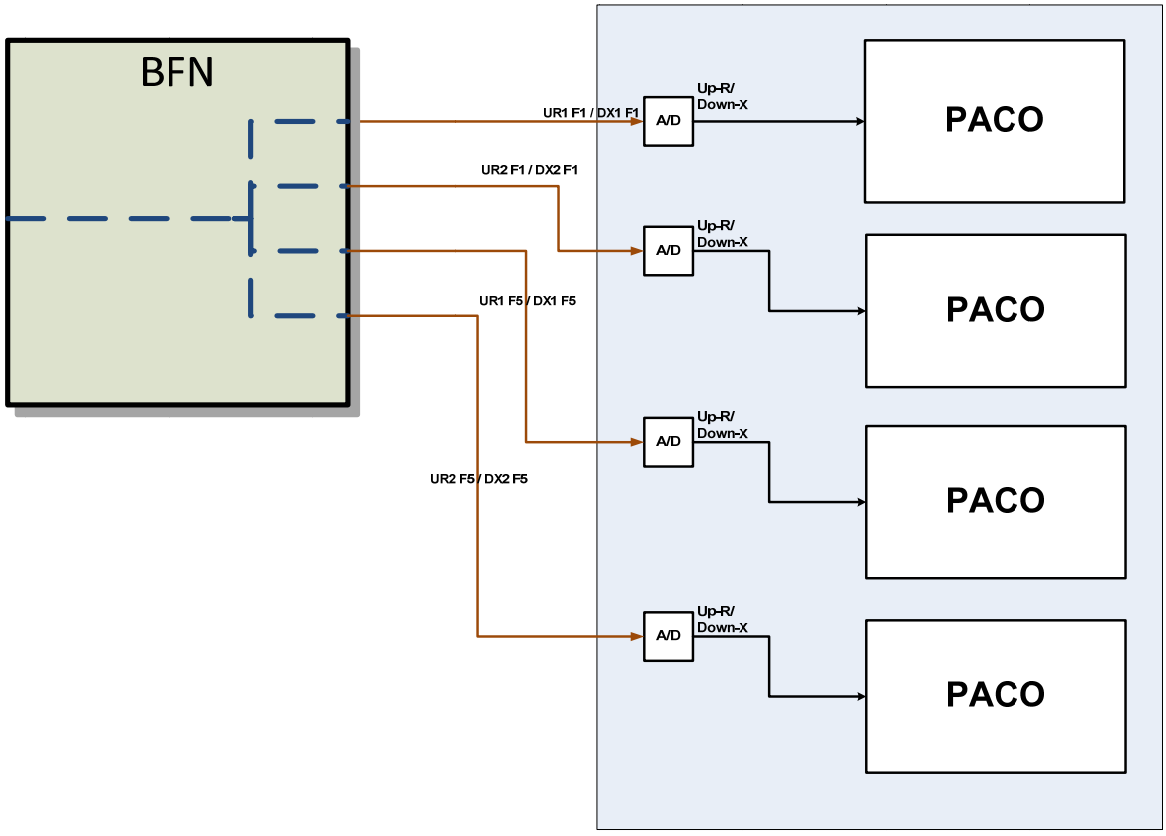


Figure 3-9 BFN-SPU interface

3.5. SYSTEM REDUNDANCY CONCEPT

The redundancy concept is the result of a trade-off between payload complexity, costs and the survival of all mission applications. Some elements are redundant per-se as part of a set of elements. Other subsystems or parts must be doubled to work in cold redundancy to avoid the loss of the mission even when some mission degradation can be accepted.

CAL/LNA elements are indeed redundant because of the array concept of the GAB .The loss of one CAL/LNA will produce some reduction on antenna performances but the mission can still continue. It is important to design a power supply chain where any failure propagation is avoided.

The presence of 2 beams per BFN allows that the loss of one beam will reduce number of simultaneous observations to only one, but the performance of this beam still persist. The DC/DC converter within a BFN is the internal SPF point. So cold redundancy is added at converter level.

Regarding the SPU, the correlator chains can be considered as functionally redundant, following the same concept as the BFN. The loss of one chain reduces the number of simultaneous observations to one, but keeping full performances functionality on the remaining chain.

The converters within the SPU are transferred to the PSU. Both converters must work nominally in hot redundancy. One single point failure in one DC/DC converter would degrade the mission to one specular point. The SPU receives the power from an isolated intermediate bus voltage coming from the PSU and the SPU implements a second stage down-conversion based on of off-the-self DC-DCs based on POLs.

The ICU is the main controller and central element of the whole instrument. It must be designed as a cold redundant unit with cross-strapped signals at the output avoiding any SPF.

For PSU the redundancy design is included to both input and output level.

- A dedicated DC/DC converter shall be associated to each 120VDC power feed (N&R).
- Two redundant DC/DC converters per CAL/LNA voltage
- Two redundant DC/DC converters per SPU voltage

LCL redundancy per payload unit (i.e. POD and ICU)

The nominal redundancy concept is summarized in Figure 3-10.

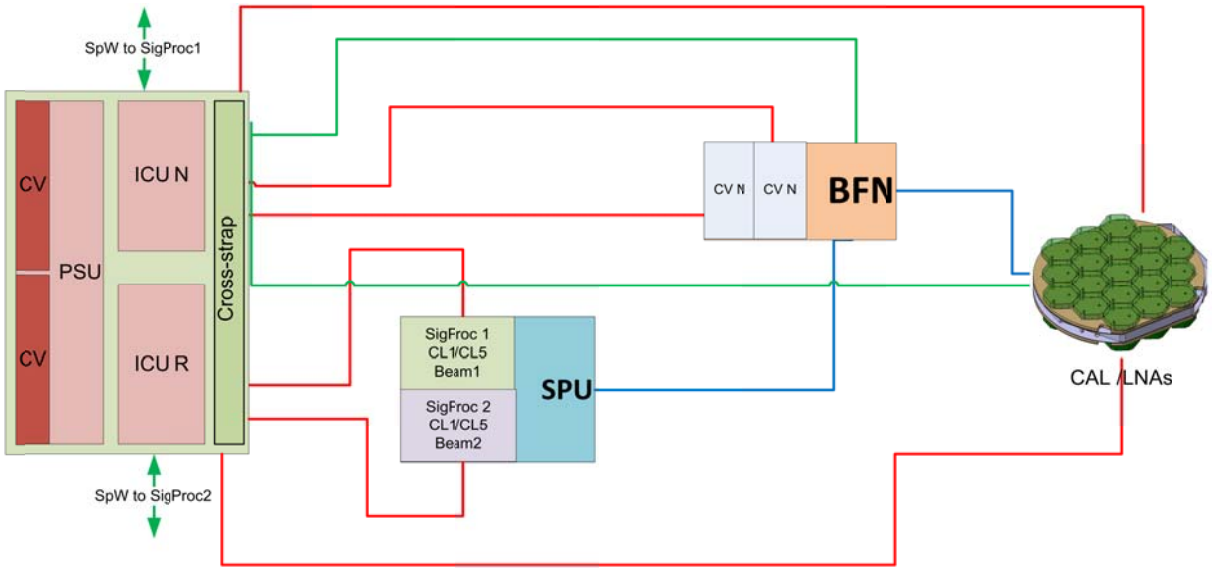


Figure 3-10 System Redundancy Concept

4. REDUCED GEROS-ISS INSTRUMENT SUBSYSTEMS

4.1. ANTENNA

From the previous GEROS-ISS concept, the antenna has the following changes (both for up-looking and down-looking arrays):

- The number of antenna patches is reduced from 30 to 28 patches. The central patch is still used for POD.
- The patches are sub-arrayed in pairs in the Φ=0º (X direction) so there are only 14 phase centres (14 subarrays of 2 patches). Patches can be combined with a T divider or Wilkinson divider contributing small losses (around 0.05 dB) implemented in the same stripline where the 90º hybrids polarizers are located.
- A tilt angle of α=20º with respect to Y axis is performed in order to improve performances at the desired field of view.

A sketch of the new array configuration can be shown on Figure 4-1.

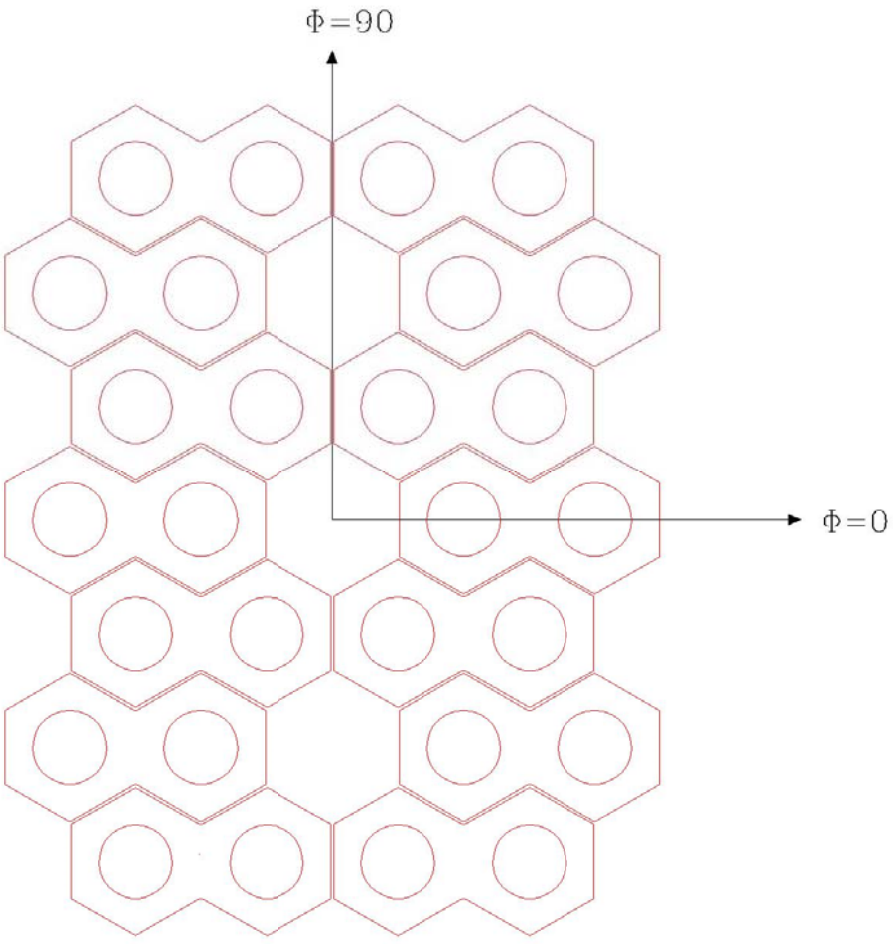


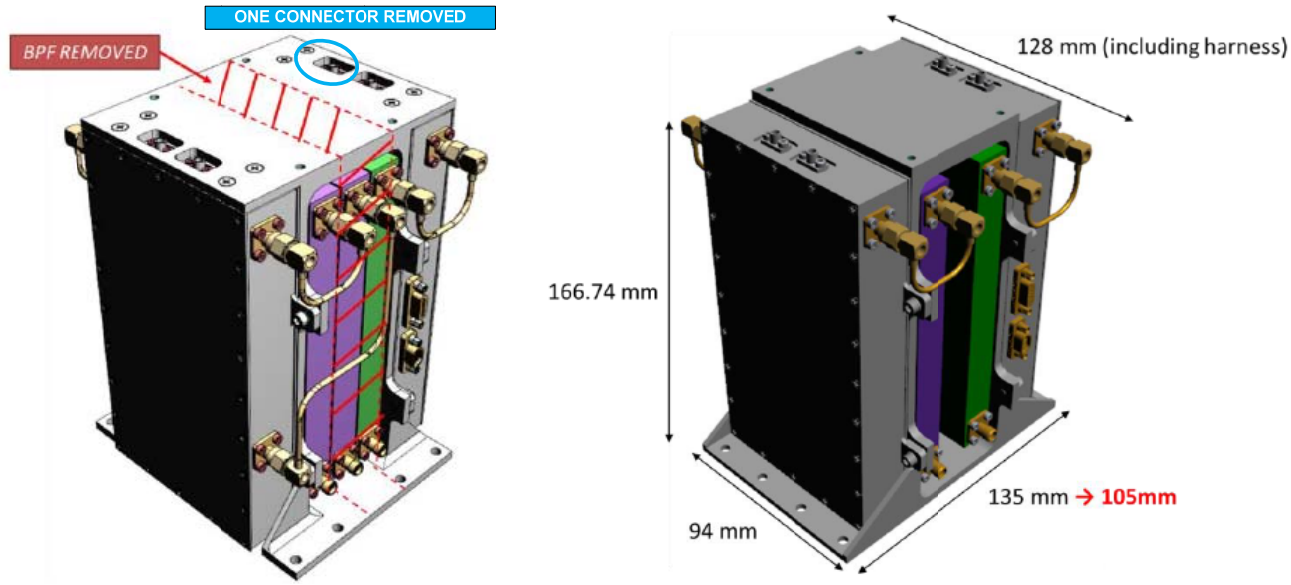
Figure 4-1 Reduced GEROS-ISS Antenna

4.2. CAL/LNA

The main performances of the designed CAL/LNAs are the following:

- The CAL/LNA Noise Figure is below 3dB, including 0.6dB of radiator insertion loss plus 0,05dB of the combiner inside the subarray plus 0,17dB loss for the cable to reach the CA/LNA. Note that the need of all notch filters will be confirmed in future stages of the project after a better refinement of the interference environment on board of the ISS.
- The CAL/LNA Gain is around 28 dB.
- The minimum back-off at the input of any of the blocks is around 67dB
- Consumption around 1,68W per CAL/LNA
- Mass is around 1.74 per CAL/LNA

The external shape of the CAL/LNA can be seen in Figure 4-2. In a) it is shown the parts that will be removed with respect to the original GEROS concept, mainly 4 cavity filters and one of the connectors the subarray- In b) it can be seen that one of the dimensions is reduced from 135 mm to 105mm.



a) b)

Figure 4-2: CAL/LNA mechanical configuration

The CAL/LNA simplification includes the following changes:

- Reduction of number of RF switches to one 1:4 per frequency
- Elimination of RF paths B and C, including BPF
- AMP custom MMIC replaced by COTS transistor
- FPGA removal and replacing by direct RS422 command lines

4.3. BFN/DOCON

The main performances of the designed BFN are the following:

- The NF of the system is not degraded by the BFN and it is maintained in 3dB maximum.
- The BFN gain is 87.8 dB.
- Consumption around 1,68W
- Mass around 15 Kg.

Phase and amplitude control interface has been simplified compared to GEROS-ISS to avoid OR'ing diodes inside the MCM modules to save cost. Instead, 2 full control serial interfaces are included for each beam. Each serial interface is independent from the other beam. Each serial interface comes is generated by OR'ing the signals coming from nominal and redundant FPGA's. With this apporach, diodes are used only once outside the MCM modules and are not multiplied by the number of RF inputs. The number of required diodes is only 12, while it was 116 with former GEROS-ISS approach.

Figure 4-3 depicts the block diagram for GEROS-ISS reduced version:

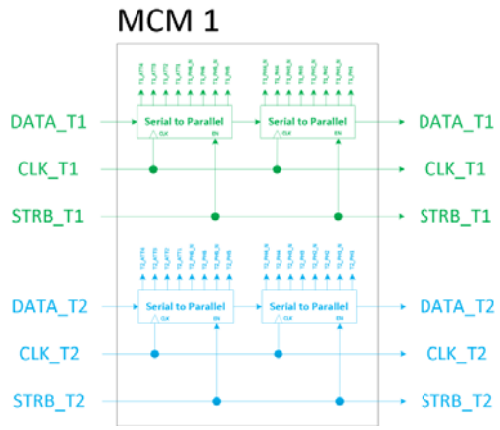
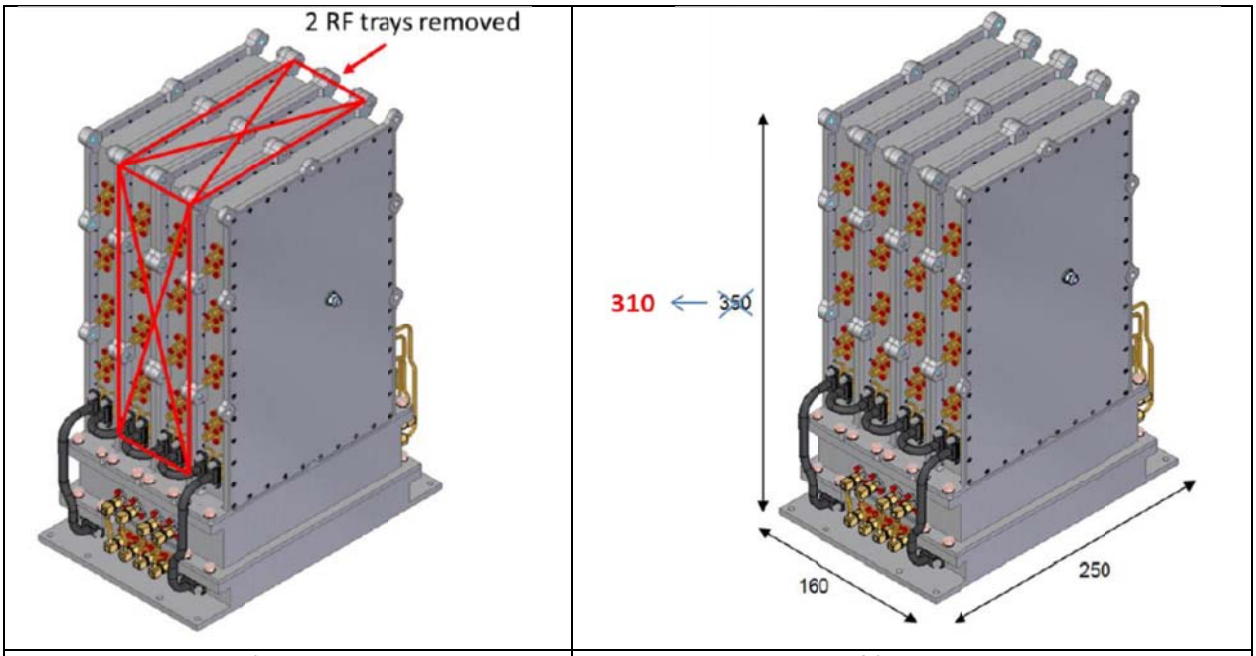


Figure 4-3: MCM TM/TC control block diagram reduced version

The external shape of one BFN box can be seen in Figure 4-4. In a) it is shown the parts that will be removed with respect to the original GEROS concept, mainly 2 trays as the satellites to be tracked have been reduced from 4 to 2. In b) it can be seen that one of the dimensions is reduced from 350 to 310 mm and the 160 mm will also be reduced to almost the half.
The full BFN contain 2 of these boxes.



a) b)

Figure 4-4: BFN mechanical configuration

4.4. SPU

4.4.1. REDUCTIONS FROM GEROS-ISS MCR

The system implications can be flowed down to the SPU design:

- Number of beams
- Semi-swapping technique
- Removal of polarimetric RO
- Removal of clean replica

At SPU level these reductions are transferred to the following main points:

- Only one SPU box with 4 PACOs, two per beam (F1 and F5)
- Only one ADC per PACO

At PACO level these reductions are transferred to the following main points:

- Clean replica removal (so, no BRAM, no extra NCO, no extra down-converter)
- Multiplexer removal
- Third input removal

Other specific reductions have been considered in order to find a simpler payload but still with good performances and application capabilities:

- No configurable FIR filters. The FIR will used pre-set Signal Bandwidths, (14, 19, 24 and 36 MHz)

Still some functionalities added during GEROS-ISS study must be maintained.:

- RFI Mitigation: Pulse blanking
- Coherent Average output

Different PACO implementation options has been traded-off. Implementation over FPGA or ASIC has been analyzed. QML-V FPGAs were considered as starting point but still COTS implementation has been also analyzed mainly from the cost point of view.

4.4.2. REDUCED PACO OVERVIEW

In the next figure the reduced design is shown. For the semi-swapping, where about half the correlation results have to be cancelled, three options are shown (in three different colors, corresponding to the colors used in next chapter).

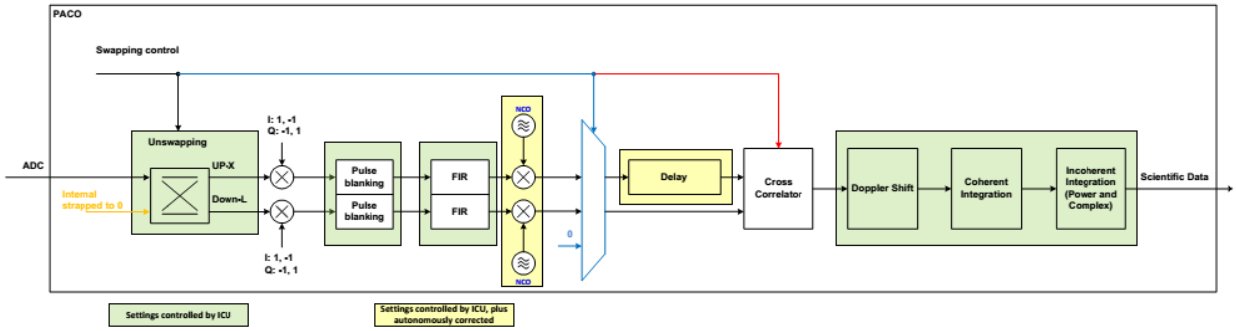


Figure 4-5 PACO for reduced GEROS-ISS concept

4.4.3. SEMI-SWAPPING CORRELATION

The semi-swapping, where only about half the time valid results are produced, adds some changes inside the PACO. Currently 3 options which give the same result inside the output buffers are shown.

Fill up at begin:
The first option consists on that during the swapping to one path, the other path is filled zeroes. This leads to the following pattern on the input of the correlator: one path being 0 for the times, when the other path is not valid. A correlation with 0 will put out 0 as well, hence the integration afterwards is not changed.

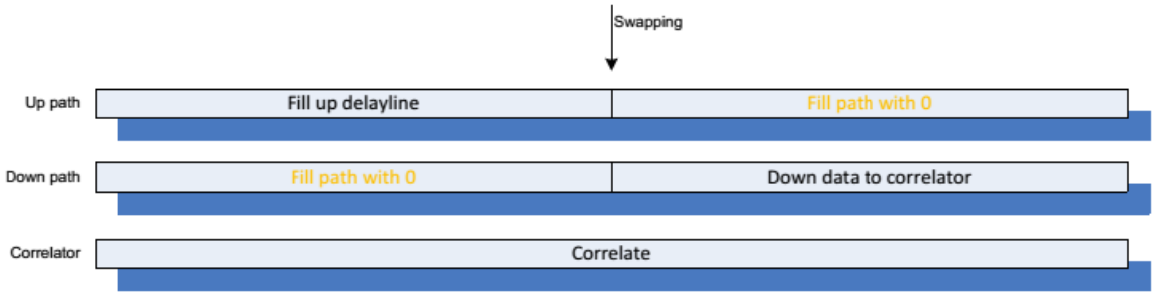


Fig. 4-1: Semi-swapping concept 1

One thing to note is, that the synchronization of when to add the 0 needs to be accurate to not mix valid/invalid input data. It has to be analysed what effect the various signal processing stages inside the PACO have on a 0 value at the input (e.g. residual error of the DC-offset compensation).

Fill up at correlator

Secondly, the fill up with zeroes can also be in front of the correlator/delayline. An advantage of this concept is, that all the signal processing stages from the beginning to the correlator input need not be analyzed for residual errors. The synchronization problem persists. The timeline is shown below

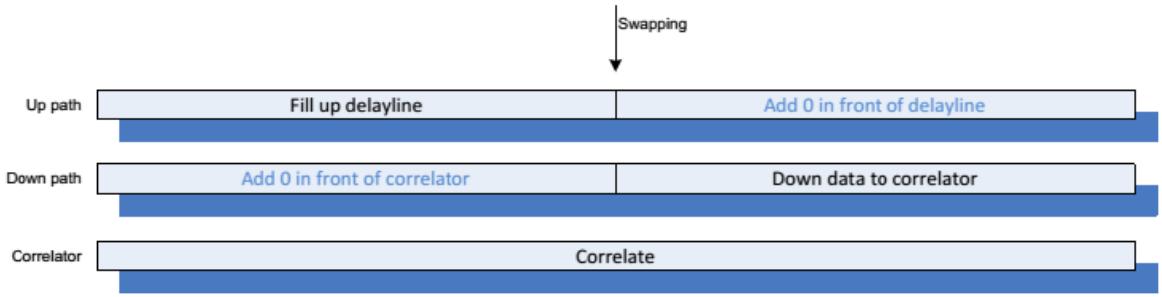


Fig. 4-2: Semi-swapping concept 2

Stopping the correlator

Using the knowledge of the swapping time, which is already known inside the PACO, the correlator could be expanded with an enable signal. Then the correlation could just be stopped and put out 0 (or a bit more complicated, feed this signal to all following stages to stop). The advantage of this would be less power consumption (TBD how much is possible). However, the synchronization problem persists, respectively is increased if all the following stages are disabled. The timeline is shown below.

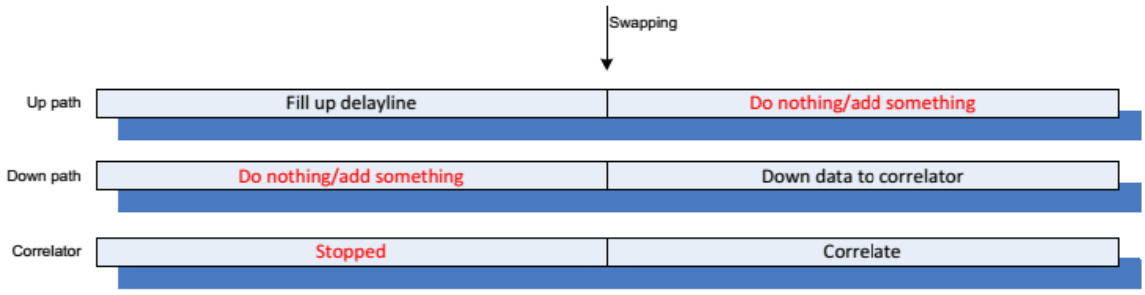


Fig. 4-3: Semi-swapping concept 3

It is currently not decided what the best option for the semi-swapping is. This will be discussed during the project, especially what the impact on software side and scientific output will be (if there is any difference at all). Preliminarily the second option seem the simpler to implement but deeper analysis is required.

4.4.4. OTHER SIMPLIFICATIONS

The following issues have been assessed as possible options in order to reduce cost but still keeping the functionality as requested in RD-1.

4.4.4.1 REDUCTION OF PACO RESOURCES

The current PACO implementation uses about 6Mbit of FPGA memory, whereas the most part of it is used by the delay line (around 4.6Mbit). The reason for the long delay line (10ms) was the original targeted orbit of the PARIS satellite. However, the ISS has a much lower orbit, where the maximum delay between the direct and reflected signal is less than 4ms. Therefore, a change of the delay line to half its size would free a lot of PACO internal resources. In addition, the reduced amount of BRAM makes additional FPGA types suitable for implementation.

Due to the ISS altitude the maximum swapping time would be 2.35ms. For radio occultation the depth of the delay line has to be equal to the longest coarse acquisition code period of all GNSS systems for the interferometric radio occultation to work. This corresponds to 4ms for the GALILEO constellation. So the depth of delay line can be reduced till 4ms. It is suggested to implement a 5ms delay-line, because reducing by exactly the half is easier to implement/adapt.

Considering the number of lag correlators (currently 400 lags => 401 results), one reduction in complexity for the PACO would be to reduce the number of correlators. This helps especially if the target technology are FPGAs, because FPGAs have a limited number of Digital Signal Processing (DSP) blocks which are used for multiplications. If these resources are already

used, the synthesis tools build the multiplier with registers and lookup tables (LUT), hence the utilization increases dramatically. However the margin of lags is so small, around 200m, that is not recommended to reduce the number of correlator. However reducing the number of Doppler lines to the strictly required by the SRD, 9 lines, is possible. In case the chosen technology is limited due to resources, this will be considered for the implementation.

4.4.4.2 REMOVAL OF SPU DC/DC CONVERTERS

Due to the reduced number of PACOs and boards, the need for dedicated DC/DC converters is not given anymore. Therefore the costs for design, implementation and test are immediate cost savers. The assumption is to receive one intermediate voltage (~5V, TBC) from the PSU and generate all necessary voltages for the SPU onboard (via Point of Load converters).

4.4.4.3 FPGA IMPLEMENTATION

The required performance as well as the computational complexity, which translates directly into increased demands of logic resources, limits the selection of suitable devices to a small set of high speed, space qualified FPGAs:

- Xilinx XQR5VFX130
- Xilinx RT-ZU19EG
- Microsemi RTG4G150
- NanoXplore NG-MEDIUM

The current time frame for the QML-V qualification of the ZU19EG is in 2018, which would suit GEROS-ISS very well. Considering the available resources, the ZU19EG is large enough to host 4 PACOs inside (including all Block RAMs). In addition, the Zynq platform features onchip processor (ZU19EG: Quad-Core ARM + Dual-Core Real Time Core), which could be used as PACO ICU. Having all the needed PACOs inside one chip, would additionally remove the need for any SpW router boards. The first ZU19EG commercial boards are already available, making first prototyping possible.

A European alternative for the Altera/Intel and Xilinx FPGAs is NanoXplore, which is going to develop a set of space qualified (QML-V) FPGAs. The current knowledge is that 3 types will be made available, referenced as NG-MEDIUM, NG-LARGE and NG-ULTRA. The NG-MEDIUM is intended to be an alternative for the Actel RTAX2000, whereas the NG-LARGE is targeted to be a competition to the RT4G150. Since the RT4G150 and NG-LARGE have about the same resources, this would be an option for the GEROS-ISS. The NG-LARGE is expected to be available (in QML-V) for 2019, which is still in the time-frame for the GEROS-ISS. It is still to be evaluated, how the actual hardware/software performs (in terms of VHDL code to hardware). Moreover, the NG-LARGE features an on-chip hard processor core, which could be used for calculations “on PACO”, instead of using the ICU.

If the selection has to be based on current available technology, only the XQR5VFX130 and RT4G150 are left. Due to the higher number of DSP blocks, which are the critical part for FPGAs due to the high number of complex multiplications inside the correlator, the RT4G150 is preferred.

All feasible space qualified FPGAs are in the same price category, hence the following cost break-down is independent of the chosen FPGA technology. A comparison to the ASIC costs

shows, that the costs for FPGAs are higher (per part), but there are no NRE costs. For the current design, the costs for ASIC and FPGAs will be about the same.

The usage of FPGAs is preferred for the GEROS-ISS project, since the lead time for an ASIC is rather long and therefore the design and verification phase will be critical. Choosing one of the FPGAs allows for early procuring a COTS breadboard for implementation on the target hardware.

4.4.4.4 COTS FPGA IMPLEMENTATION

Currently there are a wide range of COTS FPGAs available. One of these is the Cyclone V part, which is used in the commercial available MitySoM platform. RSA has already used this platform in house, especially for the validation of the PACO signal processing core, since this device is also intended for CubeSats (OPS-SAT and the PRETTY mission). Although the number of lags has been reduced for the validation, one option would be to use two Cyclone V chips in series to achieve the needed 400 lags.

Deeper analysis should be needed. The cost of FPGA parts can be divided by more than 10 times.

4.4.4.5 FPGA vs. ASIC IMPLEMENTATION

The following table sums the risks associated to every possible implementation

	PACO type	Design effort	Technology Risk	Schedule Risk	Costs
GEROS original	ASIC	↑	↓	↑	↑
GEROS reduced	ASIC	↗	↓	↑	↗
GEROS reduced FPGA	FPGA	↗	→	↘	↗
GEROS reduced COTS	FPGA	↗	↗	↘	→

Table 4.1 Risks for PACO implementations

- GEROS original ASIC: ASIC imposes high schedule risk (lead time), but low technology risk (space heritage)
- GEROS reduced ASIC: ASIC imposes high schedule risk (lead time), but low technology risk (space heritage)
- GEROS reduced FPGA: QML-V FPGAs have space heritage, but the costs are still high. However, with the currently available technology, the implementation is challenging (w.r.t resources and timing)
- GEROS reduced COTS FPGA: COTS FPGAs have the highest amount of resources available, but need to be proven for space (or cold redundant boards). Mission availability could be affected. Dedicated design techniques are needed to reduce TID and SEU effects.

4.4.4.6 PACO RESOURCES vs. FPGA RESOURCES

Below you find an overview between the Zynq and the Virtex vs. PACO utilization.

	PACO usage	Virtex 5 available	Zynq available	Factor Zynq vs Virtex	Factor Zynq vs utilization
DSP slices	379	384	1968	5.13	5.19
Block RAM	5904	16416	34600	2.11	5.86
LUT	67706	122880	523000	4.26	7.72
FF	50243	122880	1045000	8.50	20.80

Table 4.2 PACO vs FPGA resources

From these theoretical numbers, it is safe to assume that 2 PACOs fit into one Zynq, with a high chance to fit 4 PACOs.

4.5. ICU

4.5.1. GENERAL DESCRIPTION

The Instrument Control Unit (ICU) is in charge of the overall instrument control, data handling, data storage and interface towards the ISS. It reacts to ground operational commands to control all the elements of the payload.

The ICU is based on a unit composed of two completely redundant parts assembled in a common mechanical housing hosting three different types of board per section plus two boards common to both sections:

- Columbus Interface Module (CIM). In charge of the instrument's data processing and communication with the APM module and instruments down-stream units (BFNs, SPU, POD, and CAL/LNAs). This module hosts the processor and the different SW products (Boot and Service Software and Application Software) which are in charge of the GEROS payload mode management, thermal control and FDIR, and the PUS services implementation.
- Specific Interface Module (SIM). This module is in charge of generation and acquisition of discrete standard interfaces (as thermistors, voltages, currents) needed for monitoring, reporting and control of the complete instrument. Also some interfaces are delegated from the CIM such as the Spacewire router and the SPU reset signals.
- Converter Module (CM). In charge of providing Power Conversion functions, as the ICU service DC/DC Converter.
- Clock Distribution Module (CDM). Amplifying, splitting and combination of master clock signal to be distributed towards the GEROS Payload units.
- Backplane (MB) connecting all modules and performing the signals cross-strapping where needed.

The main operational functionality is implemented by software. The functional interface with the APM module is managed by the SW using HW interfaces built in an external to the processor FPGA. Operational functionalities shall be implemented by PUS Services SW modules delegating tasks to other modules and finally recurring to HW (FPGA) modules to command / control the payload.

The functionalities of the ICU can be split into general and specific to the mission. The general functionalities of the ICU are the TM/TC interface towards the master module, the APM module for GEROS, the time management, memory management, analogue housekeeping signal acquisition FDIR and thermal control.

The GEROS-ISS mission specific ones are:

- Spacewire network routing
- Ethernet interface
- Master clock generation and distribution
- Beam tables management
- File transfer service
- Scientific data management (i.e. timing, etc)

For the operational control of GEROS payload the ICU is in charge of the synchronized CAL/LNAs switching/swapping and PACO un-swapping, the BFN online beam configuration and the SPU online configuration via commands. Currently the basic commandability of PACOs is composed of Polynomial coefficients transmission, un-swapping programming, selection of coherent and incoherent integration time, the Doppler bins configuration, the Spatial resolution configuration, selection of FIR filter and down conversion frequency.

4.5.2. ICU MODULES

4.5.3. CIM board description

The main CIM elements are a microprocessor based on a Leon2-FT core and an IO Controller (IOCtrl) FPGA providing IO management functionalities for Memories, and the hardware control for the CAL/LNA and BFN buses. Other elements are the communication interfaces (LVDS, SBDL, SPI, etc.), local power regulators and memory banks.

The block diagram for the CIM based on MDPA (Multi-DSP/Micro-Processor Architecture) is shown in Fig. 4-67.

The MDPA ASIC, together with the memory banks and transceivers, implements the following CIM functions:

- Processor function
- UART controllers 1&2 (not used)
- SpW controllers (instrument and internal links)
- Two 32 bit timers
- 1553 controller

The FPGA, together with some of the transceivers, implements the rest of CIM functions:

- Ethernet controller
- Monitoring function
- Datation function
- Synchronization function
- Memory controller
- ICU internal bus controller
- Two General purpose timers
- CAL/LNA and BFN control and interface implementation
- Communications with the SIM board

This board is not relevantly simplified from the complete GEROS-ISS architecture. The FPGA module for CAL/LNA control is simpler but the number of RS422 interfaces has increased. It has been detected from the previous project that the MDPA chip does not include the Ethernet control interface and so it must be developed to be included in the FPGA.

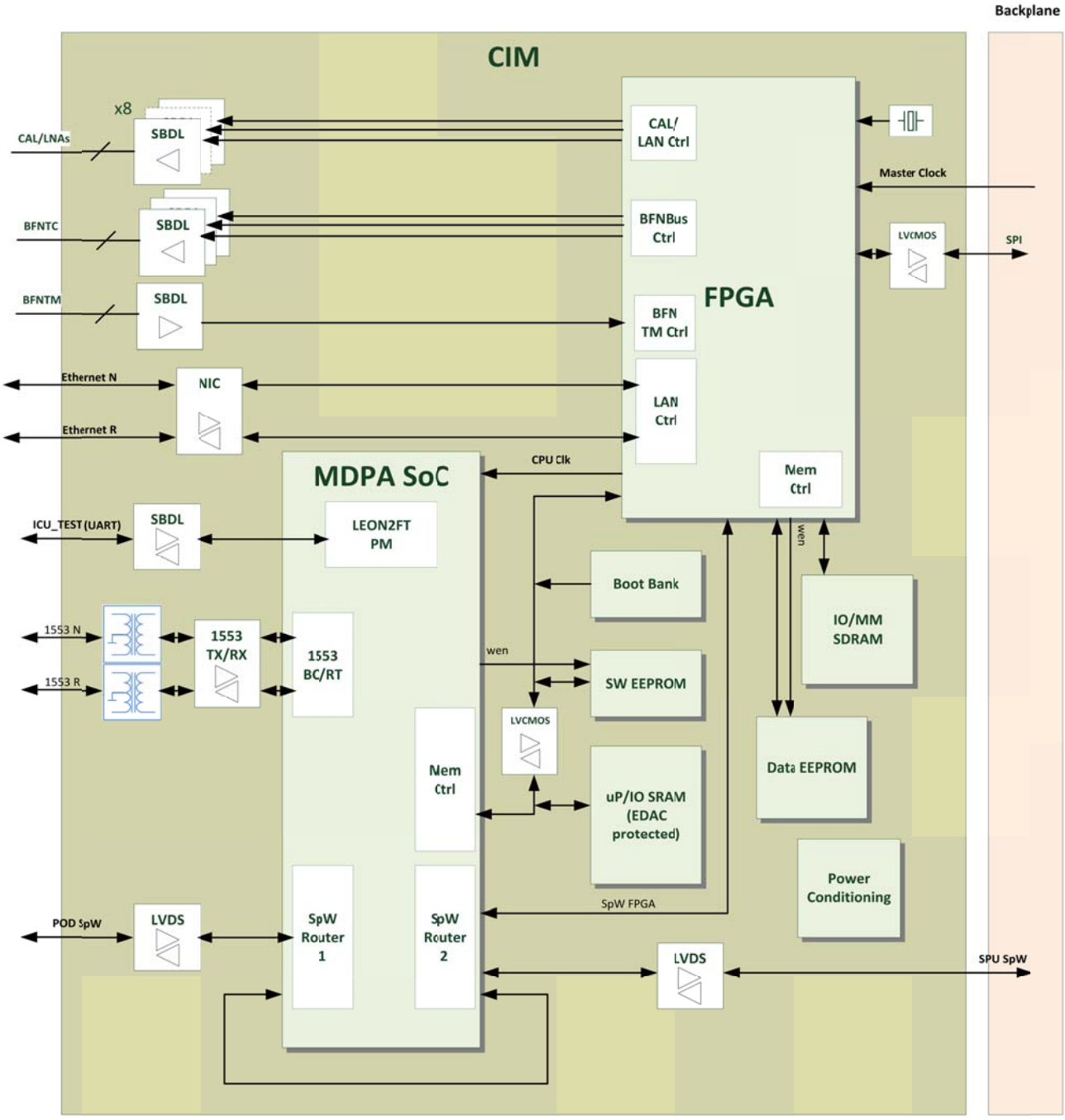


Fig. 4-4: CIM breakdown and interfaces

4.5.4. SIM board description

The SIM board is the board devoted to implement the standard interfaces for acquisition and generation for the GEROS Instrument Control Unit. SIM implements the acquisition for internal and external analog telemetries, thermistor, voltages, currents, and relay status. Other special needs for GEROS payload are implemented on this board such as the Spacewire network routing and external communication to SPU and the reset signals to the SPU.

The SIM Module implements into six main functional blocks:

- TM/TC Control FPGA or ASIC: a general-purpose module intended for communicating a slave electronic module with a master one in order to command and control their different internal functions (command generation, Bilevel / Relay status acquisition, Analog Acquisition and serial interfaces).
- External interfaces: RSA acquisition, Analog (ANY, ANP & AN2) acquisition.
- Internal interfaces: SPI.
- Spacewire routing
- Power conditioning.

This board is also not relevantly simplified from the complete GEROS-ISS architecture. The number of interfaces in order to reset the PACOs has been reduced and the router has less outputs, it is possible that a cheaper router could be found. But still both changes are not relevant for the cost.

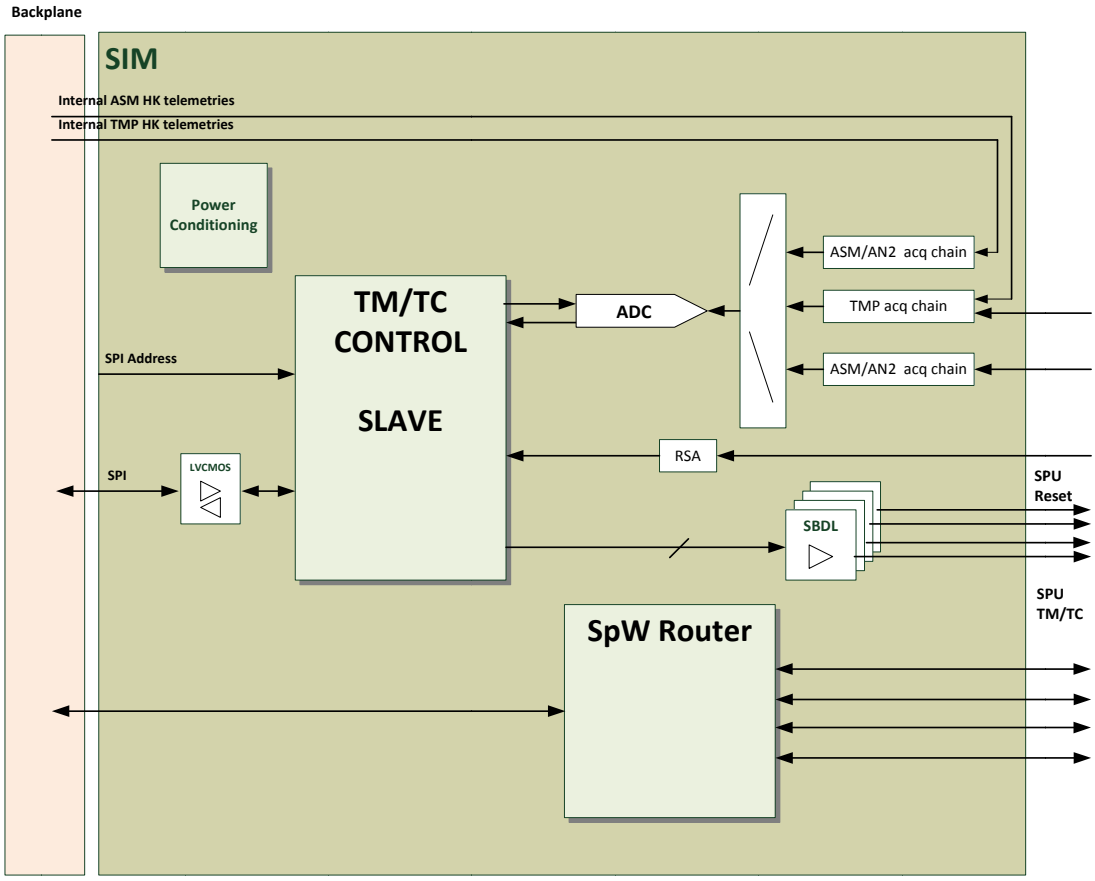


Fig. 4-5: SIM breakdown and interfaces

4.5.5. Master Clock distribution board

The GEROS payload requires a common master clock to perform synchronized operation. The commonality of the master clock is critical for the ADC sampling and the digital correlation of signals. The same clock is also used for down-conversion to IF.

It is under responsibility of the ICU to generate the common ultra-stable clock and to prepare the signal to be distributed via coaxial harness towards all the payload. The SPUs and BFNs are the destination units. Each SPU requires one clock signal per SigProc board and each

BFN requires two redundant clock signals per BFN. So a mix of signal combination and signal splitting plus some amplification is required due to the amount of receivers.

The master clock to be distributed is agreed to be a sinusoidal signal. This kind of signal helps to reduce some of the clock signal distribution problems in contrast to typical pulse or square wave clock signals. For the distribution, the CDM must ensure all master clock path lengths matching at the connector output of the unit.

Within two redundant sections, which share the same board, two ultra-stable master clocks are generated. Both clocks are filtered to minimize the clock signal harmonics to leave the clock as a sinusoidal one if not directly generated as so. Both clocks are amplified and later combined to allow the transmission of both clocks to the SPU, independently of which ICU section is switched on. And finally the master clock is split to the 18 output connectors (4 for the SPU and 1 to the BFN).

Surface mount power splitter / combiners are foreseen to be used searching for minimum phase unbalance.

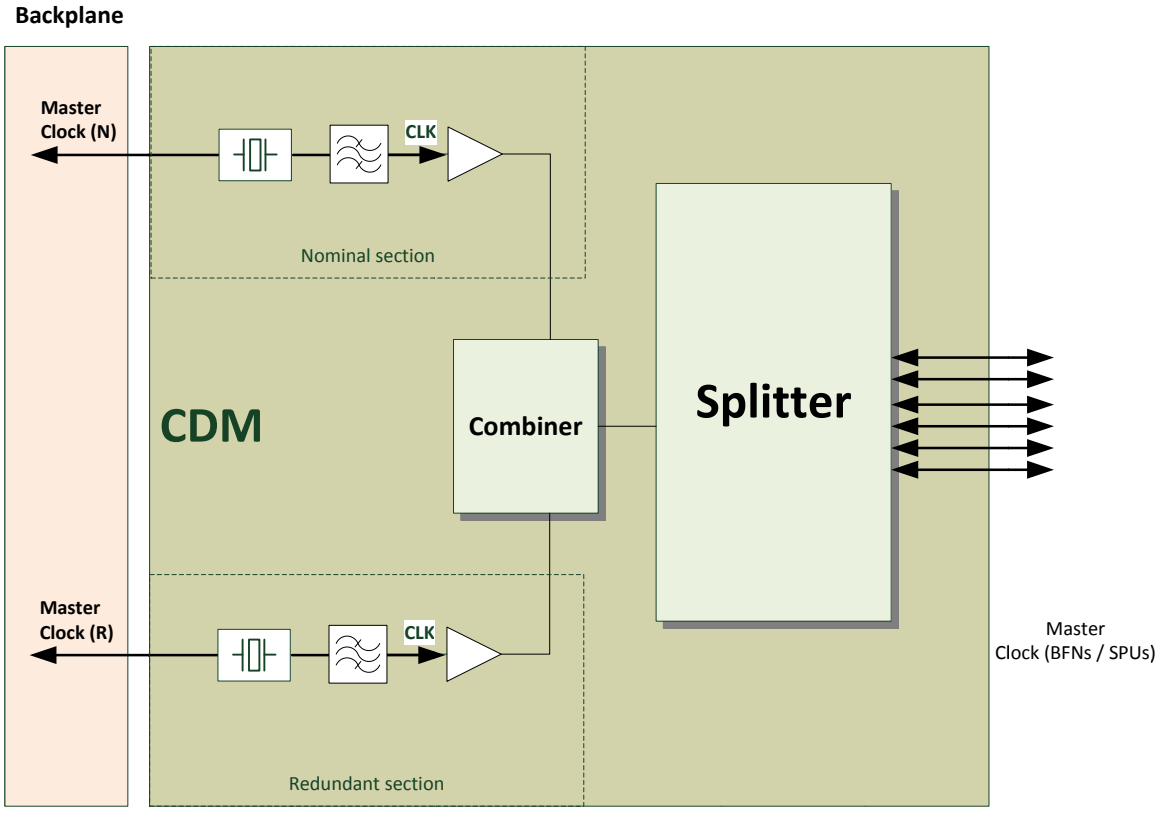


Fig. 4-6: CDM breakdown and interfaces

The splitter has been deeply simplified. This is maybe the most relevant change associated with the ICU. Still not very cost relevant.

It is worth the effort to mention the risk that a PLL is required in order to clean the phase noise of the oscillator. It is not quoted during the previous study and it is considered that a risk should be added to the cost estimation.

4.6. PSU

4.6.1. GENERAL DESCRIPTION

The PSU is capable of the following tasks:

- transformation of the 120VDC bus voltage provided by the ISS to a power bus voltage at 28VDC towards GEROS payload units (i.e. BFN, POD, ICU)
- DC power supply to CAL/LNA modules (15 modules are supplied), 2 voltages
- common LCL protection to each CAL/LNA generated voltage
- individual short-circuit protection to each CAL/LNA avoiding failure propagation
- generation, regulation and protection of the output DC voltages as required by the SPU,
- electrical input and output protection,
- limiting the power outlets (ICU, POD, BFNs) inrush current by LCLs

The redundancy level is considered at input and output level.

- A dedicated DC/DC converter shall be associated to each 120VDC power feed (N&R).
- Redundant DC/DC converter per CAL/LNA voltage
- Redundant DC/DC converter per SPU voltage
- LCL redundancy per payload unit

The CAL/LNAs share the voltage converter, so protection devices must be considered to avoid failure propagation. Due to high number of elements LCLs, one per voltage and element is not affordable so fuses are considered the best solution. A fuse is added per voltage and CAL/LNA.

The number of CAL/LNA outlets are reduced but the costly element which is the DC/DC converter is kept. A new DC/DC conversion stage has been added to provide secondary supply to the SPU.

4.6.2. BLOCK DIAGRAM / ARCHITECTURE

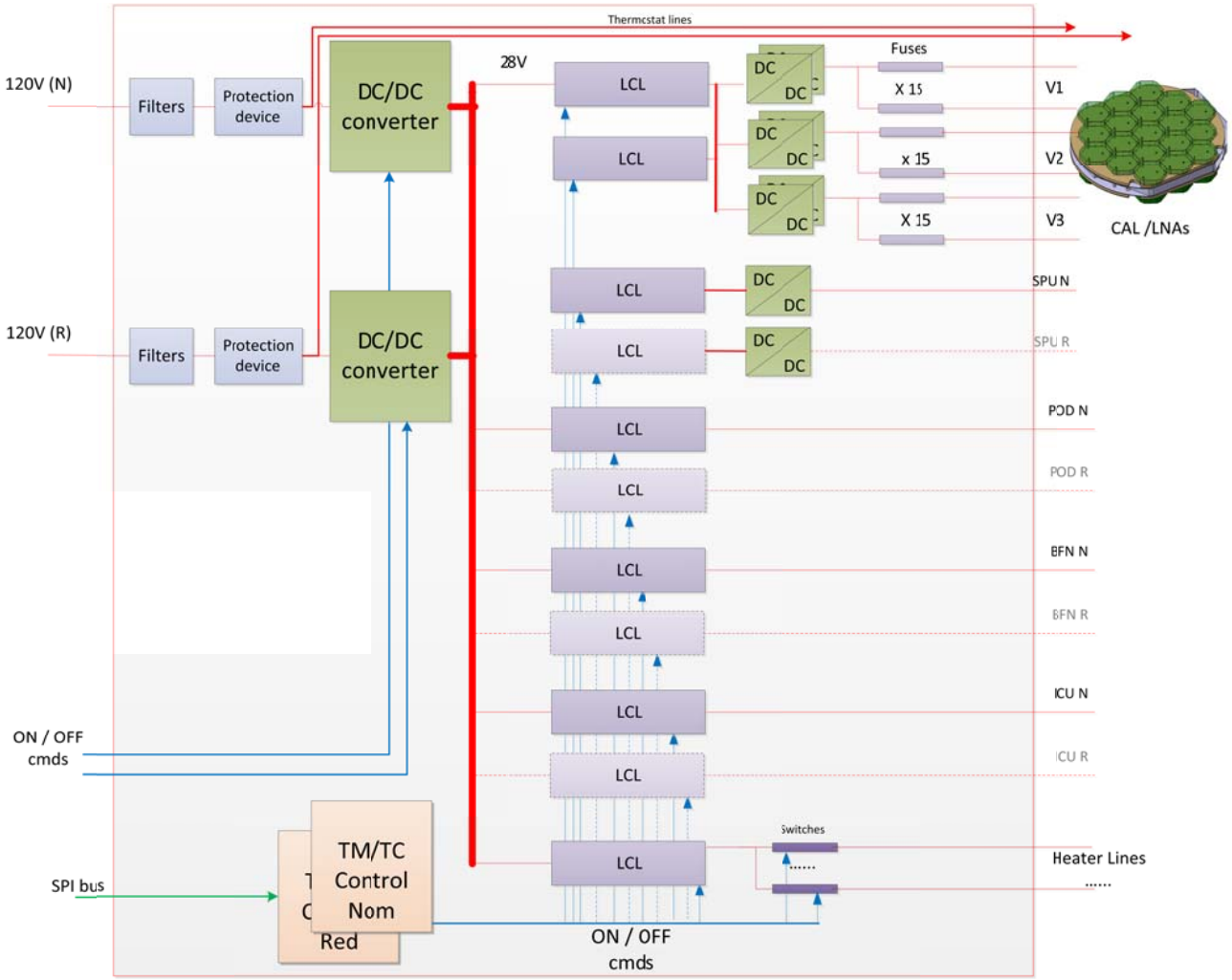


Fig. 4-7: PSU block diagram

5. BUDGETS

5.1. DATA RATE BUDGET

Following the new operational modes of the reduced GEROS-ISS Payload described below a new data rate table has been built.

Mode Number	Name	Geometry	Swapping	Down Pol	Freq	DDM	Type waveform
1.1	Near – Nadir altimetry	FoV1	Y	L	F1,F5	000-111-000	P + C
1.2	Forward Scatt. RL	FoV1	Y	L	F1,F5	333-333-333	P + C
1.3	Backward Scatt. RL	FoV1	Y	L	F1,F5	333-333-333	P + C
2.1	Grazing Altimetry	FoV2 Fov3	N	R	F1,F5	000-030-000	C
2.2	Radio Occultation	FoV2 Fov3	N	R	F1,F5	000-030-000	C
3.1	Forward Scatt. RR	FoV1	Y	R	F1,F5	333-333-333	P + C
3.2	Backward Scatt. RR	FoV1	Y	R	F1,F5	333-333-333	P + C
4	SAR Altimetry	FoV1	Y	L	F1,F5	333-333-333	P + C

Table 5.1 Operational modes

	Applications									
Parameter	ANA	(B)FSRL	(B)FSRR	RO GA	SAR					
Number of delay points	400	133	133	133	133					
Coherent integration time (ms)	1	1	1	1	1					
Size of correlations (bits)	32	32	32	32	32					
Number of beams Nb	1	1	1	1	1					
Number of frequencies	2	2	2	2	2					
Ni: Incoherent integration (1 to 1000samples)	1000	1000	1000	1000	1000					
Incoherent integration time (s)	1	1	1	1	1					
Waveform	P+C	P+C	P+C	C	P+C					
Doppler shifts (Nd) 1 means 1 bin of same number of points as specular. 0.5 means half number of points	2	8	8	0	8	Total 2 ANA	Total 1 ANA + (B)FSRL	Total 2 (B)FSRR	Total 2 RO|GA	Total 2 SAR
Beams data output data rate (Kbps)	25.6	8.5	8.5	8.5	8.5	51.2	34.1	17.0	17.0	17.0
Doppler shifts data output data rate (Kbps)	51.2	68.1	68.1	0.0	68.1	102.4	119.3	136.2	0.0	136.2
Instrument data output data rate (Kbps)	153.6	153.2	153.2	8.5	153.2	307.2	306.8	306.4	17.0	306.4
Instrument HK data (Kbps)						1.0	1.0	1.0	1.0	1.0
TOTAL Instrument Data rate (Kbps)	153.6	153.2	153.2	8.5	153.2	**308.2**	**307.8**	**307.4**	**18.0**	**307.4**
Orbital Time (minutes)	97	97	97	97	97	97	97	97	97	97
Data Generated per orbit (MB) with DC=100%	112	111	111	6	111	**224**	**224**	**224**	**13**	**224**
Downlink rate(kbps)	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000
Data Downloaded per orbit (MB)	728	728	728	728	728	728	728	728	728	728

Parameter
Number of delay points
Coherent integration time (ms)
Size of correlations (bits)
Number of beams Nb
Number of frequencies
Ni: Incoherent integration (1 to 1000samples)
Incoherent integration time (s)
Waveform

Doppler shifts (Nd) 1 means 1 bin of same number of points as specular. 0.5 means half number of points
Beams data output data rate (Kbps)
Doppler shifts data output data rate (Kbps)
Instrument data output data rate (Kbps)
Instrument HK data (Kbps)
TOTAL Instrument Data rate (Kbps)
Orbital Time (minutes)
Data Generated per orbit (MB) with DC=100%
Downlink rate(kbps)
Data Downloaded per orbit (MB)

Table 5.2 Data Rate Budget

The result is a maximum data rate of 308kbps, far below the 1126kbps of original GEROS-ISS system.

5.2. POWER BUDGET

POWER BUDGET (Dissipation)--> GEROS Instrument						
Item	Nominal Power (W)	Margin (%)	Power with Margin (W)	Quantity	Subtotal Nominal (W)	Subtotal with margin (W)
CAL/LNA	1,68	20	2,02	15	25,20	30,24
BFN	5,54	20	6,65	2	11,08	13,30
SPU	36,00	20	43,20	1	36,00	43,20
ICU	20,00	20	24,00	1	20,00	24,00
PSU	40,58	20	48,70	1	40,58	48,70
POD Rx	20,00	20	24,00	1	20,00	24,00
Heater power	0,00	20	0,00	1	0,00	0,00
				TOTAL (W)	152,86	183,43

Table 5.3 Power Budget

The average power demand is of 184W, much lower than the 395W of original GEROS-ISS system.

5.3. MASS BUDGET

MASS BUDGET --> GEROS Payload (total)						
Item	Nominal Mass (Kg)	Margin (%)	Mass with Margin (Kg)	Quantity	Subtotal Nominal (Kg)	Subtotal with margin (Kg)
Up-looking Platform	12.90	20	15.478	1	12.898	15.478
Down-looking Platform	7.08	20	8.491	1	7.076	8.491
Equiped Right Panel	1.34	20	1.606	1	1.338	1.606
Equiped Left Panel	1.34	20	1.606	1	1.338	1.606
Radiators	.20	20	0.240	30	6.000	7.200
CAL/LNA	1.74	20	2.088	15	26.100	31.320
BFN	7.52	20	9.024	2	15.040	18.048
ICU	8.00	20	9.600	1	8.000	9.600
PSU	8.00	20	9.600	1	8.000	9.600
SPU	7.00	20	8.400	1	7.000	8.400
POD Rx	6.00	5	6.300	1	6.000	6.300
Equiped CEPA Brackets	4.05	20	4.854	1	4.045	4.854
Supports Between Panels	1.18	20	1.414	1	1.178	1.414
Electrical Harness	8.00	20	9.600	1	8.000	9.600
RF Harness	.03	20	0.038	126	4.032	4.838
CEPA	117.00	0	117.000	1	117.000	117.000
				TOTAL (Kg)	233.045	255.354

Table 5.4 Mass Budget

The total system mass is of 255kg, much lower than the 375kg of original GEROS-ISS system.

Also a huge refinement is needed for the mechanical and thermal HW after a detailed thermal and mechanical analysis. The mass number can be taken as a reference anyway.

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