A rad-hard time-to-digital converter

Executive Summary

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During 2021 and first half of 2022 Magics Technologies has designed and validated a time-to-digital converter ASIC in the scope of ESA's OSIP program (ESA Contract No. 4000132900/20/NL/GLC). The project officer for ESA was Boris Glass.

The goal of this ESA ITI project was prototyping, and validation of a radiation-hardened Time-to-Digital Converter (TDC) in a commercial CMOS technology. The developed TDC ASIC is able to measure time differences between a start and stop signal and convert this to a digital value with an accuracy better than 10 picoseconds. It supports 'single shot' operation, which means it can carry out the conversion with the proposed accuracy even from a single start and stop signal, without averaging or noise shaping.

The main objectives of the project were:

- Integration and prototyping of a radiation-hardened time-to-digital converter in a commercial CMOS technology.
- Electrical characterization and performance benchmarking of the TDC. The TDC is expected to achieve sub-10 picosecond single-shot precision, with more than 100 microsecond measurement range.

The innovation content of this project was focused on the following aspects:

- Current radiation tolerant TDCs are mostly based on radiation tolerant FPGAs with a resolution of around 100 ps and radiation tolerance up to merely 10 kGy. FPGA based TDCs suffer from high power consumption, high implementation cost, large device size, and limited resolution. The TDC proposed in this project will be implemented in a mainstream commercial CMOS process, which offers highest integration level, lowest power consumption, and lower fabrication cost for volume production.
- It has been shown that ionizing radiation causes changes in transistor parameters, increases 1/f noise and worsens mismatch problems. Especially the latter two effects have a huge impact on the accuracy of TDCs. Indeed, the TDC relies on accurate delay cells which process the start and/or stop signals. It is of crucial importance that these cells maintain a constant delay in spite of the harsh radiation environment. In this project, innovations will be proposed to achieve sub-10 ps performance in the presence of ionizing radiation. The circuit will also be hardened against Single-Event Effects (SEEs) to recover quickly from any cosmic particle impinging on the circuit.
- For this circuit, a Total Ionizing Dose (TID) tolerance of 100 kGy, and an SEE tolerance up to a Linear Energy Transfer (LET) of 100 MeV/mg.cm^2 is targeted. These requirements are in line with the most extreme environments encountered in space, ITER (International Thermonuclear Experimental Reactor), the demonstrator fusion reactor being built in Cadarache, France, and the HL-LHC (High-Luminosity Large Hadron Collider) and its embarked experiments at CERN, and which all extend far beyond the current state of the art.
- The specific objectives presented above, will also encompass more generic objectives by requiring:
    - ground-breaking architectural, circuit and layout techniques for radiation tolerant time-based ICs;
    - innovative methodologies for the development of future radiation tolerant systems.

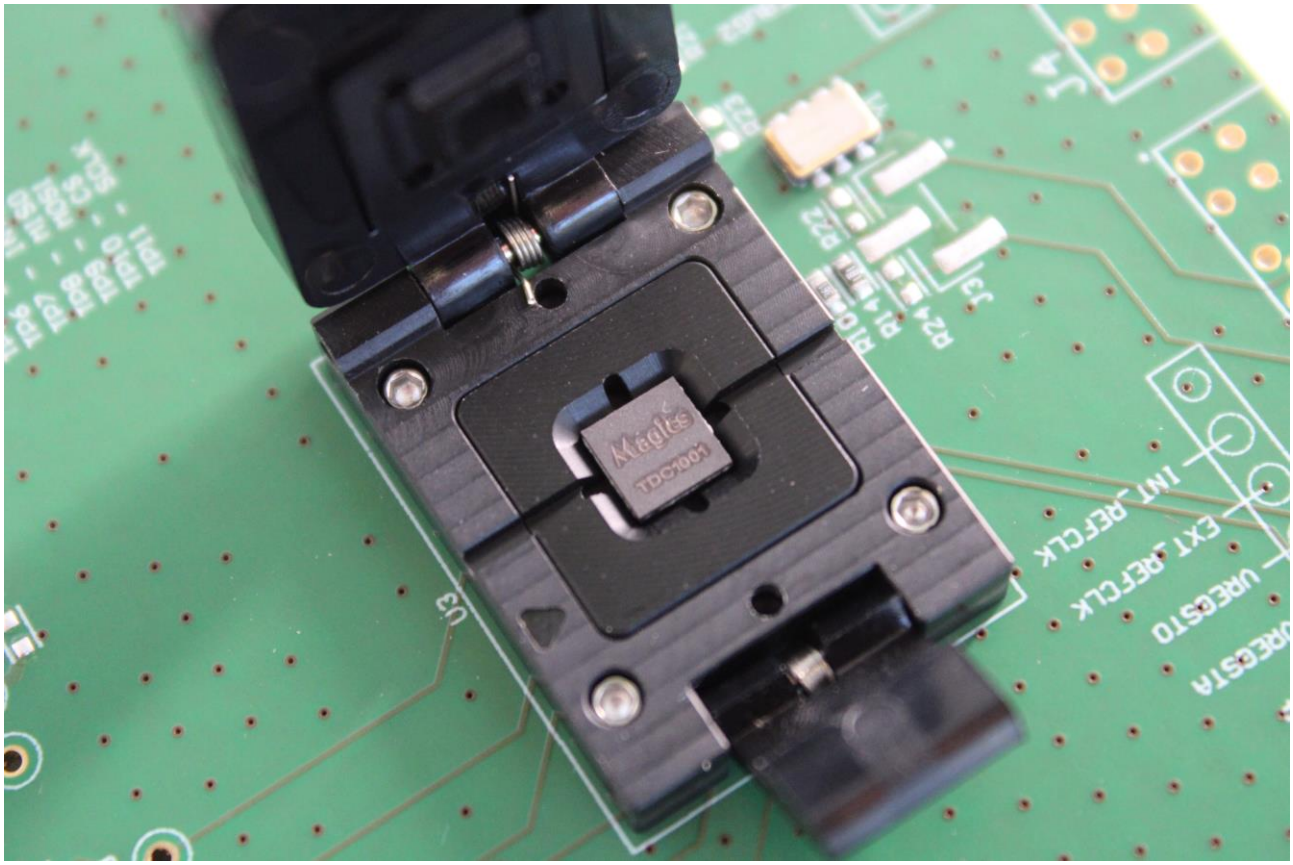

Figure 1: The TDC ASIC prototype packaged in a QFN-24 and mounted in the test socket

Thanks to the expertise of the Magics engineering team a novel architecture was selected that is able to combine fine granularity (<10ps), excellent single-shot precision, a wide measurement range with a zero dead time and low power consumption in a fully integrated ASIC solution.

The schematic and layout designs of the ASIC have been finalized in November 2021 and the manufacturing was started. When the samples arrived in March 2022, Magics managed to confirm first fully functional results under typical circumstances in less than a week time. The full charactarization of the ASIC was done in Magics' lab facilities. Full characterization of the ASIC for different supply and temperature variations was performed and confirmed that all the key specifications of the ASIC were met in a first-time-right project.

The further development and optimization of the characterization program has led to submission of the validation report by end of May 2022. It confirms that our TDC ASIC can reach sub-10ps granularity and single-shot precision in a zero-dead-zone range of up to more than 1ms under all supply and temperature variations applied in the bench characterization.

The closure of the characterization activities brought Magics to the closure of this running project. The TDC ASIC is currently at TRL 4. Irradiation measurements were not in the scope of this project. In order to further develop this chip to a higher TRL level Magics plans to bring the ASIC into a qualification program, optionally after a respin of the design for increased application friendliness. The target is to have this ASIC into flight model before the end of 2023.