

# **Project Web page**

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| HEADER INFORMATION | |
| Project short name | RESPECT-DEM |
| Project full name | Reliable Signal Processing Datapaths Design Using Iterative Techniques Based on Difference Equation Models |
| Contract number | 4000134184 |

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| Project Objectives | The project aims at developing iterative based methods for increasing the reliability of DSP circuits operating in radiation prone space environments. Three major constraints are set: (i) latency: the error free execution flow must not be hindered by the detection and correction mechanism; (ii) cost: the data storage overhead is similar to a dual modular redundancy; (iii) decoding performance: multiple errors can be corrected. The ingredients for achieving these are iterative correction loops using gradient based optimizations, and error correction codes. The first are well known methods from the optimization theory, while the second offer an efficient way to obtain redundant data. The remaining problem is to fuse these concepts such that the error correction protected data is efficiently processed by the linear transform, and in case errors occur, correction is provided by the gradient descent based method iterative loop. |
| Challenges | Two main challenges had to be addressed in this project: (i) developing an efficient decoding algorithm for real number parity based error correction codes, and (ii) providing an efficient way to embed the processing associated to the error correction code - encoding, syndrome check, decoding - into the signal processing architecture. |
| Current status | The correction uses a gradient descent based iterative algorithm for real number parity based error correction codes to extract the error from the syndrome vector. The linear transform property of the target application allows for a correction offset to be computed and applied to the output data. The proposed iterative correction method has been validated for both small parity codes - such as BCH -, as well as codes on hundreds - thousands of symbols - such as quasi-cyclic LDPC. In both cases, FPGA implementations of fault tolerant extensions for FFT architectures have been provided. |



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