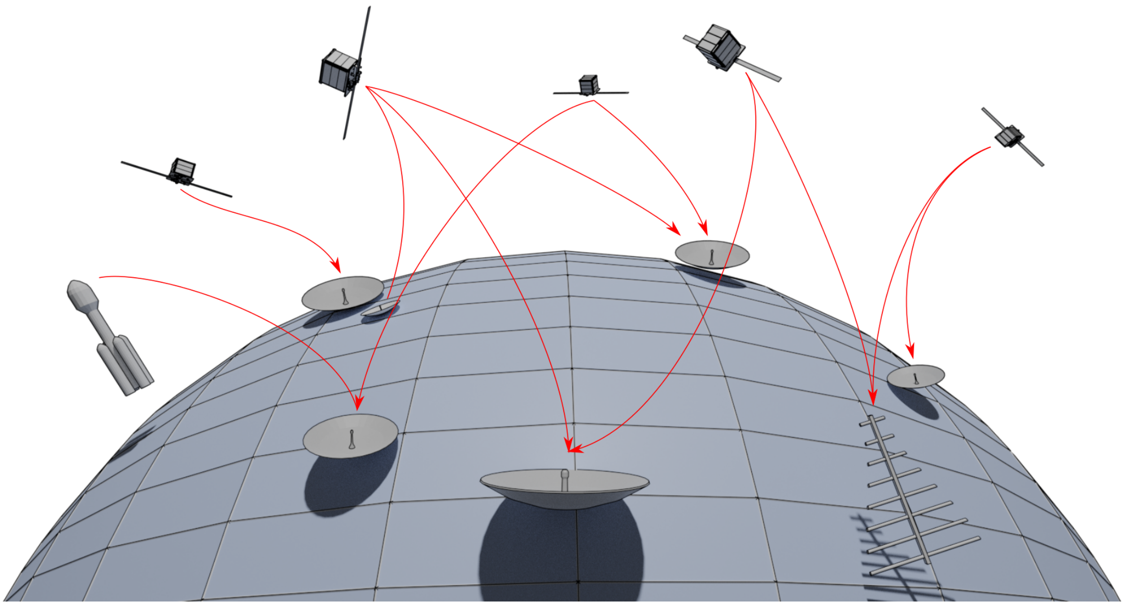

Satellite Identification and Localization experiment

Executive summary

OSIP Channel: OPS-SAT Experiments

Affiliation(s): Libre Space Foundation

Activity summary:
SIDLOC (Spacecraft Identification and Localization) is a new transmission scheme proposed by Libre Space Foundation to enable LEO satellite identification and tracking. The SIDLOC system relies on a reduced size autonomous transmitter that requires minimal integration and area on the carrier spacecraft. The ground segment of the SIDLOC system utilizes the existing SatNOGS network and the UHF band to perform the signal demodulation and identification. The SIDLOC system uses DSSS (Direct Sequence Spread Spectrum) PSK modulated signals with an effective bitrate of ~50 bits/s. The use

Publishing Date: 13/11/2023
Contract Number: 4000137338/22/NL/GLC/ov
Implemented as ESA Initial Support for Innovation>

of DSSS is crucial in order to achieve reliable reception with the minimum possible transmission power. Through an accurate Doppler frequency shift estimation mechanism, the SIDLOC system provides orbit determination capabilities, enabling open and independent SSA (Space Situational Awareness) activities. Despite the fact that SIDLOC operates using the downlink, a feature that is not available in OPS-SAT SDR frontend, vital information can be retrieved performing the mirrored case; one or more ground stations transmitting SIDLOC modulated signals to the satellite. The goal of this activity is to utilize the SDR capabilities of the OPS-SAT satellite, test the SIDLOC system under realistic conditions and identify the impact of the LEO channel impairments on the SIDLOC system.

The SIDLOC system

SIDLOC[1] (Spacecraft Identification and Localization) is a proposed standard for satellite and spacecraft identification and localization. It is developed as an ESA funded ARTES activity by Libre Space Foundation. The goal of the SIDLOC system is to provide reliable spacecraft identification and orbit determination, especially early after the deployment.

The SIDLOC system is using the DSSS modulation technique in order to provide a resilience to interference, low power transmission and accommodate multiple unmanaged concurrent transmissions. At a symbol level the BPSK modulation scheme is used for the resulting analog waveform.

The DSSS spreading is performed using a Gold[2] sequence. The period of the Gold sequence depends on the desired coding gain and the processing resources required for the demodulation. The larger the Gold sequence period, the more the processing gain. For SIDLOC the Gold sequence period is 2047 bits, which is a good compromise between the resources required for acquisition and decoding while having reliable communication for the orbits and transmissions power required by the system. To match the target chip rate of 1 Mcps (Mega Chips per Second), for each data bit the Gold sequence is repeated for 10 times as shown in Figure 1. The resulting effective data rate is:

$$R = Chip\ Rate\ /\ (len(Gold\ Sequence)\ *\ 10)\ =\ 1e6\ /\ (2047\ *\ 10)\ =\ 48\ bps$$

With the current frame format, each frame has a duration of ~7.8 seconds.

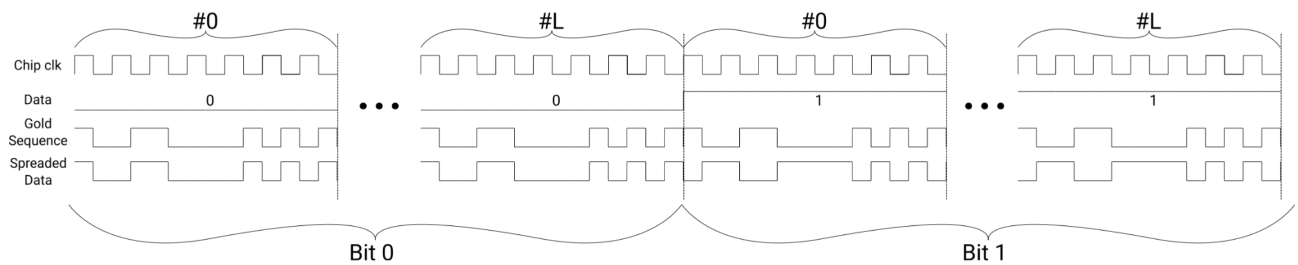

Figure 1: SIDLOC DSSS spreading process

[1] https://sidloc.org/

[2] Robert Gold. Optimal binary sequences for spread spectrum multiplexing (corresp.). IEEE Transactions on information theory, 13(4):619–621, 1967.

The repetition of the Gold sequence introduces an implementation loss in the overall link budget of the system, yet this loss is necessary to reduce the computational resources required for the demodulation and decoding of the system.

The most commonly used method for demodulation and decoding of DSSS signals is the cross-correlation based method. In this method, the incoming signal is cross-correlated with the complex conjugate of the modulated known Gold sequence. The output of the cross-correlation exhibits a strong and narrow peak, in the presence of an incoming signal with the appropriate Gold sequence. A simulated GNU Radio example can be found in Figure 2. Even in the presence of strong noise, the cross-correlation exhibits strong peaks in the presence of a DSSS signal. The drawback of this method is the computational resources required for the cross-correlation estimation. Even using FFT-IFFT to compute the cross-correlation, the huge FFT sizes do not allow for a real-time implementation. To deal with this issue a mixed approach utilizing coherent and non-coherent integration is used so the processing can be performed in real-time.

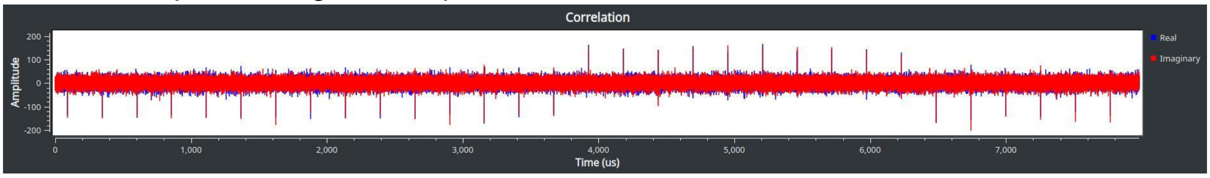

Figure 2: Cross correlation result of DSSS signal with -10 dB of SNR

Development

The goal of this experiment was to validate the SIDLOC system under realistic LEO impairments by operating all the necessary DSP tasks on-board the OPS-SAT satellite.
However, early on in the development phase the LSF team was aware of the possible limitations of OPS-SAT regarding the in-orbit execution of the SIDLOC system.

The first limitation was that the SDR could not operate into a continuous stream and the acquisition of signal was limited to 2.2 seconds at a time. This was a major and blocking issue, due to the fact that SIDLOC frames are quite long in duration. To deal with this issue the LSF team decided to add a stream-lined I/Q operation for the on-board SDR to the FPGA codebase of the satellite. To accomplish this, the DMA engine in the FPGA image was changed to a scatter-gather DMA engine. This enabled the existence of multiple receive buffers arranged in a chain which continuously store data as they arrive from the SDR. Moreover, to compensate for any delays between the SDR Core and the scatter-gather DMA engine, a dual clock FIFO was introduced between the SDR Core and the scatter-gather DMA (Figure 3). On the HPS side, a user-space driver[3] was implemented to control the scatter-gather DMA engine, providing an API for fetching the I/Q data in a continuous stream.

[3] https://gitlab.com/librespacefoundation/ops-sat-sidloc/ops-sat-sidloc-sw

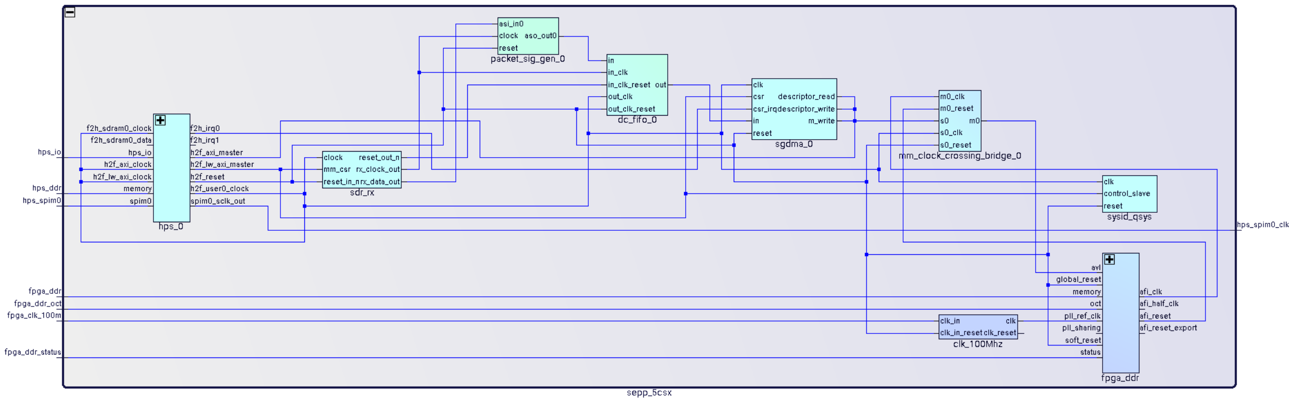

Figure 3: FPGA block design supporting streaming I/Q samples

The second limitation was related to the limited computational power of the SEPP (Satellite Experimental Processing Platform). Given the SIDLOC requirements in sampling rate and DSP tasks, it was obvious that significant simplifications would have to take place in order for the system to operate in real-time. Initially, a GNU Radio application was developed by porting the gr-sidloc[4] GNU Radio module, which is using GNU Radio 3.10, to the 3.7 version that is supported by the OPS-SAT[5]. Early tests revealed that the maximum achievable sampling rate was 50 kHz, far less than the 1 MHz requirement of SIDLOC. In an effort to meet the real-time requirements, the SIDLOC bandwidth was scaled down significantly. Several processing blocks have been removed also, like a software AGC and low pass filtering. Moreover, instead of coherent integration for the DSSS demodulation, a process that requires large sized FFT operations, the non-coherent method was used. All these simplifications had an impact on the link margin, introducing significant implementation loss. However, it was decided that this loss could be compensated by increasing the transmission power of the ground station. After a lot of effort and optimizations, the real-time limit was reached.

Unfortunately, by that time the OPS-SAT SEPP faced some issues operating in dual core more, and the only one CPU was usable. This did not allow for any DSP operation to run on real-time onboard. Therefore the choice was made to store the I/Q stream in files and fetch them later via the Data Relay Server for post processing on ground. Each I/Q capture had a maximum duration of 33 seconds, bounded by the maximum file size allowed.

Experiments

Two TX-capable SatNOGS ground stations were used during the experiments with identical RF-frontend setups (Table 1). The one codenamed “Talos” is located in Chania, Greece and the second one “Archodiko” is located in Kalamata, Greece (Figure 4).

[4] https://gitlab.com/librespacefoundation/sidloc/gr-sidloc
[5] https://gitlab.com/librespacefoundation/ops-sat-sidloc/gr-sidloc-port

In total three different runs were executed on OPS-SAT. Due to several issues with the ground stations, the third run had the biggest success. The uplink frequency used for all the experiments was 435.2 MHz.

Name	Location (lat, lon)	SDR	PA	Rotator	Antenna
[Talos]()	35.501°, 24.011°	USRP E310	RA07H4047M	Yes (SatNOGS)	Yagi X-Quad (14 dBi)
[Archodiko]()	36.971°, 22.145°	USRP B210	RA07H4047M	Yes (Yaesu)	Yagi X-Quad (14 dBi)

Table 1: Experiment SatNOGS ground stations details

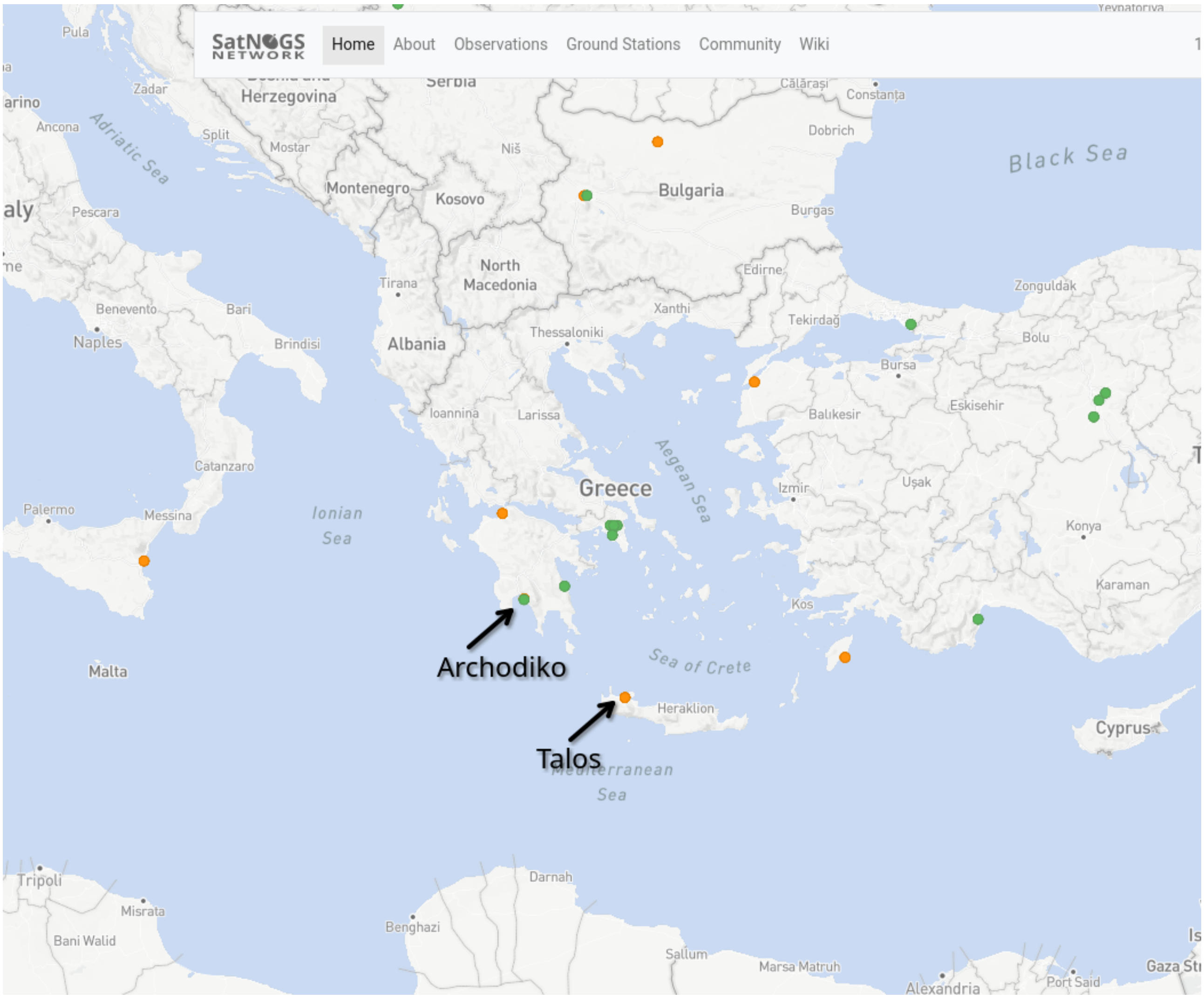

Figure 4: Experiment SatNOGS ground stations location

The experiment starting time was selected so both of the stations are in the field of view of the satellite and their transmission was initiated concurrently. The two stations were using different Gold sequences to take advantage of the low correlation properties that they provide, resulting in minimal interference between each other in the cross-correlation domain. In addition, the “Archodiko” station was also transmitting concurrently a CW tone at +250 kHz. The goal of this tone is to remove any ambiguity regarding the I/Q phase of the recording and also visually identify the progress of the experiment in the spectrum.

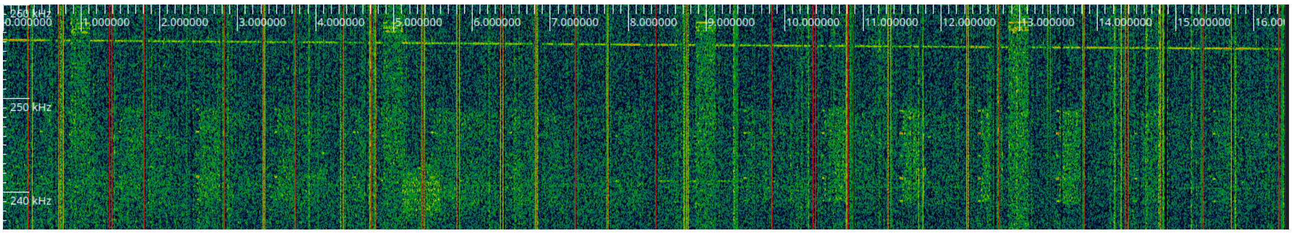

Figure 5: Spectrum of Run #1, at around +250 kHz

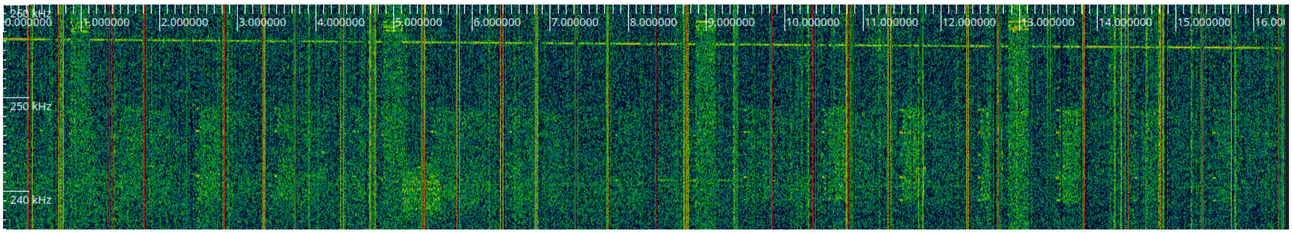

Figure 6: Spectrum of Run #2, at around +250 kHz

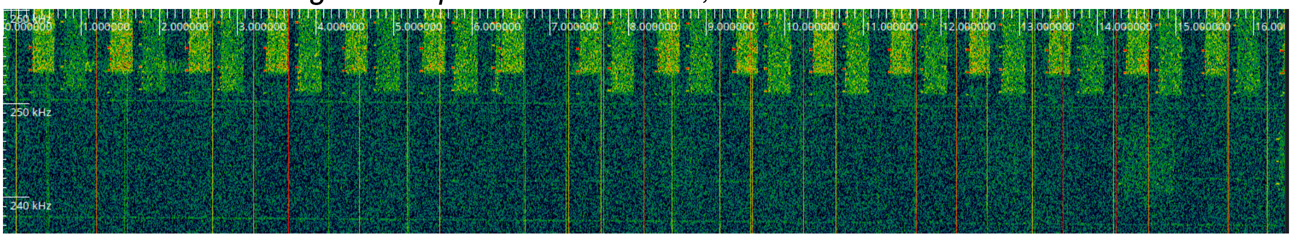

Figure 7: Spectrum of Run #3, at around +250 kHz

Careful analysis of the Doppler expected and comparison of the spectrograms of previous runs (Figures 6-8), revealed the CW signal presence at around +250 kHz, with a Doppler rate matching the expected one.

On ground SIDLOC analysis also gave more clear and distinct peaks of the GLRT metric as can be seen in Figure 8. These peaks corresponding to possible SIDLOC symbols, have a distance in time matching the symbol rate (or multiples) of the modified version of SIDLOC for OPS-SAT (~35 bits/s) increasing the confidence that the SIDLOC transmission was identified by OPS-SAT. Unfortunately, no complete frame decoding was possible.

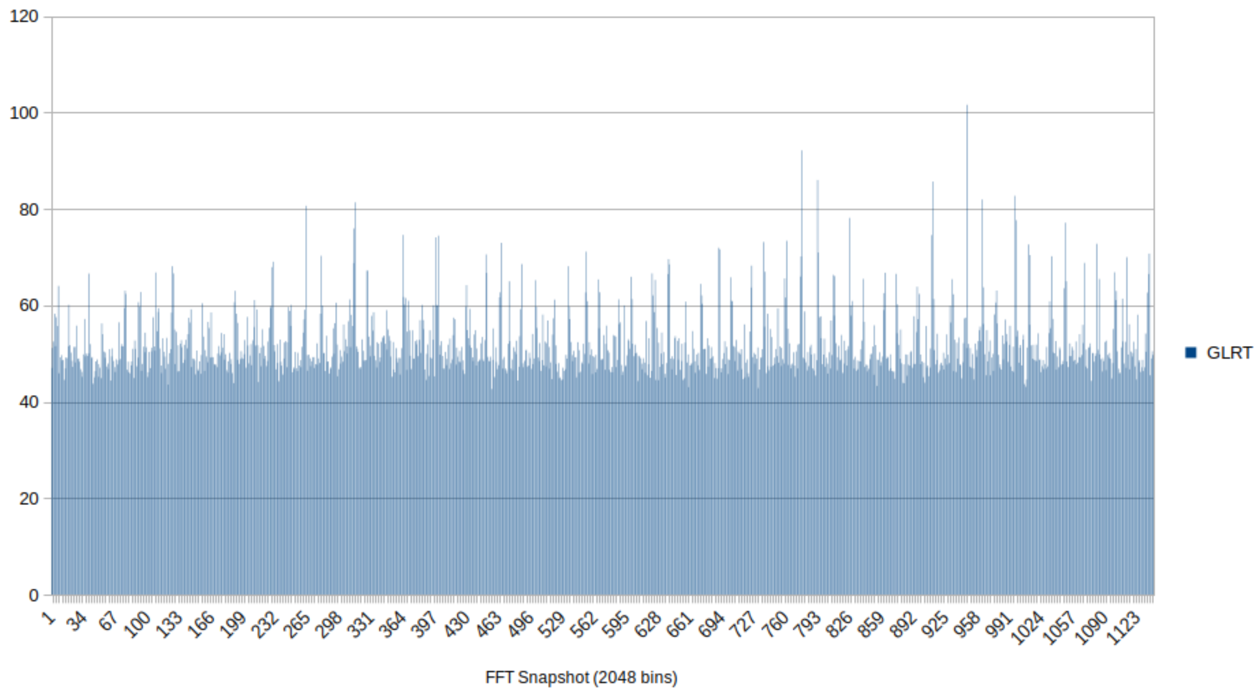

Figure 8: GLRT metric for Run #3

General findings

This is the first time that we gain access to a real view of the spectrum near the frequency of interest. From the three different experiment runs it is quite clear the high spectrum utilization, especially over central Europe.

On all three runs, there is a strong Chirp-like signal. We have not yet identified the source of the signal, but from the data captures it is clear that the SDR subsystem suffers from aliasing. According to the LMS6002D datasheet[6], a set of configurable low pass filters should be able to prevent this. From the received log, it seems that a 0.75 MHz low pass filter is set. However, as Figure 9 shows, this does not have the desired effect. The aliasing can contribute significantly to an increased noise floor from the mixing of out-of-band emissions.

[6] https://wiki.myriadrf.org/LimeMicro:LMS6002D_Datasheet#TX_and_RX_Low_Pass_Filters

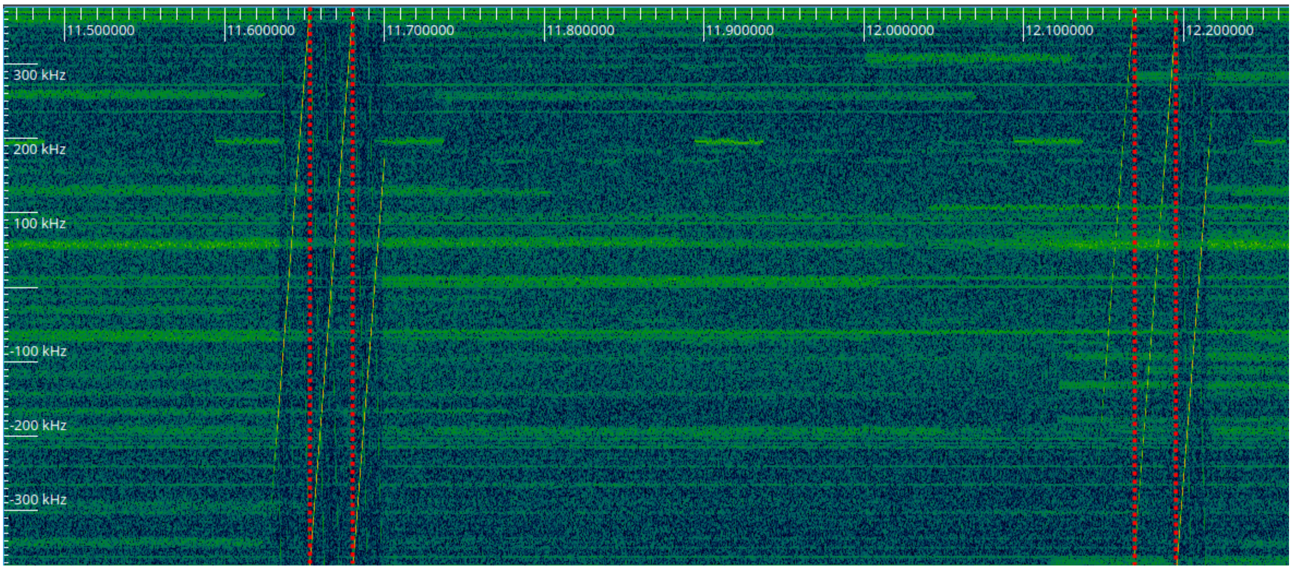

Figure 9: Aliasing effect

Another interesting finding was the high activity of data frames over Europe. The channels used are quite close to each other, making clear the significance of the compliance with the spectrum masks and proper filtering. We are quite confident regarding the frame transmissions due to the characteristic spectral lines that appear due to the use of repeated patterns, a common approach used in preambles (Figure 10). It is not clear however, if the spectrum occupancy is correct, or the aliasing of out-of-band transmissions are populating the observable spectrum.

Last but not least, based on the link budget and the TX power of the GS, we were expecting the SIDLOC signal as well as the CW tone, to have a greater SNR. This however is not the case. We are trying to identify the root cause of this issue.

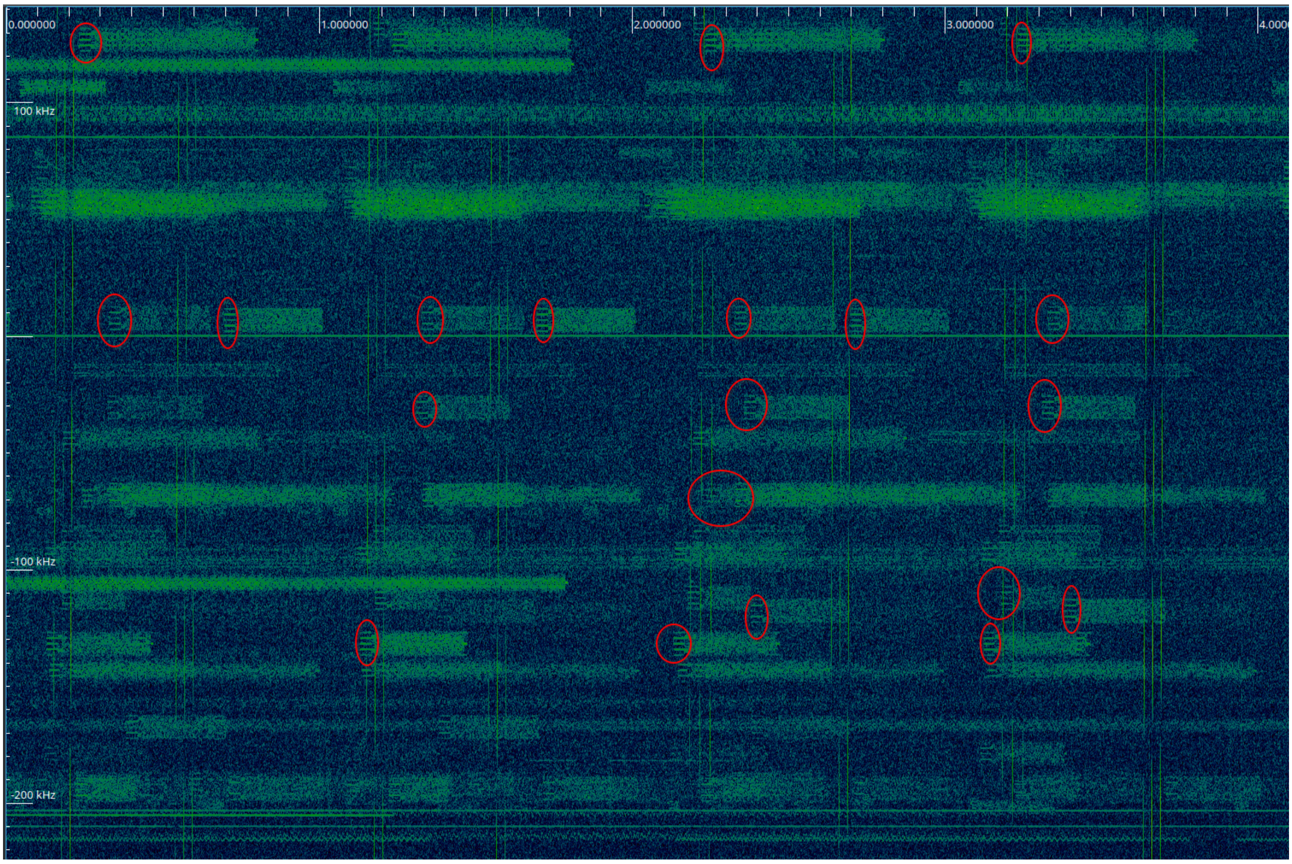

Figure 10: High activity all over the band

Acknowledgments

The entire LSF team would like to express gratitude to the whole OPS-SAT team for their support and especially to Rodrigo Laurinovics for the endless debugging sessions on the FPGA, Vladimir Zelenevskiy for scheduling and fetching the I/Q data and David Evans for his dedication and support, regardless the technical challenges and setbacks that this activity faced. Without them, this experiment would not be possible.