GSTP De-risk Project 4000134870 Deliverable ESR

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Work package:	**WP0 – Management, WP31 – Documentation**
Deliverable title:	**ESR – Executive Summary Report**
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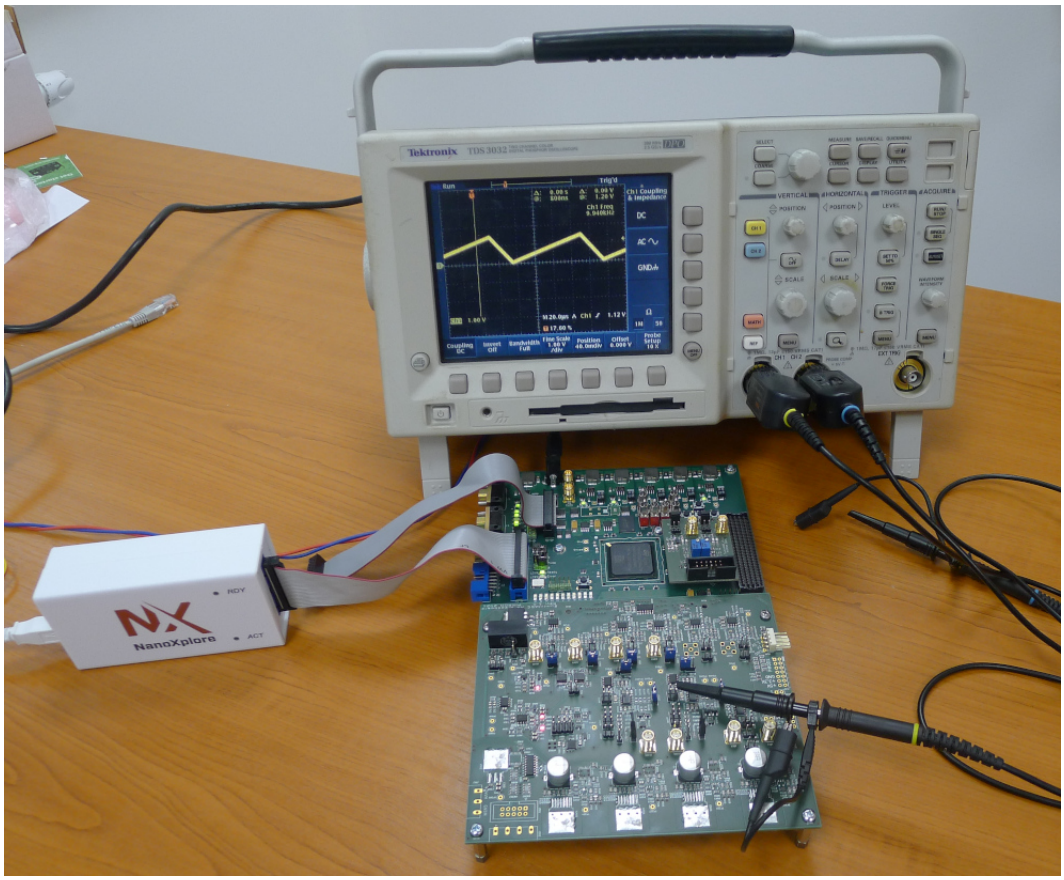


SumInt ADC Breadbard Analog Front-end SumIntADC v3 (DHW1)
Connected to NanoXplore NX1H35AS-EK FPGA Evaluation Kit

Executive Summary Report for Implementation of Sum-Int ADC IP-Core into Radiation-Tolerant NanoXplore NX1H35AS-EK FPGA FPGA and Performance Evaluation

PART 1 Objective of the project (what you were trying to achieve)

1.1 Objective of the Activity

The primary objectives of the project are verification of suitability of PiKRON's company original architecture of Analog-to-Digital Converter (ADC) for use in combination with radiation-tolerant FPGA (nanoXplore NG MEDIUM BRAVE chosen) and preparation of open-source design files which allows a synthesis of the converter control logic for multiple resolutions and sample rates according to requirements of the actual target applications. The design is already used together with consumer grade FPGAs and requires only a single external op-amp per channel and two digital I/O pins on FPGA for resolution about 12 bits. PiKRON uses the Sum-Int conversion technique even for high resolution (20 bits) applications in High Performance Liquid Chromatography (HPLC) spectrophotometric detectors. The precise (chopper stabilized) amplifiers, analog switches and comparator were required for such use. Some The secondary objective is to use developed platform for experiments which allow porting of PiKRON's motion control (PMSM, DC and stepper motors) solutions based on the Sum-Int ADC technique for the winding current sensing to the space-qualified components in future.

The main goal, minimal components realization on space-grade FPGA, has reached committing criteria. Advantages and found limitations of the solution are described in the technical and conclusion parts of this document.

1.2 Technical Objectives

The main advantage of the proposed design of middle resolution class analog to digital conversion for space application is minimal demand for additional special function/parameters components (single middle class op-amp, resistors and capacitor are enough). All other required functionality, including analog signal comparator and reference switching, can be implemented in FPGA digital subsystem for middle resolution range applications. This makes the choice of space mature/proven components easier. The design provides continuous source signal measurement with zero theoretical quantification error accumulation over multiple samples. The principle of operation has advantages over classical sigma-delta ADC: significantly lower number of reference source switching and constant mean frequency of the reference source switching.

1.3 Uncertainties Resolved by De-risk Project

Although the Sum-Int ADC has been applied in several different domains in PiKRON company products, the design has not been tested on space grade FPGA before. nanoXplore NG MEDIUM BRAVE has been used as a platform to prove and characterize realization in the space applications capable form and the performance of Sum-Int ADC has been characterized for various settings of sample rate and precision. The initial idea to characterize conversion stability over multiple temperatures to estimate stability has been extended to testing in the full NG MEDIUM BRAVE operating range from -40°C up-to 85°C.

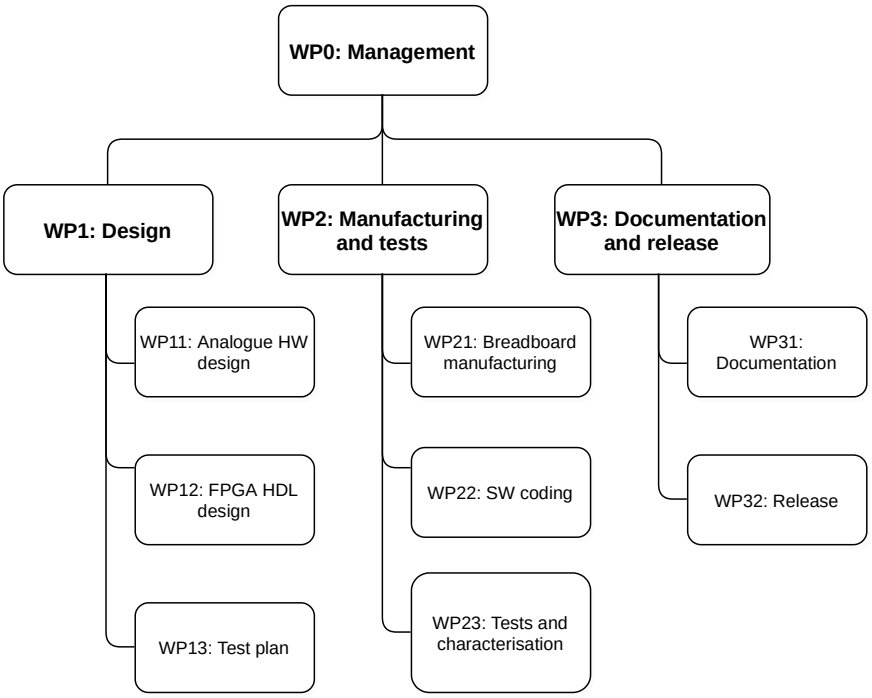
The analog behavior of nanoXplore BRAVE NG-MEDIUM FPGA digital input/output circuitry has been tested and proved in operation for simple (SIMPLE) Sum-Int ADC configuration.

As expected, the analog front-end extended by an external comparator IC and another IC reference switching provides about two times better stability.

PART 2 Project Management overview

2.1 Work Division into Work Packages

The project has been divided into 3+1 main work packages groups and then to 8+1 individual work packages.



2.2 Brief Work Overview

The nanoXplore BRAVE NG-MEDIUM NX1H35AS-EK evaluation kit was chosed and purchased as the main development platform.

The two preliminary test boards have been designed as preparatory work for final WP11 design. The first (SumIntADC_v1.1) to test SIMPLE configuration with FPGA and single op-amp only, the second (SumIntADC_v2) to test ADVANCED variant with an external comparator and a chip dedicated to reference switching. The second one is already utilizing ADA4084 components which have space-qualified chip equivalents. The second test board helped to identify problems with the use of ADA4084 in the comparator function in the intended setup and therefore AD8561 has been purchased, tested and chosen for the final design. BRAVE NG-MEDIUM digital I/O pins assessment for intended function has been tested on the modified SumIntADC_v2 board.

The digital insulator support board (IsoNXPMOD) has been designed to connect BRAVE NG-MEDIUM to data acquisition systems with minimal electrical influence on the solution under test.

The final analog front-end breadboard (SumIntADC_v3 Rev v1.0) has been designed on the base of previous experiments and manufactured (WP21). Its schematic, layout and technological data can be found in DHW1.

FPGA Sum-Int IP core HDL design version 1 (HDL1) has been developed and used with test boards and then with the final breadboard (WP12). It has been later updated to the final version (HDL2).

The test plan (DTP1) has been prepared (WP13). WP23 test and characterization work was planned for ESTEC facility but due to its limited operation (COID-19) and to make possible multiple iterations of the design, the Laboratory of Precise Electrical Measurement (METLAB) at the Department of Measurement, Faculty of Electrical Engineering, Czech Technical University in Prague (CTU) was chosen instead (confirmed by CCN1 which declares that additional expenses are covered from the PiKRON's fixed contract budget). The test software to receive serial data stream on Xilinx Zynq FPGA platform as well as automatic laboratory equipment control programs (SW1) has been developed in cooperation with the METLAB (WP22).

Test and characterization (WP23) have revealed that the input offset stability of ADA4084 op-amps over temperature is at least two times worse than required to pass specified committing criteria with reserve. The multiple design tuning has been attempted but then new offering of space-qualified op-amp (OPA4H014-SEP) from Texas Instruments has been published by manufacturer and Sum-Int ADC SIMPLE and ADVANCED channels design have been updated to use chip equivalent OPA140. This change with passive components tuning allowed passing committing criteria with reserve.

The initial SIMPLE and ADVANCED characterization (WP23) required more than 100 hours of laboratory setup run time. The required time for preparation and adjustments is not counted. Characterization with OPA140 represent additional 23 hours of run time.

The side experiment project with high resolution variant proved to be problematic to realize with the best space grade components (i.e. Ti LMP2012QML, etc.) which we could find. On demand of colleague from ESA, the previous PiKRON non space solution has been analyzed and reevaluated on initial PiKRON hardware which took more than 130 raw hours.

All characterization data have been delivered to ESA and a list with all tests is available in the measurements diary spreadsheet (DCR1 measurements-diary). The theoretical background, used methods and characterization results based on the provided methodology are documented in METLAB Report on Testing of ADC Modules Based on PiKRON's Sum-Integration Principle (DCR1 SumIntADC-PIKRONDCR1-CTU-REPORT-REV3). The overall maximal errors over all measured samples are summarized in DCR1 sumintadc-char-totals. The obtained results for SIMPLE (max abs error of individual samples $<\pm 4 \cdot 10e\text{-}3$ @4000 samples/s) and ADVANCED variant (max abs error of individual samples $<\pm 2 \cdot 10e\text{-}3$ @4000 samples/s) evaluated over whole temperature range from -40°C to +85°C against an ideal linear approximation at 25°C fit in the commuting criteria ADC performance: abs. accuracy $5 \cdot 10e\text{-}3$ @ 4000 samples/s. For ADVANCED setup even the whole range single value error is bellow commuting short-term noise $2 \cdot 10e\text{-}3$ @ 4000 samples/s.

The results of the performance tuning have been documented in the revision v1.2 of the SumIntADC_v3 schematic design. It is updated to OPA140 and final values of the components. The deliverable DHW2 SumIntADC_v3_rev1_2.pdf was finished in the frame of WP31.

The results of the project have been presented on 9th International Workshop on Analogue and Mixed-Signal Integrated Circuits for Space Applications:

Píša, P., Porazil, P., Ladman, J., Levacq, D., Peca, M., Sedláček, R., Špaček, M., Implementation and Evaluation of Sum-Int ADC IP-core on NanoXplore FPGA, In: 9th International Workshop on

Analogue and Mixed-Signal Integrated Circuits for Space Applications, Nordwijk: European Space Agency, 2022

The project is released to the public (WP32) on the GitLab including all already mentions public deliverables and final ones (FP – Final Presentation, FR – Final Report, TAS – Technology Achievement Summary, etc.)

https://gitlab.com/pikron/projects/sumintadc

2.3 List of Deliverables

Type	Ref. No.	Name /Title	Description	Replacement Value (EUR)	Location	Property of	Rights granted/ Specific IPR Conditions
Documentation	DHW1	Preliminary Analog Front-end Schematics and Board Layout	PDF outputs, KiCAD and technology files	n/a		Public	No royalties
	DTP1	Test Plan	PDF and ODT	n/a		Public	No royalties
	DCR1	Characterization Report	PDF and ODT and PDF and ODS for measurements diarry and summary results	n/a		Public	No royalties
	DHW2	Final Analog Front-end Schematics and Board Layout	PDF schematics and layout, KiCAD and technology files	n/a		Public	No royalties
	DDD1	Design Description and Implementation Guide	PDF and ODT	n/a		Public	No royalties
	DUG1	Demo Kit User Documentation/Quick Start Guide	PDF and ODT	n/a		Public	No royalties
	FP	Final Presentation	PDF and ODP	n/a		Public	No royalties
	FR	Final Report	PDF and ODT	n/a		Public	No royalties
	TAS	Technology Achievemen	PDF and PPTX	n/a		Public	No royalties

		t Summary					
	DP	Developme nt Plan for a potential follow-on activity	PDF and DOCX	n/a		ESA/ PiKRON	n/a
Hardwa re	HW1	Final Analog Front-end Breadboard	Assembled printed ciruit board	500 EUR per batch start 400 EUR per each piece	1 piece delivered to ESA 3 pices deposited at PiKRON	ESA and PiKRON (for followup projects)	Design public
Software	SW1	Final Test Software for Sum-Int ADC Control and Data Acquisition	C-sources for SumInt ADC communca tion, Python for acqusition lab control and processing, Julia scrips for THD	n/a		Public	No royalties
	HDL1	Preliminary HDL Design	VHDL souces and Python NX top level	n/a		Public	No royalties
	HDL2	Final HDL Design	VHDL souces and Python NX top level	n/a		Public	No royalties
Other	ESR	Executive Summary Report	PDF and DOCX			ESA/ PiKRON	n/a
	PH	Photograph ic Documenta tion	JPEG files archive			ESA/ PiKRON	Free to publish
	CCD	Contract Closure Documenta tion	PDF and DOCX			ESA/ PiKRON	n/a

PART 3 Brief Technical Results Overview

3.1 Sum-Int ADC Analog Front-end Breadboard

The visualization of the designed Sum-Int ADC analog front-end breadboard for NX1H35AS-EK evaluation kit can be seen in Fig.3.1.

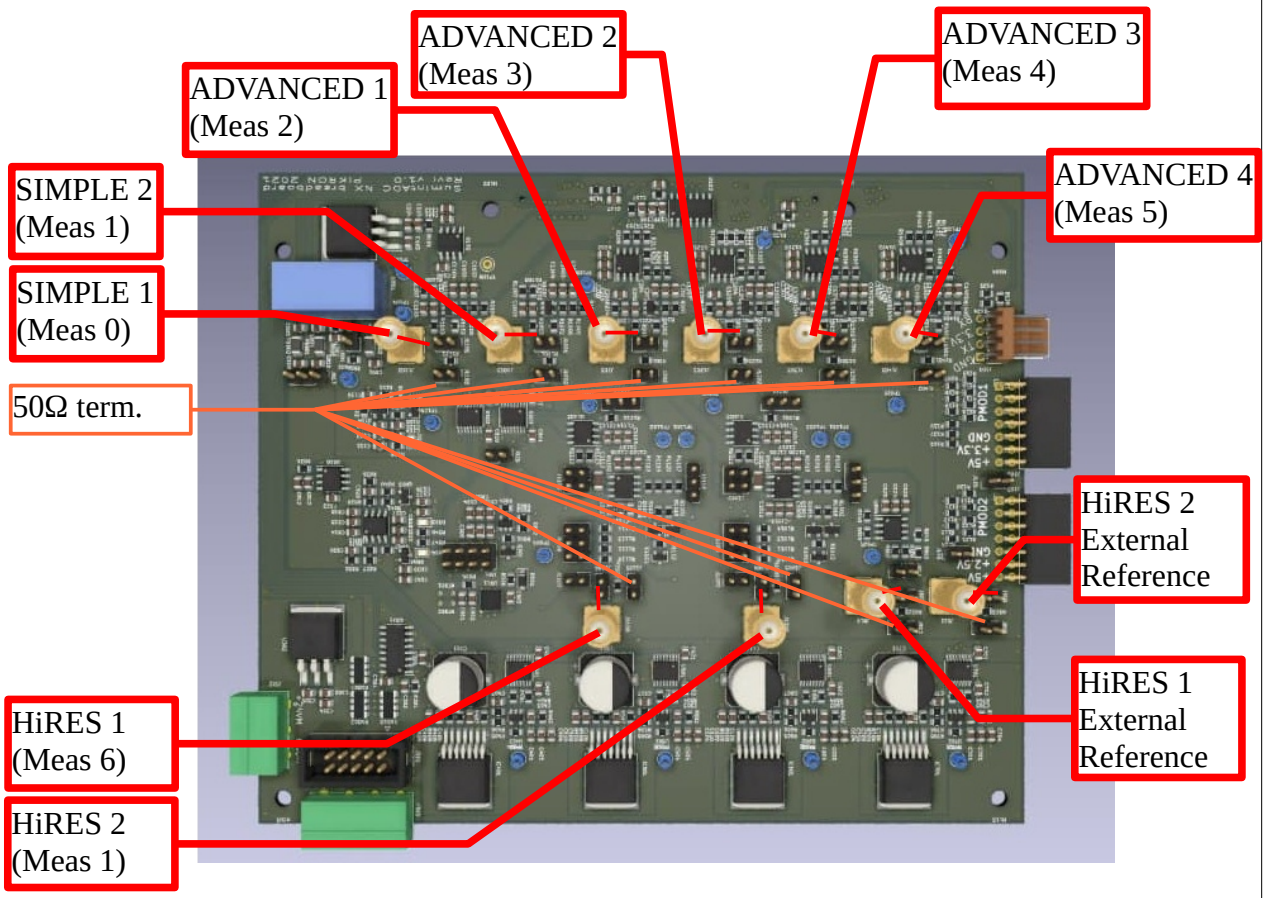


Figure 3.1: Sum-Int ADC Analog Front-end Breadboard for NX1H35AS-EK

3.2 The Implemented Functions

The evaluation of the next basic Sum-Int ADC variants has been main target objective of the project:

- 2 simple Sum-Int analog to digital converter channels
  - design oriented on minimal active components count (single op-amp per channel)
  - FPGA pins used directly as reference switch and comparator
  - input range -1.0 to +1.0 V
  - resolution equivalent to 9 to 12-bits resolution can be achieved
- 4 advanced Sum-Int analog to digital converter channels
  - a little more complex, integrator op-amp and analog comparator
  - uses cheap digital chip/logic gate for dedicated reference source switching
  - input range -1.0 to +1.0 V
  - resolution equivalent to 11 to 14-bits resolution can be achieved

The following subsystem has been used as experiment with porting PiKRON's non-space high resolution variant to space acceptable components. The actual attempt did not achieve expected resolution. The main problems has been identified but implementation from available of-the-shelf space qualified components is problematic. The analysis and new search for components would be required for next iteration. The alternative is to integrate the circuitry into some application specific chip designed with space grade quantification in mind.

- 2 high resolution Sum-Int analog to digital converter channels
  - input range -1.0 to +1.0 V (jumper select able for -2.2 to +2.2 V, -3.5 to +3.5 V and -5.0 to +5.0 V ranges)
  - analog ground separated from the rest of the system, common for both channesl and its references

The following support functions has been integrated to the breadboard for testing and future extensions:

- analog voltage source with 18/bit DAC and waveform generator for self testing
- PMOD extension connectors
- LVTTL serial port

The PiKRON company has long history record in area of motion control systems designs and realizations. That is why, hardware to enable future experiments with motion control realized on nanoXplore FPGA has been integrated into the breadboard design. The realized variant can be used for DC, PMSM and stepper motor control with or without positional feedback sensor and it uses Sum-Int ADC principle for the winding currents sensing:

- 4 channels of the power stage 24 V, 5 A with Sum-Int ADC realized current sensing
  - separate power supply input 24 VDC
  - galvanically isolated from the rest of the system
- incremental encoder input
  - ground and +5 VDC power supply from 24 VDC motor subsystem, isolated from the FPGA evaluation kit

3.3 The Achieved Results Summary

The results of the Sum-Int ADC characterization for simple and advanced configurations:

- the nanoXplore NG-MEDIUM BRAVE LVDS inputs have been characterized for simple Sum-Int ADC variant use.
- feasibility of sum-integration analog to digital conversion technique has been demonstrated with space-grade equivalent components
- the analog front-end breadboard has been designed with 2× simple (direct use of FPGA pins), 4× advanced ADC channels
- HDL design has been implemented – big advantage is its simplicity and principle guaranteed continuous input averaging
- two additional experimental channels aiming high resolution and 4× power stage for future motion control usage tests
- the AD conversion parameters have been characterized in a professional metrology laboratory over temperature

- optimal operation amplifier selected – OPA140/OPA4H014-SEP
- the simple channel design (requires only three FPGA pins and single active component per channel) maximal absolute error <±4e-3 @4 ks/s (over -40°C to +85°C)
- with external switch and comparator achieved max abs error of individual samples <±2e-3 @4 ks/s (over -40°C to +85°C)
- the continuous input integration immune to short spikes and possibility to enhance resolution by moving averaging

The simple channel summary table for two considered operational apmlifiers:

OpAmp type	Linearity at single temp.		Single raw sample at temp		Single raw sample, all temp	
	aver err	raw std	min	max	min	max
OPA140	5.78e-05	5.17e-04	**-1.19e-03**	1.10e-03	-3.25e-03	**3.84e-03**
ADA4084	4.69e-05	1.44e-04	-4.27e-04	4.70e-04	-2.68e-03	6.45e-03

The advanced channel summary table for different component values used:

OpAmp type	Linearity at single temp.		Single raw sample at temp		Single raw sample, all temp	
	aver err	raw std	min	max	min	max
1. OPA140	2.51e-04	5.11e-04	**-1.09e-03**	9.88e-04	-1.24e-03	**1.77e-03**
2. OPA140	5.49e-05	5.10e-04	-1.09e-03	9.68e-04	-3.00e-03	2.90e-03
ADA4084	4.62e-05	4.78e-05	-1.78e-04	2.09e-04	-3.60e-03	3.53e-03

The actual linearity of the conversion is much better than ±2e-3 @4 ks/s considered for the whole temperature range. When average of each 3400 samples series acquired for the given input voltage is evaluated then error for the single temperature is ten times smaller. See Fig. 3.2 for the demonstration of the linearity of each characteristic at given temperature.

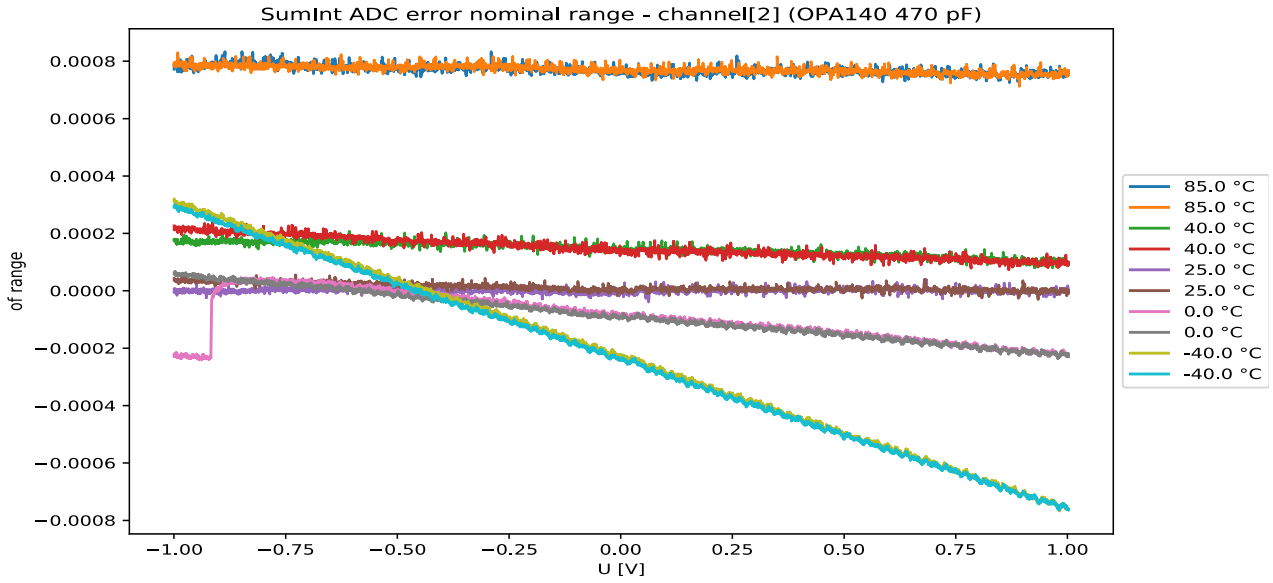


Figure 3.2: OPA140 Test on Advanced Channel 1 (2) - absolute error @1Hz averaging and linearity

The dynamic performance between 13 and 14 bits (ENOB = (SINAD_dB – 1.76)/6.02) is confirmed when non-uniform sampling is partially compensated by considering average between actual sample points times and the shifted sample time is used for sine approximation. The results for the simple channel are shown in Fig. 3.3 and for the advanced channel in Fig. 3.4.

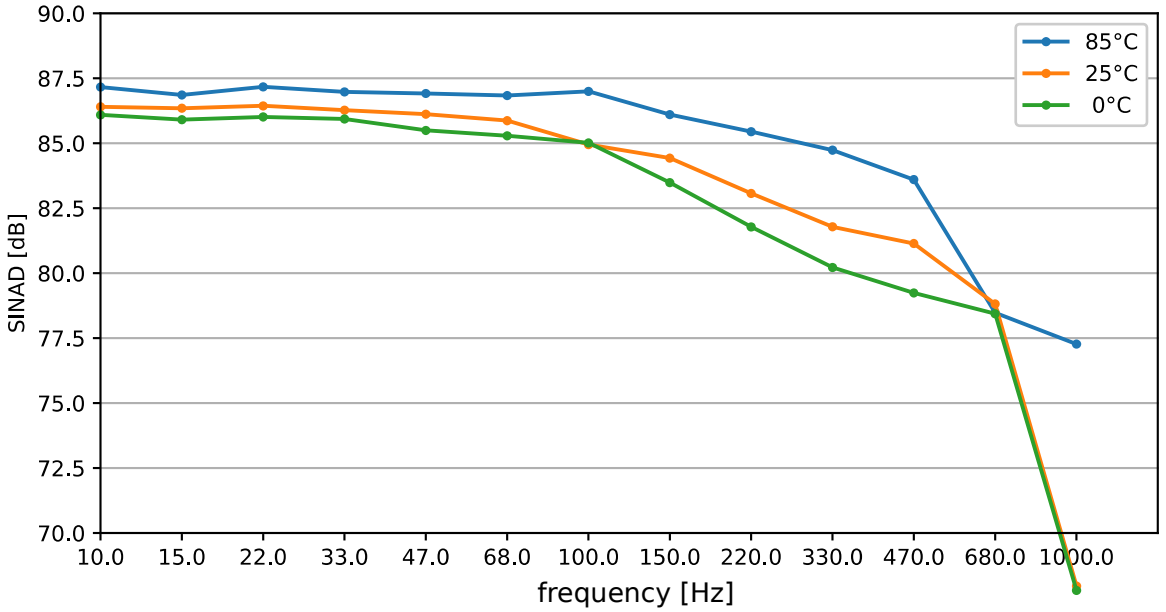


Figure 3.3: Simple channel SINAD as a function of excitation signal frequency

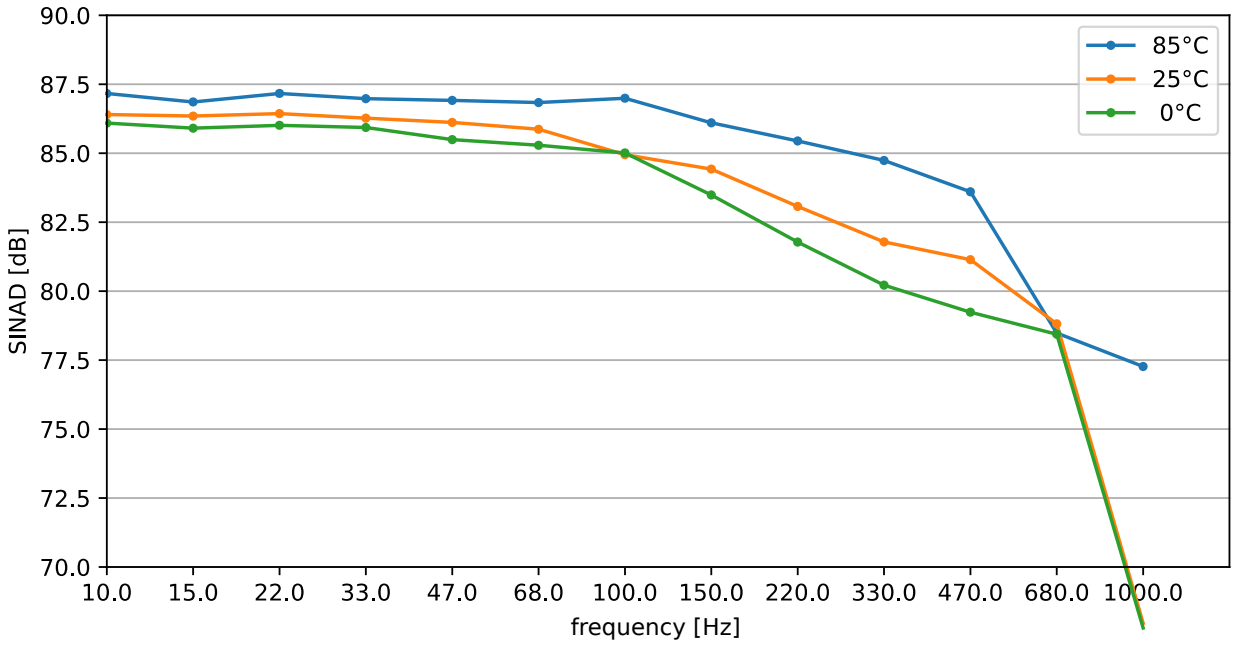


Figure 3.4: Advanced channel SINAD as a function of excitation signal frequency

3.4 The Comparison to the Project Technical Objectives and Goals

The project proposal objectives table follows

Id.	Objective	Verification	Committing
CO1	SumInt ADC implemented successfully into European, rad-hard FPGA	test	committing
CO2	ADC performance: abs. accuracy 5e-3 @ 4000 samples/s	test	committing
GO2	ADC performance: abs. accuracy 5e-4 @ 4000 samples/s	test	goal
CO3	ADC performance: short-term noise 2e-3 @ 4000 samples/s	test	committing
GO3	ADC performance: short-term noise 1e-4 @ 4000 samples/s	test	goal
CO4	ADC stability	analysis	committing
CO5	Providing HW & SW kit demonstrating function and performance	test	committing
GO6	Exposing full kit functionality via SpaceWire interface	test	goal

The comparison between the proposal committing objectives and achieved results is provided in the following table. The actual resolution objectives CO2 and CO3 are evaluated for the simple and the advanced channel realizations separately.

Id.	Objective	Value		Done
		Objective	Achieved	
CO1	SumInt ADC implemented in nanoXplore FPGA			done
CO2.s	ADC abs. accuracy @ 4 ks/s	5,00E-03	3.84e-03	done
CO2.a	ADC abs. accuracy @ 4 ks/s	5,00E-03	1.77e-03	done
CO3.s	ADC short-term noise @ 4 ks/s	2,00E-03	1.19e-03	done
CO3.a	ADC short-term noise @ 4 ks/s	2,00E-03	1.09e-03	done
CO4	ADC stability – originally analysis, done complete temperature range characterization			done
CO5	Providing HW & SW kit hardware – 1× HW1 delivered to ESTEC			done

As negotiated in the final contract, the DHW1 delivery (CO5) includes the analog front-end breadboard without nanoXplore BRAVE NG-MEDIUM NX1H35AS-EK evaluation kit. The kit price is high and ESA/ESTEC poses more of these kits bought of another one by PiKRON and managing its delivery would only complicate the project.

As for the intentional/non-committing goals GO2 and GO3, the final achieved resolution has not reach this ideal/theoretical values for these setups. The main source contributing to the higher error is known, it is deviation of the input offset and bias current of the op-amps used in the design. The situation would be better for applications with the smaller input range voltage because lower resistances connected to the both op-amp inputs suppress the contribution of error from the input currents change. Wider range of non-space grade op-amps and use in the current sensing applications with a small voltages and a low sense resistances describe why the simple solution behaves much better in PiKRON's original motion control applications. There is some space and ideas how to enhance performance even in the actual nanoXplore based setup by more components tuning.

Side goal GO6 has been abandoned/postponed due the nanoXplore FPGA confirmed limitations, which would require more time investment into porting SpaceWide IP core design proposed and by ESA side which has even promised to help from their side originally.

PART 4 Conclusion and Recommendations

4.1 Conclusions

The SumInt ADC technique has been ported to nanoXplore FPGA, actual core HDL code size is about 160 VHDL lines, the rest 200 lines are for raw data delivery to the system for evaluation. When compensation for non/equidistant sampling is required, then computation with reciprocal approximation would make design more complex. But the ratio computation (division) can be easily converted into supporting software operating at low frequency after averaging. The short-term resolution about 13 bits has been confirmed by dynamics tests. The use of a wide operating temperature range is limited by the components stability. The committing criteria defined in the project proposal

- abs. accuracy 5.0 e-03 @ 4000 samples/s
- short-term noise 2.0 e-03 @ 4000 samples/s

has been fulfilled by OPA140 based design, but further analysis of the impact of the temperature on the design is necessary to achieve expected final goal results.

The nanoXplore NG MEDIUM FPGA pins in LVDS configuration without termination switched on has been evaluated for a direct use as an analog comparator and for 2.5 VDC and signal input in the range from 0.2 to 1.9 V and its suitability required for direct Sum-Int ADC realization has been confirmed. The analog input range of 0.5 to 1.5 VDC is suggested to guarantee safety margin. The input current has been estimated at a value lower than 80 μA based on a triangle test signal with a minimal dependency on the complementary input driven in the defined safe range. Roughly estimated input capacitance including breadboard paths and oscilloscope probe did not exceed 150 pF.

Simple variant of the Sum-Int analog to digital converter operated with maximal absolute error of individual samples **<±4e-3 @4000 samples/s** with only FPGA bank power supply used as voltage reference over the whole temperature range of **-40°C to +85°C** against an ideal linear approximation at 25°C.

The advanced variant with with a precise reference, an analog comparator and a cheap HC digital circuit used for reference switching fits into maximal absolute error of individual samples **<±2e-3 @4000 samples/s**. which is true over whole temperature range of **-40°C to +85°C** against an ideal linear approximation at 25°C.

The experiment with high a resolution setup and and LMP2012, declared to be the best Texas Instruments option for space qualified offset auto-zeroing op-amp, did not result in the expected resolution. The characterization and documentation of previous PiKRON's non-space targeted solution shows that there is a potential to use Sum-Int conversion technique for higher resolution applications.

The design has advantages for limiting/suppression of cumulative error over multiple samples. The techniques how to make the design immune to many of the components parameters changes over time and temperature is known. Critical and limiting parameters are the input offset voltage and an input bias or offset current (when the bias influence is suppressed).

The conversion technique suits well the applications where integral value of the input signal matches the acquired information. The best match is for applications processing integral of ratio of the input signal against another slowly and smoothly changing signal.

The disadvantage is non-uniform interval between samples when integral/average value is delivered/sampled. However, the time to which the given integral value corresponds to the input signal course is know/represented in the output data stream. There are applications which can tolerate this timing jitter. This value is limited to one half of the modulator period. The modulator period can be chosen as any of integer multiples of the main/quantization ADC clock. The actual output rate/period can be chosen as and arbitrary multiple of the modulator period and the theoretical resolution is equal to one half of the fast quantization clock frequency divided by the output averaging frequency. The selection of the lower modulator frequency reduces demands for the precise timing and jitter of the clocks defining the reference quanta for a given resolution. The low modulator frequency releases demand for clocks jitter, but the effect of non-uniform sampling is magnified. The methods how to compute the average or fit a harmonic input signal to the Sum-Int ADC non-uniform samples interval data stream is known and has been used for some evaluations.

The frequency of the reference switching is lower than for sigma-delta conversion technique. Each switching is expected to introduce some part of non-controlled/parasitic charge transfer and reducing the umber of switching over the output sample time helps to increase the conversion resolution.

The whole project has been developed in a public GitLab repository including HDL, SW and data processing and evaluation solutions.

https://gitlab.com/pikron/projects/sumintadc/

4.2 Future Work / Potential Applications

The technique has been already used in multiple low, mid and high resolution demanding applications at PiKRON company for non-space applications. Worth to mention, photometric signal processing, motor winding current conversion and control in motion/robotic controllers. Another potential area is switched power supplies digital control. In this case, the ideal use of Sum-Int ADC is for direct conversion of voltage difference between output and preset reference where small resolution and simple implementation is enough.