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SYRLINKS	SYRLINKS

SAPHIR GSTP5

Executive Summary

	Name _ Function	Date	Signature
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REVISION

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0	21 June 2016	Yves RICHARD	Creation

1. INTRODUCTION

In the frame of the “Low Cost S-band Flexible TTC Transponder for Mini-satellites” GSTP5 project, contract number 4000112589/14/NL/FE, SYRLINKS undertook the development of a breadboard of a Telecommand and Telemetry S-Band transponder. The demonstrator has to address especially the Coherency and the Ranging functions of the transponder.

2. BACKGROUND

The Myriade Evolution program, driven by CNES, the French Space Agency, aims at developing and qualifying a spacecraft platform available for use within the 2015-2025 period. This product line will offer a platform primarily for Earth Observation or scientific applications. In the context of Myriade Evolutions program and in the context of the associated GSTP6 contract driven by ESA, the European Space Agency, SYRLINKS designed and manufactured a S-band transceiver.

3. OBJECTIVE OF THE GSTP5 ACTIVITY

The objective of the GSTP5 activity is to develop and to test a functional breadboard of a low cost S-band transponder, based on Myriade Evolutions and GSTP6 developments. It is proposed within this GSTP5 activity to develop a low cost flexible transponder for mini-satellites with the additional following functionalities:

- Coherency mode
- Ranging channel

Moreover, a second objective of the GSTP5 activity is to implement the following functionalities:

- 10 different selectable Telemetry data rates
- RF transmitted output power up to 5 W
- DcDc converter enhancement to address the 5W of output RF power
- Diplexer filter enhancement to address the 5W of output RF power
- Analysis of the cost/performance of a European GaN MMIC power amplifier versus an American GaN unit
- Discussion about a SRRC filter versus a Butterworth order 7 filter

4. WORKS OF THE PROJECT

The work was organised into the following tasks:

- Task 1 - Requirements capture and detailed specification of the unit
- Task 2 - Detailed architectural design of the upgraded S-Band Transponder
- Task 3 - Implementation of the design changes in the breadboard demonstrator
- Task 4 - Breadboard test plan and test procedure(s)
- Task 5 - Breadboard testing
- Task 6 - End Item Data Pack (EIDP) and hardware delivery

The following major reviews were held during the course of this activity:

- Kick-Off (KO)
- Requirement Reviews (RR)
- Critical Design Review (CDR)
- Test Readiness Review (TRR)
- Test Review Board (TRB)
- Final Review (FR)

TASK	Name of task	Milestone
1	Requirements capture and detailed specification of the unit	**KO RR**
2	Detailed architectural design of the upgraded S-Band Transponder	**CDR**
3	Implementation of the design changes in the breadboard demonstrator	
4	Breadboard test plan and test procedure(s)	**TRR**
5	Breadboard testing	**TRB**
6	End Item Data Pack (EIDP) and hardware delivery	**FR**

Table 1 – Tasks and milestones

5. DEMONSTRATOR PRESENTATION

5.1 Architecture of the demonstrator

The breadboard is based on previous research and development undertaken by CNES in the frame of the new generation of TT&C subsystems for the Myriade Evolutions program.

The transponder integrates:

- a receiver
- a transmitter
- a diplexer filter that separates the received signal and the transmitted signal
- a link between the transmitter and the receiver for the Coherency management
- a link between the transmitter and the receiver for the Ranging management

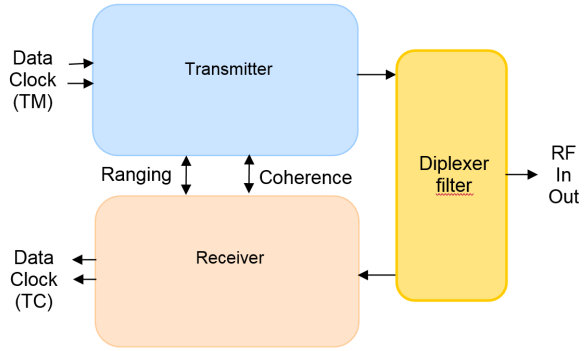


Figure 1 – Transponder architecture overview

The S-Band Transponder performs:

- Telemetry modulation and transmission in S-Band (2200MHz – 2290 MHz)
- Reception in S-Band (2025MHz – 2110 MHz) and demodulation of the RF signal in order to provide the telecommand to the On-Board Computer
- Doppler and/or Ranging for satellite tracking position

The receiver amplifies the RF input signal, translates it to low frequency band and provides this signal to the digital signal processing unit. The digital processor demodulates the SP-L/PM signal and delivers the data/clock TeleCommand signal.

The digital signal processing unit of the transmitter codes and modulates the data/clock Telemetry input signal. The QPSK, OQPSK , SP-L/PM or PSK/PM, modulated base-band signal is then provided to the RF part. Signal can then be amplified by the power amplifier and sent to the diplexer filter.

Two independent DcDc converters, having galvanic isolation, give the power to the receiver and to the transmitter. Secondary supplies and supplies protection are managed inside the equipment.

At power-on, transmitter and receiver warms up during a few seconds and initialization takes place.

After power-on, the transmitter is in low-power/stand-by mode, no RF signal is sent to output. Transmitter is then waiting for a command.

Receiver is waiting for an input RF signal. When a RF signal is detected at receiver input, the receiver demodulates this incoming signal. If the input RF signal disappears, then receiver returns to the waiting mode.

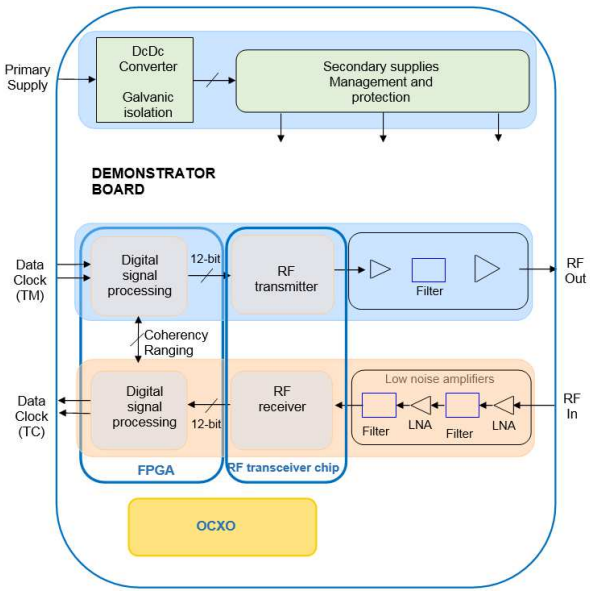


Figure 2 – Demonstrator board internal blocks

The three main components of the demonstrator board are:

- A Digital Processing Unit (FPGA)
- A RF transceiver chip
- A crystal oscillator OCXO at 32.768MHz

The coherent and ranging modes need an exchange of information between the receiver and the transmitter functions of the transponder. This exchange of information is realized through internal connections between the RX and TX functions of the FPGA.

The architecture of the FPGA – Digital Signal Processing unit – is described in the following drawing:

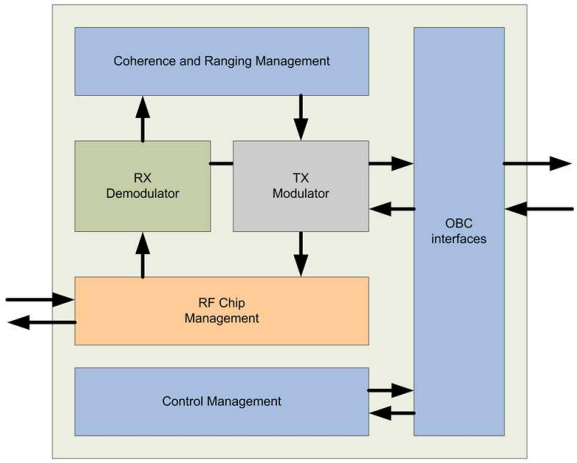


Figure 3 – Bloc diagram of the FPGA integrated functions

5.2 Physical presentation of the breadboard

The breadboard integrates all the functions on a single board, excluding the RF power amplifier.

Figure 4 – Breadboard

The demonstrator board is enclosed inside a metallic box.

Figure 5 – Demonstrator

5.3 Interface presentation of the demonstrator

Interface signals are given in the following drawing.

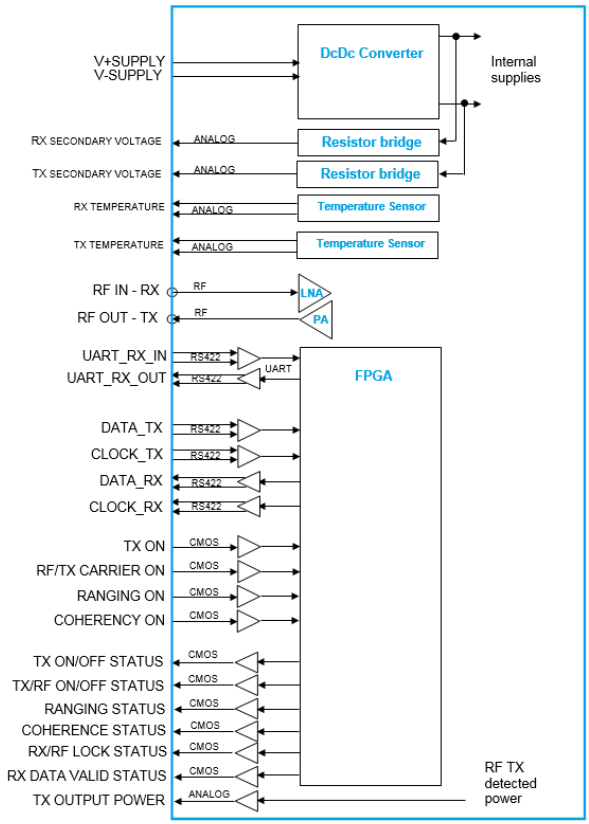


Figure 6 – Interface signals

5.4 Functional diagram

Transmitter works from Power-On according to a state machine diagram, as described after:

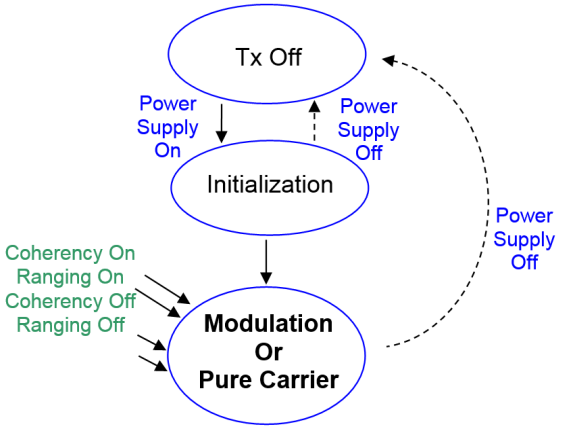


Figure 7 – Functional diagram of the transmitter

Receiver works from Power-On according to a state machine diagram, as described after:

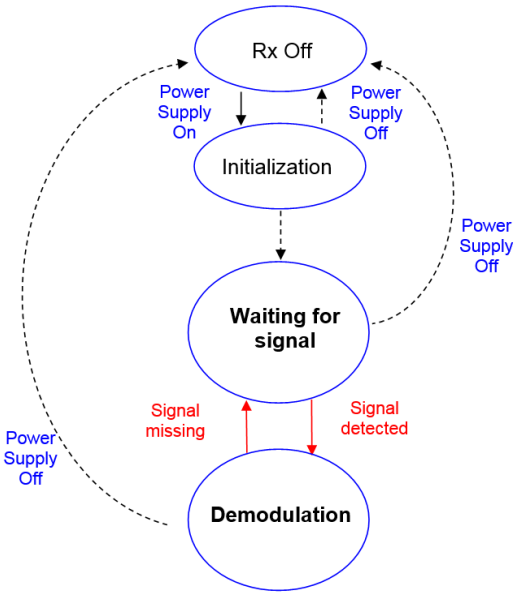


Figure 8 – Functional diagram of the receiver

5.5 UART protocol

The UART protocol implemented in the breadboard is a simple protocol used to configure and monitor the breadboard. The following table gives the format of UART words.

Function	ASCII	Structure of the frame	Response of the transponder	Description
Monitoring	S	<S>	<Sxxxxxx…>	with xxxxxx the monitoring data
Configuration	C	<Cxxxxxx…>	<COK> ou <CER>	with xxxxxx the configuration data

Table 2 – UART commands

5.6 GUI description

A Graphical User Interface - GUI – was developed under Visual Basic to configure and monitor the Breadboard. An example of one of the available screens is shown after.

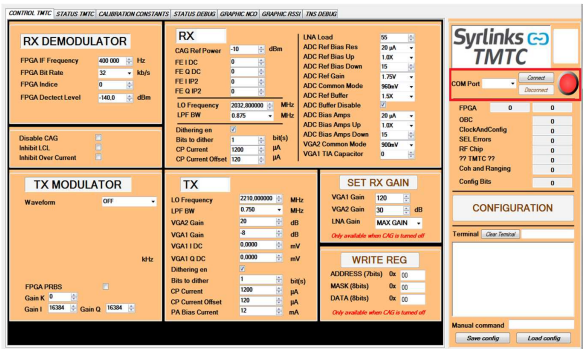


Figure 9 – GUI – Screen example

6. MAIN REQUIREMENTS

	Specifications
Modulation	PCM/PM/SP-L modulation index 0.5 to 1.25 rad ± 10%
Coding	No coding
Data Rate	16, 32 or 64 kbps
Locking process	Input carrier sweep
Carrier acquisition	Sweep rate < 32 kHz/s in a sweep range of ± 60 kHz at –120 dBm input power level
Hold lock condition	Uplink carrier swept over ± 140 kHz @32 kHz/s and @ –124 dBm
Doppler	Doppler range > ±58 kHz and Doppler rate in the range of [-1200, 0] Hz/s
Dynamic range for carrier acquisition	–125 to –50 dBm
Frequency band	2025 to 2110 MHz
Noise Figure	≤ 3 dB
Frequency Stability in temperature range	≤ +/- 0.25 ppm
Technological losses	≤ 2.5 dB

Table 1 - Receiver specifications

	Specifications
Coherency mode	Coherent mode with 240/221 turn around
Ranging mode	Transparent Ranging channel
Modulation	. Filtered QPSK . Filtered OQPSK . PCM/PM/SP-L modulation index 0.1 to 1.4 rad (data rate 16 to 256 kbps) . PCM(NRZ-L)/PSK/PM (data rate 10 to 60 kbps)
Coding (QPSK, OQPSK – selectable)	Convolutional (7, ½) Differential coding
Data rate	. PCM/PM/SP-L from 16 kbps to 256 kbps . PCM/PSK/PM (NRZ-L) from 10 kbps to 60 kbps . QPSK from 100 kbps to 1 Mbps . OQPSK from 1 Mbps to 2 Mbps
Carrier Phase Noise	< 5º rms
Frequency band	2200 to 2290 MHz
Output RF impedance	50 Ohm
Frequency Stability in temperature range	≤ +/- 0.25 ppm
Short-term frequency stability for Doppler tracking	± 1 E-9
Technological losses	< 0.5dB

Table 2 - Transmitter specifications

7. RANGING MANAGEMENT DESCRIPTION

The transparent ranging channel supports ESA code in compliance with ECSS-E-ST-50-02C. Regenerative ranging is not in the scope of this study. The peak modulation index of the ranging signal is in the range 0.1 to 1.4 rad for the link Earth to Space. The peak modulation index of the ranging signal is in the range 0.01 to 0.7 rad for the link Space to Earth. The ranging signal is demodulated in the transponder, from the Earth-to-Space link, and re-modulated onto the Space-to-Earth link carrier.

An overview of the transparent ranging management implemented in the FPGA of the Demonstrator Model is given.

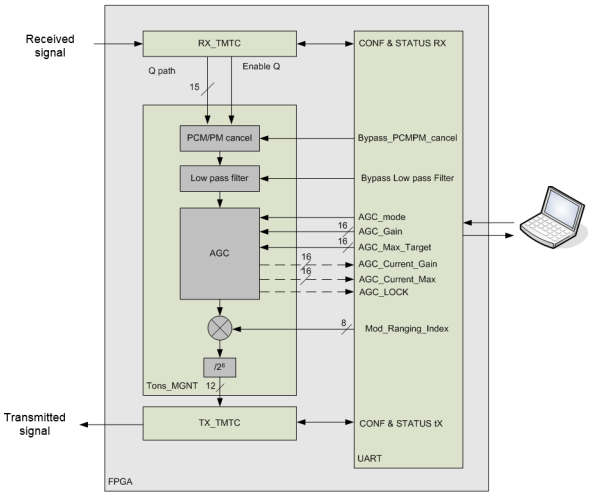


Figure 10 - Block diagram of the FPGA implementation of the ranging management

8. COHERENCY MANAGEMENT DESCRIPTION

The coherency mode is used for orbital determination in compliance with ECSS-E-ST-50-02C. The frequency turnaround ratio is 240/221.

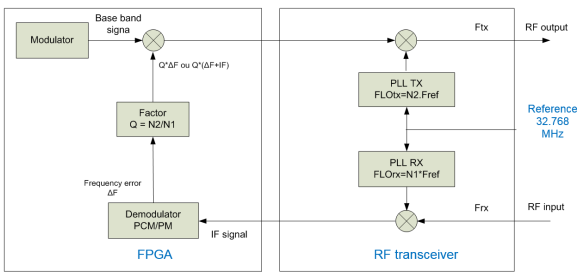


Figure 11 - Bloc diagram of the Coherent transponder implementation

9. RF AND HARDWARE CONSIDERATIONS

9.1 RF power amplifier

5 W is the RF output power requirement at the output of the transmitter. The following items have to be designed accordingly:

- RF power amplifier
- Isolator at output of the power amplifier
- Diplexer filter
- Power supply of the transmitter

Moreover a thermal simulation has to confirmed that each internal electronic device works at a temperature in compliance with the derating requirement as specified in ECSS.

The power amplifier is designed to cover a wide range of output powers from 0.5 W to 10 W in S-band with an efficiency as high as 75% at maximum output. The power amplifier stage works as close as possible to its 3dB compression point to achieve the best efficiency. The power amplifier remains in its Safe Operating Area (SOA) under all operating conditions as indicated in the following figure.

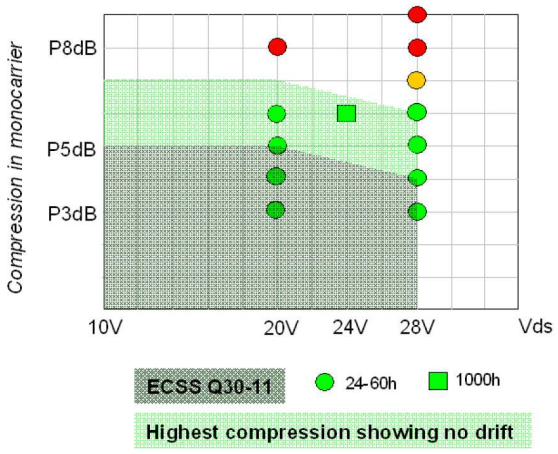


Figure 12 – Safe Operating Area of the power amplifier, determined by endurance test, versus supply voltage

The following table provides power requirements and bias condition for the power amplifier.

RF power at antenna port	5 W (37 dBm)
Required typical power at output of the power amplifier	37.9dBm
Required maximum power at output of the power amplifier	38.7dBm
Supply voltage	24V±20%

Table 3 - Requirements for the power amplifier

9.2 RF diplexer

Diplexer is dimensioned to comply with 10 W RF power, free of multipaction, plus the additional margin as required by ECSS.

Req number	Item	Nominal value / limits	Comments
REQ - 1	Tx central frequency F1	Tunable (factory) between 2200 and 2290MHz	
REQ - 2	Tx band	F1±1MHz	
REQ - 3	Insertion loss in Tx band	0.5dB typ. / 0.8dB max	
REQ - 4	Return loss in Tx Band	< -22dB	
REQ - 5	Rejection at F2 ±1MHz (see F2 definition below)	60dB min	
REQ - 6	Rx central frequency F2	Tunable (factory) between 2025 and 2110MHz	
REQ - 7	Rx band	F2±1MHz	
REQ - 8	Insertion loss in Rx band	0.5dB typ. / 0.8dB max	
REQ - 9	Return loss in Rx Band	< -22dB	
REQ - 10	Rejection at F1 ±1MHz	80dB min	
REQ - 11	F1-F2	175MHz mini	
REQ - 12	Input Power	40dBm (10W)	
REQ - 13	Multipactor	10dB margin 6dB margin 3dB margin	By simulation By test if needed (QM) By test if needed (FM)
REQ - 14	EMC		

Table 4 - Technical requirements for the diplexer unit

9.3 Power supply

The main DcDc converter has to provide at least 24V to the power amplifier. Required DC power is 17 W. The architecture of the DcDc converter of the transmitter is based on the FLYBACK technique working in continuous mode. The DcDc converter works with a 200 kHz switching frequency.

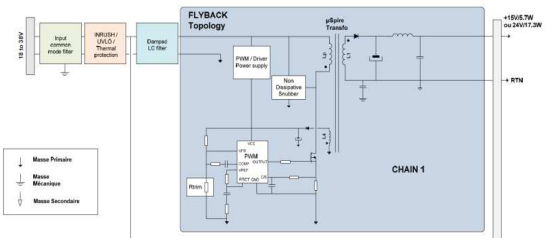


Figure 13 - DcDc converter architecture – High-voltage part

10. SIMULATION RESULTS OF THE DIGITAL PROCESSING

10.1 Introduction

Simulations focus on:
- The coherency mode
- The ranging mode
- The PSK/PM/NRZ-L modulator

10.2 Coherency

A Matlab test bench was developed in order to simulate the Coherency function performance.

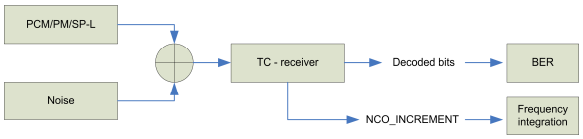
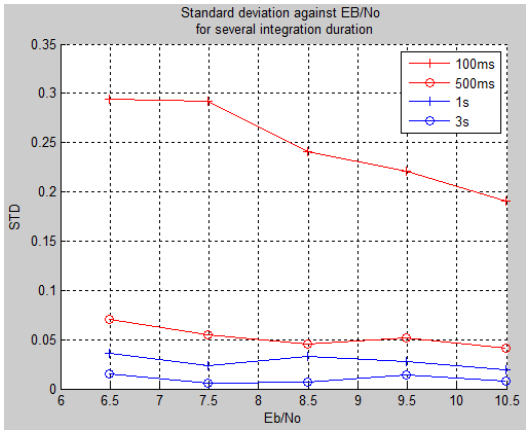


Figure 14 - Synoptic of Matlab simulator

The main functions of the bench are:
- PCM/PM/SP-L waveform generator - This function generates a PCM/PM/SP-L signal at 8, 16, 32, 64, 128 or 256kbits/s
- Noise generator - This function generates a white noise which is added to the PCM/PM/SP-L signal
- TC receiver - This function is a PCM/PM/SP-L receiver. This receiver is the model used for the development of the receiver implemented in the FPGA
- BER - This function computes the BER by comparing the modulated bits to the demodulated bits
- Frequency integration - This function integrates the frequency measurement over a configurable duration



- **Figure 15 –** Example - Data rate 32kbits/s – Frequency standard deviation (Hz) for several integration duration

10.3 Ranging

A Matlab test bench was developed in order to simulate the Ranging function performance.

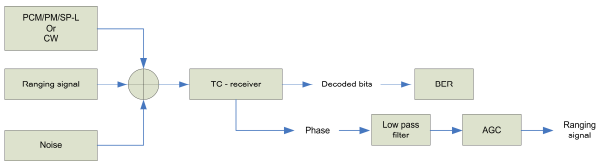


Figure 16 - Synoptic of Matlab simulator for transparent ranging

The main functions of the bench are:

- PCM/PM/SP-L waveform generator - This function generates a PCM/PM/SP-L signal at 8, 16, 32, 64, 128 or 256kbits/s
- Noise generator - This function generates a white noise which is added to the PCM/PM/SP-L signal
- Ranging signal generator - The function generates a tone at a configured frequency with a configured modulation index
- TC receiver - This function is a PCM/PM/SP-L receiver. This receiver is the model used for the development of the receiver implemented on the FPGA
- BER - This function computes the BER by comparing the modulated bits to the demodulated bits
- Ranging signal computation - This function is composed of a digital FIR filter and an ALC

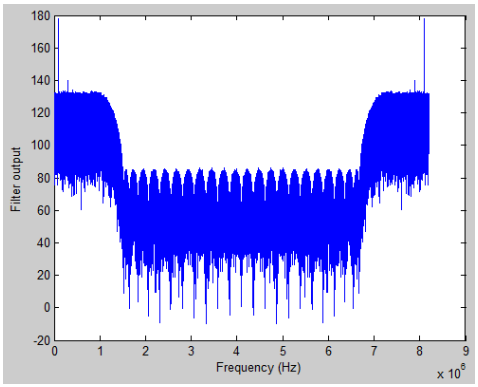


Figure 17 – Example – Signal at the output of the ranging filter (Eb/N0 set to 20dB)

10.4 PSK/PM modulation

The PCM(NRZ-L)/PSK/PM modulation is implemented in order to allow simultaneous ranging and telemetry functionalities.

The PCM(NRZ-L)/PSK/PM modulation is implemented with MATLAB. The following figures show the signal at the output of the PCM(NRZ-L)/PSK/PM modulator with the following parameters :

- Data rate : 4 kbps
- Sub carrier frequency : 4*Data rate = 16 kHz
- Modulation index = 1.0

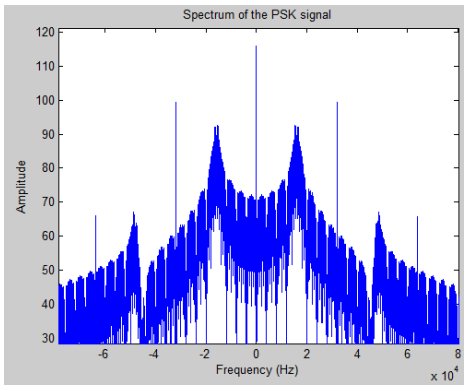


Figure 18 – Spectrum at the output of the PSK modulator (modulation index = 1.0)

11. TEST OF THE DEMONSTRATOR

11.1 Laboratory tests benches

Test benches are defined for every parameter to measure.

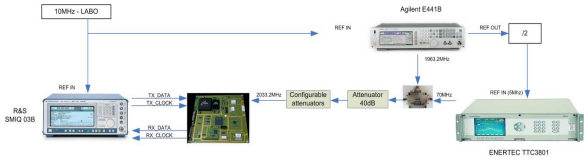


Figure 19 – Example - Bench to measure receiver performances

11.2 Tests results

11.2.1 Introduction

Results are globally in accordance with the requirements. Some examples of results are given.

11.2.2 Implementation loss of the receiver

The implementation losses are plot on the following figure:

- Blue curve: Theoretical performances
- Red curve: Measured performances
- Gray curve: Theoretical curve + 1dB of implementation loss

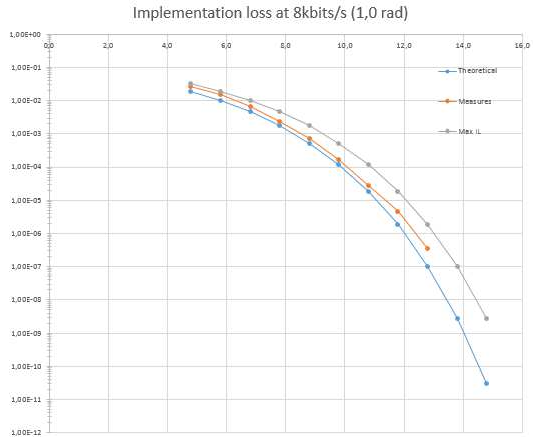


Figure 20 - Implementation loss of the receiver at (Conditions 8kbits/s - 1.0 rad)

Implementation loss of the receiver is a few 0.1 dB, compliant to the requirement that is 2.5 dB maximum.

11.2.3 Acquisition and tracking of the receiver

This test checks that the receiver is able to acquire and lock onto a Continuous Wave carrier transmitted from ground. For this example, the frequency sweep range is set to +/-140 kHz, and the frequency slope is set to 32 kHz/s. Input power is set at -120 dBm. The following figure shows the value of the frequency shift in Hz measured by the receiver.

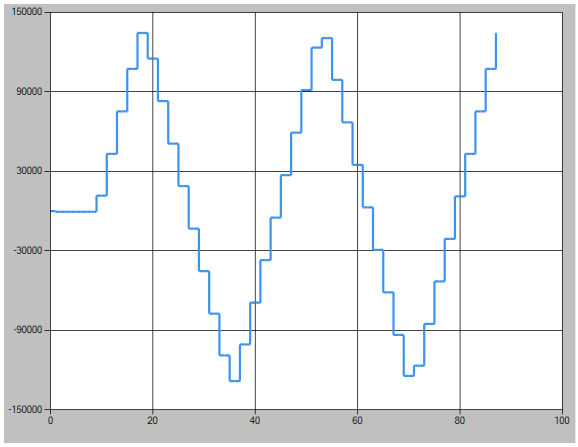


Figure 21 - Frequency shift in Hz measured by the receiver

11.2.4 Transmitter phase noise

The phase noise at the output of the transmitter in coherent mode

The RMS error is around **1.5°**. The excess of phase noise at 100 kHz is due to the RF transceiver chip (phase locked loop filter of the RF synthesizer).

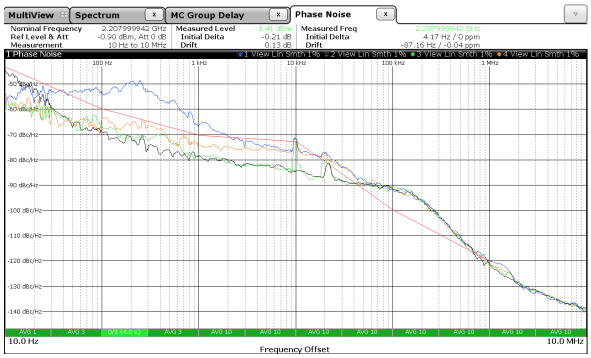


Figure 22 - Phase noise in coherent mode

- Red curve: Phase noise mask required in the ECSS
- Black curve: Phase noise in non-coherent mode
- Green curve: Phase noise in coherent mode without signal at the input of the receiver
- Orange curve: Phase noise in coherent mode with an input signal at -114dBm
- Blue curve: Phase noise in coherent mode with an input signal at -60dBm

There is an influence on the transmitted signal phase noise of the power of the signal applied at the input of the receiver.

11.2.5 Frequency stability in coherent mode - Allan variance

This test checks the carrier frequency stability at the output of the transmitter when it operates in coherent mode. The square root of Allan variance is measured up to 10s.

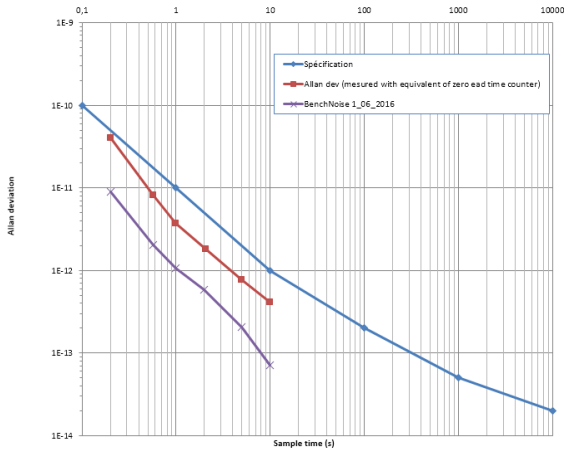


Figure 23 - Square root of Allan variance on the transmitted signal in coherent mode

11.2.6 Group delay in ranging mode

The measure of the variation of the group delay with a tone frequency ft of 100 kHz is given after.

Figure 24 - Group delay variation between 0.3*ft and 1.7*ft (ft=100kHz)

The group delay variation is around 10.7 ns compliant with requirement of 30 ns. The absolute value of the delay of the ranging signal from the RF input to the RF output of the breadboard is equal to 6.6 µs (this delay does not take into account the delay introduced by the power amplifier of the transmitter, nor the delay introduced by the diplexer unit).

11.2.7 Delay in coherent mode

The measure of the delay in coherent mode is difficult to achieve. Anyway a test bench was built using a turn-around ratio between the transmitter and the receiver of 221/221 instead of 221/240. The result gives a delay of 4.5 µs, to be compared to the computed value of 4.3 µs.

12. EUROPEAN GAN MMIC VERSUS AMERICAN MMIC

The 5-W RF power amplifier is designed at the moment around a power amplifier (MMIC) from an American source. This power amplifier is a Gallium Nitride (GaN) component. Some investigation was done in order to identify a possible European source for this power amplifier.

United Monolithic Semiconductors (UMS), a European company proposes a similar product as the one used in the actual design.

A brief comparison between the European and American sources is made.

	European GaN power amplifier	American GaN power amplifier
Frequency	Up to 6 GHz	Up to 6 GHz
Small signal gain	15 dB	16 dB
Saturated power Psat	18 W	13 W
Efficiency at Psat	65 %	65 %
Nominal power supply	28 V	28 V
Cost	A few 100 €	A few 100 €

Table 3 – Comparison between European and American GaN power amplifier

The European and American devices are similar. If the European source has to be chosen, then an evaluation campaign for the component should be done according to space application.

13. SRRC FILTER VERSUS BUTTERWORTH FILTER ORDER 7 IN TRANSMITTER

The actual filtering, implemented in the digital processing unit of the transmitter section, is a Butterworth order 7 digital filter. This approximation was chosen in order to use a reasonable amount of gates/memory inside the FPGA unit, while being able to address 10 different data rates selectable in-flight.

SRRC filtering could have been used, but this kind of filter is more dedicated to only one data rate implemented in the equipment. Addressing 10 different data rates would have led to use a greater amount of gates/memory inside the FPGA unit.

Some simulation experiments were done on a similar application. The difference in performance between SSRC filter and the Butterworth filter order 7 is very slight: technological loss difference is in the order of a few 0.1 dB.

14. CONCLUSION OF THE GSTP STUDY

In the frame of the GSTP5 activity, a S-Band transponder demonstrator was developed. The demonstrator project is conducted in parallel with the Myriade Evolutions and GSTP6 projects that consist in developing and manufacturing a S-Band transceiver.

Two main functions of the S-Band transponder were implemented during the GSTP5 program:
- Coherency
- Ranging channel

Moreover, the following functionalities were developed:

- 10 different selectable Telemetry data rates, selectable in-flight
- RF transmit power up to 5 W
- Definition of the DcDc converter that is able to provide the power for a 5-W RF output power
- Definition of the Diplexer filter that is able to provide the power for a 5-W RF output power
- Analysis of the use of a European GaN MMIC versus an American GaN MMIC
- Discussion about a SRRC filter versus Butterworth order 7 filter

The demonstrator, is a set of items: hardware board and all the associated software, digital codes and user interface. The demonstrator was developed, built and tested. The main conclusions are:

- Coherency tested successfully
- Ranging function tested successfully
- 10 different selectable Telemetry (TM) data rates tested successfully
- Validation of a 5-W RF output power
- Definition of the DcDc converter
- Definition of the Diplexer filter
- Analysis of the use of a European GaN MMIC
- Discussion about a SRRC filter

The outcome of the GSTP5 activity is very successful and SYRLINKS is now ready to propose an efficient S-Band transponder for satellite platforms.

ACRONYM

BER	Bit Error Rate
CNES	Centre National d'Etudes Spatiales (French space agency)
COTS	Components Off The Shelves
ESA	European Space Agency
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
MMIC	Monolithic Microwave Integrated Circuit
OBC	On Board Computer
OCXO	Oven Controlled Crystal Oscillator
RF	RadioFrequency
Rx	Receiver
TC	TeleCommand
TM	TeleMetry
TT&C	Telecommand Telemetry
Tx	Transmitter