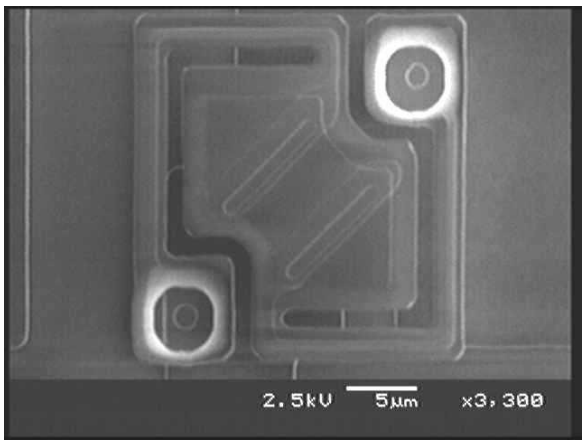

Executive Summary Report

Vanadium Oxide High-resolution Uncooled Bolometer Array

(MegaVoX)

Doc ref.: XP-Space-03-REP-XE-032R3.0

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Rosa Maria Vinella – Xenics

05/12/2018, Leuven, Belgium

Revision history

Issue	Issue date	Affected page(s)	Modifications	Modified by
R1.0	05/06/2015	All	Creation of the document	See list of authors
R2.0	29/04/2016	All	Release of the document	See list of authors
R3.0	05/12/2018	All	New Release of the document	See list of authors

1. Introduction

The ability to quantify Earth's optical properties in the thermal infrared spectral region is a frequent requirement. This has traditionally been achieved using semiconductor photon detectors which require cryogenic cooling. However, cryogenic operation, even at moderate temperatures ranging between approximately 50K and 150K, is costly and represents a major drive towards increased instrument and spacecraft system complexity. Advances in uncooled thermal detectors over the last decade, both in North America and Europe, are changing the landscape of TIR detectors for space applications. An increasing number of space missions, for both Earth Observation and Astronomy, are currently flying, integrating, planning or envisaging payloads designed around room temperature micro-bolometer (RTμB) arrays. The sensing element in a resistive micro-bolometer usually consists of a thin film micro-bridge: a thermometer-absorber thermally isolated by being suspended above the underlying substrate. The substrate is mostly manufactured in standard CMOS technology and incorporates the read-out circuit (ROIC). The materials of the planar micro-bridge currently competing on the market today are, essentially: Vanadium (di) oxide or VO_x, amorphous Silicon or α-Si, and Silicon-Germanium or Si-Ge.

This GSTP project aimed at further pushing the micro-bolometer VO_x technology and capabilities for push-broom and 2D imaging to meet generic goal requirements for future EO missions. For this purpose, a 2D megapixel array format was targeted that would achieve equivalent or better than the state-of-the-art uncooled micro-bolometer sensors worldwide.

Xenics and INO collaborated to develop an LWIR 17μm pixel-pitch, 1024x1024 resolution, micro-bolometer FPA: Xenics was responsible for designing the ROIC suitable for the proposed format and frame rate; INO shouldered the responsibility of micro-bolometer design and fabrication. Together, we optimized some of the ROIC and micro-bolometer parts and processes based on the knowhow derived from a previous joint project on the design of a 35μm pixel-pitch micro-bolometer FPA.

2. ROIC and micro-bolometer pixel development

The specifications targeted for the FPAs are detailed in Table 1. As usual with projects of such complexity, an accurate performance model was developed in order to estimate the expected micro-bolometer performance for typical pixel values and typical ROIC settings (integration time, integration capacitance, and bolometer bias). The model helped in optimizing lots of ROIC and micro-bolometer design parameters and showed that most of the important performance parameters such as, NEP, thermal time constant, thermal dynamic range and thermal responsivity were met.

NEP (Noise Equivalent Power) was considered the main performance design driver.

Table 1: Target system level specifications for the uncooled micro-bolometer sensor

Spec. No	Detector parameter	Threshold value	Goal value	Design value
1	Array size	768 x 768	1280 x 1024	1024*1024
2	Pixel pitch	25µm	17µm	17µm
3	Fill factor (FF)	> 0.8		>0.5
4	Spectral range	[8-12 µm]	[7-15 µm]	> [8-12 µm]
5	Spectral response variation (spectral flatness)	< 10 %	< 5 %	
6	Spectral response slope	--		--
7	Signal dynamic range	200 – 350 K		>100 K
8	Thermal responsivity	7 mV/K		
9	Noise Equivalent Power (NEP)	< 15 pW		15 pW
10	Spatial NEP	< temporal NEP		
11	Thermal time constant	< 8 ms	< 4 ms	7 ms
12	PRNU	< 5 % rms	< 1 % rms	
13	Crosstalk	< 1 %		
14	Linearity	< 1 %		
15	Operability	> 99.5 %	> 99.9 %	
16	TDI function	Yes		No
17	Frame rate	65 Hz	130 Hz	60-200 Hz
18	Power consumption	--	--	<500mW

The ROIC is a 2D megapixel readout IC with a core of 1024x1024 pixels.

The pixel architecture is CTIA based and it is designed on a 17µm pitch. It supports up to 8 analog outputs for frame rates up to 200 fps. An on-chip digital core contains the SPI configuration interface and a sequencer generating the protocol to control the analog core.

Along with the optimization of the performance in order to fulfill required NEP<15pW, additional challenges for the ROIC design were represented by the introduction of a novel architecture able to support readout up to 200fps, namely the Rolling Shutter mode with Parallel Line-based integration. In this case the frame is subdivided in several horizontal sections called segments; these segments are read out in a rolling shutter mode with line based integration. The benefit of this segmentation lies in the fact that parallelism is created in the integration operation such that the integration time can be increased with the number of segments, whereas reaching high frame rate.

The top metal layer of each pixel consists of metal paths which serve as connection points for the micro-bolometer.

Some special features were also implemented in the ROIC

a) CDS: Correlated Double Sampling to remove the fixed noise and offsets

b) Segmentation: The whole array was segmented in 8 parts so as to make them work in parallel. This helped in optimizing the integration time need for the targeted frame rates
c) On-chip NUC: In the previous generation of the micro-bolometer ROICs, the non-uniformity compensation bits were loaded dynamically during the integration phase. This was not possible in this higher resolution array, so a mechanism was brain-stormed and implemented to achieve on-chip NUC.
d) Over-exposure detection: The micro-bolometer pixel does not suffer from temporary heating as long as it is biased for short periods of time and there is sufficient time for cooling down. In typical operating scenarios, these conditions were automatically ensured. But, in the event of malfunctioning or inappropriate settings, there was a real possibility that some of the micro-bolometer pixels were addressed and biased for an unacceptable long period of time. A detection mechanism was implemented to achieve this.

The design drivers for the bolometer pixel consist in the large FPA format and 17µm pitch selected. The pixels proposed for this project are based on design and process improvements of the legacy 35µm-pitch pixels, focusing on three challenges mainly associated with the smaller pixel pitch.

The first challenge is to provide sufficient thermal isolation to simultaneously meet the pixel responsivity and thermal time constant requirements. Indeed, as the pixel is scaled down from 35 µm to 17 µm, the size of the platform does decrease more rapidly than the leg length, leading to a reduction of the response time and thus to a non-optimal responsivity and NEP. To overcome this issue, approaches to further reduce the thermal conductance need to be pushed forward. To address this challenge, the proposed pixel process supports reduced pixel leg width and thickness, and increased leg length. Sufficient mechanical stability is kept to meet the environmental conditions typically associated to space missions.

The second challenge to address is the pixel absorption, which can be negatively impacted by the smaller fill factor. The pixel proposed here is based on a modified layout to optimize the fill factor, combined with the use of a specific absorber. The resulting pixel provides adequate absorbance to meet the pixel-level responsivity requirement.

Besides the two responsivity-related issues mentioned above, reduction of the noise level is also a critical aspect when reducing the pixel pitch. While the VO_x volume decreases with the pixel size, the pixel 1/f noise coefficient increases proportionally. Approaches involving the improvement of the vanadium oxide film properties and the relative enlargement of the pixel platform were therefore privileged.

Based on INO's historical data, and on a development lot fabricated during the project which included different process-level splits and pixel design variants, the baseline pixel was established. A SEM picture of the selected pixel is shown in Figure 2-1. This pixel was found to be an acceptable compromise between manufacturing complexity and compatibility with FPA operation, while meeting the pixel-level requirements established with some margin.

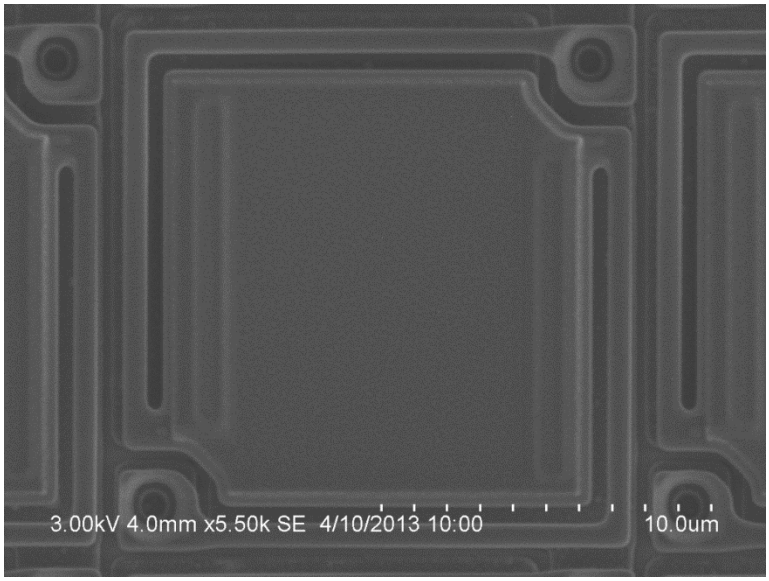

Figure 2-1: SEM picture of the pixel selected as the baseline approach.

3. Analysis of the results

The micro-bolometer pixel results were good and it was possible to demonstrate that 17µm pixel-pitch developed during the course of the project are in line with pixel-level requirements and thus support the FPA system level requirements.

A detailed characterization of active and reference test pixels was performed on one wafer of the ROIC fab (Table 2). Because of the sheet resistance issue, the test had to be conducted at +12°C instead of the nominal -10°C temperature originally targeted. It was found that at +12°C the resistance of pixels from W08 are close to the nominal 200 kΩ and have a TCR close to the targeted value at -10°C. The active test pixels were found to be compliant to the requirements, and provided for a thermal time constant of 6.73 ms and a responsivity of 912 kV/W. The 1/f noise coefficient of active and reference pixels were measured to be of the order of 1 X 10^{-12}.

Table 2: Radiometric characterization results for FPA W08

Pixel parameter	Pixel-level requirement	Active pixel variant	
		Pixels with absorber	Pixels without absorber
Test temperature	-10°C	+12°C	
TCR (absolute value)	> 2.6%/K	2.74%/K	
Time constant	< 8 ms	6.73 ms	6.51 ms
Responsivity (1 V)	> 600 kV/W	912 kV/W	741 kV/W
Thermal conductance	N/A	21.8 nW/K	21.5 nW/K
Effective absorption	>36%	72.6%	58.3%
Thermal mass	50-200 pJ/K	147 pJ/K	140 pJ/K
1/f noise coefficient	< 3 X 10^{-12}	~1 X 10^{-12}	

Due to the stringent requirements for the u-bolometer fabrication about size of the openings, passivation planarity and residual topology, it was decided to customize the finishing of the ROIC wafers. The ROIC wafers were manufactured (TSMC) unpassivated, meaning skipping the full passivation step in the CMOS process. A customized passivation and planarization process has been developed together with ENAS-Fraunhofer Institute, resulting in a very planar ROIC surface with almost zero residual topology.

After the passivation and planarization the ROIC wafers have been tested for basic electrical functionality before and after coring down to 6inch, required by INO. This process flow, challenging on its own, was proven to be successful and ROIC wafers were shipped to INO, according to the requirements.

During the first testing phase at ROIC wafers level, only functional checks were done. Correct slave bias voltages were read from the test pins, proving that the band-gap reference and current generation circuits supply the correct voltage values to the front stage. However, during the performance tests, the chip didn't react correctly to the change in control signal timings. Detailed investigation showed that when the frame grabbing mode was enabled, bias voltages driving the CTIA and segment buffers deviated drastically from their expected values.

The design problem related to the biasing circuit was solved during a ROIC re-spin. Nevertheless, the correct biasing of the circuits showed problems with the performance of the ROIC. Due to the large size and complex structure of the segments, the ROIC does not respond as uniformly as expected, and the on-chip NUC algorithm cannot compensate for the large non-uniformity due to the ROIC design.

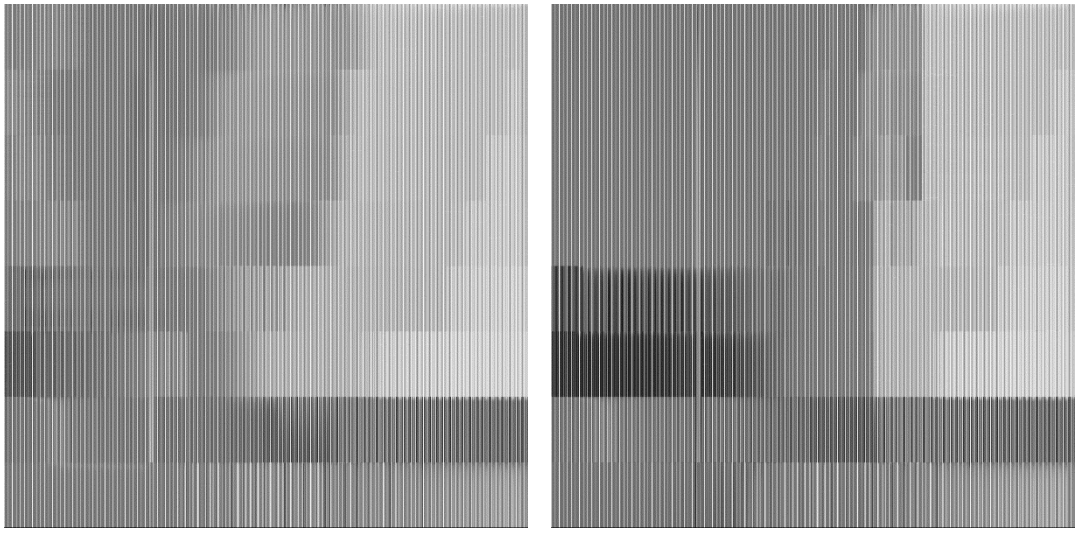

Figure 3-1: NUC algorithm start (left) and end (right) images.

The target of the algorithm is to obtain a uniform image. The histogram of the end image is depicted below.

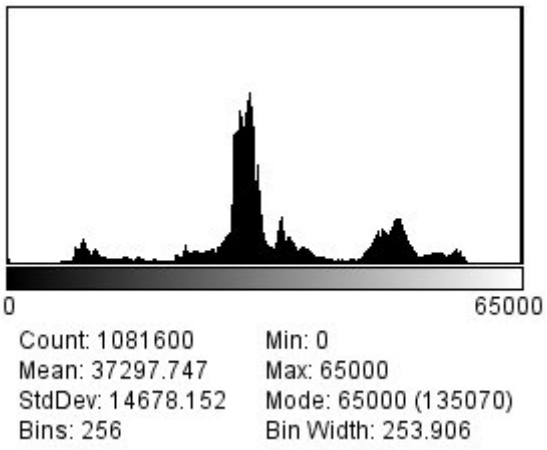

Figure 3-2: Histogram of NUC algorithm test end image

Although there is a clear peak in the middle of the histogram as expected. There are other “humps” in the histogram as a result of the brighter and darker areas in the image. Nevertheless, if we consider a window of interest of 512x512 pixels in the top left corner of the FPA, the histogram of this section shows one clear peak.

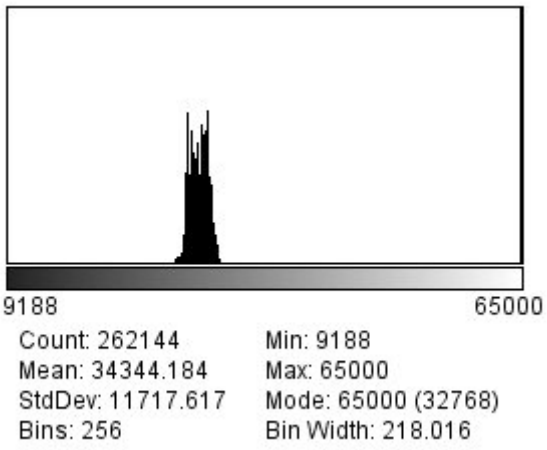

Figure 3-3: Histogram of a 512x512 window of NUC algorithm test end image.

To fully characterize the performance of the detector and to measure the radiometric properties of the chip, a dedicated test setup was designed and built as shown in Figure 3-4. This setup was intended to be compact enough to fit inside a climate chamber, allowing the radiometric test to be conducted in different ambient temperatures/conditions. An additional thermal electrical cooler was foreseen inside the detector package for extra temperature stability. A packaged die is shown in Figure 3-5.

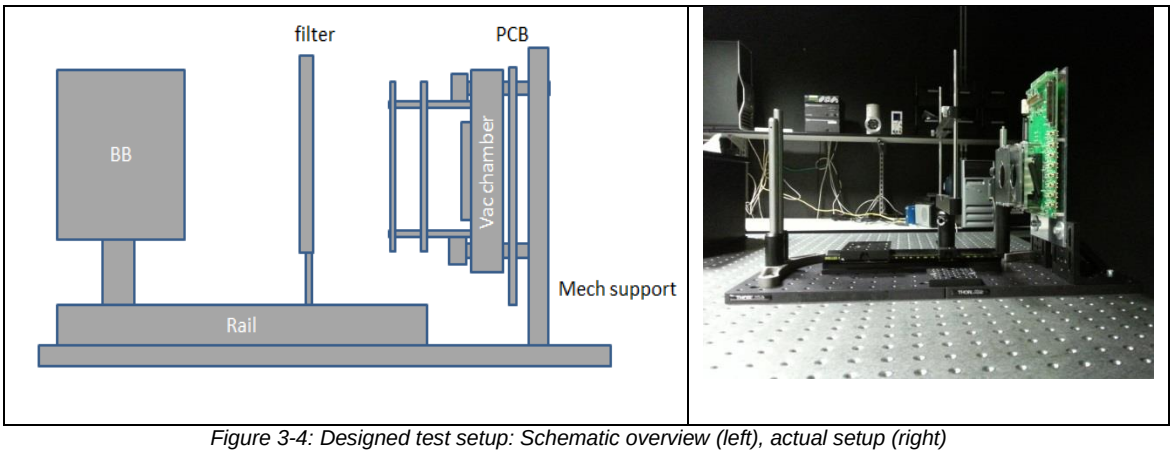

Figure 3-4: Designed test setup: Schematic overview (left), actual setup (right)

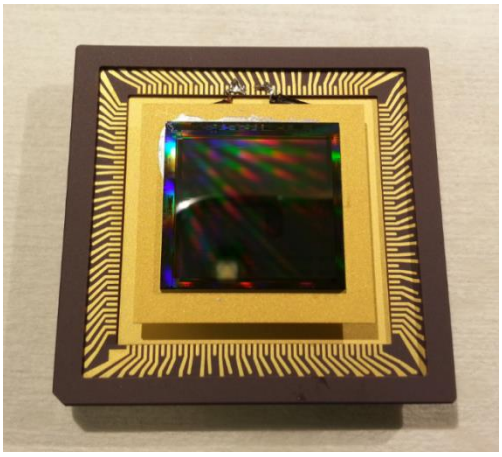

Figure 3-5: A packaged die

Due to the not-optimal performance of the ROIC, the micro-bolometer was not deposited onto the ROIC wafer; as consequence, the full radiometric characterization was not completed.

4. Findings and conclusions

Overall, several roadblocks in the development of high resolution micro-bolometer based FPAs have been identified, brain-stormed and solved during this development project. The experience gained should help in reducing the pixel pitch below 17µm or increasing the array resolution or both to enable future EO space missions. Here are some of the roadblocks and takeaways:

a) A state-of-the-art micro-bolometer 17µm pixel-pitch was designed, fabricated and verified.
b) It was observed that novel ROIC architectures and readout mechanisms were needed to go beyond VGA resolution of micro-bolometer FPAs. This is linked to way micro-bolometer arrays are operated and their variability across the array.
c) High resolution ROICs need exhaustive and much more robust verification methods than planned.

A new re-spin of the ROIC with improved bias generation circuits was completed; together with promising results achieved within the project by INO, the authors were confident to be able to demonstrate and fulfill the initial requirements for NEP. Unfortunately the NEP could not be tested and demonstration of the initial requirements could not be completed.