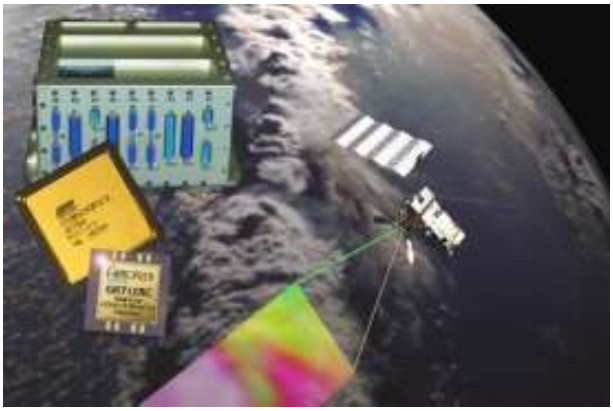
On-board Payload Processing
LEON with Fast Fourier Transform Co-processor (LFCP)



Satellites become more and more complex, with sensors that have a growing demand in bandwidth, resolution, sensitivity and accuracy. This results in higher data volumes generated by these sensors. The downlink capacity also increases, but not in the same pace resulting in a limited downlink capacity. This can be solved with data compression or more on-board data processing (aiming for less data to be downloaded).

Some instruments can highly benefit from processing with the aid of the Fast Fourier Transform (FFT) operation. So far, satellite system engineers tried to avoid this complex operation, as there was not enough processing power available onboard the spacecraft. Space qualified processors were not fast enough to perform FFTs on the high speed data streams; FPGA-cores were not accurate or not flexible enough. This has changed with the availability of the SkyFFT (also known as Fast Fourier Transform Co-processor – FFTC); a space qualified ASIC that can perform all kinds of FFT-operations in combination with an ALU (arithmetic / logic unit)

The developed module demonstrates all capabilities of the SkyFFT/FFTC

Key features:

- Boards size of this EM-model: 245 x 125mm (could be reduced to 125 x 125 with external power conditioning)
- SkyFFT / FPGA / SDRAM are space grade

- Full floating point FFT accuracy
- 1D FFT of 1024 points in 10 us
- Long 1D FFT of 1 million points in 20 ms
- 2D FFT of 1024 x 1024 points in 20 ms

- Four additional memory ports on which SDRAMs can be attached for storage of intermediate results, giving the opportunety of 2D FFT operations or long FFT upto 1M FFT operations.
- Variety of input formats
  - Full floating point (IEEE 32 bits)
  - Signed / unsigned long integers (32 bits)
  - Signed / unsigned Integer (16 bits)
- ALU (part of SkyFFT) gives several options:
- Variety of FFT operations / ALU instructions
  - FFT / Inverse-FFT
  - Addition / Substraction / Multiply
  - Conjugate / Conjugate Multiply

Interfaces:

- TM/TC via SpaceWire
- High speed data input/output via SpaceFibre (up to 1.6 Gbit/sec)
- Low speed data input/output via SpaceWire (200 Mbit/sec)

Other characteristics:

- Power supply of 3.3 Volt
- Max power consumption of 10 Watt
- Weight: approx 2500 grams
- Envisaged temperature range
  EM-model: -45 – +70 °C
  FM-model: -55 – +100 °C
- Envisaged Radiation FM-model:
  TID: 100 krad
  LET: free upto 60 MeV-cm^2/mg.

Architecture

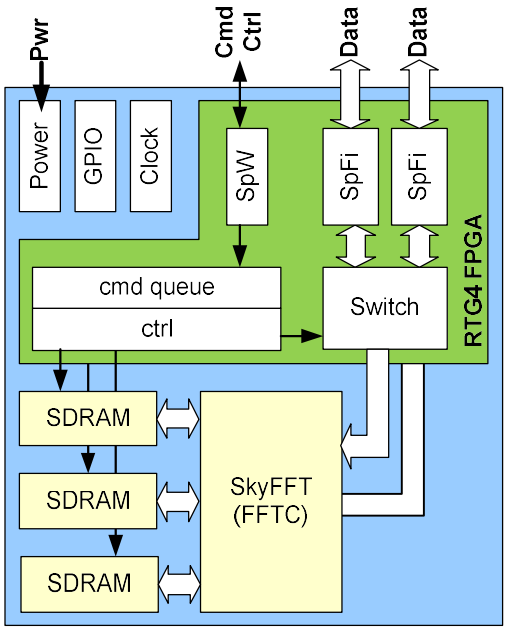


Figure 1: LFCP-board architecture

The board consists of

- The SkyFFT/FFTC
  (in prototype package, but with the space qualified die in it)
- MicroSemi RTG4 FPGA, for the control
- 3D_SD_2G64_VB4488
  SDRAM memory of 3Dplus
  (2Gbit, organised as 32M x 64 bit)
- SpaceFibre data interface
- SpaceWire command and control interface

SpaceFibre interface / SpaceWire interface

The board is equipped with two SpaceFibre interfaces with a data switch in the FPGA. Input data can be selected on SpFi1 and output on SpFi2 or input- and output both on SpFi1 (bidirectional).
The SpaceFibre has a gross data rate of 2.5 Gbit/s; net 2 Gbit/s. SpFi interfaces are available by edge SATA3 connectors. The SpFi signals are A/C coupled to the RTG4 SERDES blocks.

The SpaceWire interface is used for commanding. For the control of the SkyFFTC, an entire series of low level commands, including the memory addressing scheme, is loaded into the control queue inside the FPGA. On a ‘go’ command this macro is executed. This is done to prevent that the commanding is becoming the bottleneck in the data processing chain.

This macro definition is a rather complex definition in order to support all input and output data formats of the SkyFFT, all possible SkyFFT commands and the different SkyFFT configurations, but also for corner turning, loop contructions, ping-pong constructions, settings for the FPGA itself, etc. Once the macro is loaded even an endless loop can be made for continues instrument data processing.

SpaceWire can also be used for low speed data interface

Control FPGA

- Decoding of the macro command script
- SDRAM addressing (including refresh), such that the FFT processor is independent of external memory type
- Low level command of the SkyFFT
- SpFi interfacing
- SpW interfacing
- Fill rate: 4LUT 15% -- DFF 11% -- RAM 11% -- SerDes-blocks 17%

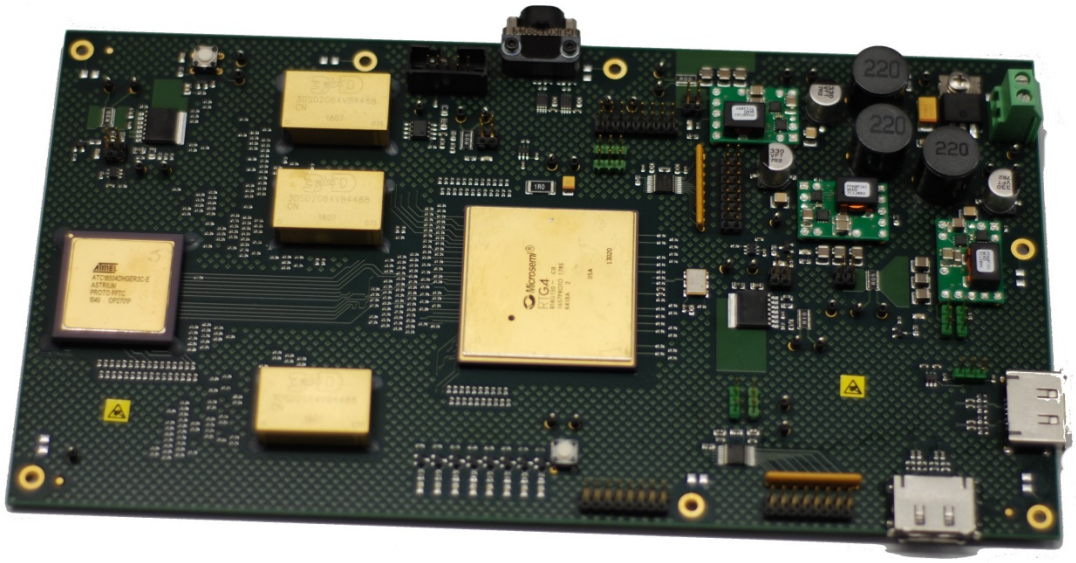


Figure 1: LFCP-board

Figure 1: The RTG4 FPGA on the LFCP-board

Figure 1: SkyFFT / FFTC on the LFCP-board

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