









# CORHA: Non-volatile Memories

<u>S. Gerardin<sup>1</sup></u>, M. Bagatin<sup>1</sup>, A. Paccagnella<sup>1</sup>, P. Beck<sup>2</sup>, C. Tscherne<sup>2</sup>, M. Wind<sup>2</sup>, M. Poizat<sup>3</sup>

<sup>1</sup> DEI - University of Padova, Italy
<sup>2</sup> Seibersdorf Labor GmbH, Austria
<sup>3</sup> ESA - ESTEC, The Netherlands







# Introduction

- Non-volatile Memories for Small Satellites
- Devices and Storage Concepts
- Experimental Results
  - Total Ionizing Dose
    - Lot-to-lot Variability Study
  - Single Event Effects:
    - Heavy lons
    - Protons
- Conclusions





- Microcontrollers and FPGAs used in small satellites require low-footprint non-volatile memories (NVM) for configuration, code, and data storage purposes
  - The **Serial Peripheral Interface** (SPI) is low-pin count: simplified routing and small board area occupation
  - The **Flash NOR** interface has a larger pin-count and footprint, but provides faster random access











	MB85RS256TY	CY15B102QN	CY14V101PS	MT28EW128ABA		
Part Type	SPI Ferroelectric RAM	SPI Ferroelectric RAM	SPI Non-volatile SRAM (SONOS)	Parallel NOR Flash Memory (Floating Gate)		
Manufacturer	Fujitsu Semiconductor	Cypress	Cypress	Micron Technology		
Size	256 kbit	2 Mbit	1 Mbit	128 Mbit		
Operating Voltage	1.8 to 3.6 V	1.8 to 3.6 V	Core 2.7 to 3.6 V; I/O 1.71 to 2.0 V	Core 2.7 to 3.6 V; I/O 1.65 to 3.6 V		
Operating Temperature	-40°C to 125°C	-40°C to 125°C	-40°C to 85°C	-40°C to 85°C		
Package	SOP8	SOIC8	SOIC16	TSOP56		







- Storage concept: Inject or remove charge between the control gate and the channel
- Charge storage element: floating polysilicon gate (FG), charge-trap layer (e.g. Semiconductor Oxide Nitride Oxide Semiconductor - SONOS)
- Radiation can remove stored charge





Polarized by an electric field



- When an electric field is applied across a dielectric materials, polarization of the dipoles occurs.
- When the field is removed, the polarization disappears unless ferroelectric materials are used
- Cells are not very sensitive to radiation, peripheral circuitry can be, but voltages are low





# TID Irradiation and Annealing



HE RREACT Forgetful File Scripts Action	s Window Help						- 0	×
Arrange ing -00 Connection -01 Sorpt C:(Detaly -02 Instruments -03 Connection -04 Write ICC -04 Write ICC -04 Read ICC -04 Standly ICC -04 Steep ICC	Improvement     Construction     Construction </td <td>1784     4.0       1784     4.0       1784     4.0       1787     4.8       1787     4.8       1787     4.8       1787     4.9       1797     4.9 <td>083</td><td>Characteri Parameter IV ID II ICC_W L BER_R 0 ICC_R L BER_RET 0 ICC_STB 1.</td><td>ation alse 91118110342 1769e-003 8021e-000 2455e-004</td><td>Unite Unite A</td><td></td><td>-</td></td>	1784     4.0       1784     4.0       1784     4.0       1787     4.8       1787     4.8       1787     4.8       1787     4.9       1797     4.9 <td>083</td> <td>Characteri Parameter IV ID II ICC_W L BER_R 0 ICC_R L BER_RET 0 ICC_STB 1.</td> <td>ation alse 91118110342 1769e-003 8021e-000 2455e-004</td> <td>Unite Unite A</td> <td></td> <td>-</td>	083	Characteri Parameter IV ID II ICC_W L BER_R 0 ICC_R L BER_RET 0 ICC_STB 1.	ation alse 91118110342 1769e-003 8021e-000 2455e-004	Unite Unite A		-
	# A: F, IDO, ISB, IZZ, fCK, tCH, tCL, BERret	90.738 *	15478/15490	100,54,899 8. U.R 2	2465e-006	A rs		-
			6 7 8	0.0001246	0 0.5	1 1.5 2	2.5	,
	Steep ICC 😝 🐨 🐼							
	8.35'006 8.15'006 8.16'006 0 0.5 1 1.5 2 2.5 3							

Custom SoC-based system for parametric characterization and power analyser

- Functionality
- Power: operating, standby, etc.
- Timing: read, program, setup and hold time, etc.







Simone Gerardin



- Co<sup>60</sup> source at Seibersdorf Laboratories
- Dose rate: 2.4 krad(Si)/hour
- Steps: 2, 5, 10, 15, 50, 100 krad(Si)
- 24+ hours annealing at room temperature + 1 week at 100°C
- Devices
  - 5 samples under static bias (memories were idle, but selected, ready to operate)
  - 5 unbiased samples (grounded pins)
  - References for each experimental conditions
- Parametric degradation measured and failure modes identified up to 100 krad(Si)











- Ferroelectric memory from Fujitsu
- No issues with cells (FRAM)
- Minor parametric (power consumption) between 15 and 50 krad(Si) in all the biased samples
- Functional failures between 50 and 100 krad(Si) in all the biased samples











- Ferroelectric memory from Cypress
- No issues with cells (FRAM)
- Minor parametric (standby power consumption) between 15 and 50 krad(Si) in 4 out 5 biased samples
- Functional failures between 50 and 100 krad(Si) in biased samples





CY15B102QN (2)

- Limited sample-tosample variability within tested lot
  - One device marginally better and below the set limit
- Current increases also in unbiased devices, but stays below max spec







- Non-volatile SRAM memory
- No issues with functionality of volatile (SRAM) or non-volatile (SONOS) storage
- Tolerable power consumption degradation in the peripheral circuitry above 50 krad(Si)
- No functional failures







- Supply current during write
- Some sample-to-sample variability
- Current marginally increases also in unbiased devices, but stays well below max spec







168 h

100°C

RT

NOR Flash memory I<sub>CC,STB,B</sub> 6 -I<sub>CC,STB,U</sub> No issues with functionality of cells (Floating Gate) 4 Increase in standby Fails current, both in biased and unbiased components 2 No functional failures 0 2 15 50 >24 h

0

5

10

Dose [krad]



MT28EW128ABA (2)

- Some sample-tosample variability
- Current increases also in unbiased devices over Max limit, but much less than in biased devices





## CY15 – TID Lot-to-lot Results

# TID variability study

- Same steps and measurements as during the first campaign
- CY15 FRAM ferroelectric memory







→ 12 → 13

100

RT

HT

🗕 16 Ref

– 6 Ref

6 Ref.

Max (10x)

- Functional failures after 50 krad(Si) in all three lots
- Lot-to-lot Variability is visible in stand-by current evolution with TID
- Recovery of some samples after 100°C annealing. N.B. Lot A (black) irradiated to 100 krad(Si), lot B and lot C (red and blue) to 50 krad(Si)
- All other parameters do not show significant variations across lots



CY15 – TID Lot-to-lot results, grounded components

No failure observed

UNIVERSITÀ DEGLI STUDI DI PADOVA

- Increase in stand-by current (not so different from biased components)
- N.B. Lot A (black) irradiated to 100 krad(Si), lot B and lot C (red and blue) to 50 krad(Si)







# Setup for SEE Tests



#### SEE test setup

- SoC-based motherboard and Power Analyzer (similar to TID setup) + adapter boards
- Start/stop beam commands with dedicated interface
- Delidded components soldered on one side of the adapter board, with heater on the other side
- A sensor is used to monitor the temperature of the board
- Calibration in vacuum to measure die temperature





### Heavy-ion Measurements





# Experimental setup in HIF vacuum chamber



Simone Gerardin



# Detection of SEU and SEFI

#### SEU test sequence:

- > The memory is **written**
- Powered off for non-volatile cells, standby for volatile
- Exposure to a given fluence of particles,
- Power on
- Read
- The number of SEU is logged and used to calculate the cross section

#### SEFI test sequence:

- The memory is continuously exercised through a loop of (erase)/program/read (SEFI full) or read (SEFI read) operations
- When a large number of events is detected or some other exceptional conditions occur, the control PC stops the beam and power-cycle the memory
- When and if the device becomes operational again, the test is resumed
- The number of SEFI is logged and used to calculate the cross section

#### SEL test sequence:

- The memory is biased and heated to the target temperature (RT for the most sensitive devices)
- Exposure in idle ready-tooperate conditions (to maximize the visibility of SEL)
- The supply current is monitored and when a sudden increase is detected, the power and beam are cut
- Brief test to see if memory is operational and if so, then exposure is resumed.
- The number of SEL is logged and used to calculate the cross section







- FRAM technology
- Cells are immune up to > 60 MeV·mg<sup>-1</sup>·cm<sup>2</sup>
- SEFI σ considerably lower than in the Cypress devices
- No SEL @ 85°C









Simone Gerardin





- FRAM technology
- $\blacktriangleright$  Cells are immune up to > 60 MeV·mg<sup>-1</sup>·cm<sup>2</sup>
- Cross sections for SEFIs and SEL (at room temperature) are very close
- Hard to tell if there is a spike in the current, when the device is operating and dynamic current dominates, but it is likely









- nvSRAM (SRAM+SONOS)
- NV cells are immune up to 62.5 MeV·mg<sup>-1</sup>·cm<sup>2</sup> (higher LET will be tested)
- SRAM cells are sensitive
- SEL (RT), SEFI o are similar (again, hard to tell if there is a spike in SEFI events, but it is likely)











- > NOR Flash
- Cells sensitive at 62.50 MeV·mg<sup>-</sup> <sup>1</sup>·cm<sup>2</sup>, σ < 10<sup>-10</sup> cm<sup>2</sup>
- Destructive events with Xe (inability to program and erase). Likely charge pump failure, not related to TID







# **UPD** Proton Tests



- The two most sensitive devices have been tested with protons
  - CY14 nvSRAM
  - CY15 FeRAM
- TIFPA Trento Facility in Italy
  - Flux ~ 3e8

DUT energy [MeV]	Range [mm Si]	LET [MeV/(mg/cm²)]
70	22	8.016·10 <sup>-3</sup>
119	56	5.370·10 <sup>-3</sup>
169	104	4.220·10 <sup>-3</sup>
202	141	3.617·10 <sup>-3</sup>



# CY14: Proton Results



- Events (SEU, SEFI and SEL) with protons consistent with heavy-ion sensitivity
- Large error bars and significant dose for SEFIs









# CY14: SIMPA & PROFIT









Overestimation of proton effects by PROFIT and SIMPA for SEFIs, underestimation for SEU

Models developed many years ago for SEU:

- Fewer materials in the semiconductor industry
- Larger feature size
- Peculiar RAM with associated NV element



# CY15: Proton Results



Events (SEFI and SEL, no SEU) with protons consistent with heavy-ion sensitivity









# CY15: SIMPA & PROFIT

Overestimation of proton effects by PROFIT and SIMPA for SEFI and SEL

Models developed many years ago for SEU:

- Fewer materials in the semiconductor industry
- Larger feature size







# Different SPI memories and a NOR Flash were tested Total Ionizing Dose

- All memory cells, regardless of the storage technology, behave well
- Increase in the supply current in various conditions and to various extents is the most common issue at doses below 50 krad(Si)
- Functional failures can appear above 15 krad(Si)
- In general, the samples show a consistent behavior even between lots in the case of the CY15
- Small differences are visible in stand-by current for the biased components





# Single Event Effects

- All tested NV cells are pretty hard with respect to SEU
  - data loss only with Micron NOR Flash with Heavy lons (HI) at an LET of 62.5 (small  $\sigma)$
- CY14 nvSRAM has expected SEU sensitivity in the SRAM cells (both HI and p)
- Significant and consistent SEL/SEFI  $\sigma$  in Cypress devices (both HI and p)
- Destructive events in the Micron NOR Flash with HI at an LET of 62.5 MeV · mg<sup>-1</sup> · cm<sup>2</sup>

# PROFIT & SIMPA

 Large discrepancies (both overestimation and underestimation) between predicted and measured proton sensitivity

