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# EXECUTIVE SUMMARY REPORT

## ESA-HRLTP

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## 1 INTRODUCTION

The objectives of the ESA-HRLTP project were to:

- Analyse present and future protocol stacks based on previous activities., identify shortcomings in the chosen protocol stacks, define alternatives, simulating performance accordingly.
- Consolidate the potential protocols into a generic protocol stack suitable for high-rate applications.
- Propose modifications and optimisations to this protocol stack in order to support these high rate use cases.
- Analyse the applicability of ARQ protocols, including (but not limited to) LTP, minimizing required uplink data rates.
- Develop prototype on-board and ground segment implementations of the ARQ protocol described in the previous steps.
- Provide input to relevant standardisation organisations (CCSDS, IETF, etc.)

### 1.1 SCOPE AND OUT OF SCOPE

This document aims to give a very brief and high overview of the ESA-HRLTP activities, including a brief overview of results and challenges. It is not intended to be an exhaustive list of the results; an interested reader should read the various project deliverables outlined in section 1.2.

### 1.2 APPLICABLE AND REFERENCED DOCUMENTS

The following documents form part of this document to the extent specified herein. The applicable documents are those referenced in the Contract or relevant to the work at hand, while reference documents are used amplify or clarify its position and contents of this documents.

References within this document are proved in the form [type.num]; e.g. [AD.1]

Within the document, they are:

Ref.	Title	Code	Version	Date
[ITT]	GT10-305GS - Optimised CCSDS Protocol Stack for High Data Rate Invitation to Tender AO/1-10779/21D/MRP	ESA-CIP-POM-MRP-LE-2021-597	-	12 July 2021
[AD.1]	Directory of Definitions, Acronyms and Abbreviations	GMV-HRLTP-DIR-0001	V1.0	08/02/2022
[AD.2]	Technical Note – Link Characterization	GMV-HRLTP-TN-0001	V3.0	21/04/2022
[AD.3]	Technical Note – Downlink Scenarios	GMV-HRLTP-TN-0002	V1.4	21/04/2022
[AD.4]	ARQ Scheme Evaluation and Definition	GMV-HRLTP-TN-0005	V2.0	27/09/2022
[AD.5]	HRLTP Interface Control Document	GMV-HRLTP-DOC-ICD	V2.0	27/09/2022
[AD.6]	Licklider Transmission Protocol (LTP) for CCSDS	CCSDS 734.1-B-1	1	May 2015
[AD.7]	CCSDS 734.2-B-1, CCSSD Bundle Protocol Specification. Blue Book	CCSDS 734.2-B-1	1	September 2015
[AD.8]	Bundle Protocol Version 7	IETF RFC 9171	00	January 2021
[AD.9]	Space Packet Protocol	CCSDS 133.0-B-2	2	June 2020
[AD.10]	Encapsulation Packet Protocol	CCSDS 133.1-B-3	3	May 2020
[AD.11]	Unified Space Data Link Protocol	CCSDS 732.1-B-1	1	October 2018

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Ref.	Title	Code	Version	Date
[AD.12]	TM Space Data Link Protocol	CCSDS 132.0-B-2	2	September 2015
[AD.13]	TC Space Data Link Protocol	CCSDS 232.0-B-3	3	September 2015
[AD.14]	AOS Space Data Link Protocol	CCSDS 732.0-B-3	3	September 2015
[AD.15]	Proximity-1 Space Link Protocol--Data Link Layer	CCSDS 211.0-B-5	5	December 2013
[AD.16]	Generic framing procedure	ITU-T G.7041/Y.1303.	1	August 2016
[AD.17]	Space Data Link Security Protocol	CCSDS 355.0-B-1	1	September 2015
[AD.18]	Flexible Advanced Coding and Modulation Scheme for High Rate Telemetry Applications	CCSDS 131.2-B-1	1	March 2012
[AD.19]	Optical Communications Physical Layer with Pink Sheets. Draft standard	CCSDS 141.0-P-1.1	1	July 2020

## 1.3 LIST OF ACRONYMS

See [AD.1].

## 2 STUDY OVERVIEW

### 2.1 STUDY OUTLINE AND GOALS

Modern space missions produce ever-increasing volumes of data which must be delivered to the ground in a timely fashion. To cope with this challenge, traditional downlinks are being replaced with high-throughput optical and RF links which promise multi-gigabit downlinks at the expense of a reduction in reliability. Multiple approaches have been studied to balance the requirement for reliable data transfer with the volume of data required, including Adaptive/Variable Coding and Modulation as well as network/application-layer Automatic Request Repeat (ARQ) protocols such as CFDP or TCP.

The 12-month HR-LTP activity, performed by GMV (Germany), TESAT (Germany) and the Deutsches Zentrum für Luft- und Raumfahrt (DLR) (Germany) developed and prototyped an Automatic Request Repeat (ARQ) protocol, designed for use at rates of 10 gigabits and above. The design of this protocol was rooted in a novel Model based System Engineering approach, as well as a wide-ranging market study of the existing state of the art of similar protocols. The protocol was implemented in two different prototypes, where the first is based on a modern state-of-the-art FPGA, while the second was designed for ground segment applications and decided for deployment within a ground station.

To ensure that the protocol was capable of enhanced data throughput in "real-world" conditions, an in-depth evaluation of space-to-ground links was performed, and representative scenarios were created. These scenarios were codified into datasets which could be ingested by a network emulation system, allowing users to test the system with representative data.

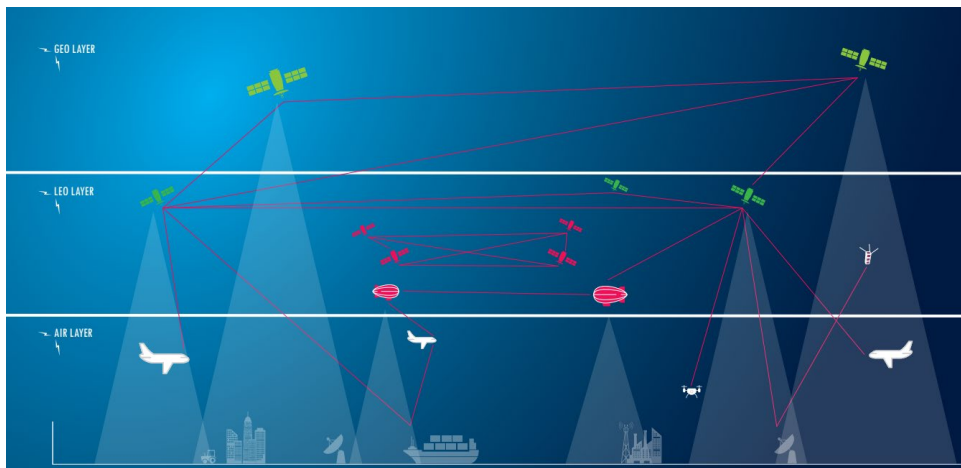
The project, while on an aggressive schedule, was successful and pushed the state-of-the-art within space-to-ground protocols. This final report outlines the preparatory activities, protocol design, prototype development, as well as the final testing of the prototypes. Some activities, such as the submission of the new protocol to CCSDS are on-going, so the present progress is also listed here.

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## 2.2 LINK CHARACTERIZATION AND SCENARIO DEFINITION

The first step of the activity was an analysis of the available link types (for RF, optical, and Inter-Satellite Links) and availability, considering the use of multiple ground stations in diverse locations. Additionally, to help bind the scope of the ARQ protocol, all scenarios will be characterised in terms of:

1. simultaneous uplink availability – for uplink capable ground stations
2. deferred uplink availability – for geographically separated ground stations and unidirectional Direct-to-Earth and Inter-Satellite Links



**Figure 1: Communication Scenarios (image courtesy of Tesat-Spacecom GmbH & Co. KG)**

Both Ka and optical downlinks were considered for the downlink aspect of all scenarios. For the optical scenarios, the project considered data downlinks at 10Gbps and uplinks at 100 kbps with wavelengths in the vicinity of 1550nm, which are divided on the ground and space. The channel characterization considered the minimum feasible power on the uplink beacon for effectively executing the pointing and tracking operations as well as the data reception on the receiver front end to be able to receive the ARQ packets. The link budget for the ground segment considers the opposite operation for the downlink.

## 3 PROTOCOL DESIGN

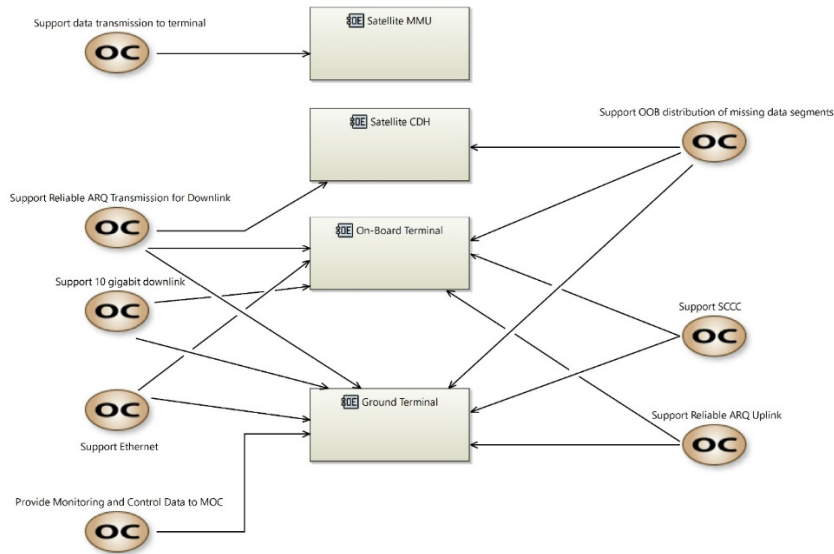
The protocol designed as part of this activity, ultimately deemed version 2 of the Licklider Transmission Protocol (LTPv2), was designed to function across a wide range of performance envelopes and deployment options, while providing a user-friendly interface by which users can interact with the system. To ensure that these diverse requirements were met, the protocol was largely designed via a Model-Based System Engineering (MBSE)-based approach, based upon the Arcadia method.

The following high-level objectives were utilized prior to the initial system engineering effort:

1. The protocol must be deployable within FPGA's/ASIC's, as well as on standard computing hardware.
2. The protocol must allow a range of protocol sizes, etc.
3. The protocol must provide verifiable retransmission capabilities, and not rely on underlying layers.
4. Any buffering required by the protocol may be managed internally or externally.

These objectives were transformed into a set of Operational Capabilities, which are a fundamental concept within the Arcadia method. In the use-case demanded by this activity, an Operational Capability is functionally like a use-case, which is mapped to an actor or other entity.

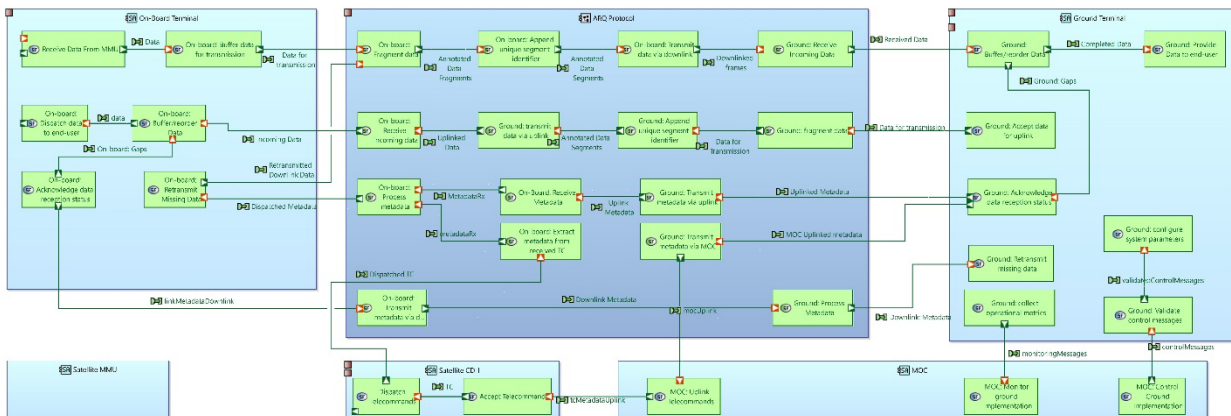
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**Figure 2: Protocol Operational Capabilities Breakdown (OCB)**

## 4 PROTOTYPING

The HR-LTP project produced two different interoperable prototypes of the LTPv2 protocol: the first, running on standard x64-based servers, is intended to represent and be deployable within ground stations, while the second uses an Xilinx Versal-based FPGA to represent next-generation avionics hardware. The LTPv2 protocol specification has been independently implemented on each prototype, using different development methodologies and frameworks.



**Figure 3: System Overview**

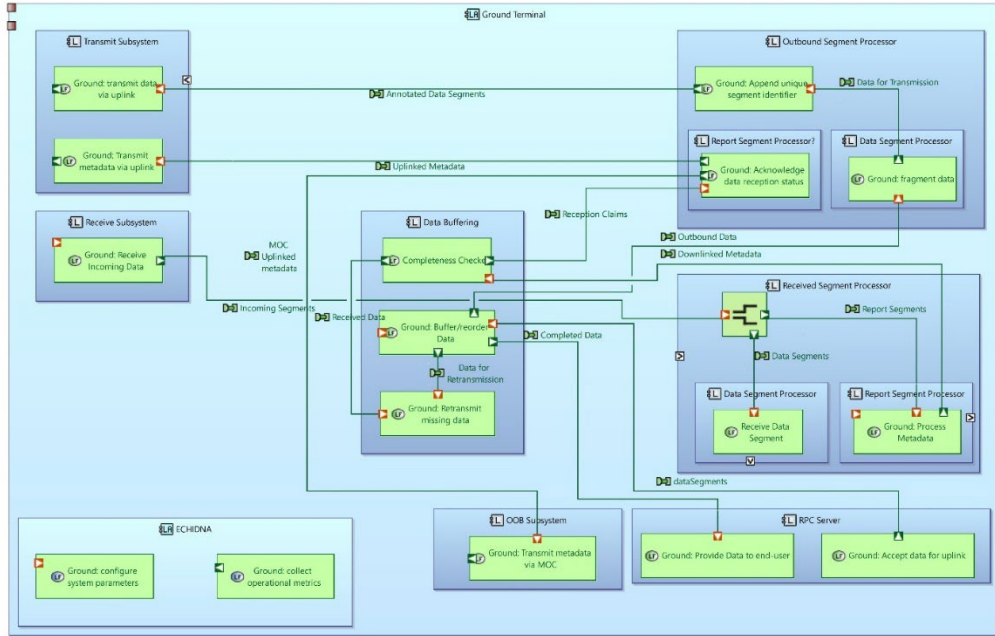
The design of the prototypes followed the system engineering methodology used throughout the project; prior to the design of either prototype, a functional analysis was conducted, leading to the system overview shown in Figure 3. This functional exchange was the final step of the “abstract” system design and guided the later phases of the LTPv2 design as development.

Both prototypes conveyed data within the CCSDS Unified Space Data Link protocol (USLP), relying on the encapsulation and tailoring guidelines outline during the design phases, using UDP as the underlying network prototype. Additional details on the prototype-specific interfaces can be found in the project ICD [AD.5].



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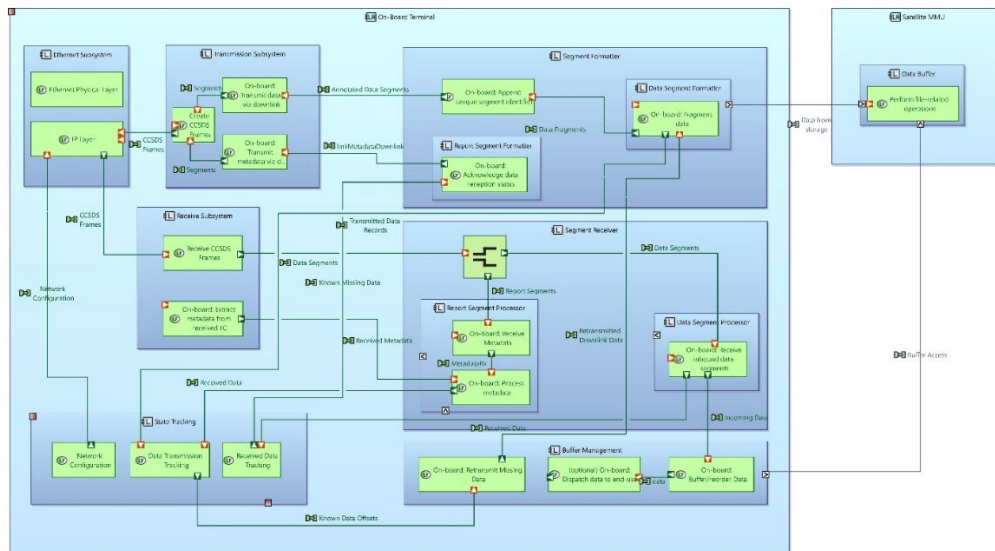
## 4.1 GROUND PROTOTYPE



**Figure 4: Ground Implementation Overview**

The ground prototype showcased all features of the protocol and was representative of the requirements of a ground station implementation.

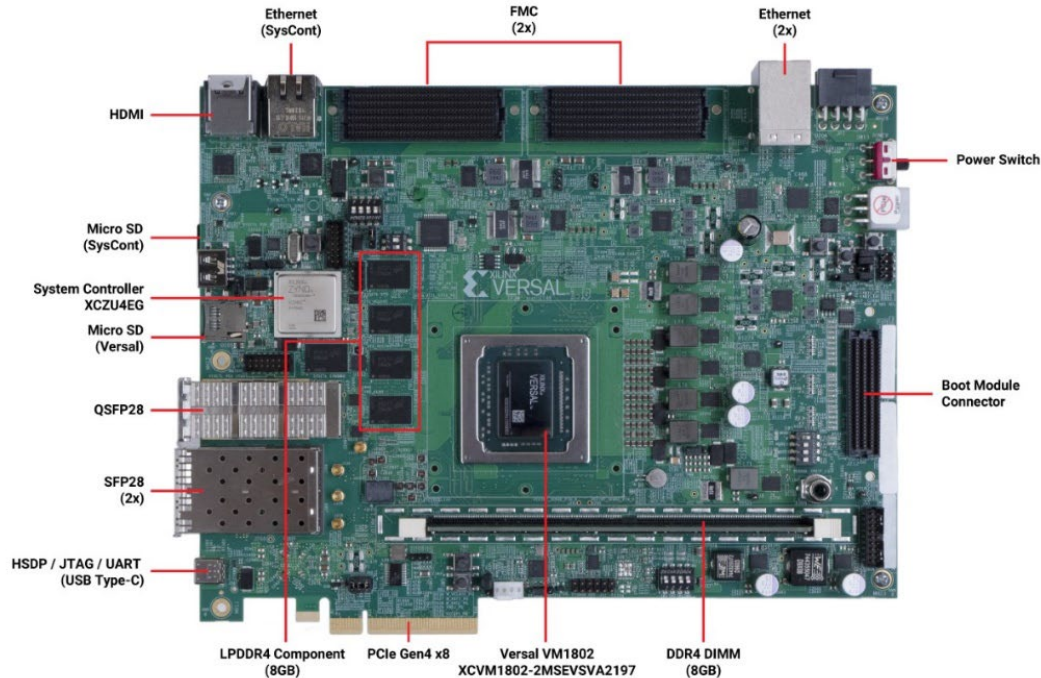
## 4.2 ON-BOARD PROTOTYPE



**Figure 5: On-board implementation**

The on-board prototype must transmit data from a mass memory to the PC-based prototype via LTPv2. The logical design of this prototype is shown in Figure 5, which also showcases the components which must, for performance reasons, be implemented on the FPGA fabric and those which may utilize a CPU for ease of implementation.

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**Figure 6: Xilinx Versal VM1802 evaluation kit**

The external interfaces of the on-board prototype have been built using open-source IP stack implementations for FPGAs, and the entire prototype is deployed on a Xilinx Versal VM1802 evaluation kit, as shown in Figure 6. This board represents the top of the line in Xilinx FPGAs and contains 25/100gbps network interfaces which far exceed the 10GbE requirement outlined in REQ-2.

## 5 VALIDATION AND TESTING

To validate the performance and behaviour of these implementations, a robust validation and testing approach was defined. This approach makes use of industry-standard interfaces (such as OpenMetrics) in conjunction with custom developments. The FPGA and ground prototypes were integrated into the GMV high-rate testbed, which provides a high-performance testbed for high-performance applications. The ground implementation and MMU emulator were deployed on both bare-metal Intel-based servers, as well as via containers. Additional bare-metal testing was run on AMD-based servers used for other projects.

### 5.1 HARDWARE VALIDATION

During early stages of the FPGA validation, it was possible to use extra code synthesized to collect data inside the FPGA and transmit it to a debugging computer by means of JTAG/DSU interface (Waveform Simulation on-board). The main objective of the test procedure was to define a set of steps to verify and validate the hardware LTPv2 implementation.

Given the network-centric nature of this project, extra attention was paid into the performance and behaviour of the network stack, relying upon the robust diagnostic capabilities available within the Xilinx development environment.

### 5.2 VERIFICATION PHASES

Multiple phases of validation were performed, each of which relied on different components:



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- Protocol layering testing – ensures compatibility of the USLP and UDP encapsulation.
- Functional testing – ensures functional completeness within a single prototype.
- End-to-end testing – validates the compatibility of the LTPv2 protocol.
  - Site Acceptance Testing – performed during the delivery of the FPGA from TESAT to DLR

Each class of testing encompassed both manual and automated testing, and largely relied on the facilities available within GMV.

### 5.2.1 PROTOCOL LAYERING TESTING

Throughout the development phase, the development team carefully validated the protocol layering options. Initially, files were exchanged through the development team, each of which contained one or more PDU's from USLP, etc. These were used to validate the interoperability without relying on a full synthesis cycle. These files were stored within Jira, as well as the GitLab repository containing the software USLP implementation.

The tests were fully successful; the USLP implementation present on both the hardware and software prototypes were fully interoperable, as was the underlying USLP protocol stack.

### 5.3 FUNCTIONAL TESTING

These tests were largely ground-specific, and performed by the development team, using the google test framework and/or bespoke testing scripts. Each test was intended to verify the functional completeness of one or more modules within ECHIDNA. All functional tests were maintained within a GMV-internal testing repository and transferred to the ESA Jira.

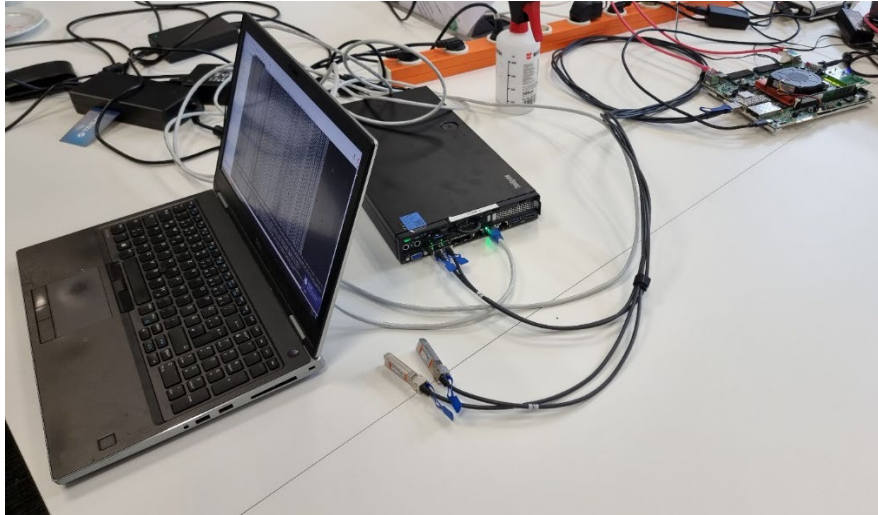
### 5.4 END-TO-END TESTING

The final phase of validation was performed via end-to-end testing, where the system was tested in an end-to-end fashion. These tests were subdivided into multiple categories, each of which was intended to focus on different aspects:

- **Software Node Specific testing:** interconnected two ECHIDNA instances on different servers to validate transmission and reception behaviour.
- **Full End-to-End Testing:** used the FPGA, ground prototype, and associated tooling (e.g., the MMU emulator) to perform end to end validation of the protocol and both prototypes.
- **Scenario Testing:** added network emulation to provide representative data loss behaviour.
- **Long Duration Testing:** ran both prototypes for longer time periods.

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## 5.4.1 SITE ACCEPTANCE TESTING



**Figure 7: Site Acceptance Testing Setup**

Additional end-to-end tests were performed as part of the Site Acceptance Testing (SAT) campaign conducted at TESAT. For these tests, GMV used a lightweight X64-based server (the black box shown on the left of Figure 7), procured as part of another project and typically used for “on-site” testing. This server, equipped with dual 10 gigabit ethernet ports, was used to run both the mmu Emulator and the ECHDINA-based ground prototype, while the FPGA was connected via a 10gbE to 100gbE breakout cable. Once the system was configured, reliable and unreliable data transfers were successfully conducted between the FPGA and the ground prototype, ensuring that the LTPv2 protocol stacks were interoperable.

## 6 CONCLUSION

The tests showcased as part of this study showed that data rates of 10gbps could be achieved between both prototypes, using MMU emulation and reliable/unreliable transmission, the protocol being implemented in a modern FPGA, representative of the next generation of space avionics.

Both prototypes were developed in geographically separated locations, using the development processes of GMV and TESAT. Interoperability was ensured via a series of tests, conducted with representative data exchanged via file and packet captures. These tests showed interoperability between the two projects, as well as ensuring that the performance requirements outlined the ITT could be met.

In parallel, representative space-to-ground scenarios were analysed and updated, ensuring that the protocol met real-world mission objectives.

The project was successful, largely due to the close coordination of the technical team and the agile project scheduling methodology. The project team has committed to finalize all relevant documentation for CCSDS and to, acting on behalf of DLR and ESA, promote it within the space standardization community.