IROC Technologies
2 Square Roger Genin
Grenoble
Tel : +33.4.38.12.07.63
Fax : +33.4.38.12.96.15

AO9828 D13
EXECUTIVE SUMMARY REPORT

24-JULLY-2023

Version 1.2

Authors:

Maximilien Glorieux (IROC Technologies)
Thierry Bonnoit (IROC Technologies)
Thomas Lange (IROC Technologies)
Issam Nofal (IROC Technologies)

Revision History

Version	Date	Author	Comment
1.0	10-JUL-2023	IROC	Initial version
1.1	19-JUL-2023	IROC	Included correction following to ESA feedbacks
1.2	24/JUL-2023	IROC	Add activity timeline and remove some details related to TCAD simulations

1 Introduction

The AO9828 activity consists in the evaluation of the suitability of Ultra Deep SubMicron Technologies (UDSM) for space applications and the development of mitigation strategies against radiation effects (Single Event and Total Dose). The activity is carried out following a prior analysis performed by a dedicated working-group, composed of ESA and key European space technology and solutions providers. During this preliminary work, two FinFET technologies were identified as suitable candidates for space applications. The objectives of the AO9828 activity are to [1]:

- Carry out an assessment and a comparison of both pre-selected technologies for space applications, in terms of technical performances, accessibility and sustainability.
- Select the most suitable technology and design, manufacture and characterize a test chip to quantify the radiation sensitivity of existing commercial libraries and possible radiation effects mitigation techniques that would improve the radiation hardness.
- Develop TCAD models of the cells integrated on the test chip to perform simulations of their SEE sensitivity. Correlate the simulations results with measurement results to validate the models. Make the models available to the space community for future evaluations of radiation-hardened cells in the selected technology.
- Draw conclusions on the suitability of the selected technology for next-generation space ICs based on the test-chip validation and the TCAD simulation results.
- Elaborate guidelines for the future development of a radiation-hardened mixed-signal standard cell library and IPs and a business case for a space IC platform including financial aspects/ considerations with respect to design and manufacturing costs. Evaluation, results and conclusions shall be made available to all users in ESA member and participating states.

This executive summary report provides an overall description of the work performed in the context of the activity and the main results achieved.

The activity was started in October 2019 and a significant delay at the beginning of the activity was induced by the difficulty to sign the required NDA documents with foundries (TSMC and GLOBALFOUNDRIES). The main project milestone and their corresponding dates was:

- July 2020 – SRR: Review of technology pre-assessment and TCAD simulation plan
- December 2020 – PDR: Review of the test vehicle specifications and TCAD simulation report
- May 2021 – CDR: Review of the test chip design before tape-out
- June 2021 – Tape-out of the test vehicle
- January 2022 – Reception of packaged test vehicles at IROC
- January 2022 – Successful electrical bring-up of the test vehicle
- March 2022 – Heavy-ion test campaign at RADEF facility (Finland)
- April 2022 – High-Energy Proton test campaign at PSI facility (Switzerland)
- June 2022 – TID test campaign at ESTEC Co60 Facility (Netherlands)
- September 2022 – TR: Review of the test reports
- November 2022 – FR: Final review of the main activity

Significant delay to the activity progress was induced by the difficulty to sign NDA documents with the foundries, by the longer test chip manufacturing time than expected and the difficulty to get access to beam time. In addition, the analysis of test results and the redaction of corresponding reports took more time than expected on IROC side.

Given the unexpected single-event-latchup sensitivity observed during the radiation test campaign, a CCN was proposed to ESA by IROC to perform a complementary characterization of the test vehicle under heavy-ion. This test campaign was performed at UCL facility (Belgium) in April 2023 and the CCN was closed in July 2023.

2 Candidate Technology Pre-assessment

The first task of the activity consisted in a detailed state of the art review of the suitability of ultra-deep submicron technologies for space application and the comparison of TSMC and GLOBALFOUNDRIES solutions.

The state-of-the-art review mainly focused on the publicly available data about the behavior of UDSM technologies in presence of radiation. Globally, UDSM technologies provides a good resistance to radiations. The reduction of the charge collection volume to the transistor fins limits the effects of charge diffusion in the substrate. This decreases the amount of collected charge for a given ionizing particle, thus reducing the number of errors due to single event upsets, compared to previous bulk planar technologies. Regarding Single Event Latch-up, several papers report that FinFET technologies may be more sensitive than planar ones. Regarding the total ionizing dose, few papers relate that FinFET transistors seems to be quite resistant.

In parallel to this review of the technical literature, the characteristics of candidate technologies were studied in detail in order to identify potential differences that may impact their suitability for space applications. As an overview, we can state that both candidate technologies have similar features and provide technical performances in adequation with the needs of future space missions. Advanced FinFET processes and solutions increases the achievable throughput of telecommunication satellites and the on-board processing capabilities of earth observation constellations. The high degree of integration of these new technologies, embedding complex and configurable digital functions as well as analog and mix circuit, provides a complete solution to receive, process, store and transmit large volume dataset coming from up-link connections or on -board sensors. Such “single IC” architecture reduces the complexity, the weight and the volume of on-board processing capabilities.

The presented characteristics of UDSM technologies make them suitable for next generation payload of telecommunication and earth observation satellites. In addition, the development of UDSM technologies is driven by mobile applications, which requires aggressive low power design techniques. Some examples of these design approaches are clock gating, power gating or dynamic voltage frequency scaling. The benefit of these solutions in term of power consumption and dissipation can be very valuable for space application, especially for small satellites. Moreover, recent autonomous driving and mobility applications created many opportunities for complex imaging and AI solutions, increasing the range and applicability of FinFET processes. Functional Safety and Reliability aspects are now a critical part of the development and

manufacturing flow, globally increasing the quality of the technology and helping Space and Avionics applications that traditionally require High Reliability. Lastly, the 12/14/16nm process node has a good price/performance ratio and was, at the beginning of the activity, be a very good “sweet spot” for cost-effective applications that still require good features and performances.

Even if the two pre-selected technologies meet the requirements for space applications, each of them has some advantages and limitations with respect to the other candidate. As TSMC being largest pure-play foundry and has released 16 nm finFET technologies several years before GLOBALFOUNDRIES, its ecosystem is richer. Thus, more choice of basics, memory, digital and analog/mix signal IPs is available for TSMC N16FFC platform. On the other hand, GF reliability calculation spreadsheet is very helpful to estimate the hard failure rates induces by aging, temperature and electric fields considering the exact sizing of the device. In addition, the PDK and IP documentations of GLOBALFOUNDRIES technology seems more clear and complete than the one provided by TSMC.

The outcome of this technology pre-evaluation was the selection of TSMC technology for the following phases of the activity. As both candidates showed similar technical performances, the larger eco-system around TSMC solution and its wider usage across the design community is the main argument that led to its final selection.

3 TCAD Simulations

The second important task of the activity was to perform an overall study of the robustness of the selected technology with respect to single event effects with the help of TCAD simulation tools. The simulation work was organized in two phases, to evaluate transient effects (SEU/SEL) and Single-Event-Latchup respectively.

3.1 SEU/SET Simulation

The aim of the first phase of the project is to understand the Single Event Upset and Single Event Transient sensitivity of the selected UDSM technology in typical space environment.

SEU and SET simulations were performed using Accuro TCAD tool, from RobustChip Inc and TFIT tool from IROC Technologies. Results from both tools were compared in term of accuracy, IT resources (execution times, licenses used and so on) and ease of use.

UDSM technology foundries provide a large number of standard cell libraries to help designers to select the most appropriate building blocks for his particular design and to optimize the trade-off between performance, power consumption, die area and reliability. Therefore, a subset of representative sequential cells widely used in typical digital circuits has been proposed for the SEE simulations.

Simulation results shows both simulation tools evaluate that 16nm FinFET technologies orbital error rates are one to two orders of magnitude lower than previous planar solution (such as 65 or 28 nm planar CMOS).. In addition to these very low intrinsic upset sensitivities, TSMC provides a set of radiation hardened flip-

flops, whose SEU orbital error rates are reduced by more than 2 orders of magnitude. These elements make 16 nm FinFET technologies very reliable for harsh radiative environments compared to previous solutions.

TFIT and Accuro simulation tools were used to perform these simulation campaigns and provided similar results.

3.2 SEL Simulation

The objective of this second phase of the simulation is to identify if the selected UDSM technology and typical devices and structure implemented in this technology can be sensitive to single event latch-ups.

The SEL simulations have been performed using the 3D TCAD tool from Synopsys. The model of the FinFET transistors and the device characteristics (in term of geometry, dimension and doping) have been built based on information publicly available

As the state of the review reported that only1.8 V transistor are likely sensitive to SEL, the simulations were focused on these thick oxide devices.

The simulation results demonstrate an effective SEL sensitivity of high voltages transistors in 16 nm UDSM technologies. This work demonstrated the low impact of the number of Fins, the STI depth as well as the size of the contacts compared to the impact produced by variations in the values and doping profiles of the entire structure.

4 Test Vehicle Definition, Design and Manufacturing

4.1 Test Vehicle Objective

Following to the state-of-the-art review and the simulation activities, the next major task of the activity was the definition and the design of a test-chip to assess the suitability of TSMC 16 FFC nm technology for space applications. and especially characterize the behavior of this technology in presence of ionizing radiations.

The test vehicle was manufactured in TSMC N16 FFC technology, through the CyberShuttle service, with IMEC operating as Value Chain Aggregator. The test chip, with a 4 square millimeters area was taped-out date in June 2021. IROC named the test chip SHARC-FIN for **S**EE **H**ardening **A**nd **R**adiation **C**haracterization of **FIN**fet Technologies. In order to ease the device preparation for radiation test campaign, wirebound CERQUADFP 128 package was selected for the test vehicle.

As the sensitivity of UDSM technologies to ionizing particle is expected to be relatively low, a specific care was taken to ensure that a statistically significant number of events can be measured in a reasonable time.

4.2 Definition of test structures

Based on these objectives, a dedicated set of test structure was specified and designed to characterize radiation effects in the selected technologies. The main structures of the test vehicles are:

- An SRAM Array, to measure the upset sensitivity of each memory compiler to heavy-ions and protons
- Some flip-flop chains, with on-chip error counting capability
- A single event transient detector and pulse width measurement circuitry
- A clock disturbance detector, connected at the PLL output
- A memory BIST, to measure SRAM performance degradation with TID.

4.3 Test Vehicle Architecture

A dedicated top-level logic, with a configuration interface, an interruption circuitry and a clock generation and distribution functionality, was designed to allow the concurrent measurement of all test structure in parallel during the radiation test campaign and thus optimize the beam time and results statistic.

Figure 1 shows the area distribution between the different test structure of the SHARC-FIN test circuit. The chart is normalized to 4 mm², showing that a small portion of the circuit is not allocated. The 'Top' portion to the top-level glue logic, including the multiplexing and configuration logic, the PLL, its test harness and the SRAM BIST.

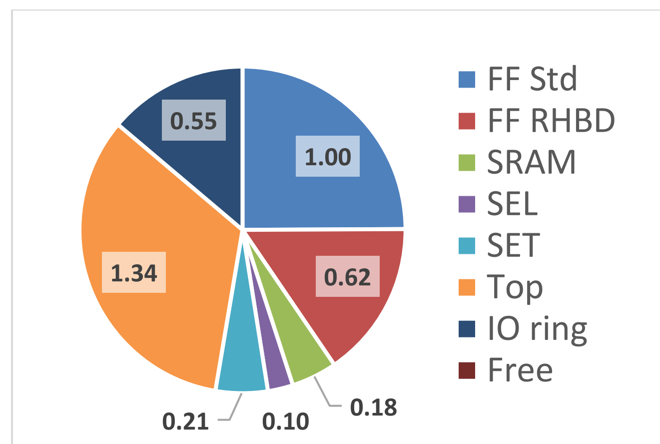

Figure 1: Area Distribution between SHARC-FIN Test Structure, Normalized to 4 mm².

4.4 Test Vehicle Design, Manufacturing and Packaging

Following to the specification, the test vehicle was designed using state-of-the-art tools and methodologies. The development was based on SIEMENS Menthor Graphics flow.

Following to implementation and verification, the test vehicle was manufactured and packaged, as shown in Figure 2.

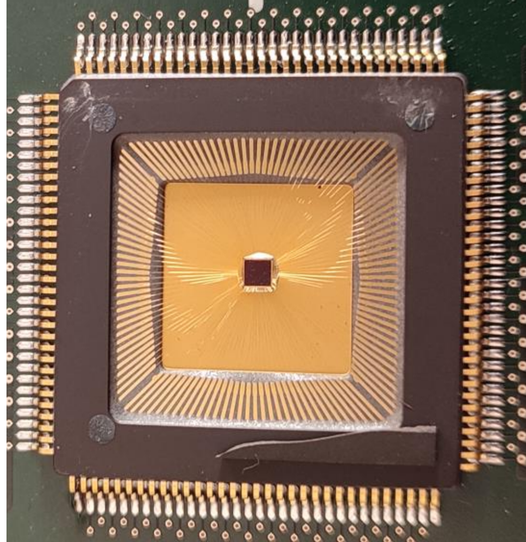

Figure 2: SHARC-FIN Test Vehicle in CERQUADFP 128 Package.

5 Test Vehicle Validation

Following to the manufacturing and packaging of the SHARC-FIN test vehicles, dedicated test boards were developed for SEE and TID characterization. These boards were also used for the functional validation of the test vehicle.

5.1 SEE Characterization

A dedicated SEE test board was designed and manufactured for SHRAC-FIN test vehicles. Two devices under-test are soldered on each test board, as shown in Figure 3.

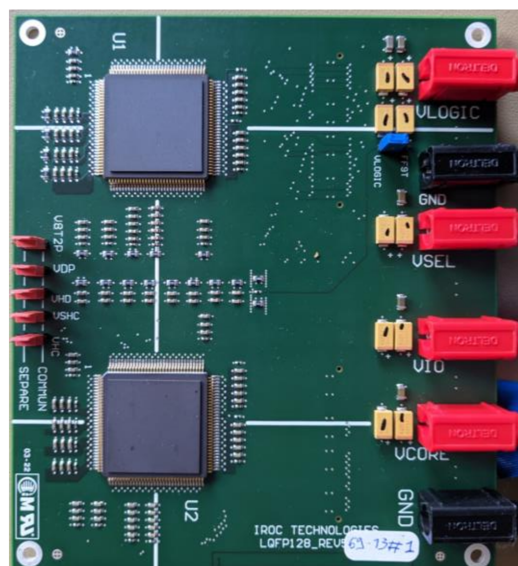

Figure 3: SHARC-FIN SEE Test Board.

Heavy-ion radiation test was performed at RADEF Facility, in Jyväskylä University, Finland. RADEF was selected to take profit of the high flux available. High-energy proton test was run at PSI PIF Facility, in Switzerland.

5.1.1 Heavy-Ion Test Results

Figure 4 reports the heavy-ions FLIPS cross-sections of the six available SRAM bit-cells in TSMC n16FFC technology.

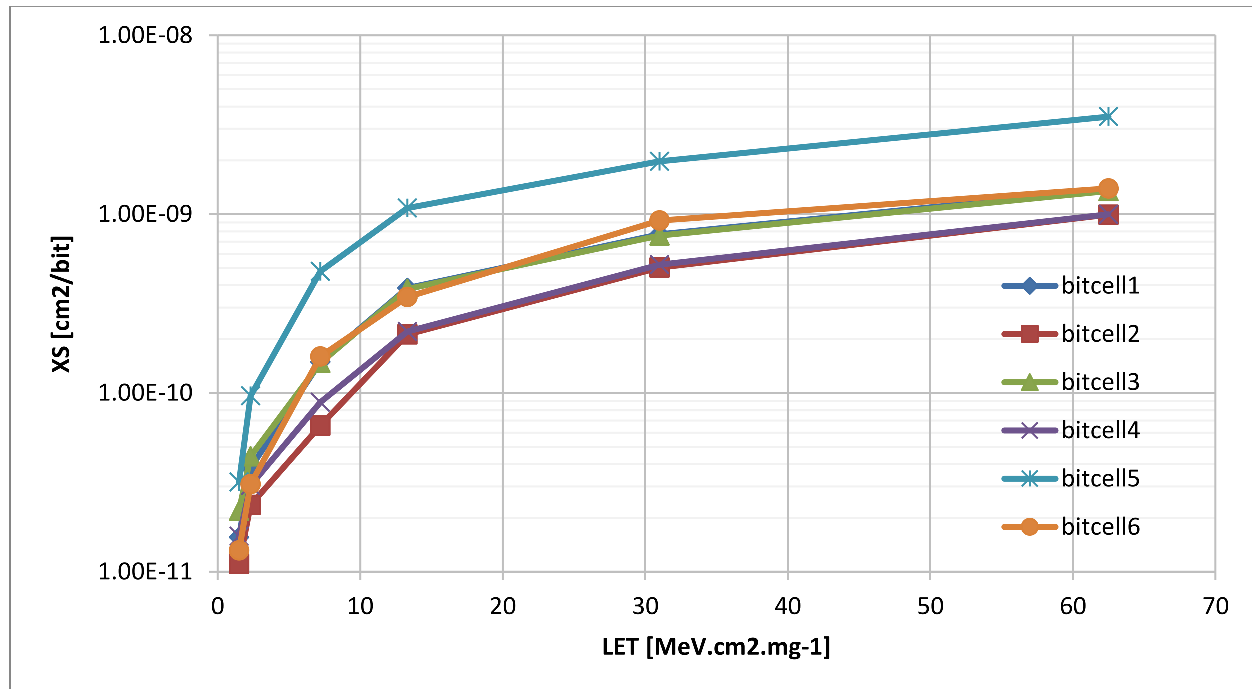

Figure 4: Comparison of SRAM Bit Cells Heavy-Ion FLIPS Cross-Sections.

In addition, the heavy-ion test campaign demonstrated that the SET cross-section of combinational logic is significantly lower than the one of flip-flop. Finally, some phase shift event was observed on the PLL with a saturation cross-section of 5E-5 cm² and an LET Threshold of 7 MeV/cm²/mg.

Regarding the Single-Event-Latchup test results, some events was observed on all the test structure, as predicted by the TCAD simulation. This shows building a standard-cell layout topology with 1.8 V transistor which is not sensitive to latch-up is not possible. Some SEL hardening layout techniques are still possible as no SEL was observed on the PLL.

Finally, some SEL events was observed on the flip-flop power domain, while operating in worst case conditions (Vmax, Tmax). The LET threshold seems to be relatively variable across the different samples.

5.2 TID Characterization

In addition to SEE characterization, the second major objective of the SHARC-FIN test vehicle is to measure the impact of Total Ionizing Dose Effects on TSMC N16FFC Technologies.

Total ionizing dose radiation test was performed by exposing 10 DUT to a cobalt 60 gamma ray source. An additional DUT, non-irradiated, was measured at each step of the experiment, for reference

The SHARC-FIN total ionizing dose characterization was performed at ESTEC Co-60 facility, in Noordwijk, The Netherlands. The TID test plan included 6 read points representative of typical space missions and considering the annealing effects.

Experimental TID characterization of the TSMC n16FFC technology showed a limited impact of the total dose on the performance of the tested devices. The parameter for which the drift is the most significant is the frequency of ring oscillators, where a somehow arbitrary behavior was observed. This behavior was not expected and not yet fully understood.

Other parameters characterized during the TID test campaign showed a very limited drift up to 300 krad and no impact is expected at circuit level for typical space applications.

6 Assessment of the suitability of TSMC N16FFC Technology for Space Applications

TSMC n16 FinFET process is one of the major technological nodes, that were massively used for customers and ground level applications. It was one of the first publicly available FinFET technology, since 2013, and two improvements of the process were proposed in 2015 (n16ffp) and 2016 (n16ffc), with design compatibility. Depending on the required wafer volume, the technology is either available directly by TSMC or through value chain aggregators (VCA) such as IMEC and GUC. For prototyping purposes, TSMC Cybershuttles programs provides MPW on a large set of technological nodes.

As the 16nm process was a popular technological node, used in many customer and commercial applications, a large set of standard cell libraries are available. TSMC provides a large set of standard cell libraries and a several memory compilers which fits the need of typical digital applications. A large set of standard cells libraries, memory compilers and mixed signal IP are also available from partners of TSMC ecosystem.

Radiation effects susceptibilities of the main design elements were evaluated through a set of test campaigns, in heavy-ions, high-energy protons and total ionizing dose facilities. Test results shows that TSMC n16FFC technology robustness to single event effect is very strong, with orbital error rates approximately two orders of magnitude lower than bulk planar technologies. The state-of-the-art review predicted this behavior and this result can probably be generalized to other UDSM process nodes. In addition, TSMC provides radiation hardened cells that can help digital designer to reduce even more the error rates of circuit at low design cost and risk. This overall low error rates make UDSM solutions very attractive for space applications.

However, the heavy-ion characterization showed that TSMC technology can be susceptible to single event latchup. High voltage transistors (1.8V), with thick gate oxide, shows a relatively high sensitivity when they are implemented in standard cell topologies. Furthermore, some SEL events were also identified in core voltage transistors. This was not expected from the preliminary analysis. This SEL cross-section is

relatively low and a strong variation from part to part was observed. Using a high well contact density seems efficient to mitigate the SEL sensitivity of core voltage transistors.

Regarding the results of the total ionizing dose characterization, no critical drift of the technology was observed. The parameters which show the most significant variations are the ring-oscillator frequencies, for which the highest variation can be up to twenty percent increase or decrease for some specific ring oscillator instances. This metric is expected to measure the drift of the delay induced by the total ionizing dose and such large variations are not expected.

To conclude, we can state that TSMC n16FFC technology provides a strong platform, with a very rich ecosystem to implement complex integrated circuits and reduces the integration complexity of modern satellites. The technology provides strong robustness against radiation effects even if some specific layout rules are needed to ensure single event latchup immunity and fully anticipate the drift induced by total ionizing dose. Compared to more advanced nodes such as the 7 or 5 nm FinFET, n16FFC process is probably an interesting option to consider for space application as its cost is much more affordable for small volume products and it still has the advantages of FinFET process in term of resilience to radiation effects.