ESA STUDY CONTRACT REPORT

ESA Contract No : 4000103322.	SUBJECT : GaN Power stage based on European technology for Navigation SSPA in L-Band		CONTRACTOR : Thales Alenia Space - France
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ABSTRACT:
This document is the Executive Summary of the TRP contract N° 4000103322 where L-band power stage based on European GaN technology with output power in the range of 120-150W capable of power flexibility has been developed.

The work described in this report was done under ESA contract. Responsibility for the contents resides in the author or organization that prepared it.

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EUROPEAN SPACE AGENCY CONTRACT REPORT

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TABLE DES MATIERES

1. INTRODUCTION

This document is the executive summary of the TRP contract N°4000103322

2. SUMMARY OF THE ACTIVITIES

The aim of this new ESA-TRP study is to develop a SSPA output power section for navigation in L-band in the range of 120-150 W capable of power flexibility. This power stage will be based on GaN technology coming from an European industrial Foundry. The main proposed activity is to design, manufacture and test a hybrid HPA module at L-band based on the United Monolithic Semiconductors 0.5µm (GH50) technology.

This activity is composed of two contractual phases:
- Phase 1 for the definition of the SSPA architecture and development of RF transistors
- Phase 2 for HPA detailed design and test

3. PHASE 1 SSPA TOPOLOGY AND DEVELOPMENT OF RF TRANSISTORS

3.1 SSPA OUTPUT SECTION ARCHITECTURAL DESIGN

This activity is dedicated to identify the topology of a SSPA output section at L band for future navigation applications to achieve the following technical performances specified

Within Operational Temperature Range	Galileo E6 Signal (SIGNAL 1)		CW Mode (SIGNAL 2)	
	Value	**Comments**	**Value**	**Comments**
Nominal Output power	>150W	@ P2dB Requirement	Estimated >190W	@P2dB **Estimation only**
Power Added Efficiency	>50%	@ Nominal output Power	>55%	@ Nominal output Power **Estimation only**
Power flexibility	3dB output back-off power range with 4 points efficiency degradation Max			
Centre Frequency	1278.75 MHz		1278.75 MHz	
Gain	>15dB	@ Nominal output power	>15 dB	@ Nominal output power
BW[(1)]			>50MHz	@ Nominal output power. See (1)
Phase shift referenced to IBO=-20dB versus input power			3 deg. max -20<IBO<-10dB 6 deg. max for -10<=IBO<-5dB 15 deg max -5<=IBO<-0dB 20 deg. max 0<=IBO<+3dB	
Phase Linearity v.s. frequency			2.5 deg peak-peak	Distance between actual phase shift v.s. Frequency to a linear phase within the whole BW
Input Reflexion coefficient	<-15 dB	@ Nominal output power, over BW	<-15 dB	@ Nominal output power, over BW
2nd harmonic rejection	>30 dBc		>30 dBc	
Main DC voltage supply	>40V		>40V	

Table 1 : required performances

Thanks to GaN technology, the baseline L-band SSPA RF tray has been simplified with regard to the equivalent GaAs solution .The preferential topology in term of mass and efficiency improvements is to have only one HPA module for the SSPA. With this topology, we must check in detail all the elements in terms of maximum power and thermal dissipation. In order to present and maintain good VSWR on the SSPA output, the power isolator has been conserved.

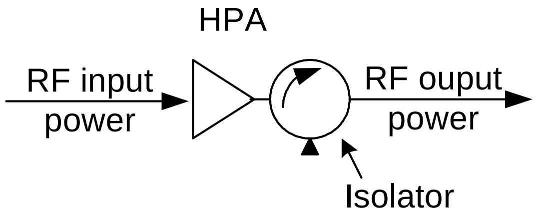

Fig. 1: Baseline Output section SSPA topology.

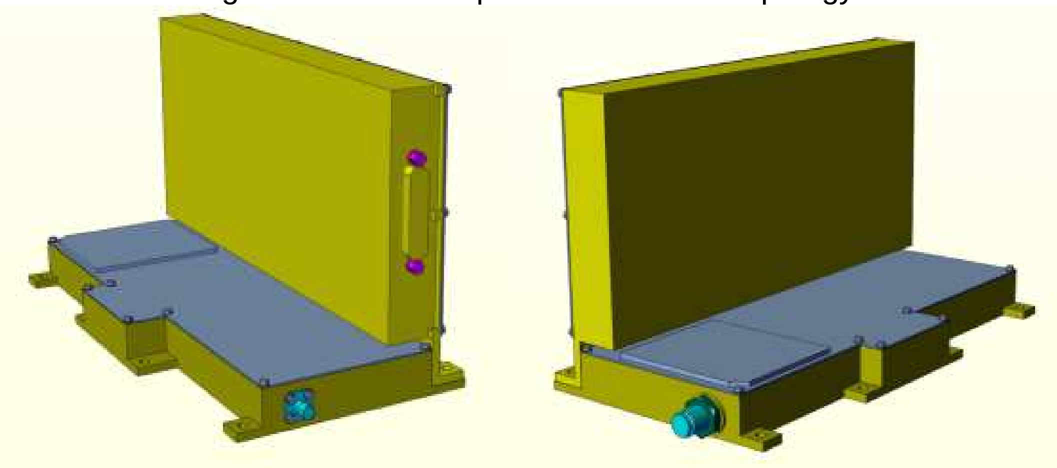

Fig. 2: preliminary overview of the L-band GaN SSPA

3.2 Power Flexibility techniques

For power flexibility techniques, TAS-F think that the change in drain voltage is the most appropriate in industrial situations. Because we have to develop only one type of HPA. For the Doherty we have to develop 2 type of specific HPA (Peaking and carrier) which present good impedance over the RF drive and 2 specific couplers (input and output). This is not going in the direction of cost reduction

3.2 Development of RF transistors

The transistor and power bar specifications were chosen to enable the best possible trade-off between output power and power added efficiency. In that way, 2 transistors gate widths were considered (250µm and 400µm) and were implemented in 2 different power bars in the final tile: this power bar exists on the standard UMS mask-set call 'TREK'

- 8x8x250µm
- 8x10x400µm

Performances of the 2 power bars are given on the table below. No thermal coupling effect as well as phase recombination at transistor level are taken into account. These performances have been simulated based on the transistors load-pull simulation).

POWER BAR TYPE	SIZE	POUT@5dBcomp	Max. PAE	POWER GAIN
8x10x400µm	32 mm	50.5	70.6	>20
8x8x250µm	16 mm	47.8	71	>20

Table 2 : Power bars performances.

3.3 Thermal analysis

The objectives of this thermal study done by XLIM was first to determine and compare the junction temperature for two transistors GH50 of the UMS foundry. The first one was an 8 fingers, 250µm width. The second one was a 10 fingers, 400µm width. Thermal simulation of powerbars was also proposed.
Several cases studied to provide to the designer an overview in terms of thermal performances.

The thermal resistance for the 8x10x400 varies from 0.45°C/W to 0.51°C/W. If we multiply these values by 8, we obtain 3.6°C/W and 4.08 °C/W which is very close to the value obtained for the elementary cell (3.5°C/W to 4°C/W.).
This revealed also a poor thermal coupling from cell to cell and a quasi-constant temperature along fingers.

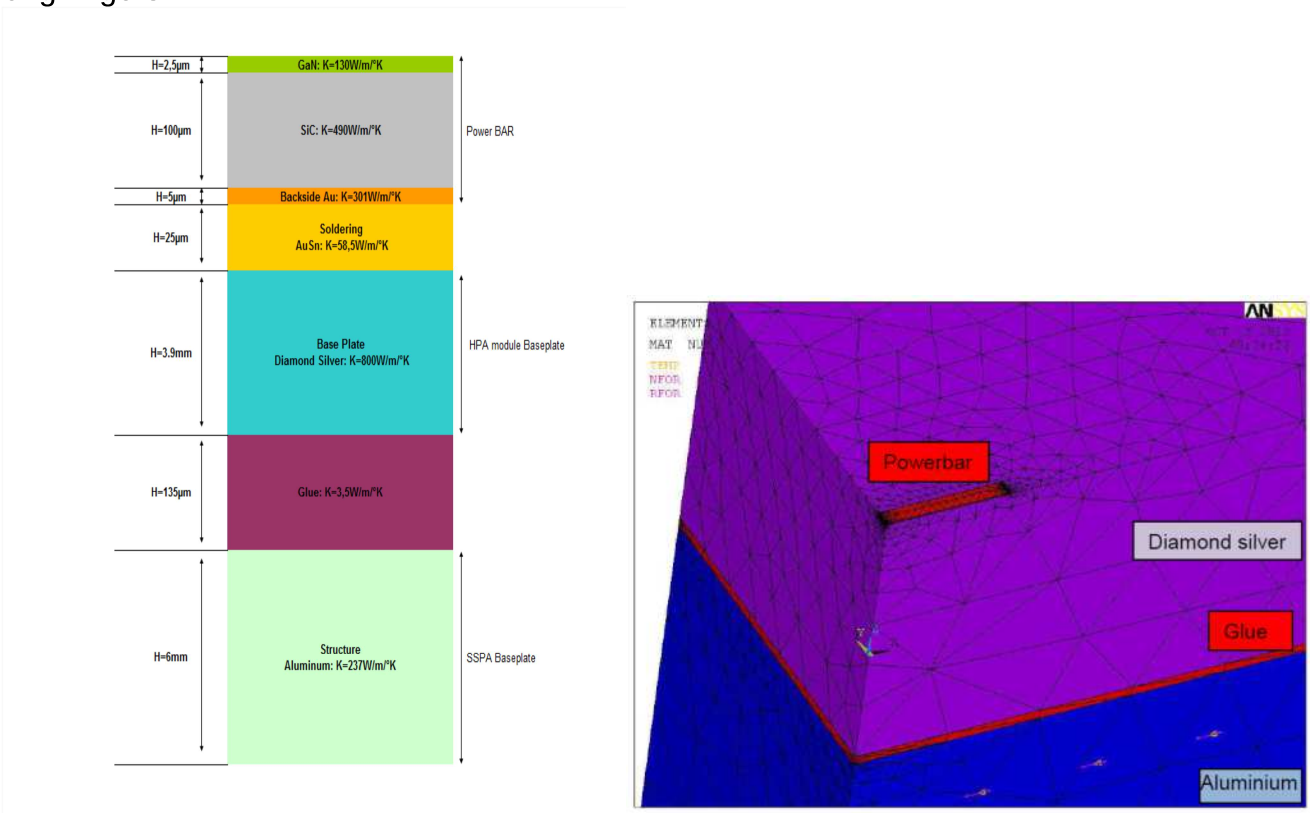

Fig. 3: Materials and dimensions and Mesh of the structure

The study was performed to quantify the influence of the packaging. The first conclusion was that at least 7°C is lost in the glue. The second conclusion was that the use of diamond silver was a very good choice to decrease the thermal resistance of the stack.
To compute the junction temperature of the power bar we need to add the several contributions:
Example: for Tcase: 50°C and 50W dissipated in the power bar 8x10x400. The baseplate temperature will be 92°C. At 92°C the thermal resistance of the powerbar is 0.5°C/W.

Tjunction = Tcase + ΔTcase_to_baseplate + ΔTbaseplate_to_junction
ΔTcase_to_baseplate = 0.84*50 = 42°C
ΔTbaseplate_to_junction = 0.5*50=25°C
And Tjunction = 117°C

3.4 RF Transitor Performance Validation

UMS was in charge of wafer manufacturing, on-wafer tests and power bars delivery.
AMCAD was in charge of Transitor and power bar Performance Validation

The system set up for the devices characterization is described below.

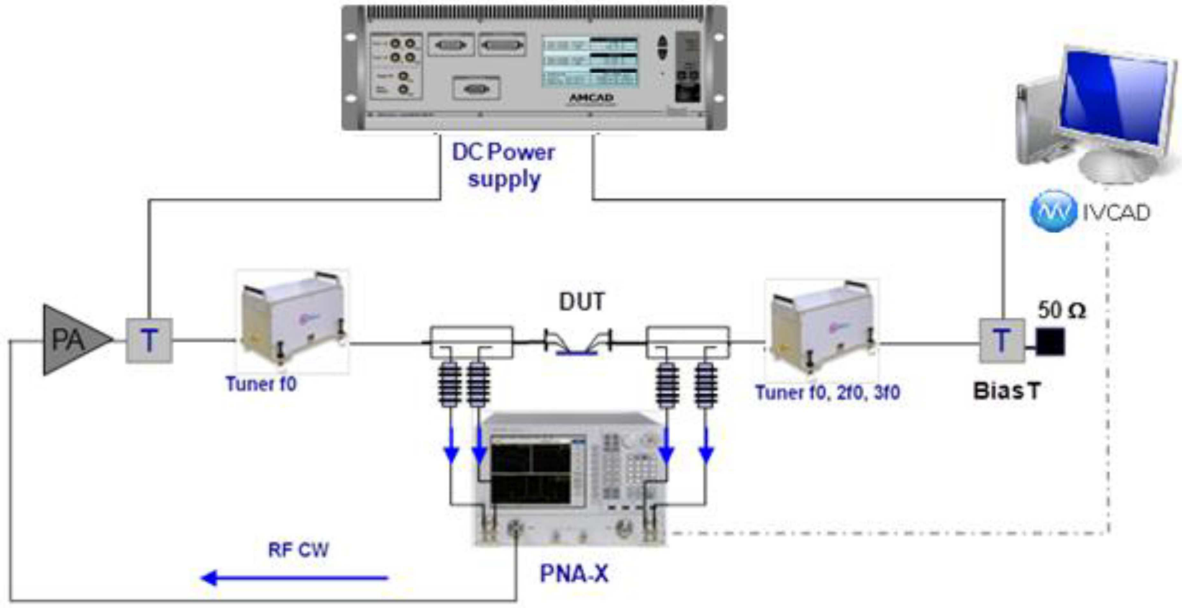

Fig. 4: AMCAD VNA-based load-pull system

All 8x10x400um power bar samples provided more than 75% PAE and more than 110 Watts output power.

Sample 1	Operating Gain (linear)	Pout (W)	PAE (%)
Sample1	20.8	105	81
Sample2	20.1	116	78
Sample3	20.3	114	79
Sample4	19	110	76
Sample5	20.1	116	77

Table 3 : Performance summary for all samples on Zopt PAE (F0, 2F0):

The agency considered the results of phase 1 and the status of the GaN technology selected as condition to go ahead with phase 2.

4. PHASE 2 HPA DETAILED DESIGN AND TEST

4.1 Transistor Nonlinear modeling

AMCAD Engineering I(V) and S-parameters achieved measurements and realized modelling activities on the transistors (10x400µm) and the power bar (8x10x400µm).

The model adjustment is a tradeoff between all the types of measurements (I(V), [S], load-pull, ...) and the different operating conditions (bias, temperature, frequency...) in order to have a coherent model.

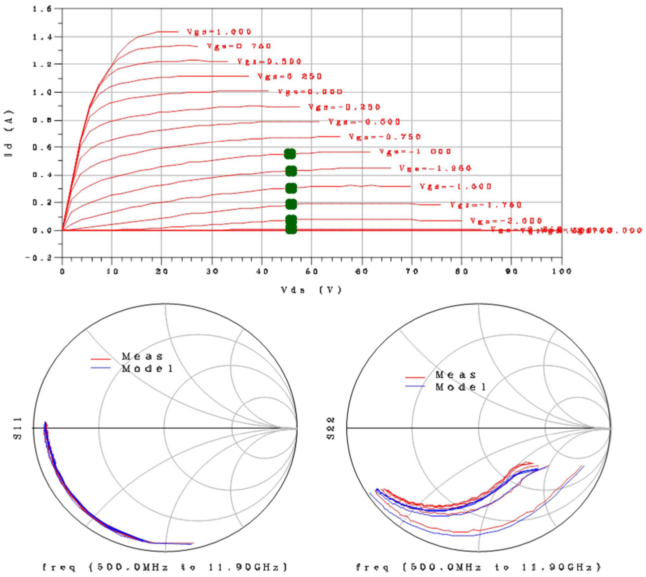

Fig. 5: Meas. vs Model 10x400

4.2 Detailled design of the HPA MODULE

This design was achieved by applying the following work philosophy :

1. Load pull simulation of the powers bar to find the optimum Load (PAE, Output Power, compression).
2. Design of the output network
3. Design of the input network compromised of gain , stability , return loss
4. STAN analysis

4.2.1 CW Simulation

The main RF performance obtained, output power, PAE and power gain are presented below versus input power and versus frequency (Fig. 6) :
For all the simulations an extensive use of the electromagnetic simulator up to 10 GHz(MOMENTUM) was done.
The transistor junction temperature is provided by the electro-thermal model.

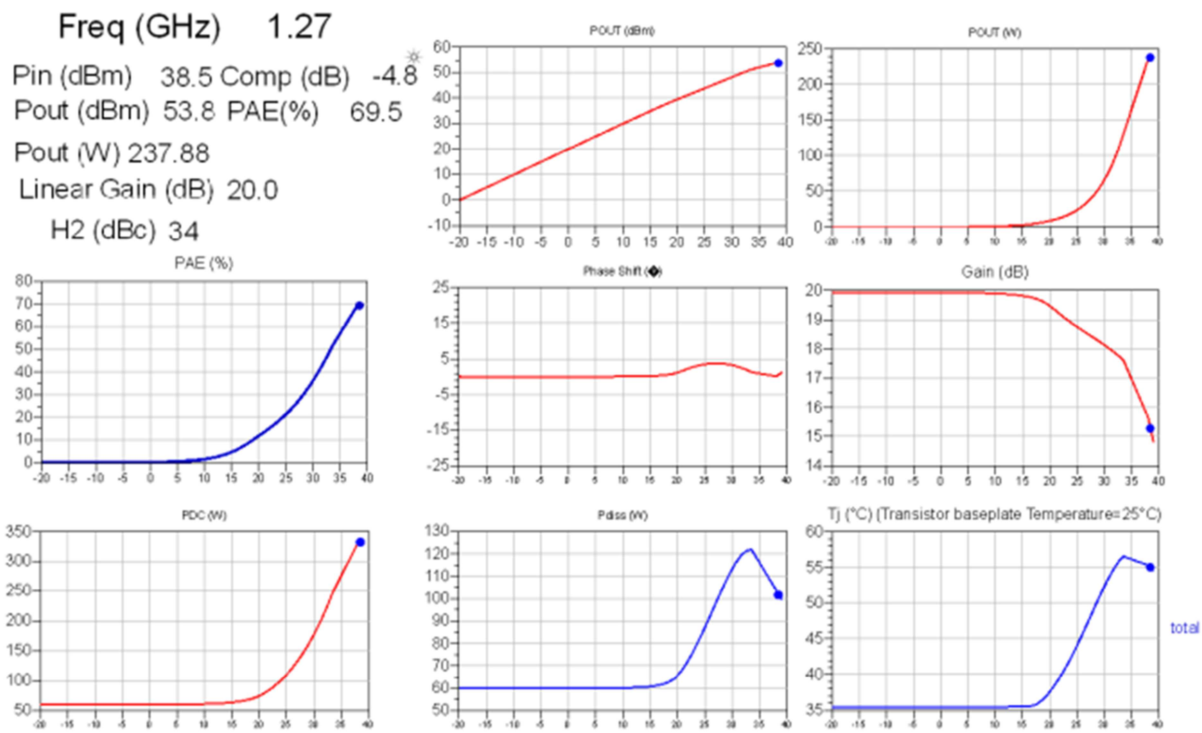

Fig. 6: HPA RF performance versus input power (dBm) at center frequency 1.27GHz

4.2.2 Power Flexibility Simulation

A non-linear simulation was done by varying the drain voltage from 20V to 45V.
The simulation shows that we can achieve the specification of 3dB output back-off power range with 4 points efficiency degradation Max.

VDS	Pin	Pout	PAE	Linear Gain	Power Gain
20	37.3	46.7	65	14.2	9.4
25	37.8	48.7	67.7	15.7	10.9
30	38	50.3	69.1	17	12.3
35	38.3	51.7	69.8	18.1	13.4
40	38.5	52.8	70.1	19.1	14.3
45	38.5	53.8	69.8	19.9	15.3

Table 4 : CW Power Flexibility Simulation

4.2.3 CW Simulation over frequency bandwidth

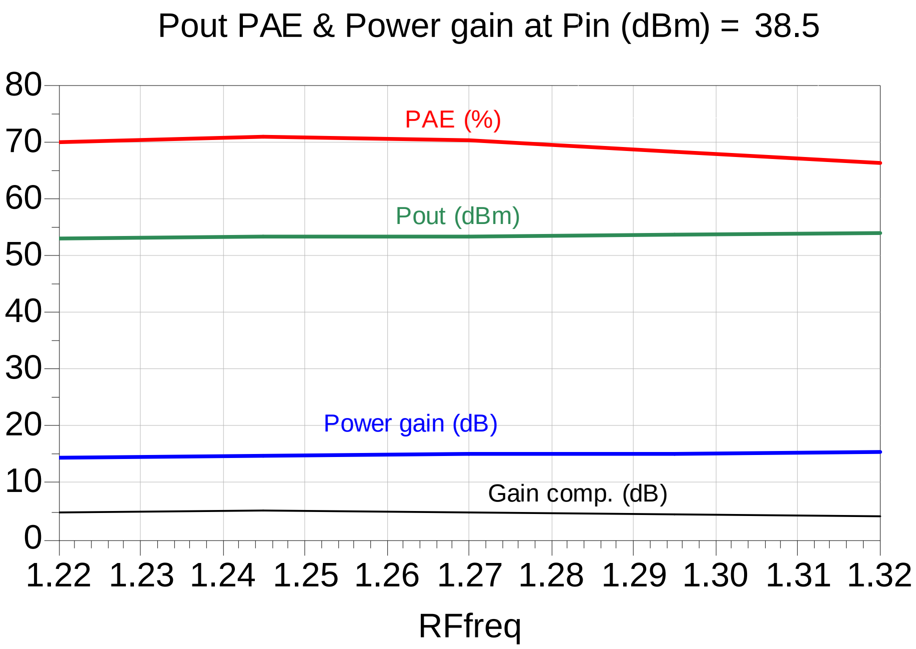

Fig. 7 : HPA CW RF performance. Pout(W), PAE(%), Gain(dB) versus frequency (GHz) for Pout=200W

The frequency bandwidth reaches 100MHz for a center frequency of 1.27GHz (8% of relative bandwidth). The overall power added efficiency varies from 68 to 70% and is associated to an output power of 200W. It corresponds to a Pout = 3.75W/mm at transistor Level . Power Gain and gain compression have been also drawn.

The following tables summarize the HPA simulated performance reached for the center frequency 1.28GHz in both CW and with E6 Galileo signal.

CW mode : PAE performance for an input power of 38.5dBm		
Parameters	**Specification**	**Simulation**
Output Power	53dBm	53.7dBm
PAE	61%	>69%
Power gain	15 dB	15 dB
Gain compression	2dBcomp	5dBcomp

Table 5 : Summary of simulated CW performance at HPA level

Simulated performance with E6 Galileo Signal		
Parameters	**Specification**	**Simulation**
Output Power	150W	200W
PAE	55%	59%
Power gain	15dB	16dB

Table 6 : Summary of simulated performance at HPA level with E6 Galileo Signal

4.3 Test of the HPA module

4.4 Measured performance Compliance Matrix

CW mode : Measured performance for an input power of 38.0dBm				
Parameters	**Specification**	**Measurement**	**Compliance**	**Comments**
Output Power	> 190 W	148 W (1) 160 W (4)	N/A	Worst case
PAE	55%	65%(1) 53%(4)	N/A	Worst case
Power Flexibility 3dB back off	4 % efficiency degradation	4.2 % (4)	NC PAE >55%	
Center frequency	1278.75 MHz	1278.75 MHz	C	
Power gain	15 dB	14 dB (1) (4)	NC	
Gain compression	2dBcomp	5dBcomp (1) (4)	NC	
BW	>50MHz	50MHz	C	
Phase shift	3 deg max -20<IBO<-10dB 6 deg max -10<IBO<-5dB 15 deg max -5<IBO<-0dB 20 deg max 0<IBO<+3dB	6 deg (4) 7 deg (4) 7 deg (4) Not measured	PC 7 deg max of phase shift	
Phase Linearity v.s. frequency	2.5 deg peak-peak	<2.5 deg (4)	C	Delta phase shift @Pin 37dBm over 50MHz
Input Reflexion coefficient	<-15dB	<-15dB (1) <-8dB (4)	PC	Over frequency range
2nd harmonic rejection	>30 dBc	> 45 dBc(4)	NC	
Main DC voltage supply	>40V	40V	C	
Temperature	-10/+80 degrees All performance met junction temperature below 150 deg. C	measured only at 25°C	NC	For 100W of dissipation at 85°C junction temperature is around 110°C see (5)

(1)HPA N°1 (4)HPA N°4 (5) D3b 0.5µm Transistors an Power Bar thermal analysis

Table 7 : Summary of Measured CW performance at HPA level

E6 Signal : Measured performance				
Parameters	**Specification**	**Measurement**	**Compliance**	**Comments**
Output Power	> 150W	100W(1) (4)	NC	at VDS =40V @20°C for HPA1 at VDS =30V @20°C for HPA4
PAE	50%	62%(1) 43%(4)	PC	
Power Flexibility 3dB back off	4 % efficiency degradation	6.6% (1)	NC PAE >55% (1)	
Center frequency	1278.75 MHz	1259.50 MHz(1) 1278.75 MH(4)z	PC	
Power gain	15 dB	13 dB (1) 15 dB (4)	PC	
Gain compression	2dBcomp	5dBcomp (1) (4)	NC	
Input Reflexion coefficient	<-15dB	Not measured	NC	
2nd harmonic rejection	>30 dBc	Not measured	NC	
Main DC voltage supply	>40V	40V	C	
Temperature	-10/ +80 degrees All performance met. junction temperature below 150 deg. C	HPA4 measured at 20°C 60°C 80°C	NC	For 100W of dissipation at 85°C junction temperature is around 110°C see (5)

Table 8 : Summary of measured performance at HPA level with E6 Galileo Signal

4.5 MULTIPACTOR AND CORONA TEST ON HPA PACKAGE

The increase of power in the HPA modules due to GaN transistor technologies induces stronger impact on Multipactor and Corona safety margin, especially in L band. This has now a direct impact on manufacturing constraints for the HPA micropackage leading to degrade the RF performances of the module. The purpose of this study was to validate margin taken for HPA micropackage (RF power >> 50W). With this aim in view, Multipactor and Corona tests were be performed on very high power test jig with up to P~1200W @ f=1.25GHz able to validate the multipactor margin established using analysis ESA tool according to ECSS E20-01-A.

4.5.1 Design

The HPA test jig was designed with 2 mains objectives.

- The first one was to withstand 250 W RF with a 6 dB margin versus multipactor.
- The second one was to present at the input and the output of the test jig a S11< -18 dB.

In order to be compliant with the multipactor objective, a high power TNC connector (ref: EPH11003-13) from RADIALL was used. This one could withstand 250 W RF with a 6 dB margin versus multipactor effect.

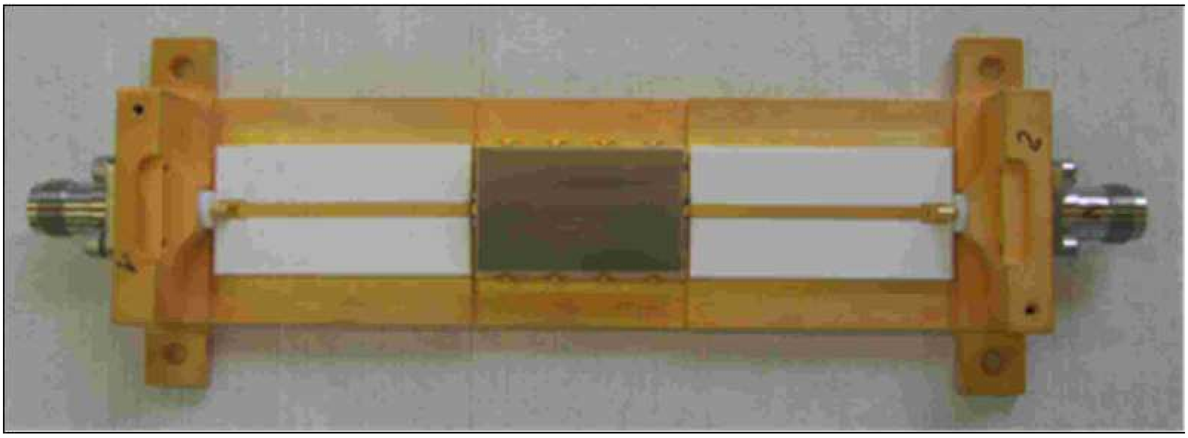

Fig. 8 : Test structure.

4.5.2 MULTIPACTOR AND CORONA TEST CAMPAIGN

The aim of this Multipactor campaign was to validate the RF feedthrough versus Multipactor constraint.
To determine multipactor threshold we need to have an HPA micro package hermetically closed, while to evaluate the corona behaviour it is necessary to have the inside of the micro-package at the same pressure level as the vacuum chamber.
These constraints implied that the Multipactor campaign was to be realised before the Corona campaign.

Multipactor tests validated the HPA micro-package feedthrough for a RF power 250 W with a 6 dB margin (>1000W). This threshold was validated on 2 HPA-micro-packages. As patented, the RF feedthrough was designed thanks to the ECSS multipactor tool version 1.0 and the design method applied gave relatively good results. In order to have a more optimized design with complex geometry thanks to particle simulators, it is necessary to have more information about dielectric behaviour (S.E.Y. characterisation).

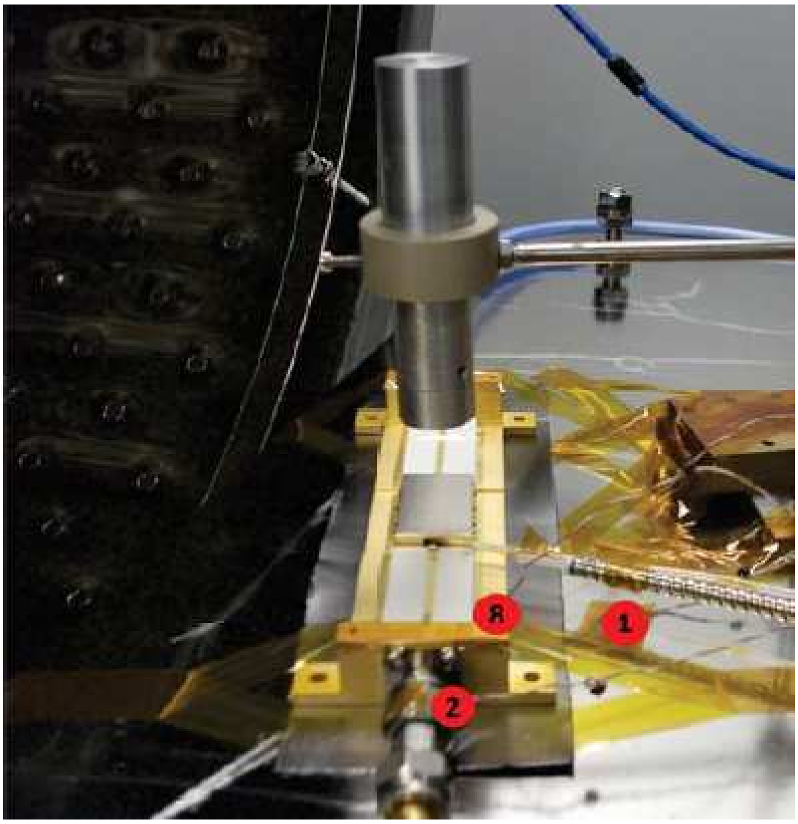

Fig. 9 : Multipactor Detection mode ad radioactive source placement

During Corona testing in L band at 1.25 GHz, corona events occured at 39 mbar for a power of 777 W and a temperature of 55°C, and at 145 W for a pressure of 2 mbar and a temperature of 23°C. These events occured inside and outside the HPA micro-package despite very different physical environments (geometry, materials). At this time, It is difficult to determine which area activated first and if it could be possible to have propagation between both areas.
Even if TAS hermetic sealing (seam welding) allows keeping a pressure above 2 mbar during a complete space mission of 15 years, further analyses are necessary to better understand corona events in an environment adapted to SSPA equipment especially for next generation of GaN based SSPA delivering up to 300W (180W per GaN HPA module: 2x modules in parallel in output section) in L-band for navigation applications like G2G.

5. CONCLUSION

Thanks to this ESA-TRP study, TAS developed a new GaN SSPA output power section in L-band in the range of 120-150W with E6 signal and capable of power flexibility. This output section is based on a single hybrid HPA module using 0,5µm GaN technology from UMS and a new dissipative hermetic package including high power RF feed through. The measurements are excellent and are showing that output power is over 160 W in CW with more than 60% of PAE. In the other hand, Multi-pactor test validates HPA micro-package feed through for a RF power 250 W with a 6 dB margin (>1000W). Even if the HPA micro-package hermetic sealing allows keeping a pressure above 2 mbar during a complete space mission of 15 years, further analyses are necessary to better understand corona events in environment adapted to SSPA equipment.

Based on these results, a preliminary 300W SSPA for future G2G applications has been sized and simulated. With two GaN HPA modules used in parallel in the output section, more than 300W can be delivered with an associated PAE of 51%. An Improvement of PAE is still expected by using all the design's outputs identified in this study (harmonic matching at input and output of the transistors, use of MMIC ULRC for power divider in order to improve stability and frequency bandwidth, use of low losses high power output capacitor etc…).

This study helped us to identify and remove nearly all technological barriers such as transmitting high power on alumina, having reliable and lossless DC-block capacitance ability of using a thermal approach thanks to a specific camera when tuning the module in real time. This study has provided us a very rich return on experience, through the various encountered problems. It has enabled us to identify technological solutions:

The HPA module designed, manufactured and tested in the frame of this study has proven its ability to deliver very high output power at L band over 160W with efficiency above 60%. These excellent performances made it a perfect candidate to the high power SSPA at L band, as well as at S band the derived HPA module, with a straightforward adaptation to the new frequency.
This module will be the heritage power building block for the High Power L/S SSPA product that will make use of a single HPA, and also for the Very High Power L/S SSPA which power section will be built around two HPA modules in parallel.

One major target program for these products at L band is the Galileo program, with several tens of unit. But several other prospects are already identified: digital radio satellite payloads at S band where overall emission power is over 3 kW and is achieved on current programs with several 250W class TWTA, communications channels and GNSS augmentations systems where 50~100W SSPA are commonly used.

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