#### WE LOOK AFTER THE EARTH BEAT

## SpaceWire Backplane Project Final Presentation

Alan Senior 10/12/14

10

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- The work presented is part of the ESA funded SpaceWire Backplane activity contract (No.4000104085, reference TEC-EPD/2010.88)
- The contract value is 130 kEuro,
- 🛰 The ESA Project Manager is Jörgen Ilstad
- The principal aims of the activity were:
  - analyse and trade different backplane architectures and technologies
  - produce a SpaceWire backplane specification for standardisation with input from SpW WG members
  - identify or prototype an impedance matched backplane connector suitable for space

Note: The contract was originally awarded by ESA to the Space division of SEA which is now part of Thales Alenia Space - UK







3

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#### The black box view of an Spacecraft avionics unit

- A Spacecraft avionics unit can be considered to be a "black box" that performs a specific function within a system
- At this black box level we do not care how the internal functions are interconnected; the large number of interconnects over the backplane are hidden from view



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#### Why do we need a SpaceWire Backplane Standard?

- The signal carrying backplane electrical interfaces within a unit are not dictated by customer requirements and are typically non-standard, consisting of discrete lines, parallel busses, device specific serial busses
- The mechanical interfaces for each PCB module are vendor specific
- Module level AIT is complicated by the large number of interface types, so emulating a module that is still in the development cycle is non trivial
- A solution is to create a Backplane Standard around SpaceWire, module reuse between missions and instruments is then practical



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#### Task 1: Applications for a SpW backplane

- >> Any Spacecraft unit that contains a number of modules which:
  - Need to communicate with data rate in the range 10Mbps to 2Gbps
  - ~ Contain functions that are suitable for re-use in future spacecraft

#### - For example:

- >> Spacecraft Management units
- m Data handling units
- Platform control units
- Instrument control units
- mass memory units
- >> Perhaps SpW Backplane not as applicable to:
  - Low rate Remote Interface Units (RIUs)
  - Instrument and sensor front-end applications

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6

#### Task 1: Data handling application of a SpW Backplane



- S modules in non-redundant "unit" above, but we may have more I/O modules
- Typical spacecraft non-redundant unit has 3 to 8 modules

7

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- A survey was published online and 33 SpW WG attendees from 13 different countries were approached
- The survey currently had 13 respondents and showed preferences and trends
- A backplane and connector requirements specification was produced with inputs from the SpW Backplane survey
- These requirements were then used as inputs into the ECSS Backplane Specification drafted within Task 3 and the prototype connector design

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#### Task 1: Physical attributes – compatibility issues

- >> Board size: large or small?
  - Adopt existing standard eg Eurocard, PCI express, microTCA?
  - Existing spacecraft board sizes are driven by device level packaging:
    - 352 pin quad flat packs
    - BGA technology as used for miniature terrestrial applications not generally used
    - Backplane connector
    - Unit external interface count and connectors
- Connector card guide specification must allow for thermal conduction paths
- Board retention (e.g. Simple slot, Bircher, Camloc or Wedgeloc)
- Front panel and associated mechanical interfaces

9

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#### Task 2: Desirable connector characteristics

- SpW signalling rate compatible (up to 400 Mbps)
- SpFi Cu capable? (minimum 2.5Gbps, up to 5Gbps for FR4 PCB)
- Minimum of 2 SpW ports (4 SpFi Cu ports):
  - >> 8 impedance controlled (100 Ohm) differential pairs required
- ∽ Power:
  - Minimum of 2 pins, normally are paralleled up with many more grounds than +\- power rails
  - >> +28V and +5V minimum capability
  - At least 4 Amp rating (20 Watts at 5V)
- Signal lines:
  - Ideally avoided but... this is sometimes not practical
  - Typically single ended, clocks, synchronisation, on/off, FDIR etc.
  - 20 to 40 pins adequate?

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#### **PCI** Backplanes:

🛰 cPCI

- ➣ cPCI PlusIO and Serial
- ∽ cPCI Expresss
- 🛰 VITA Standards
  - ∽ VXS
  - 🛰 VPX
  - 🛰 VPX REDI
  - ∽ Open VPX
  - AdvancedTCA
  - microTCA

Note: SpaceVPX has only recently been introduced and hence was not surveyed



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#### Task 2: Slot bandwidth of different standards

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#### Task 2: Open VPX and VPX REDI offer mechanical standards



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#### Task 2: OpenVPX 6U topology example



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- VITA OpenVPX standards offer the flexibility and potential to be adopted with tailoring
- A connector and backplane requirements specification was produced and with inputs from the SpW Backplane survey
- The connector specification was submitted to Hypertac for evaluating potential design solutions in Task 4



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#### Drafting of ECSS Backplane Specification

- The ECSS draft SpaceWire (SpW) Backplane Specification offers the opportunity timprove re-use of developed functions
- reduce development costs
- simplify integration/test activities
- permit Modules from multiple vendors to be integrated together within a unit

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#### Task 3: SpW backplane standard - advantages











17

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#### Task 3: Drafting of ECSS Backplane Specification

- A draft standard has been produced and released for comment to selected SpW Working Group Members
- The draft focussed on the electrical functions rather than the mechanical or thermal aspects
- Comments have been collated for incorporation into a future version
- While drafting the specification SpaceVPX came onto the scene
- The draft is NOT currently under control of the ECSS system
- Potentially the ECSS Specification could tailor SpaceVPX and hence gain leverage from that standard in particular for the mechanical aspects



18

### Task 3: Draft ECSS specification



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+24V POL and 0V	+5V and 0V	+3V3 and 0V	SpaceWire 1 Data in/out	SpaceWire 1 Strobe in/out	SpaceWire 2 Data in/out	SpaceWire 2 Strobe in/out	SpaceWire 3 Data in/out	SpaceWire 3 Strobe in/out	SpaceWire 4 Data in/out	SpaceWire 4 Strobe in/out	LVDS clock in/out	LVDS Synchronisation in/out	Low rate serial in/out	Low rate serial in/out	Logic level inputs	Logic level inputs	Logic level outputs	Logic level outputs	Analogue inputs and outputs	+/-5V and 0V analogue supply	+/-12V and 0V analogue supply	
000	0000	0000																		0000	0000	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

View of mating face of module connector

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#### Future -tailoring of SpaceVPX via the ECSS standard?



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21



🛰 VME 64X

#### 🛰 cPCI

- 🛰 🛛 3M UHM
- Hypertronics cPCI
- 🛰 VPX
  - Multigig RT2
  - Viper Modular interconnect
  - Hypertronics KVPX
- Advanced TCA
- microTCA
  - Con:CARD

- 🛰 Generic
  - Fortis ZD
  - High Speed
    Ruggedized (HSR)
  - MPACT
- SpaceWire
  - Hypertac HPH-SpW



22

#### Task 4: Potential connector candidates



## Task 4: Survey conclusion

- Hypertronics connectors offer the greatest promise for the SpW backplane connector from "existing" terrestrial
- Possibility of a dedicated Hypertac modular connector development targeted at high speed signals not excluded

🛰 Issues:

- ITAR restrictions on Hypertronics parts
- Is Hypertronics KVPX connector actually in production?
- Can a dedicated SpW backplane connector development be justified?
- How will the need for lower cost systems be accommodated in is the avionics development phases



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# Task 4: Hypertac (Smiths Connectors) Nexus connector development







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#### Task 4: ESCC Detail Specification – draft generated



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### Task 4: Connector test setups





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#### Task 5: Synthesis and Final Presentation

- The activity concluded with:
  - Review of test results
  - Identifying other target markets for Nexus connector
  - Commercial evaluation of Nexus connector development for
    - Space market
    - Military market
  - Identifying future developments and activities
  - >> Summary Report
  - this presentation!

#### Thank you – any questions?



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