# KIPSAT2.X

## DEVELOPMENT OF A DEEP SUB MICRON 65NM RAD HARD LIBRARY PHASE 2.1 / HSSL IP IN SPACE CMOS065LP PHASE 2.2

## *STM DELIVERABLE FOR AR MILESTONE – D1M DOCUMENT*

### Project

| | |
|---|---|
| Technology | SPACE CMOS065LP / C65SPACE |
| Description | Development of a Deep Sub Micron 65nm Rad Hard Library – Phase 2.1<br>HSSL IP S7RADVAL / S7– Phase 2.2 |
| Provider | STMicroelectronics |

### Document

| | |
|---|---|
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# Revision history table

| Version | Author | Date | Description |
|---|---|---|---|
| V0.1 | Thierry Scholastique | 12/06/17 | Initialization |
| V1.0 | Thierry Scholastique | 10/12/15 | First release |
| V3.0 | Thierry Scholastique Laurent Hili | 17/08/17 | Update taking in account ESA feedback (LH) |
| V3.1 | Peter Nayler | 01/09/17 | Proof reading |
| V4.0 | Thierry Scholastique | 01/09/17 | Fine adjustment before proposing to ESA |
| V5.0 | Thierry Scholastique | 18/10/17 | Fine adjustment proposed by ESA |
| V6.0 | Thierry Scholastique | 27/10/17 | |
| V7.0 | Laurent Hili | 07/12/17 | Very last comments |
| V8.0 | Thierry Scholastique | 12/12/17 | Final updates agreed |

# Table of Contents

# Section 1. PURPOSE OF THE DOCUMENT

The executive summary report presents a synthesis of the work performed in the frame of the contracts mentioned below.

- Phase 2.1 (Development of a Deep Sub Micron 65nm Rad Hard Library) contract n°4000107162/12/NL/LvH)
- Phase 2.2 ((Development of a hardened High Speed Serial Link**)** contract n°4000107730/12/NL/LvH)

The key objective of those activities was the development of a space grade ASIC library based on the hardening of ST 65nm commercial node. All the elements present in the final Rad Hard offer can withstand extended environmental constraints, total dose 300Krad (Si), 20y mission profile and junction temperature from -55 °C … + 125 °C.
All the elements present in the library have undergone heavy ions and protons (low and high energy) characterisations. In total, no less than 12 test vehicles (4 variants) were designed and used to perform extensive characterisations (electric, temperature, radiations). The library encompasses the following features:

- ~ 1000 standard cells available in low and high VT allowing design optimisation for speed or power consumption (low leakage).Hardened flip-flop
- Hardened EDACs for memory protection (double error detection, single error correction)
- Hardened clock tree buffers (SET filters)
- Hardened high speed serial links (6.25Gbps, 3.125Gbps or 1.56Gbps)
- Hardened PLL (from 200MHz … 1200MHz)
- Cold spare IOs
- LVDS buffers (up to 2.6 Gbps)

# Section 2. SUMMARY

This document presents a synthesis of the work performed in the frame of "KIPSAT2.1 and KIPSAT2.2" projects funded by ESA and executed by ST, with the contribution of the consortium partners TAS, Airbus, ISD and Micross (originally called Atmel at the start of the project).

The project started in September 2013 and ended in 2017.

Main achievements are listed below:

## KIPSAT2.1 (Key IPs for SATellites phase 2.1)

Starting from a preliminary release of the C65SPACE Design Platform developed in the frame of KIPSAT Phase1, the following tasks were performed in KIPSAT-2.1:

- Electric and radiation characterisation of the new elements of the C65SPACE Design Platform:
  - New Hardened combinatorial cells (clock tree buffers)
  - New faster Flip Flop cells (>300MHz)
  - New extra-macro cells required by customers
    - Dual Port Memory
    - Rad Hard Thermal Sensor
    - PLL (1.2GHz)
    - High speed LVDS (2.6 Gbps)

- ST validated the C65SPACE design platform (CAD flow) thanks to application tests chips (ATCs) such as, telecom ASIC from TAS, quad LEON core from Cobham and High Performance DSP processor (HPDP) from Airbus

In addition to heavy ions tests performed in the frame of KIPSAT2.1 activity, complementary low/high energy proton characterisation campaign was carried out and also total dose (TID) on IO structures.

## KIPSAT2.2 (Key IPs for SATellites phase 2.2)

Starting from an existing High Speed Serial Link IP available in ST 65nm commercial library, the following tasks were performed in KIPSAT-2.2,

- Substantial design modifications to commercial HSSL IP were carried out in order to be immune against gamma rays, heavy ions, low and high energy protons. The hardened HSSL IP was prototyped in a test vehicle called S7RADVAL and used for electric and radiation characterisations.
  - S7RADVAL was characterised under environmental conditions listed here below:

  - SEGR (Single Event Gate Rupture) immunity was verified up to 60MeV/mg.cm², in worst case condition (Power Supply 1.32V and temperature 125°C)
  - SEL immunity verified up to 60MeV/mg.cm², in worst case condition (Power Supply 1.32V and temperature 125°C).
  - SEE Errors were monitored
    - Immunity was verified under proton irradiation for energy ranging from 1MeV to 50MeV
    - Under Heavy Ions
      - In static configuration registers,
        - Threshold LET was characterised and above proton triggering
        - No Single error events observed
        - Very rare events were observed at high LET (<5 for 1e7 ions), partly originating from the test chip rather than the IP itself
      - HSSL IP error rate in GEO < 5e-8 event/day (CREME96, GEO, Solar Min, 100mils, σsat spread among 7 Sensitive Volumes )

The HSSL IP is fully characterised and available in the C65SPACE final offer.

# Section 3. Reference Documents

# Section 4. GLOSSARY

| | |
|---|---|
| PLL | PHASE LOCKED LOOPS |
| LVDS | Low Voltage Differential Signaling |
| HSSL | High Speed Serial Link |
| TMR | Triple Mode Redundancy |
| BER | Bit Error Rate |
| CDR | Critical Design Review |
| CDR | Clock and Data Recovery |
| DC | Direct Coupling |
| HSSL | High Speed Serial Link |
| I2C | Inter-Integrated Circuit |
| MDIO | Management Data Input/Output |
| PRBS | Pseudorandom binary sequence |
| PJ | Periodic jitter |
| Rx | Receiver |
| SJ | Sinusoidal jitter |
| Tj | Junction temperature |
| Tc | Case temperature |
| Tx | Transmitter |

# Section 5. PROJECT EXECUTIVE SUMMARY

## 1. PROJECT OVERVIEW

### 1.1.1. PAST EXPERIENCE AND CONTEXT

The 65nm process from ST microelectronics was identified in 2008 (KIPSAT Phase1.0 kick off) as the most suitable ASIC technology able to fulfil the requirements for European Space applications due to its inherent properties with respect to radiation hardening, long term reliability (20 years @ Tj 125 degrees) and performances (speed / area / power).

The topics listed below were addressed in KIPSAT Phase1.0 activity kicked off in February 2008 and the results reinjected as an input in the subsequent KIPSAT Phase2.1 and 2.2 activities kicked off in September 2013.

- Specification refinements and technology node selection (65nm)
- Reliability study
- Design in reliability techniques (DIR)
- Radiation study
- Design for radiation hardening techniques
- Rad Hard ASIC specification
- Rad Hard ASIC design & manufacturing
- Rad Hard ASIC characterization (electrical / radiation)
- Radiation hardening assessment of an existing HSSL IP (6.25Gbps) developed by ST Telecom ASIC division

Thanks to KIPSAT 1.0 a preliminary release of Design Platform, 'Alpha release' was made available to early users (Thales France, Airbus Germany, Micross and ISD)

After the closure of KIPSAT 1.0, a Phase 2.0 named LIBEVAL under CNES funding was kicked off in order to perform an ESCC evaluation of the existing elements.

KIPSAT phase 1.0 'alpha release' was used as an input to consolidate the final C65SPACE offer developed in the frame of the Phase2.1 and Phase2.2 contracts. The deployment of the final offer was made available through a partnership between ST and Micross.

### 1.1.2. SCOPE OF THE STUDY AND MAIN GOALS

The main goal of KIPSAT Phases 2.1 and 2.2 was the design of a new set of Test Chips (TCs) and their electric / radiation characterisation.
The following TCs were developed:

- TC1 → hardened standard cells digital libraries
- TC2 or PIRADVAL → hardened analogue macros, LVDS and PLL
- TC3 or S7RADVAL → hardened HSSL

The objectives of those new TCs are described here below:

**TC1V4:** (hardened standard cells)

The objective was the upgrade of the design platform with new hardened cells, flip-flops, memories, clock tree buffers. The following cells were produced:

- New combinational hardened cells
- New Flip-Flops cells achieving higher speed performance (>>300MHz)
  - With ECC/parity testing in micro-processor critical paths
  - Evaluating the new Flip-Flops and high speed TMR
- Extra-cells required by end customers
  - Dual Port Memory, Rad Hard Thermal Sensor

TC1V4 specification was defined under ST supervision with the involvement of consortium partners (Thales, Airbus). The resulting test chip specification is described in the work-package WP2110. In addition to the electric and radiation characterisations, TC1 also used by the Partners to exercise and improve the CAD flow (C65SPACE Design Platform).

Finally complementary tests, low/high energy proton as well as TID up to 300Krads, were carried out to fully characterise the C65SPACE final offer.

**TC2V2:** (hardened analog IPs)

The objective was the upgrade of the design platform with 2 new enhanced analogue IPs (PLL and a LVDS buffer),

- 1.2GHz PLL suitable for clock tree delay compensation (clock de-skew, delay compensation up to 8ns)
- 2.6Gbps LVDS buffers consistent with high speed flip-flop offer

**TC3V2:** (hardened HSSL IP)

The objective was the upgrade of the design platform with the hardened HSSL IP (6.25Gbps) and its full electric/radiation characterisation. Such an IP was highly desired by Telecom customers since identified as a key enabling technology for the new generation of telecom payload processor.

To complete this work, CNES ran LINK-EVAL activity using TC3 in order to assess HSSL IP reliability aspects (ESCC evaluation).

#### 1.1.2.1. MAIN ELECTRICAL PERFORMANCE TARGETS

**TC1V4** (hardened standard cells)

TC1V4 was used to validate the following tasks:

- Library deployment on 3 projects (Telecom ASIC with Thales, High Performance Digital Processor with Airbus, Next Generation Micro Processor with Cobham).
- Design and test of a new high performance Flip-Flops (>>300MHz)
- Design and test of a new dual port memory
- Complementary radiation test campaigns:
  - Low/high energy proton campaign: (<50MeV, down to 500keV)
    - With detection of hard failures: Single Bit Upset (SBU), Multiple Cell Upset (MCU), Multiple Bit Upset (MBU) and Single Event Latchup (SEL)
  - A radiation TID test campaign: with an accumulated dose of about 300 krad(Si) at a dose rate of 200 rad(Si)/hour

**TC2V2** (hardened analog IPs)

TC2V2 was used to validate the following tasks:

- PLL: Clock tree delay enhancement
- LVDS: data rate enhancement from initial 800Mbps to 2.6Gbps (new version)

**TC3V2** (hardened HSSL IP)

TC3V2 was used to validate the following tasks:

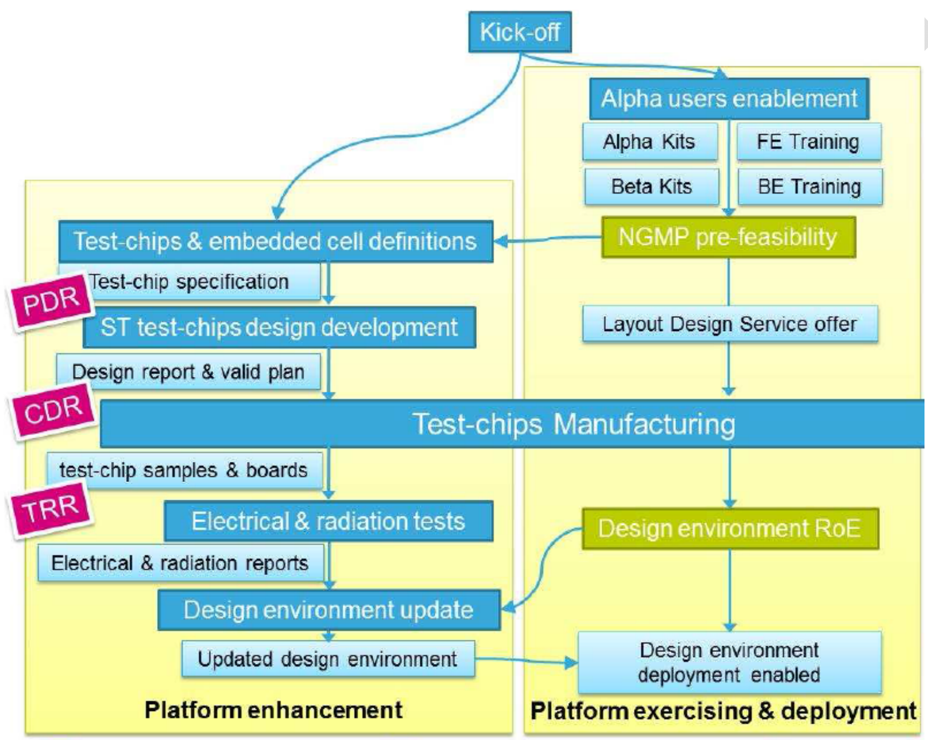
- Bit Error Rate (BER) performance below 10^-14 in terrestrial conditions (target spec)
- Immunity to Single Event Latch-up (SEL) in worst case conditions, max LET up to 60MeVcm2/mg, max temperature 125°C Tj and maximum voltage supply voltages
- No Single Event Failure Interrupts (SEFIs) measured in worst case conditions
- BER characterisation under heavy ions and protons

### 1.1.3. Tasks

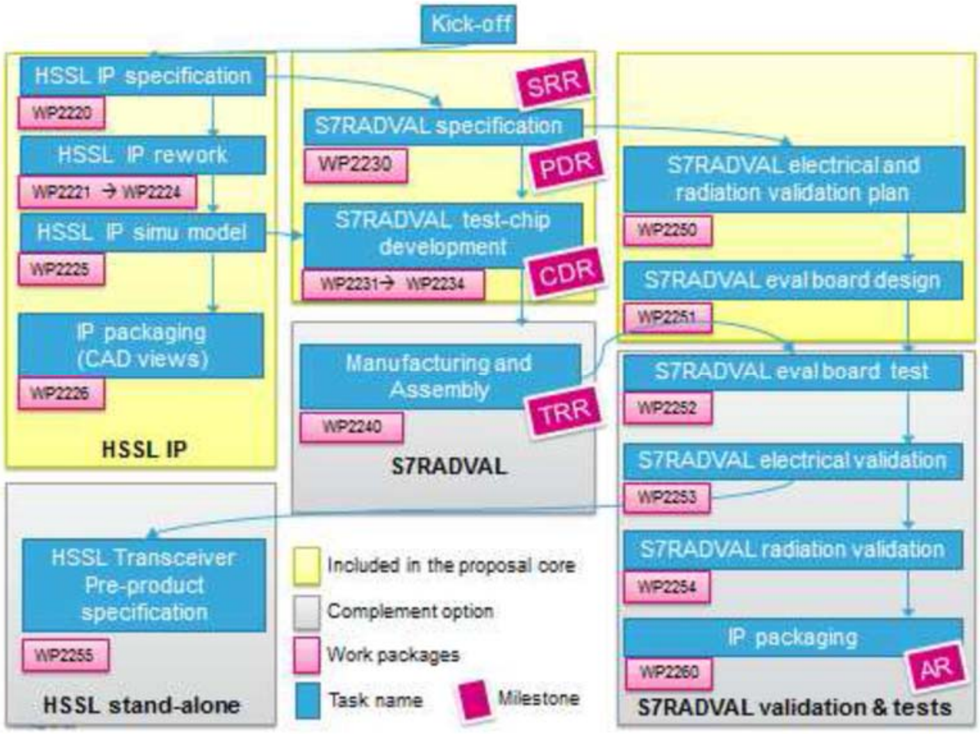
The work logic for Phase 2.1 and Phase 2.2 is presented below.

Phase 2.1 objectives, the development of hardened digital standard cells and analog IPs (respectively TC1 and TC2 also called PIRADVAL test chip).

Phase 2.2 objectives, the development of a hardened high speed link (TC3 also called S7RADVAL test chip)




*Phase 2.1*

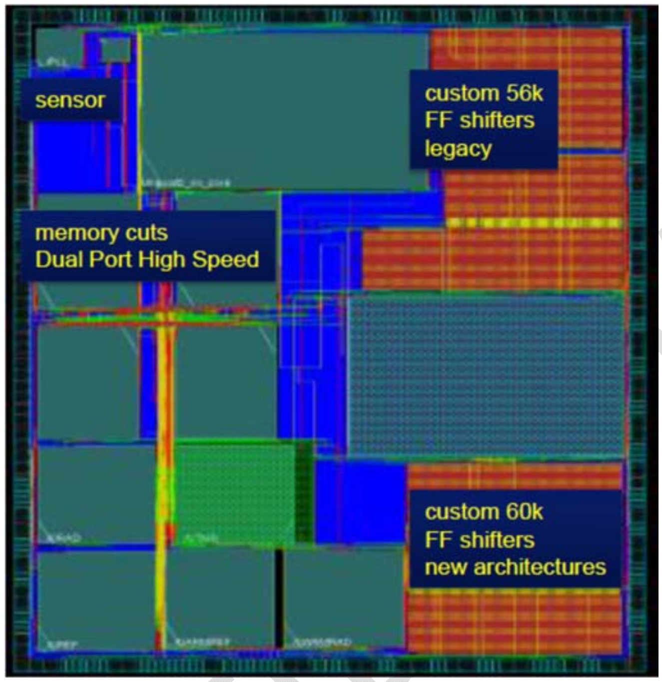

Kick-off
HSSL IP specification
WP2220
HSSL IP rework
WP2221 → WP2224
HSSL IP simu model
WP2225
IP packaging (CAD views)
WP2226
HSSL IP
SRR
S7RADVAL specification
WP2230
PDR
S7RADVAL test-chip development
WP2231→ WP2234
CDR
Manufacturing and Assembly
WP2240
TRR
S7RADVAL
S7RADVAL electrical and radiation validation plan
WP2250
S7RADVAL eval board design
WP2251
S7RADVAL eval board test
WP2252
S7RADVAL electrical validation
WP2253
S7RADVAL radiation validation
WP2254
IP packaging
WP2260
AR
S7RADVAL validation & tests
HSSL Transceiver Pre-product specification
WP2255
HSSL stand-alone
Included in the proposal core
Complement option
Work packages
Task name
Milestone

***Phase 2.2***

# 2. Description of the 3 test vehicles

## 1.1.4. Test Vehicle architecture & main features: TC1V4

ST proposed the following architecture for TC1V4 test-chip:

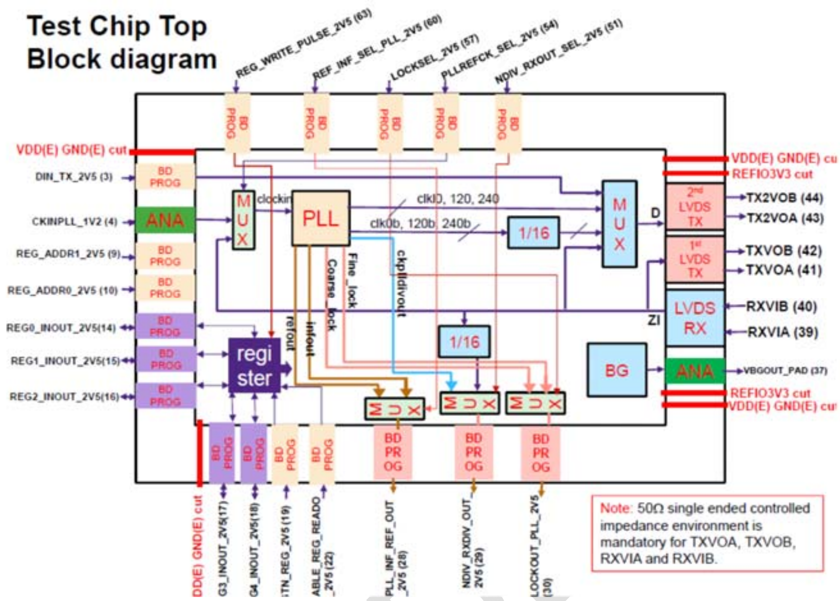



With New digital Space IPs:

- Rad-Hard Dual Port SRAM High Speed with ECC
- Rad-Hard 1+GHz Flip-Flop libraries
- Rad-Hard New TMR cells
- Rad-Hard thermal Sensor

### 1.1.5. TEST VEHICLE ARCHITECTURE & MAIN FEATURES: TC2V2

ST proposed the following architecture for TC2V2 test-chip so called PIRADVAL 2:

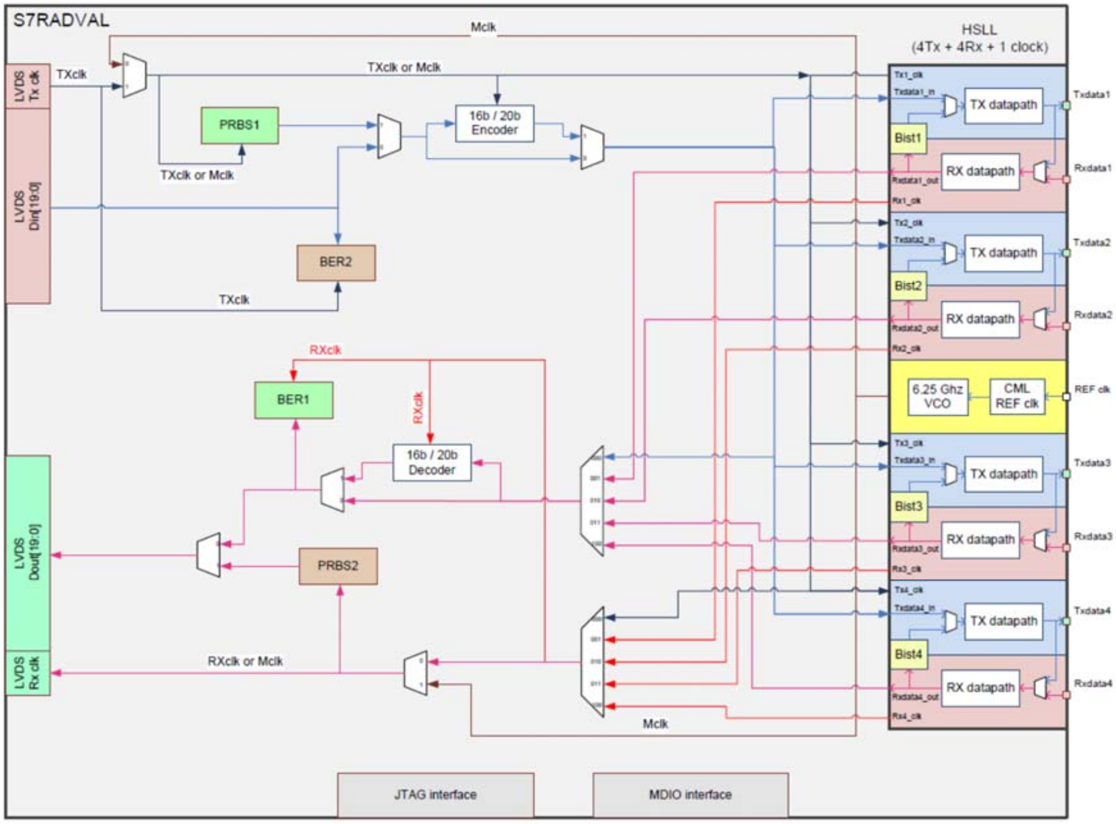



With New analogue hardened IPs:

- RH PLL (1.2GHz)
- RH LVDS (2.6 Gbps)

### 1.1.6. TEST VEHICLE ARCHITECTURE & MAIN FEATURES: TC3V2

ST proposed the following architecture for TC3V2 test-chip so called S7RADVAL:




S7RADVAL block diagram

The S7RADVAL is composed of the following functional blocks:

- HSSL IP (4 data slices + clock slice)
- 20 bit LVDS Din input bus
- 1 bit LVDS Tx_clk clock input (for TxData sampling)
- 20 bit LVDS Dout output bus
- 1 bit LVDS Rx_clk clock output (for RxData sampling)
- JTAG interface
- MDIO interface
- Two identical PRBS generators
- Two identical BER monitors
- 16B/20B Encoder
- 16B/20B Decoder
- The S7RADVAL has 3 internal clocks: Txclk, Rxclk and Mclk.

# 3. Outputs

## 1.1.7. Design

The 3 tests chips as described above were manufactured with a different focus:

- TC1 → hardened standard cells (Flip-flops, clock tree, gated clock EDACs, IOs)
- TC2 → hardened analog IPs (PLL 1.2GHz and LVDS 2.6Gbps)
- TC3 → hardened High Speed Serial Link (6.25 Gbps)

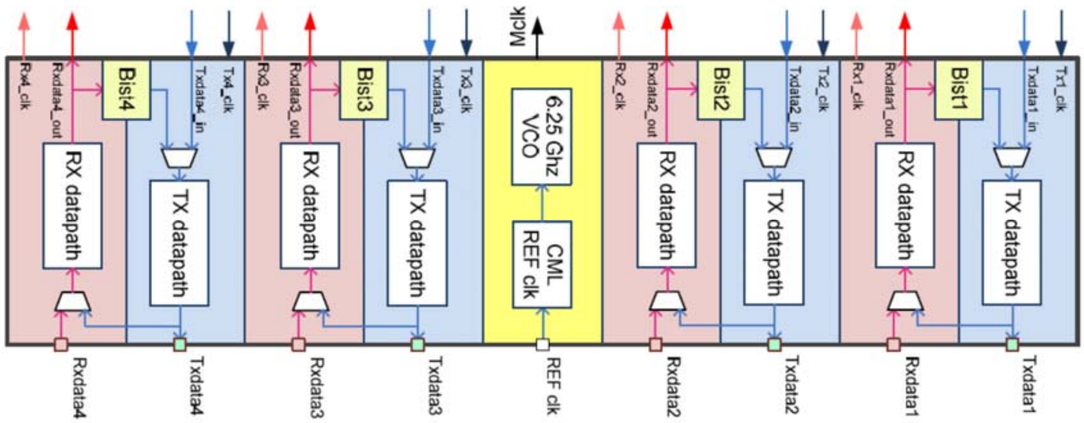
The design activities went through a classical development process of SRR (System Requirements Review) followed by a PDR (Preliminary Design Review), CDR (Critical Design Review) and finally the manufacturing of 3 test chips (tape out).

The consortium Partners (Thales, Airbus, Micross) were involved in all the steps of the development, from the specs and architecture definition (SRR, PDR) until detailed design review (CDR).

### 1.1.7.1. TC3 verification

The design, hardening and verification of HSSL IP (TC3) represented a significant effort over KIPSAT activities. Therefore a special focus is made in this chapter, on describing TC3 verification strategy.

- RTL Digital Verification
- Analogue Verification
- Back Annotated verification of the digital part
- Functional mixed mode verification



HSSL IP Top diagram

## RTL DIGITAL VERIFICATION

Digital functions (RTL) were simulated with Cadence NCSIM.
Analog elements within NCSIM framework were simulated thanks to behavioural cycle accurate models, allowing a quick check of interactions between digital and analog functions:

- control loops
- clock recovery
- phase aligners

The top level HSSL IP encompasses 1 clock slice shared with 4 data slices. Several simulations were run at the top level to ensure a proper connection of all the blocs as well as overall IP performances.

## ANALOGUE VERIFICATION

Pure analogue functions were simulated thanks to SPICE. The following functions were verified.

***Clock slice verification*** consisted in: DC/Polar, AC (stability), Transient, Noise transient and AC Noise, AC PSRR, Rad-Hard, HCI/NBTI

***Data slice verification*** consisted in: DC/Polar, AC (stability), Transient, Noise transient and AC Noise, AC PSRR, Rad-Hard

## BACK ANNOTATED VERIFICATION OF THE DIGITAL PART

***Static timing analysis:***

- First static timing analysis run at clock slice and data slice separately
- Static timing analysis was run on the top of HSSL IP using 1 clock slice and 4 data slices.
  For each netlist, the static timing analysis was performed in the following corner cases:

- Process best case, VDD = Max, temperature Min, RC minimum.
- Process best case, VDD = Max, temperature Min, RC maximum.
- Process worst case, VDD = Min, temperature Min, RC minimum.
- Process worst case, VDD = Min, temperature Min, RC maximum.
- Process worst case, VDD = Min, temperature Max, RC minimum.
- Process worst case, VDD = Min, temperature Max, RC maximum.

***Method of timing back-annotated gate simulations*:**

The back annotated netlist was simulated in conjunction with the analog behavioural models. Thanks to this setup interfaces and performances between digital and analog were checked.

Timings were checked under environmental described below:

- best case process, VDD = Max , temperature Min, RC minimum.
- nominal case process, VDD = Typ, temperature Max, RC typical.
- worst case process, VDD = Min, temperature Max, RC maximum.

***Clock slice verification:***

Clock slice back annotated netlist was simulated running the regression tests also used for RTL simulations.

***Data slice verification:***

Same methodology applies for the data slice.

The following tests were run at gate level:

- o Tx and RX configured to be mission representative (telecom)
- o BIST mode and TX to RX loop back
- o Eye mapper check

***Scan chains:***

ATPG simulations were run at gate level in best case and worst case conditions.

## FUNCTIONAL MIXED MODE VERIFICATION

- o ***Goal 1:*** connections verification to ensure that functionality is guaranteed when replacing the analogue behavioural description by a SPICE description.

- o ***Goal 2:*** digital/analogue timing interfaces verification to ensure that the functionality is guaranteed when taking into account process corners and parasitic extraction. Verilog gate netlist + timing back annotation were used for digital part. For the analogue part, a SPICE description was used, including process corner and Parasitic Layout Extraction.

***Clock slice verification***

- Verify connectivity (goal1)
- Verify timings at digital/analogue interface (goal 2)

***Data slice verification***

The simulations checked the dynamic analogue-digital interface signals.
These simulations also checked the following mixed signal features:

- the TX phase aligner, including the digital phase aligner and the analogue rotator
- the RX phase aligner, including the digital CDR (clock and data recovery), the 2 analogue rotators “edge rotator” and the “centre rotator”,
- the digital eye phase aligner and the analogue “eye rotator”,
- the TX to RX loop-back



### 1.1.7.2. WAFER DIFFUSION AND PACKAGE SAMPLES

The pictures below illustrate the 3 test chips produced in the scope of KIPSAT Phase 2.1 & 2.2. However all along KIPSAT activities, 4 families of test chips were manufactured and characterised to allow full Evaluation of C65SPACE.

**TC1 → hardened standard cells and memories**


Photo 1 – Device top view

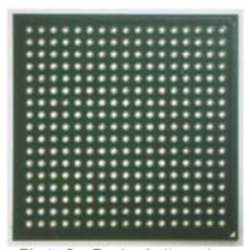
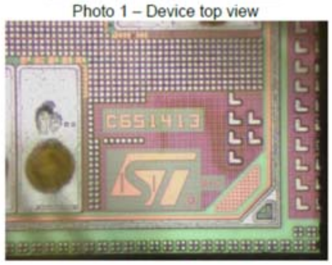
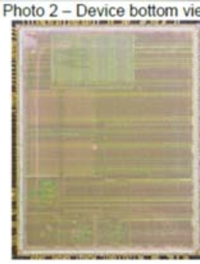


Photo 2 – Device bottom view





## TC2 → analog macros (PLL, LVDS)

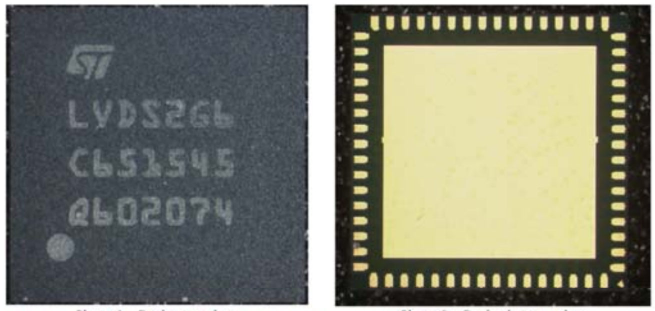
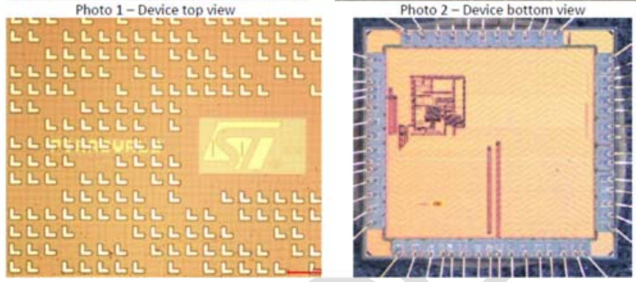
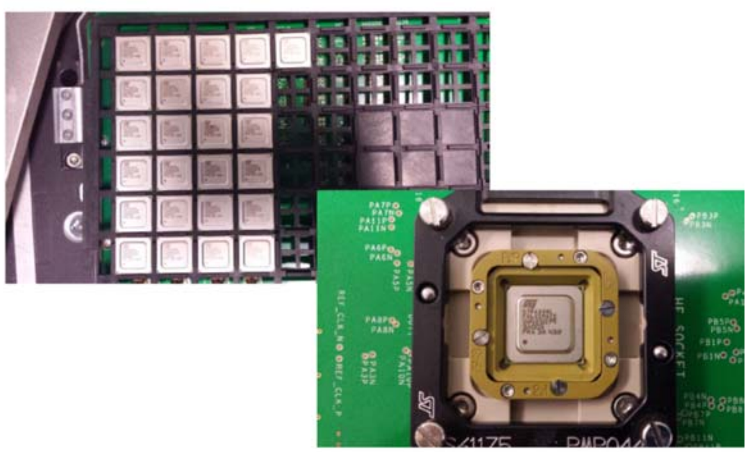



Photo 1 – Device top view

Photo 2 – Device bottom view



## TC3 → high speed serial link



### 1.1.8. ELECTRICAL VALIDATION & CHARACTERISATION

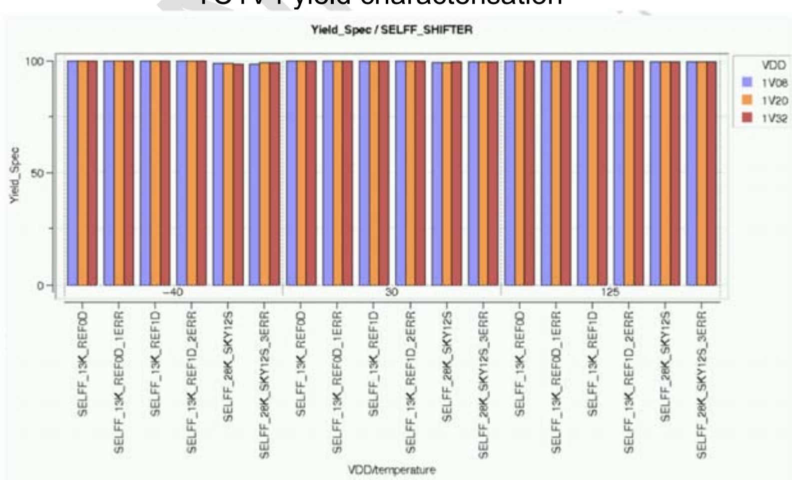
The 3 test chips passed the internal ST milestone validating full electric and reliability characterisations before production phase (MAT 30).
The following tasks were carried out:

- The electrical characterisation over the full process range (Process, Voltage, Temperature variation)
- Timing and power consumption measurements. Alignment / correlation with CAD models
- Radiation characterisations

**TC1V4**

- The measurements done on TC1V4 showed that the hardened cells from SKYROB65LPLVT and SKYROB65LPSVT libraries exhibited an excellent yield over voltage and temperature. The wafer tests were characterised at the limits of the specified operating temperature and voltage conditions
- The delays and power consumptions of the combinatorial / sequential cells measured on the wafer are within the CAD window.
- Flip-flop timing constraints were modelled in the CAD tools and showed adequate yield
- The SKYROB libraries were fully characterised and therefore ready for production
- The new features such as dual port memories and hardened thermal sensor IPs were fully characterised and are now part of the final SKYROB offer.

TC1V4 yield characterisation



## TC2V2

Two new IPs, the PLL and LVDS, were characterised thanks to TC2.

**PLL 1.2GHz:**

- PLL is functional across the supply voltage and temperature ranges mentioned in the PLL specifications.
- Analog/digital current consumption in normal mode and in power-down mode are within specifications.
- The lock time and power down pulse width are within PLL specifications.
- Jitter at output clock is within PLL specifications.

**LVDS 2.6Gbps:**

- For LVDS Transmitter Measurements:
  - DC Currents
  - Output thresholds (VOL,VOH, ΔVOD, ΔVOS )
  - VOA & VOB Tests
  - Wake up time from Power Down condition
  - Ro (o/p impedance)

  Transient measurement were also done for TX with 2 different loads, although specs not available for these parameters
  - Rise-Fall time
  - Propagation Rise-Fall delay
  - Duty cycle
  - Max Frequency

- For LVDS Receiver Measurements:
  Following Currents & DC measurement were performed and all measured values are within specs
  - DC Currents
  - Input DC resistance
  - Wake time from PD

- For Bandgap Measurements:
  Following measurement were performed and all measured values are within specs
  - DC Currents
  - REFE Voltage (Reference Output Voltage)
  - Tstart (startup time)

## TC3V2

The HSSL IP passed all ST qualification criterions. The following tasks were carried out:

- o Electric, voltage and temperature characterisations
- o Performance, timing and power are within CAD window
- o BER (Bit Error Rate) below 10-14 (spec)

| | Test description. References | Data Rate [Gbps] | P | V | T [C] | Status | Notes |
|---|---|---|---|---|---|---|---|
| Functional tests | MDIO interface | 6.25 | TT | Typ | nom | Pass | |
| | I2C interface | 6.25 | TT | Typ | nom | Pass | |
| | LVDS interface | 6.25 | TT | Typ | nom | NA | not feasible (requires running 20-bit parallel bus - instruments limitation) |
| | Data generation and BER, without HSSL | 6.25 | TT | Typ | nom | Pass | |
| | Thermal sensor charachterisation | 6.25 | TT | m/T/M | all | Pass | |
| | Long term BER | 6.35 | TT | min | all | Pass | done 69h test @ Tamb, Vnom --> BER=0 |
| | Long term BER with ref clock static variations | | TT | min | hot | Pass | lock the AUTOTUNE, stop it, then add ppm and do the long term BER<br>done 3h test, with -100ppm on ref clock, @ 125C, 1.14V --> BER=0 |
| Loopback & Link | Internal Loopback | 6.25<br>3.125<br>1.5625 | TT | Typ | nom | Pass | eyes available @ FR, HR, QR.<br>Measures vs VT are covered by ATE tests |
| | External Loopback | 6.25<br>3.125<br>1.5625 | TT | Typ | nom | Pass | eyes available @ FR, HR, QR.<br>Measures vs VT are covered by ATE tests |
| | Snake Test LR (~10dB) | 6.25 | TT | m/T/M | all | Pass | SERDES IP functional, with limitation, offset loop ko, low margins at High Temp and High attenuation |
| Clock slice | Fout vs LCCOARSETUNE value | | TT | m/T/M | all | Pass | Pass with limitation, at Hot and min supply there are some failures but far from the applications frequency |
| | VCO free run limits | | TT | m/T/M | all | Pass | |
| | VCO stability vs supply and T | | TT | m/T/M | all | Pass | |
| | Phase noise vs CP and LCVCOTRIM | | TT | m/T/M | all | Pass | |
| | Ref clock phase noise characht. | | TT | Typ | nom | Pass | |
| | Loop behaviour vs ref clock dynamic variations | | TT | Typ | nom | Pass | no unlocking with +/-100ppm refclock variations |
| | Loop behaviour vs ref clock static variations | 6.25 | TT | min | hot | Pass | |
| | Tx FIR pulse shape | 6.25 | TT | Typ | nom | Pass | |
| | Tx eye and speed vs supply and T | 6.25 | TT | m/T/M | all | Pass | |
| | Tx termination | 6.25 | TT | m/T/M | all | Pass | Impdeance programmation it has been update on latest spec |
| Receiver | Jitter tolerance vs MAXBANG | 6.25 | TT | Typ | nom | Pass | |
| | Jitter tolerance vs supply and T | 6.25 | TT | m/T/M | all | Pass | |
| | Sensitivity vs supply and T | 6.25 | TT | Typ | nom | Pass | |
| | Sensitivity vs Eq slope and gain | 6.25 | TT | m/T/M | all | Pass | |
| | Impedance vs supply and T | 6.25 | TT | m/T/M | all | Pass | Impdeance programmation it has been update on latest spec |
| | Rx return loss | 6.25 | TT | m/T/M | all | NA | |
| P. Cons | CS consumption vs supply and T | 6.25 | TT | m/T/M | all | Pass | done on 3 samples |
| | Tx consumption vs supply and T | 6.25 | TT | m/T/M | all | Pass | |
| | Rx consumption vs supply and T | 6.25 | TT | m/T/M | all | Pass | |

*Table 5-1. validation summary*

### 1.1.9. RADIATION TESTS

#### 1.1.9.1. TID (Total Ionising Dose)

TID tests were performed at UCL (Louvain Catholic University / Belgium). A Cobalt60 source was used with the possibility to adjust the dose rate by modifying the distance from the source. The dose received by the devices was permanently controlled by a dosimeter placed on the board.

Intermediate electrical characterization were performed every 50krad steps. Currents and voltages were monitored and parametric drifts measured.

The TC2 vehicle was characterised up to 300 krads(Si) at a dose rate of 200 rad(Si)/hour. Thanks to TC2, the LVDS, I2C and BDPROG IO cells were extensively characterised at max dose (300 Krads) and under max supply voltages.

**In conclusion:**
No functional failure observed at max TID (300 krad) and max supply voltage, 1.32V core supply, 3.6V for BDPROG / I2C and 2.75V for LVDS.
Parametric drifts < 1% in worst case conditions (static and dynamic tests).

Finally IOs cold spare functionality were tested also at max TID and max voltages in order to characterise leakage currents. Marginal currents were recorded (nano amps range).

### 1.1.9.2. PROTON TESTING

**TC1V4** (hardened standard cells)

#### High Energy Proton

Two radiation test campaigns were carried out at the PSI test facility (Paul Scherrer Institute / Switzerland / May 2015).

- The test were performed in conformance with ESA/SCC 25100.
- The test setup was built in a way to allow for the detection of Single Event Latchup (SEL) and for memory, Single Bit Upset (SBU), Multiple Cell Upset (MCU), Multiple Bit Upset (MBU).

#### In conclusion:

The test campaign permitted the characterisation of, four Dual Port High Speed RAM (DPHS) configurations, 11 shift-registers at low clock frequency (50MHz) and 4 shift registers at high clock frequency (600MHz).

The measurements on the dual port high speed SRAMs confirmed:

- SEL immunity at the highest proton energy (200 MeV) cumulated with worst operating conditions (1.32V, 125°C and 1e11 protons/cm²).
- Efficiency of ECC wrapper (Hamming). The Dual Port SRAM is immune to protons at highest energy (200 MeV).

Experimental measurements at low frequency (11 shift registers) demonstrated a SEU cross section 1 to 2 magnitude of order better for SKYROB DFFs (hardened cells) than CORELIB (commercial cells).

However CORELIB DFFs combined with Triple Modular Redundancy (TMR) have demonstrated a full SEU immunity.

Characterisations performed at frequencies up to 600MHz on the 4 shift registers structure using the newly developed BIST (Built In Self-Test) architecture have demonstrated the following:

- 1 to 2 magnitude of order improvements regarding SEU cross section for SKYROB DFFs (robust and ultra-robust) over the CORELIB ones (commercial).
- SKYROB 2G (2nd generation) cell while being faster than SKYROB FD12S (1st generation) has a similar proton SEU cross section.

## Low Energy Proton

A Low Energy Proton (<50MeV, down to 500keV) test campaign was carried out at RADEF test facility (Jyvaskyla / Finland / April 2015).

- The test were performed in conformance with ESA/SCC 25100.
- The test setup was built in a way to allow for the detection of Single Event Latchup (SEL) and for memory, Single Bit Upset (SBU), Multiple Cell Upset (MCU), Multiple Bit Upset (MBU).

The characterisation campaign essentially focussed on  SRAM structures.

**In conclusion:**

The measurements confirmed a SEL immunity at the highest proton energy.

SEU events have been flagged thanks to the ECC used in combination with the DPHS for energies ranging from 500keV to 52MeV (nominal supply voltage and ambient temperature).

ECC wrapper (Hamming) used with DPHS has demonstrated a quasi SEU immunity in highly accelerated conditions 1E8 p.cm2/s and total immunity in "natural" non-accelerated conditions.

## **TC3V2** (hardened HSSL IP)

test campaign was carried out at RADEF test facility (Jyvaskyla / Finland / April 2015).

3 types of events were monitored during proton tests:

- Single Event Latchup (SEL)
- Single Event Failure Interruption (SEFI)
- Bit Error Rate (BER)

**In conclusion:**

- ***Low energy protons (1MeV to 5MeV)***
  No event detected. HSSL IP is therefore immune.

- ***High energy protons (19MeV to 60MeV/mg/cm2 )***
  No SEL no SEFI observed, only very rare bit errors were detected at max fluence of 1E11 particles per cm2**.**

### 1.1.9.3. Heavy Ions Testing

The 3 test chips (TC1V4, TC2V2, TC3V2) undergone a Heavy Ion test campaign.
The test were performed in conformance with ESA/SCC 25100.

**TC1V4** (hardened standard cells)

Two radiation test campaigns were carried out at the RADEF test facility at Jyvaskyla, Finland in March and May 2015.

- The test procedure was compliant with the ESA/SCC specification 25100.
- The following events were monitored, Single Bit Upset (SBU), Multiple Cell Upset (MCU), Multiple Bit Upset (MBU) and Single Event Latchup (SEL).

The experimental measurements on Dual Port High Speed SRAMs have confirmed:

- SEL immunity with the highest heavy ion LET (60 MeV.cm²/mg), cumulated with worst operating conditions (1.32V, 125°C and 1e7 ions/cm²).
- ECC wrapper efficiency (Hamming) by detecting single and double errors and correcting single errors. The Dual Port SRAM is quasi-immunity to heavy ions at the highest LET (60 MeV.cm²/mg). In GEO configuration Dual Port SRAM can be considered as immune
- That ECC feature is totally operational

The experimental measurements at low frequency on flip-flop shift registers structures have confirmed:

- The robustness of the SKYROB library over CORELIB (commercial) at all LET up to 60Mev
- The TMR allowed for an improvement of the LET threshold by a factor 10 and an improvement of the saturated cross section by a factor 100 over the standard CORELIB flip-flops (commercial non hardened).

The experimental measurements at high frequency (600MHz) on flip-flop shift registers structures using hardened BIST confirmed:

- A better cross section at all LETs for SKYROB flip-flop (hardened) versus CORELIB. A SEU cross section improved by a factor 100 at medium and high LET (60Mev).
- The performance (speed) of the 2nd generation hardened flip-flop "SKYROB2G" while keeping similar cross section with respect to "SKYROBFD12S" (low power hardened DFF)

## TC2V2

Heavy Ions test campaigns were carried out on PIRADVAL2 test chip, in December 2016 at UCL Louvain-la-neuve Belgium and in January 2017 and February 2017 at RADEF University of Jyväskylä, Finland. For each campaign, three parts were characterised under heavy ion beam.

In summary:

All new analog macros, 1.2GHz PLL and 2.6 Gbps LVDS are latchup immune in worst case conditions (VDDmax, Tj=125°C, LET=60MeV/mg.cm²) and fully SEE characterised.

## TC3V2

The test campaign was conducted at RADEF facility in June 2016. High speed serial link macro was characterised under heavy ions. The following events were monitored, Single Event Failure Interrupt (SEFI), latch up (SEL), Single Event Upsets (SEU) and Bit Error Rate (BER).

In summary:

- No latch up recorded in worst case conditions (VDDmax, Tj=125°C, LET=60MeV/mg.cm²)
- No SEFI recorded
- Estimated SEU rate in GEO ~ $5.10^{-8}$ event/day (CREME96 solar min configuration)
- LET threshold characterised

## 4. Conclusion

ST65nm hardened technology for space or C65SPACE library represents a major leap with respect to former European ASIC technology based on 180nm node. C65SPACE offers unprecedented performances in terms of integration capacity (x10 times factor) but also improvements in speed and power consumption. Another major achievement relates to the hardening of the high speed serial link IP. Such an IP was a key enabler for new developments in the field of digital telecom payloads where hundreds of those HSSL interfaces are used. Therefore offering 6.25Gbps data rates while keeping the consumption relatively low and at the same time guarantying radiation robustness (300Krads, no SEL, no SEFI) was a major challenge. Today ST HSSL IP delivers a x30 times speed improvement over SpaceWire (~200 Mbps) deployed on many ESA missions. ST hardened library, or C65SPACE, was successfully deployed on few ESA path finder projects such as:

- Thales Very High Speed Telecom Satellite (VTHS). Digital transparent processor product (DTP).
- Next Generation Microprocessor (NGMP) a Cobham-Gaisler product also referenced under code name GR740.
- High Performance Digital Processor (HPDP) an Airbus Defence and Space product.
- BRAVE FPGA a product developed by Nano-explore.

In the frame of KIPSAT activities a 3000 pages data book was released compiling all information required for the designers but also the radiation results of the various test campaigns (heavy ions, protons, TID). The document is available from ST under NDA.

Finally acknowledgements to ST Prime and its Industrial Partners (Thales, Airbus Defence and Space, ISD, ATMEL) for their commitment during all those years.

Special acknowledgement to CNES for its financial and technical support (CNES reliability analysis laboratory).

C65SPACE development has paved the way for a durable cooperation with ST Microelectronics in the field of hardened ASIC technologies for Space applications. New supply chain is under certification by ESCC. Next step is already engaged with even smaller node (28nm) and will open new technology possibilities and new market opportunities.