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Verification of SEU-mitigation techniques in 3rd/4th generation Flash FPGA

Executive Summary Report

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1. Introduction

1.1. Context

Flash-based FPGAs are relatively new additions to the portfolio of space-grade FPGAs, and the development flows targeted to the specific requirements of these FPGAs are not up to date, in most cases. Microsemi is the main provider of these types of FPGAs and currently has in its portfolio the 3rd and the 4th generation of such products. In Microsemi's Flash FPGA product portfolio, some families like PROASIC3 and IGLOO2 are not specifically designed to be used for space, nevertheless this FPGAs have also been used in space-related applications on low cost equipment. The proper implementation of SEU mitigation techniques commonly applied for these families such as TMR, "safe" FSM coding, Hamming-3 FSM coding, etc. is difficult to confirm and verify in an automatic and thorough manner. At the moment, formal verification EDA tools, such as Synopsys Formality and Mentor Formal Pro, cannot confirm logic equivalence of a design employing such SEU-mitigation techniques against its unmitigated counterpart, and verify that these techniques have actually been properly implemented in the specified areas of the design.

Microsemi has also developed two Flash-based FPGA families specially for space: RT Polarfire and RTG4. Since these devices are relatively new, their space heritage is quite limited, compared to other more stablished solutions like Microsemi's RTAX antifuse family. In addition to that, these new families offer a high number of high-performance programmable logic resources, large and fast onboard memories, and high performance I/O - SERDES, LVDS, DDR, etc. All the elements are very appealing in high-bandwidth data processing payload applications, but also high-performance on-board computing so a detailed understanding of the behavior of the FPGA fabric under radiation is necessary. AS&D, in collaboration with NASA/GSFC (see RD-10) have done a study on the SEE characterization of the logic fabric in the RTG4, i.e. SEUs in flip-flops, global routing behavior (SETs in clock and reset lines), as well as configuration cell updates and reprogrammability susceptibility to SEE. In addition to that The Radiation Effects group in ESTEC/ESA also run an activity on the characterization of the memory blocks in RTG4 (see RD-11).

Considering the above-mentioned background, ESA published an ITT to address the following two main objectives:

1. The Development of (formal) verification methods for verifying the proper implementation of SEU/SET mitigation techniques for Flash based FPGAs, applied at RTL level or netlist level (such as TMR, "safe" Finite State Machines, etc.)
2. Perform an Extensive radiation test campaign, targeting 4th generation Flash FPGAs from Microsemi (RTG4 in particular) with the following aims:
    a) Characterization of PLL performance (SEE sensitivity) under radiation.
    b) Sensitivity of the FPGA fabric, and of the test vehicles used, to SEFI.
    c) Characterization of the I/O blocks. In particular, the following types of I/O buffers will be characterized: 3.3V/2.5V/1.8V/1.5V/1.2V LVCMOS, LVTTL, PCI, LVDS, LVDS33, SSTL2I, SSTL2II, HSTLI, HSTLII, and SERDES.

ARQUIMEA and UC3M in consortium presented a proposal based on ARQUIMEA's background on microelectronics design and radiation testing of ICs and UC3M's experience on fault tolerant design, emulation and verification of mitigation techniques, which was finally selected.

1.2. Scope

This document provides a summary of the work done during the project including its context, a description of the program of work, and the main results achieved. Finishing with the conclusions.

1.3. Document References

1.3.1. Applicable documents

Ref.	Number	Title
AD-1	4000123942/18/NL/GLC	ESA Contract - Verification of SEU-mitigation techniques in 3rd/4th generation Flash FPGA
AD-2	TEC/2016.42	Statement of Work
AD-3	ARQ-P-17023	Proposal "Verification of SEU-mitigation techniques in 3rd/4th generation Flash FPGAs"
AD-4	ECSS-Q-ST-60-02C	Space product Assurance ASIC and FPGA development

Table 1-1: List of applicable documents

1.3.2. Reference documents

Ref.	Number	Title
RD-1	ARQ_18104_DDD_001	Detailed Design Document for formal verification methods
RD-2	ARQ_18104_DDD_002	Detailed Design Document for all test vehicles
RD-3	ARQ_18104_DDD_003	Test setup description
RD-4	ARQ_18104_VPL _001	Verification Plan for formal verification methods
RD-5	ARQ_18104_VRP _003	Verification Report for formal verification methods
RD-6	ARQ_18104_TPP_001	Test Plan and Procedure - Verification of SEU-mitigation techniques in 3rd/4th generation Flash FPGA
RD-7	ARQ_18104_UMN_001	User Manual for formal verification methods
RD-8	ARQ_18104_RPT_001	Test samples preparation report
RD-9	ARQ_18104_RPT_002	Radiation Test Report
RD-10	Paper 1	"NEPP Independent Single Event Upset Testing of the Microsemi RTG4: Preliminary Data", Berg et al, June 2016. https://ntrs.nasa.gov/search.jsp?R=20160009477
RD-11	2016_RADECS_DW_Paper_JJW	Single Event Effects Hardening on 65 nm Flash Based Field Programmable Gate Array
RD-12	Statement of Work for Call of Order 2 to ESTEC/ESA Contract No. 4000113697	"Radiation testing of EEE parts in support of ESA R&D activities", Call of Order 2 "Heavy ion SEE Testing of Microsemi RTG4 flash based FPGA", ESTEC TEC-QEC

Table 1-2: List of reference documents

1.4. Acronyms

Name	Meaning
AD	Applicable Document
ARQ	ARQUIMEA Ingeniería S.L.
CAN	Controller Area Network
CCC	Clock Conditioning Circuitry
CCSDS	Consultative Committee for Space Data Systems
DUT	Design Under Test
EPCS	Extended Physical Coding Sublayer
FPGA	Field Programmable Gate Array
I/O	Input/Output
IP	Intellectual Property
LET	Linear Energy Transfer
LETeff	LET Effective
LETth	Linear Energy Transfer Threshold
LVCMOS	Low Voltage Complementary Metal-Oxide-Semiconductor
LVDS	Low Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
MeV	Mega electron Volt
PLL	Phase Locked Loop
POR	Power On Reset
RD	Reference Document(s)
RO	Ring Oscillator
RTCAS	Rad-Test Control and Acquisition Software
RTL	Register Transfer Logic
RX	Reception
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch-up
SERDES	SERializer - DESerializer
SET	Single Event Transient
SEU	Single Event Upset
SN	Serial Number
SR	Shift Register
SSTL	Stub Series Terminated Logic
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TV	Test Vehicle
TX	Transmission
WSR	Windows Shift Register

Table 1-3: Acronyms

2. Programme of work

2.1. General description

As described in the introduction, the project was planned with two main objectives:

- *Task 1: This task will address the development of formal verification methods for verifying the proper implementation of SEU/SET mitigation techniques for Flash based FPGAs, applied at RTL or netlist level (e.g. TMR, "safe" Finite State Machines, etc.).*
- *Task 2: The objective of this task shall be an extensive radiation test campaign, targeting 4th generation Flash FPGAs (Microsemi RTG4), with the following aims:*
    a) *Characterization of PLL performance (SEE sensitivity) under radiation.*
    b) *Sensitivity of the FPGA fabric, and of the test vehicles used, to SEFI.*
    c) *Characterization of the I/O blocks. In particular, the following types of I/O buffers will be characterized: 3.3V/2.5V/1.8V/1.5V/1.2V LVCMOS, LVTTL, PCI, LVDS, LVDS33, SSTL2I, SSTL2II, HSTLI, HSTLII, and SERDES.*

Both tasks have run in parallel during the project execution accordance with the original proposal, Task 1 ended at TRR whereas Task 2 lasted until the project was formally closed.

2.2. From KO to MS1 (SRR and DDR meetings)

The verification methods for SEU/SET mitigation techniques task started with the definition of the requirements for the formal verification methods. The radiation characterization of 4th generation flash-based FPGAs task was launched addressing the definition of the test procedure. The SRR meeting was held on October the 10th, 2018

The design implementation activities run in parallel for both the verification tool and the test vehicles. The command-like tool verification tool was developed jointly with the Validation Plan and test designs. The test vehicles were split into two different designs: Design A and Design B to be radiation tested. The DDR meeting was successfully held on April the 10th, 2019

2.3. From MS1 to MS2 (TRR meeting)

In this phase the software developed to check the SEU mitigation techniques was verified. To do so a set of reference designs and several IP cores, hardened by using different approaches, were tested with the tool. The validation experiments were intended to prove that the requirements approved in the SRR were fulfilled.

Regarding the radiation characterization activity, in this phase two major subtasks were performed: The preparation and programming of the samples and the setup preparation/dry testing. In order to perform radiation testing on the parts, they had to be de-lidded and back grinded following the recommendations provided by Microsemi. The TRR meeting was successfully held on October the 22nd, 2019.

2.4. From MS2 to MS3 (TRB meeting and Final Review)

In this phase two main tasks took place, the radiation testing and the analysis or radiation results. The Heavy ions test campaign took place at RADEF, Finland, in two shifts on November the 4th and 5th. SEE tests were run according to the radiation test plan without major issues.

The Protons test campaign took place at PSI, Switzerland, in three shifts on November the 12th, 13th and 14th . Proton tests were run according to the radiation test plan. The TRB meeting was successfully held on the 17th of December. In this meeting all actions from TRR were closed and a preliminary review on the radiation tests results was performed. The Acceptance review took place on the 26th of February, formally closing the project.

3. Main results

3.1. Formal verification methods

The developed Formal Verification Tool (FVTool) consists in a console application, with a twofold objective. It can be used to formally verify the correctness of a variety of SEE mitigation techniques to harden digital designs. As well it is intended to formally verify the functional equivalence between a hardened design and the original version (before hardening). FVTool reports on the success or failure of equivalence analysis as well as on the correct implementation of the mitigation techniques. In case of failure, it shows a counterexample in order to help designers to identify the origin of the difference.

FVTool is applied in three steps (see Figure 3-1) by using several commands:

1. Parsing the input files to generate AIG formats (.hag file). This first step generates the intermediate files that will be analysed and processed in the following steps.
2. Verifying the correctness of mitigation techniques. This step generates another intermediate file, also in AIG format, where the existing redundancies have been removed (a merged netlist). In case errors in the mitigation techniques are detected, they are reported as well as an input vector as proof. The supported techniques are:
    - Local, distributed, block and I/O TMR
    - Safe FSM encoding (automatic error recovery of the FSM to the state specified in the "Reset" condition)
    - Safe Case FSM (automatic error recovery of the FSM to the state specified in the "others/default" clause)
    - Hamming-3 FSM encoding (detection of invalid FSM transitions)
    - Duplicate and compare
    - SET filtering by triplication of the clock and reset trees, with insertion of delay elements on each of the three clock/reset nets
3. Verifying the functional equivalence between the pre-processed hardened version of the circuit and the original one.

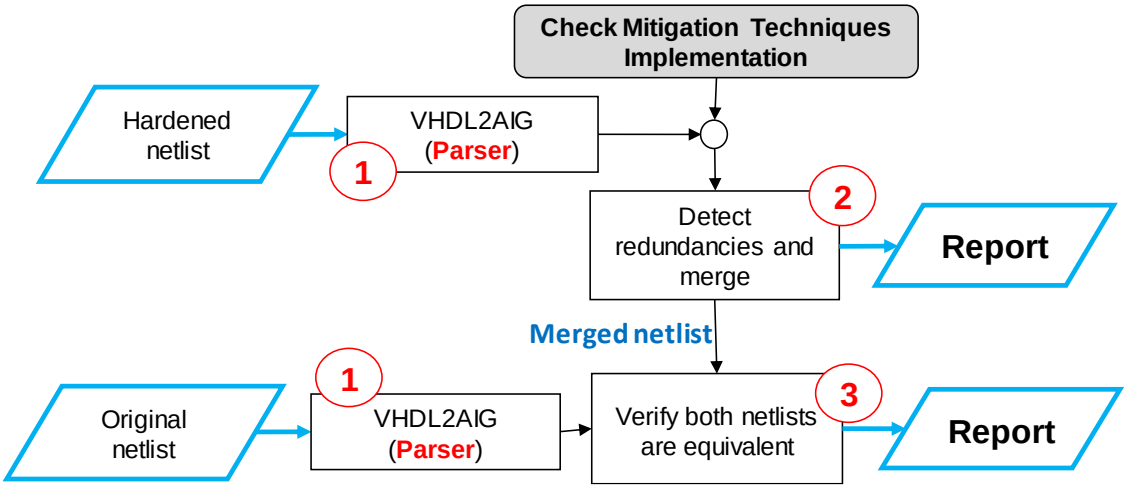

Figure 3-1. Execution flow

3.2. Radiation testing

3.2.1. Specimens under test

The parts radiated in this activity are RTG4 FPGAs from Microsemi, manufactured on a low power µMC 65nm process, with the main features detailed hereafter:

- High-speed signal processing
- Highest performance with the most logic resources of any RT FPGA
- Immune to radiation configuration upsets
- Radiation-hardened by design

Eight DUTs were provided by ESA to the project team. Six out of the eight parts were radiation tested whereas two of them were left as spare. Two designs were available for programming the parts: Design A and Design B. Each design contained a different set of test vehicles as detailed in Table 3-1 . All parts were back grinded so that the radiation testing could be performed on them. Some tests vehicles were conceived to check their performance against SETs whereas others were inspected for their SEU sensitivity. Latch up monitoring is done on all the parts during SET and SEU runs at room temperature.

Test Vehicles (TV)	TV Number	Design Type	Heavy Ion		Proton	
			SET	SEU	SET	SEU
Windowed Shift Register	7	A		X		X
Ring Oscillators	3	A	X		X	
Counters	32	B		X		X
Output Pad	6	A & B	X		R	
Input Pad to output pad	6	A & B	X		R	
SpaceWire CODEC	2	B		X		X
CCSDS 121	2	B		X		X
CAN Bus Controller	2	B		X		X
ARM M0	2	B		X		X
SerDes	1	A		X		
PLL	1	B	X		X	
Power-On Reset	1	A & B		X		X
CCC	1	A	X		X	

Table 3-1: Test vehicles included in each Design (A/B)

3.2.2. Test setup

The setup consists on the elements depicted in Figure 3-2.

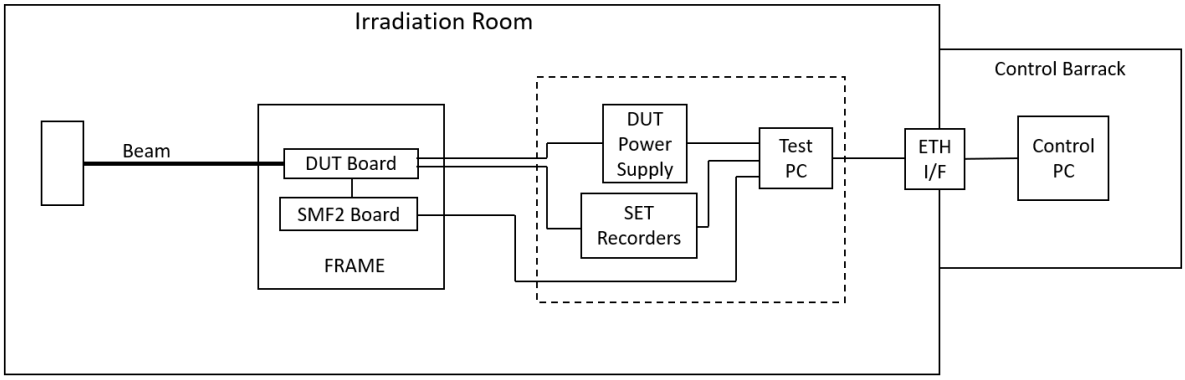

Figure 3-2: Radiation tests setup top level block diagram

3.2.3. Test Results

3.2.3.1. Heavy ions results

The test to characterize the performance against heavy ions were defined by different TV, as mentioned above, these TV (Windowed Shift Register, Ring Oscillators, Counters, SpaceWire, CCSDS, CAN Bus, ARM M0, SERDES, PLL & CCC) shows results in accordance with previous researches like RD-11 and RD-12.

Some tests were design for the pads with the following results:

The input to output pad configuration test results show that the occurrence of SETs when the pads are set to HIGH or to LOW level is different depending on the technology. The PADs set to high level are more sensitive to transients that when they are when set to low.

As for the output configuration, test results cannot be generalized in this respect since some pads like LVCMOS33/25 show a higher count whereas the rest seem to be performing similarly with independence of the value set to the pad.

In general, it can be said that high speed pad technologies are more sensible to this effect in terms of number of transients collected and sensibility to lower energies. SSTL2 and LVDS got transients with low energies (13.4MeV), 3.3V technologies as LVCMOS33 and LVTTL33 instead were robust up to high energy values (48.5MeV) getting very little transients per run. LVCMOS25 response was slightly worse, getting low level transients at 24.6MeV.

Let Threshold was very similar for the input to output configuration as for the output standalone one, whereas the number of events is slightly lower in the case of the output configuration which means that the transient contribution from input pads is very small.

Regarding the Power-On Reset, the window trigger for the recording of POR events was configured from 2.3v to 2.75V. Two SET events were recorded in this test vehicle, one on RUN 16 and another one on RUN 17. Error counters in Shift registers and PLL test vehicles for RUN16 present a big error jump that might be caused by a POR SET. In RUN number 17, Shift Registers and PLL Test Vehicles counters got saturation, because of that, data results from RUN 17 for all test vehicles were discarded. No events were recorded up to 48.5MeV

3.2.3.2. Protons results

The test results recorded for the different TV (Windowed Shift Register, Ring Oscillators, Counters, SpaceWire, CCSDS, CAN Bus, ARM M0, SERDES, PLL & CCC) reveals good performance, as no mayor events were recorded.

Some tests were designed to verify the pads:

SETs have been observed in some tested pads both when checking the input to output connection and the output. Almost all the recorded SETs are wide.

The input to output pad configuration test results show that very low events were recorded at HIGH and some as LOW. As for the output configuration very few events were recorded on the high speed pads when set to HIGH. Output pads set to LOW have shown no transients.

4. Conclusions

4.1. Formal verification methods

According to the experimental results, the VHDL parser and AIG generation software module have passed all the tests. Regarding the verification module, it can be stated that the considered hardening techniques have been successfully included and that FVTool is able to formally verify if the implemented error mitigation techniques are correct or not. It generates a verified netlist without the redundant logic due to mitigation techniques, what allows the comparison with respect to a not hardened version.

With respect to the equivalence checker, the result is successful for TMR, DTMR, BTMR and DWC for circuits without FSMs. For circuits with FSMs, the result of the equivalence checking depends on the synthesis over the unreachable states, what is out of the control of the FVTool.

In conclusion, all the requirements have been achieved although there are some limitations. Therefore, there are some improvements that could be implemented as future works.

4.2. Radiation testing

The radiation testing campaigns provided a quite interesting set of results. On one hand, the radiation performance of the RTG4 FPGAs reported in previous reports like RD-11 and RD-12 has been confirmed. For the main FPGA internal building blocks two main regions of operation are clearly identified: al lower energies the number of errors is smaller and the SET filtering feature improves significantly the performances whereas at higher energies the number of errors is bigger and the SET filtering has no effect (being therefore the SEU the dominating factor). The SET filtering feature also improves the performances at high frequencies where the SET events have a higher impact. The results of other FPGA fabric building blocks like the PLL and the SERDES are also in line with the ones reported in the literature. The PLL presents some SET and SEFI sensitivity but with a cross section good enough for most of the applications whereas the SERDES presents a big casuistic of error types with a degraded BER under radiation, including a complex scenario of SEFIs.

On the other hand, the testing performed in this activity shows some results that had not been previously reported, i.e. the SET sensitivity of the pads. SETs have been observed in all the tested pads both when checking the input to output connection as well as when checking the outputs fixed at a constant value. Many of those SETs have a width below 10 ns however very wide pulse transients have been recorded as well. In addition to that, the POR circuitry was routed to a pad in order to characterize its radiation performance and a few SETs were observed. Nevertheless it cannot be fully confirmed if all measured SETs on this test vehicle are related to the actual POR or the pad. Further investigations on this matter are recommended.

As for the investigations found on the IPs, it was confirmed that the radiation performance is quite dependent on the design and the observability/recoverability of the potential errors.

In beam programming has also been tested concluding that with low fluxes, the reprogramming of the parts can be done at various energy levels.

Further testing on the parts (the ones used, and the ones left as spare) could be easily conducted in the future based on the developed setups in order to get further knowledge on this technology.