Digital Sun Sensor
On Chip

SSOC

ESTEC CONTRACT 21835/08/NL/ST

EXECUTIVE SUMMARY

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CONTRACT REPORT

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ESA STUDY CONTRACT REPORT

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ESA Contract Number	Subject		Name of Contractor
19520252/06/NL/JA	**Sensor on a Chip SoaC**		GALILEO AVIONICA
* ESA CR ( ) No	* Star Code	No. of volumes This is Volume No.	Contractor's Reference

Abstract

Objective of this work was to:

- To design and manufacture a SSoC detector chip with integrated MEMS optics at prototype level
- To produce a preliminary design of the final SSoC product with justification analysis and accuracy estimation
- To derisk, by test, challenging design topics like the custom package

Results:

The industrial team composed by SELEX Galileo, CMOSIS and BAE Systems, with the support of Thales Alenia Space, implemented the design of a miniaturized prototype of a Sun sensor on chip. The design involved the chip itself (with the on chip embedding of the FPA, all the logic, the voltage regulators, oscillator and SpW interface), the MEMS optics and its integration on the chip, a prototype packaging solution and the manufacturing of a mechanical housing to demonstrate assembly and integration concepts.

Characterisation tests have been carried out on the unit and sub assemblies.

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GENERAL

The ESTEC CONTRACT 21835/08/NL/ST under a TRP program is related to the design, manufacture and test of Digital Sun Sensor on a Chip Prototype.

The contract was subdivided into two phases:

- Phase 1 was related to the design of the sensor at system level and chip level up to tape-out.

- Phase 2 was related to the manufacture and test of:
  - the prototype chip
  - the electrical breadboard
  - a mechanical demonstration model (mock up)

The electrical breadboard is comprised of a PCB that accommodates the SSoC chip packaged into a standard package with the pinhole bonded on it. The mechanical mock up is representative of the final product design.

The activities have been carried out by a project team composed by SELEX Galileo (Italy), CMOSIS (Belgium), BAE SYSTEMS (UK) and Thales Alenia Space (France). Each of the partners have brought into the project their own expertise and technical background such as attitude sensor design and development for SELEX Galileo, imaging detector development and characterization for CMOSIS, optics and MEMS capabilities for BAES and system integration and AOCS expertise for Thales.

Figure 2.1-1: The SSoC Industrial Team

Within the contract, SELEX Galileo has the role of prime contractor and the responsibility for the unit design, verification of the electrical breadboard and the mechanical mock up.

CMOSIS has the responsibility for the chip design, manufacturing and characterization.

BAES has developed the design of the pin hole optics, manufactured, verified and bonded on chip the pin hole. It also has assessed the feasibility custom package for the final product by means of a mock up.

Thales gave their contribution in the design overview of the final product and prototype, as final user. In particular, they were responsible for ensuring the compatibility of the electrical and mechanical interfaces with the s/c design They participate only on phase 1 of the contract.

The contract started in October 2008 with phase 1 that was completed with the CDR at chip and unit level after approximately one year. The second phase that includes the manufacturing and tests of the deliverable items (chip prototype with integrated pin hole, electrical breadboard , custom package and sensor housing mock-ups) started in December 2012 and was completed with the test review board in November 2010.

DOCUMENT CHANGE RECORD

REV	DATE	CHANGES DESCRIPTION	PREPARED
0	December 20111		E. Monnini

1 INTRODUCTION

The Sun Sensor on a Chip (SSoC) is a highly miniaturised, plug and play, medium to high accuracy digital Sun sensor suitable for use on all classes of mission from nano satellites (<10kg) to GEO telecoms (18 year lifetime) and planetary rovers (e.g. high dust environment).

The SSoC design and concept is initially verified through a prototype chip.

The prototype chip is mounted on a breadboard PCB, while the final product is designed and verified by analysis. A mock -up of the mechanical housing, as well as a mock-up of the custom package, has been developed according to the preliminary design of the final product.

In the following figure the chip prototype and the mechanical housing mock-up is reported.

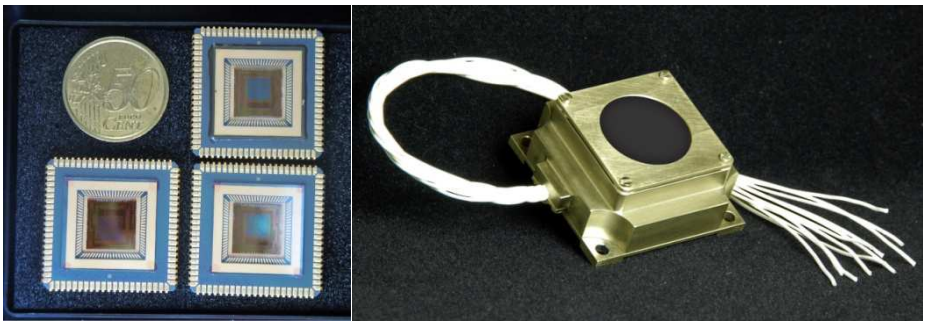


Figure 2.1-1: First SSoC prototype in the standard package (left) and mechanical housing mockup (right)

2 SSOC DESIGN

2.1 SENSOR DESIGN DESCRIPTION

The SSoC consists of:

- A mechanical housing designed to allocate the sensor core chip and the limited off-chip electronics and to allow the integration, alignment and thermal control of the sensor on the satellite. An attenuation filter that shall be positioned as the closure window of the sensor housing and whose attenuation can be mission dependent without jeopardizing the recurring cost of the unit.

- A sensor core chip that includes not only the electro-optical sensitive part but also the logic for the Sun position determination and operating modes management, the power conditioning and the digital data interface. The EQM/FM core chip shall be packaged in a custom package. The prototype is packaged using a standard package.

- A glass sandwich with a pin hole that shall be integrated on the chip and shall be used to enlarge the sensor FOV without a strong degradation in performance, offering also a good shielding effect that protect the chip from the incoming radiation levels.

The SSoC has two main operating modes, Sun Acquisition Mode (SAM) and Sun Tracking Mode (STM), a FOV of max 64° with the possibility to blank two rectangular areas in the detector to avoid appendices from the satellite. The overall accuracy is less than 0.05° in the whole FO V.

The operating modes are shown in Figure 2.1-1 and Figure 2.1-2.

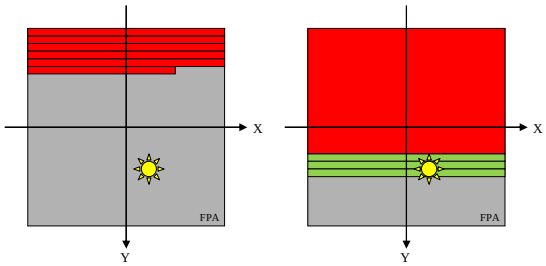


Figure 2.1-1: Sun Acquisition Mode: full frame scan until the Sun image is detected

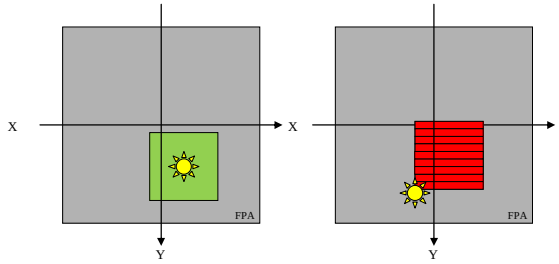


Figure 2.1-2: Sun Tracking Mode with window scan: tracking (right), loss of Sun (right)

Sun Acquisition Mode is entered upon power-on or reset. In this mode the SSoC scans a user defined field of view (normally the full 511 x 511 pixel frame) at user defined rate (normally 5Hz) and searches it for the occurrence of a bright object that matches the dimensions of the Sun image. Once such an object is found, the SSoC determines its exact position, interrupts the full frame scan and transitions to Sun Tracking Mode.
Sun Tracking Mode positions and maintains a user defined readout window (by default 80 x 80 pixels) around the Sun image, at a user defined rate (by default 10Hz, but up to 60Hz and even more). Each window is scanned completely, after which the position of the bright object that is most likely the Sun is extracted. The window position is updated and the cycle repeats. If no Sun image is encountered, the SSoC transitions back to Sun Acquisition Mode.
At all times the coordinates of the Sun image's photometric centre of gravity are extracted and made available on the TM interface. Furthermore, the presence of the Sun in the field of view is always flagged on the SunPresent chip pin as a logic output.

The assembly concept, described in the following pictures, is based on a main structure constituted by an titanium alloy frame. The choice for this material is because its Thermal Coefficient of Expansion (TCE) matches the assembly with glass (closure window) and the ceramic package of the detector. In addition it offers better radiation shielding within the same volume.

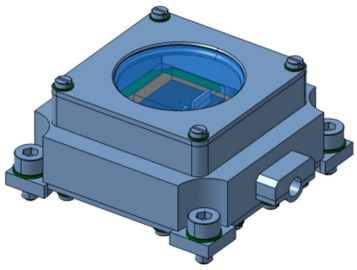


Figure 2.1-3: Sun Sensor housing

In the final product chip a tiny circuit board, hosting few off chip components, will be fixed to the main structure of the sensor, in order to increase its stiffness, while a pig tail connection technique allows lower volume and mass.

The upper cover supports internally an attenuation filter, attached to the upper cover with Armstrong bonding. If needed, the attenuation filter can be tailored to the mission needs, and selected on a “mission by mission” case.

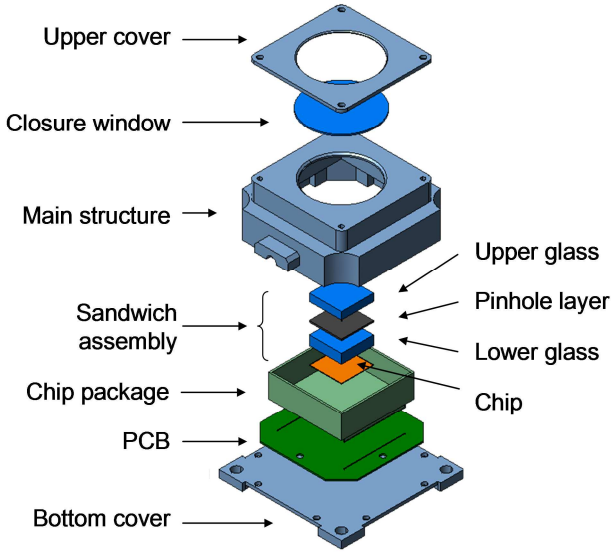


Fig. 1:

Figure 2.1-4: Sun Sensor Assembly

The latest generation of star sensor APS chips were built with .35µm CMOS processes, but still during the study on the System on a Chip the need for .18µm processes was put in evidence. While 3T pixels could possibly meet the optical performance requirements for a Sun sensor, CMOSIS opted for 4T pixels justifying the additional costs to the aim of a pre-development and de-risking phase also for a future star tracker chip.
A strong desire for physical robustness led to a fully radiation hardened design. For the analogue circuits this was done by layout. For the logic the hardness was obtained using IMEC's DARE library of rad-hard core and IO standard cells for the UMC 0.18µm CMOS foundry and process.
Tape out to UMC was done in January 2010. First silicon returned in June 2010 and was tested and characterized through the rest of the year.
The approach to a new foundry or process, like in this case, should be to pre-evaluate it with a test chip with a multitude of experimental pixel variants. For reasons of budget and schedule such was not feasible in this project and a valid product had to be designed from scratch. However it was agreed with the foundry to divide the CMOS manufacturing run into a number of phases, with

within each phase a number of wafers processed according to slightly varying conditions in order to drive towards optimal pixel performance.

The sensor chip includes:

- Analogue section: the 512x512 10 µm pitch 4 T rolling shutter pixel array, 10-bit column ADCs, and readout circuits, all rad-hard
- Digital section: the Processing Logic with image filtering implementation and the SpaceWire/UART Telemetry/Telecommand (TM/TLC) interface
- Power section: the 3.3V and 1.8V power regulator, the 5V input voltage
- Oscillator
- LVDS drivers
- Power On Reset

In the following figure the sensor chip block diagram is reported.

Only few components (quartz and other passive components) are still needed off chip.

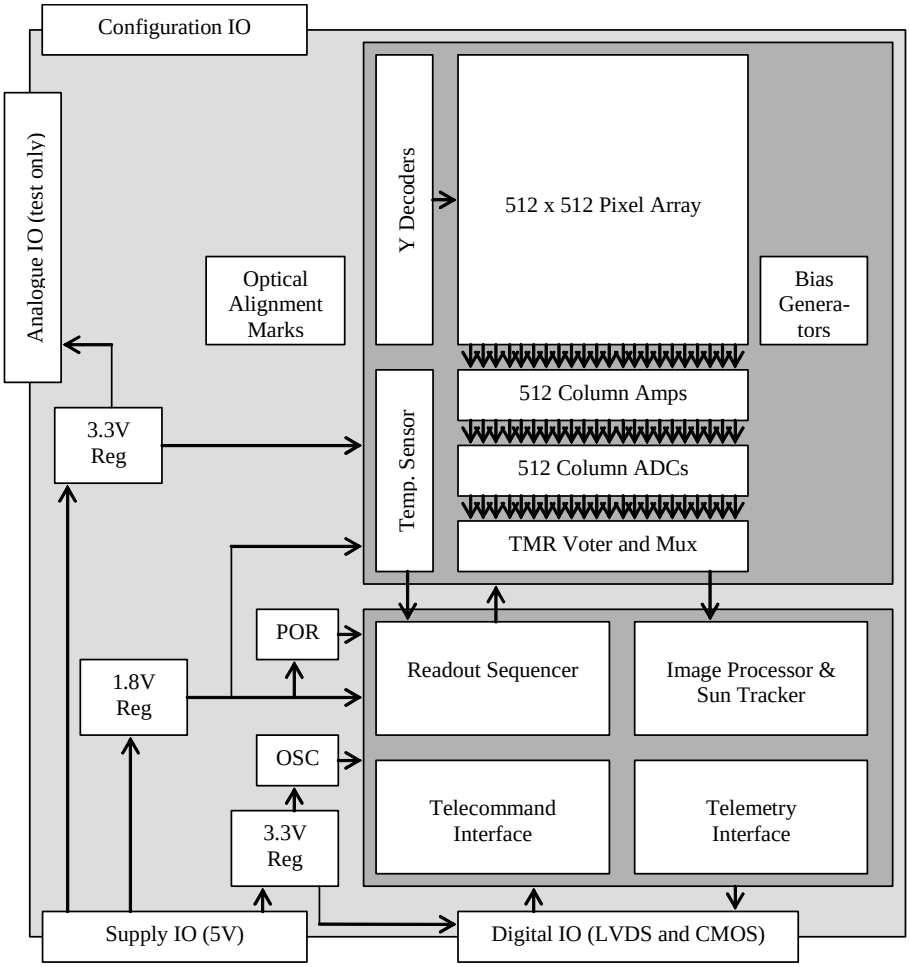


Figure 2.1-5: Sensor chip block diagram

Upon power-on the sensor is intended to autonomously acquire and then track the Sun. No telemetry data are generated: the host must query the sensor for data. The chip can be used interactively as well: modes, configurations, and parameters are stored in registers that are user accessible over the TC interface.
The sensor chip circuitry requires 3.3V and 1.8V power supplies. These can be sourced from the system board, or alternatively from three on-chip linear voltage regulators. The regulators are rated for 5V input (5.5V maximum), although short term (i.e. hours) tolerance to a raw supply input of up to 6.7V has been observed in the lab, and over full temperature range.
The on-chip quartz oscillator operates with a specific 10MHz external crystal. A direct clock input is also available.

The basic design of the optical chip consists of a metal pinhole layer spaced above the sensor chip by a thick glass layer creating an optically immersed chip. A top glass layer is added above the pinhole layer providing immunity to assembly dust and additional radiation blocking.

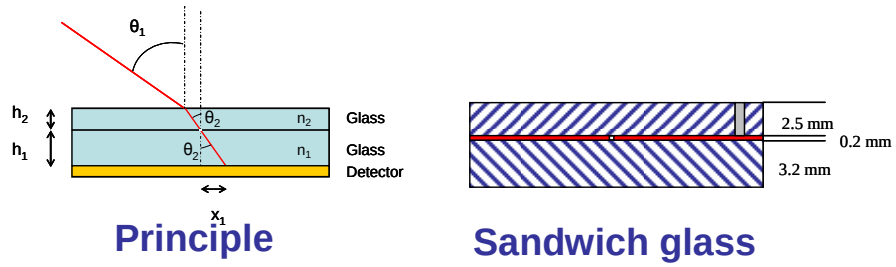


Figure 2.1-6: Optics design concept

The overall design consists of a conventional electronic package with single-in-line pins on four sides underneath, routing layers between the pins and bond pads aligned with the chip pads for wire bonding.

The package lid will be a custom kovar metal cap. It is required to be relatively tall to accommodate the integrated chip and must also support hermetic sealing at two locations, one to the electronic package and one to the top of the optical chip, as shown in the diagram below. The mock-up integrated chip in package is reported in Figure 2.1-8

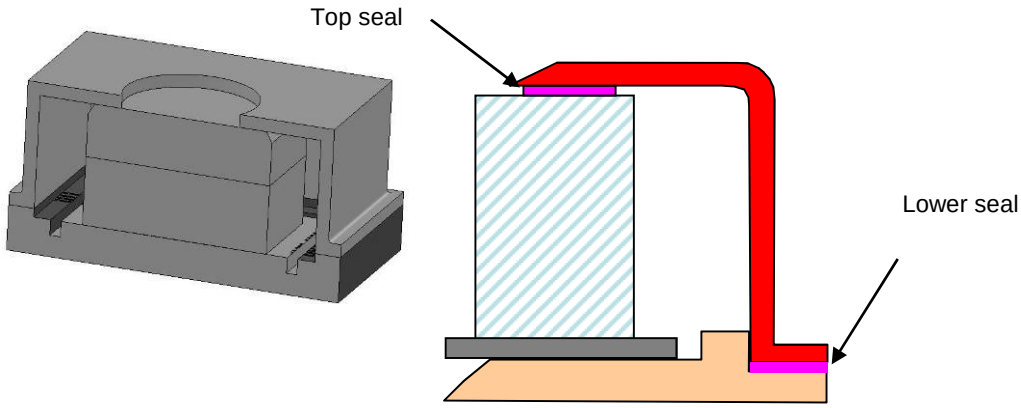


Figure 2.1-7: Section through package (left), Top and lower seals (right)

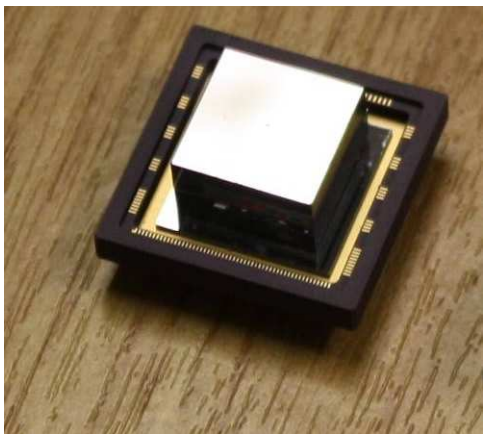


Figure 2.1-8: Mock-up integrated chip in package

2.2 SSOC PROTOTYPE

The SSoC protype consists of:

- Prototype chip manufactured by CMOSIS
- Integrated chip MEMS manufactured by BAES
- Electrical breadboard representative of the final electrical design of the SSoC that includes the prototype chip with integrated pin hole. This has been manufactured by SG. The breadboard hosts voltage regulators and oscillator, to be used instead of the chip ones, and the RS422 drivers in addition to the SPwire drivers
- Housing mock-up chip manufactured by SG
- Package mockup chip and MEMS manufactured by BAES

The prototype has been verified, as reported in Figure 2.2-1 in order to validate the manufacturing process and design with the demonstration of the assembly

feasibility, functionality and a first estimation of the overall accuracy of the SSoC. Tests at chip level include also radiation tests.

A chip prototype was tested also at ESTEC (Control Hardware Lab) using the same test setup that allowed testing the LCMS detector (512x512 Active Pixel Sensor APS 3T pixel with internal sequencer and logic).

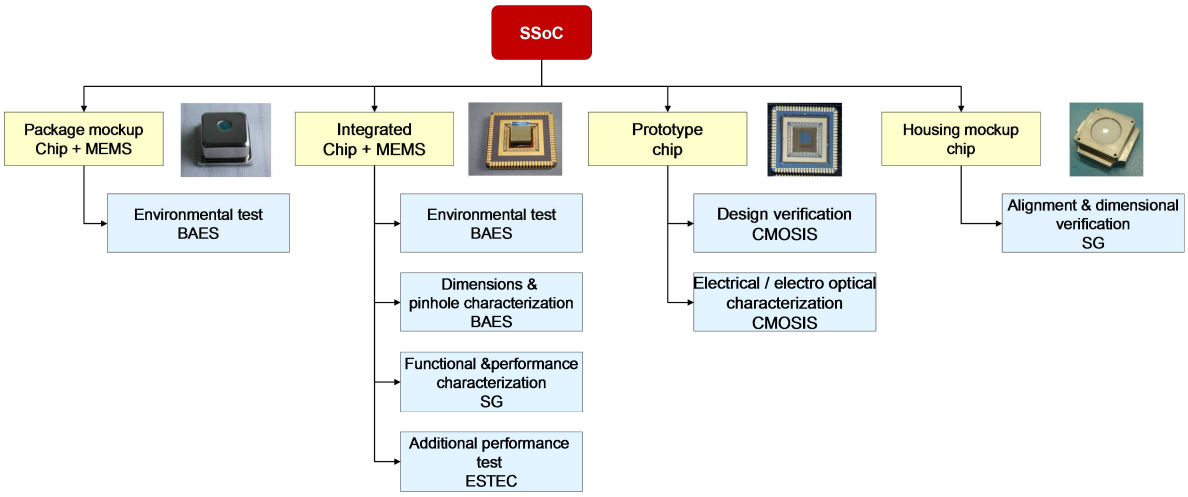


Figure 2.2-1 prototype samples testing activities

The SSoC sensor chip was fully functional, including all logic, processing, supply voltage regulators, power-on-reset, and clock oscillator. Nevertheless some performance issues were discovered during the testing. The key ones of note were:

- pixel dark current, while acceptable for Sun tracking, is too high for star tracking. Further investigations other wafer runs and process variations are part of a separated CCN.
- the output of the supply regulators is slightly too high although fine for demonstration purposes. This should be remedied for an FM
- a timing error in the ADCs causes a number of secondary problems with noticeable impact on electro-optical performance (it will be repaired with a metal fix for the current production, while the ADC will be fully fixed by design in the following steps of the chip development):

Soft-programming of SSoC registers was able to mitigate some of these effects.

Total dose testing and annealing (at room temperature and in the thermal chamber) has been performed at ESTEC during February 2011, with several steps, up to 300Krad. Dark current is not a major contributor to the performance in this specific application (integration time is as low as 30 microseconds) but it was important to verify that logic survived and that no important drift in FPN, DC, DCNU or Reset Noise appeared.

For the Sun sensor application, no issues were found with all the components survived and maintained operability, even at 300 kRad and no dark current evolution after radiation (20 kRad) has been identified in the best pixel variant.

Latch Up and Single Event Upset testing was done over a time of two hours at the Heavy Ion Irradiation Facility of UCL (Louvainla-Neuve, Belgium), in October 2010. The sensor chip was operated with its internal supply regulators and clock oscillator. The SpaceWire interface was used for telemetry and raw image download. No Latch Up was experienced. No SEU was seen on the POR block. No SEUs were seen during download of normal telemetry data. Some SEUs were seen in the output data during the sustained download of raw image data. These SEUs did not disrupt the sensor's operation and would not affect its use on board a S/C.

The SSoC breadboard with the prototype chip was tested using the SG testing facility (three axes rotating table and 1/100 Sun power collimated lamp for the Sun simulator).

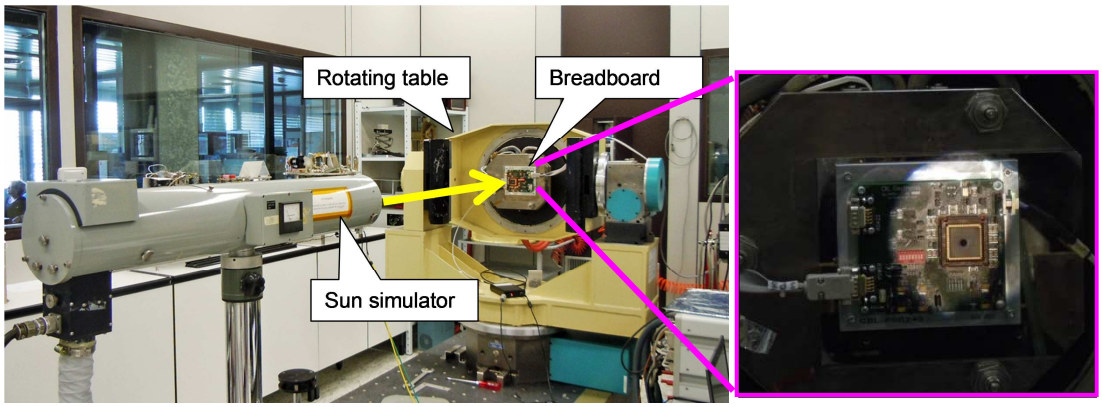


Figure 2.2-2 SSoC prototype on the testing facility

The accuracy was evaluated in terms of bias error and Noise Equivalent Angle (NEA). Different X,Y into α, β conversion methods were also tested, based on test data polynomial fitting or on the use of the inverse transfer function derived by the geometrical model of the sensor.
Prior to calibration the RMS bias error was ~0.5 deg in the whole FoV. These results were obtained using only the inverse transfer function with nominal geometrical and physical properties, i.e. without any dedicated characterization of each single flight unit. It was also demonstrated that bias error can be improved down to ~0.09 deg (approx 5.4 arcminutes) along α, β axes, by using an optimized equivalent focal length coming from characterization tests. Even better values can be achieved correcting the test results with a polynomial function of high order, and this will be further exploited in the next phases of the development.
The measured random error contributions are lower than 18 arcsec in terms of NEA and 14 arcsec in terms of high frequency error. However, this result is dominated by the aforementioned ADC defect and its resulting injection of static

and temporal noise. With a repaired ADC design the error is expected to be reduced to 3 arcsec.
An accurate study and optimization of the test setup, capable of minimizing the misalignments between the detector, the rotation axes and the Sun simulator is also expected to improve the measured bias.

Sensor functionalities were also tested in presence of the real Sun using a Neutral Density (ND) attenuation filter as shown in Figure 2.2-3. It autonomously recognized the Sun in the FoV and tracked it for the whole duration of the test execution (roughly 100 minutes).

Figure 2.2-3 Real Sun Test setup (left) - SSoC on the breadboard protected by ND filter (right

3 CONCLUSIONS

In the activities related to this contract (ESA Contract 21835/08/NL/ST) the industrial team composed by SELEX Galileo, CMOSIS and BAE Systems, with the support of Thales Alenia Space, implemented the design of a miniaturized prototype of a Sun sensor on chip.

The design involved the chip itself (with the on chip embedding of the FPA, all the logic, the voltage regulators, oscillator and SpW interface), the MEMS optics and its integration on the chip, a prototype packaging solution and the manufacturing of a mechanical housing to demonstrate assembly and integration concepts.

The first prototypes of the chip, including MEMS, were manufactured in 2010 and tested, at different levels, by the partners, demonstrating the feasibility of the project for use as a Sun sensor, even in a real Sun test demonstration.

Despite few issues highlighted during the prototype chip testing, which will need some fixes in the next prototype / product chips manufacturing and production, the results obtained so far are very promising, thus will be the basis for the future development of an EQM model.

An industrialization process will also follow the prototyping and on-ground qualification activities, to allow production and testing of several units at the same time, in order to reduce the recurrent cost.

The development activities done until now in the field of “sensors on-a-chip” have shown a way to combine all of the desired aspects of a Sun sensor (reliability, accuracy, albedo insensitivity, large FoV and low cost) in one unit with very low mass and suitable for use ‘as is’ on almost all missions. It is therefore expected that, upon the Sun Sensor “on-a-chip” development completion and on-ground/in-flight qualification, the Sun sensor market will change noticeably and these “on-a-chip” Sun sensors will become the dominant sensor.

Sun sensors are an essential part of a spacecraft AOCS for all missions. It is usual to find between 3 and 6 units per spacecraft.

As the Sun sensor requirements are often very similar among different missions and applications (in GEO or LEO, in Scientific or Earth Observation or Telecommunication space-crafts) and there is a keen market pressure on the recurring price, a miniature Sun sensor would fit most of the missions’ kinds and orbits, and thus should have a large sales volume (a proper target might be around 30 flight units per year), as long as the recurring price of the unit can be kept low.

The final target price will clearly depend strongly on the recurring cost of the detector itself, but in order to match the above mentioned sales expectation, it shall be kept low, in particular in the applications where a coarse accuracy Sun sensor would be sufficient (the largest share of the market in number of required flight units).

In fact, the coarse accuracy sensors market can be covered by this "on-a-chip" Sun sensor applying reduced calibration activities (a time consuming and thus cost impacting effort). This version of "on-a-chip" coarse Sun sensor, if confirms to be price competitive, will also offer the technical advantage of being a fully digital Sun sensor and to be insensitive, differently from other sensors in the same business segment, to albedo effects.

Table 2.2-1 summarizes the main results achieved on the SSoC prototype developed and tested so far and with the goals for the SSoC final product.

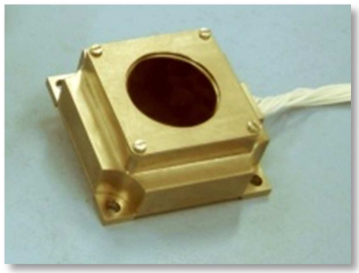
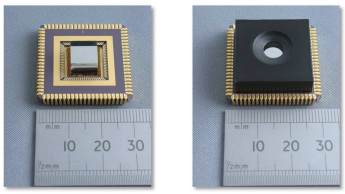
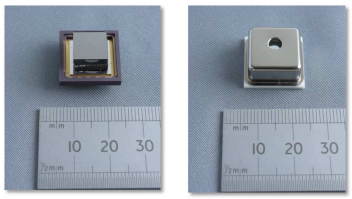
Physical characteristic	SSoC Prototype	SSoC Final product goal
Envelope (X, Y, Z)	(42, 45, 42) mm 	(40, 40, 30) mm
Total mass	53.25 gr measured on the mock up without off chip electronics	62 gr
APS Detector	512x512 10 µm	512x512 10 µm
Package	Commercial JLCC84 	Custom design 
FoV	±64 deg half cone	±64 deg half cone
Accuracy, bias error (1σ)	No calibration: 0.5 deg (whole FoV) 0.4 deg (α, β axes) Focal length calibration: 0.14 deg (whole FoV) 0.09 deg (α, β axes) 6th order polynomial on special case of one rotation angle only (ESTEC test): 0.03 deg (only Y axis)	No calibration: 0.5 deg (whole FoV) 0.4 deg (α, β axes) With dedicated calibration: 0.02 deg (whole FoV)
Accuracy, NEA (1σ)	< 18 arcsec	< 5 arcsec
Resolution	< 0.002 deg (1/128 pixel)	< 0.002 deg (1/128 pixel)
Power Consumption	186mW chip only with on-chip regulators and clock oscillator	< 200mW
Data I/F	SpaceWire UART I/F	SpaceWire UART I/F (option)

Table 2.2-1 SSoC product data sheet