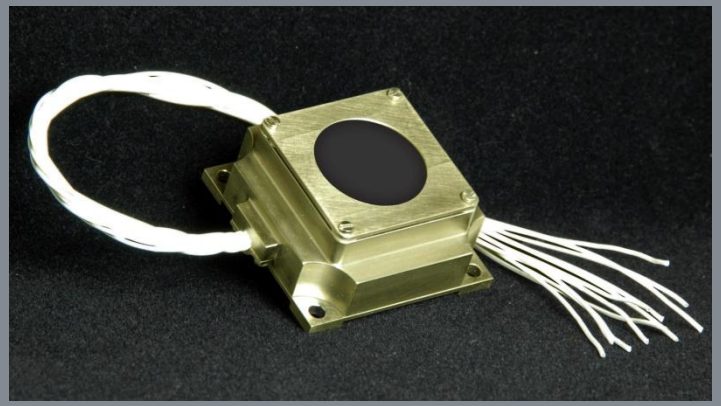
DIGITAL SUN SENSOR ON A CHIP PROTOTYPING
ESTEC CONTRACT 21835/08/NL/ST
FINAL REPORT



Final Presentation

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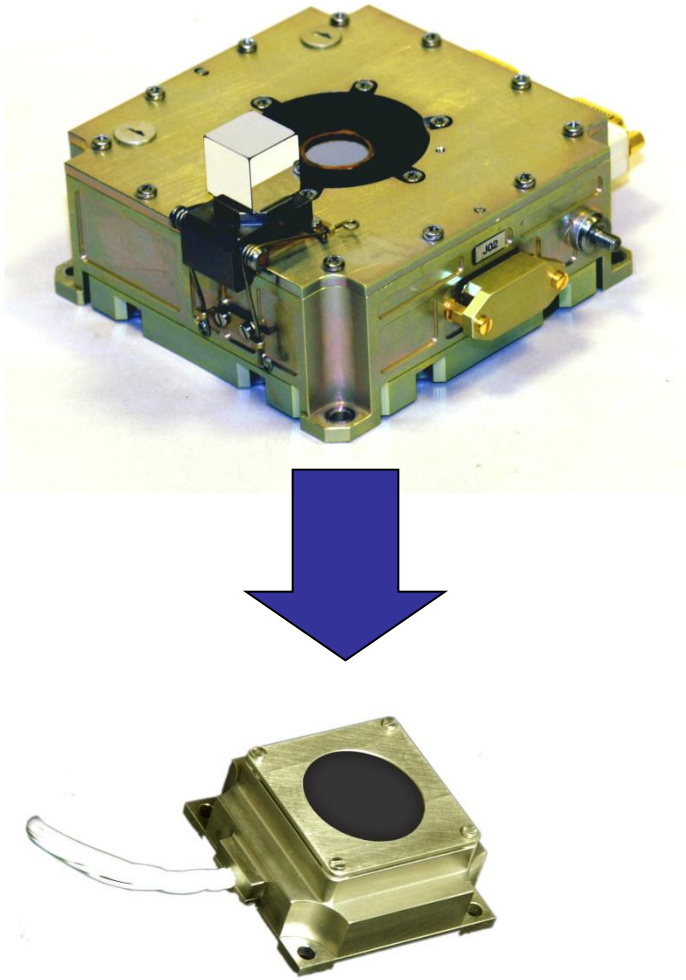
Contents

- **Contract Overview**
- **Design**
  - Optics & MEMS
  - Sensor Chip
  - Mechanical housing mockup
- **Characterisation test results**
  - MEMS optics
  - Final package mockup
  - Sensor Chip
- **Future Development**
- **Conclusion**



Contract Overview: the scope

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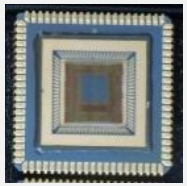
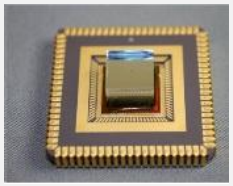
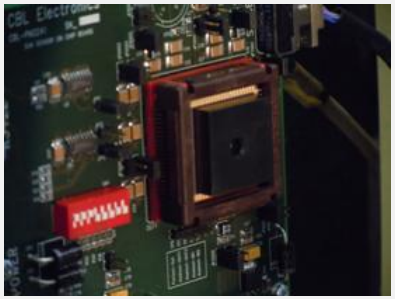
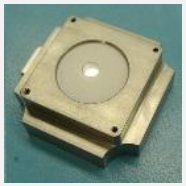
- Design and manufacture a SSoC detector chip with integrated MEMS optics at prototype level
- Produce a preliminary design of the final SSoC product with justification analysis and accuracy estimation
- De-risk, by test, challenging design topics like the custom package and pixel



SSoC: The Project Team

An industrial team led by SELEX Galileo (Italy), composed by CMOSIS (Belgium) and BAE Systems (UK) and with the support from Thales Alenia Space (France) expertise in AOCS, designed and developed a prototype of a miniaturized digital Sun Sensor on Chip

esa Contract 21835/08/NL/ST

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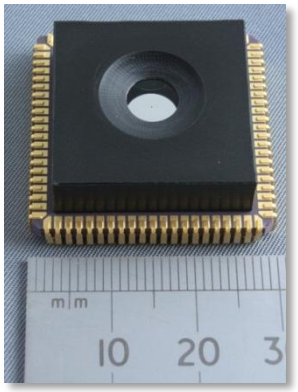
Long experience in attitude sensors

CMOSIS image sensors

Machine vision sensors

BAE SYSTEMS
Advanced Technology Centre

MEMS Technology



Low volume

Low mass

Low power consumption

ThalesAlenia Space
A Thales / Finmeccanica Company

AOCS expertise

Contract Overview: the key objective

- Implement the Digital Sun Sensor specification defined by Selex Galileo into a product that can be qualified, industrialised and that fits mass, dimensions, power consumption and cost of the final unit
- Design, manufacture, and characterize a Digital Sun Sensor chip Prototype using:
  - 0.18 micron process and true radiation hardness libraries and design
  - a System on Chip 512 x 512 pixel image sensor with 10-bitADCs, digital signal processor, SpaceWire and UART telecommand and telemetry interfaces, three linear voltage regulators for 3.3V and 1.8V, a clock oscillator, and LVDS transceivers
  - low dark current pinned diode pixel
  - 0.18 micron CMOS image sensor process (UMC) and true rad hard logic libraries
- Single chip Sun sensor design with integrated pin-hole and functional/performance verification
- Custom package design with verification of the main issues (sealing and pin hole layer bonding) by means of a mock up.

The pixels developed in this contract have been designed to be re-usable in a future single-chip star tracker, with the aim to de-risk future developments

Contract Overview: the main tasks

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- The contract was subdivided into two phases

- **Phase 1** - design
  - preliminary design of the final SSoC product with justification analysis and accuracy estimation
  - prototype chip design up to tape-out
  - electrical breadboard design

  The completion of phase1 was carried out with the DDR of the chip and the CDR of the sensor unit

- **Phase 2** - manufacture and test
  - the prototype chip
  - the electrical breadboard (functional representative of the final product)
  - mechanical demonstration model (mock up)
  - custom package mock up

  The completion of phase 2 was carried out with the TRB, including test results on the chip, pin hole, sensor performance and mock ups.

Contract Overview: programmatic history

ID	Description	Location	Contractual date	Actual Date
Phase 1				
KO	Kick Off	Teleconf	15.10.2008	15.10.2008
PM1	Progress meeting 1	CMOSIS	09.02.2009	23.02.2009
PM2	Progress meeting 2	Teleconf	10.04.2009	23.04.2009
DDR	Detector Design review Close out	CMOSIS	12.06.2009	12.10.2009 17.02.2010
CDR	Critical design review	SELEX Galileo	30.06.2009	02.12.2009
Phase 2	Following CCN003			
P2KO	Phase 2 Kick off	Teleconf	14.12.2009	02.12.2010
PM3	Progress meeting 3	BAES	31.03.2010	15.04.2010
TRR	Test Readiness review	Teleconf	3.05.2010	01.07.2010
TRM	Test Review meeting	SELEC Galileo	4.09.2010	16.11.2010

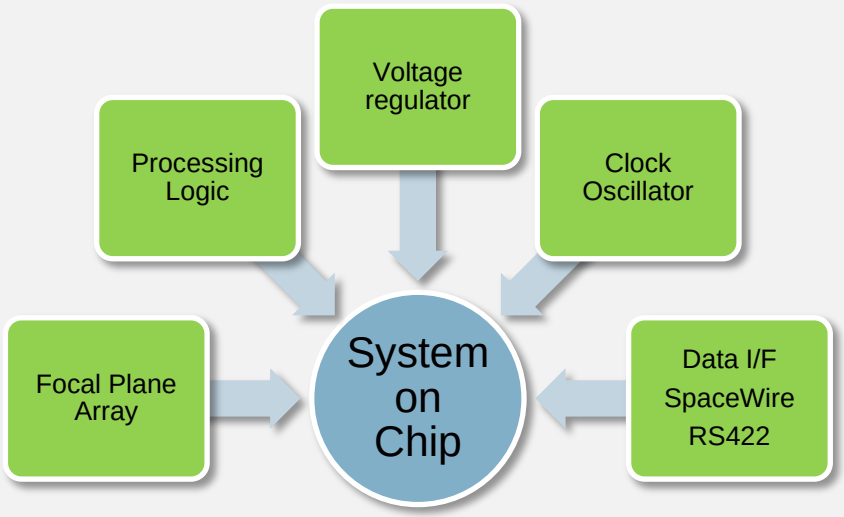
Contract Overview: Contract Change Notice

CCN004 is still running and results will be reported in a dedicated final report

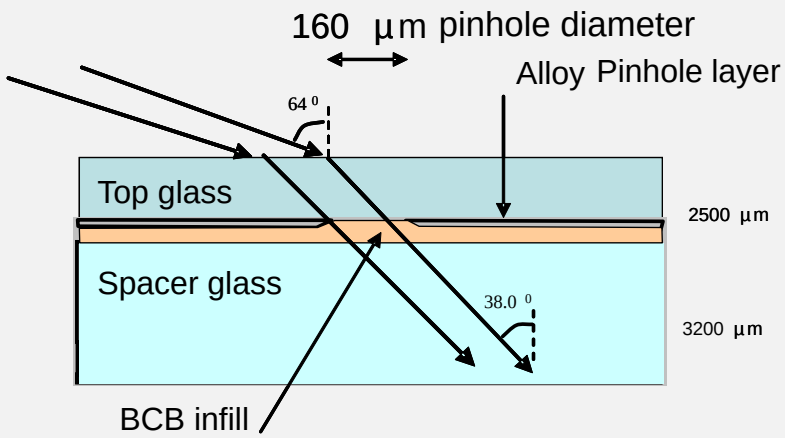
CCN	Title	Description
CCN001	SPACEWIRE IP	ESA authorize SG and CMOSIS to use the Space wire IP
CCN002	METAL SHIELD	Feasibility study, mock-up manufacturing and verification of possible solutions for the custom package. It includes verification on different sealing methods and connections of the pin hole layer to the package case.
CCN003	PHASE 2	ESA authorization to go on with the Phase 2 of the contract with the agreement on the phase 2 schedule. In this CCN radiation tests on pre-existing samples of 4T pixels.
CCN004	Rework and retest of Silicon	Additional activities for CMOS, repairing ADC bug and re-risking of pixels and Dc\Dc for star trackers.

Design concept

- Fully digital Sun sensor (X/Y output coordinates)
- “System on chip” philosophy
- Few off chip components
- Custom design package
- Robust mechanical housing for radiation hardening

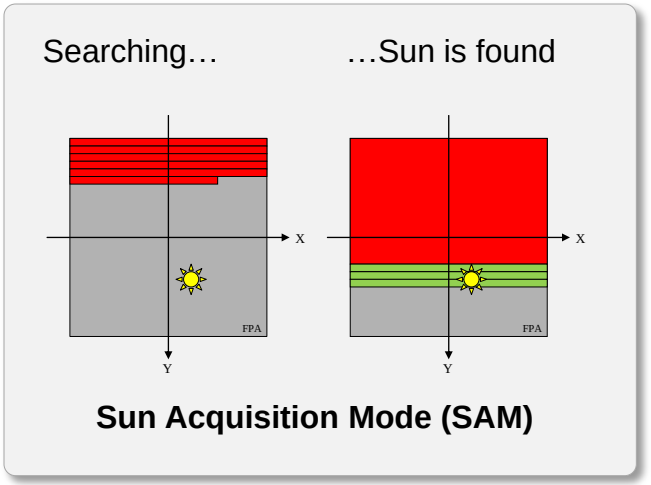


- Simple optics with pinhole
- Broad Field of View (64 deg half cone)
- Glass MEMS stack with integrated pinhole
- MEMS stack attached directly on the chip
- Aluminium alloy for pinhole layer
- Fused silica glasses bonded with BCB

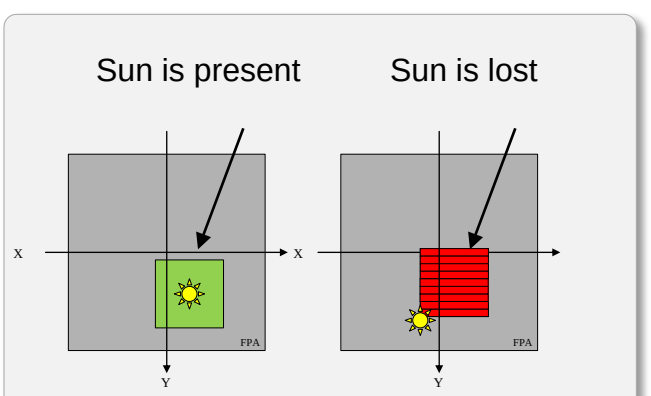


Sun detection and tracking

- Autonomous sensor with two main operating modes
- Automatic “power on to Sun tracking” transitions
  - Sun profile programmed in chip registers
- XY Sun coordinates calculated as Sun spot barycentre
- Sun Acquisition Mode (SAM), default at power on
  - Full frame reading (programmable, nominal 511x511)
  - Automatic transition when Sun is detected
- Sun Tracking Mode (STM)
  - Window reading (80x80 pixels, programmable)
  - Sun tracking with automatic window position update
  - Nominal cycle rate 10Hz (60Hz possible)
  - Automatic transition to SAM when Sun is lost
- Optional 8- or 10-bit full image download, at reduced rate



Sun Acquisition Mode (SAM)

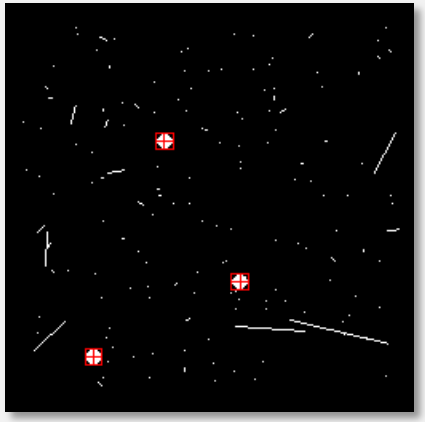


Sun Tracking Mode (STM)

Detector design /1

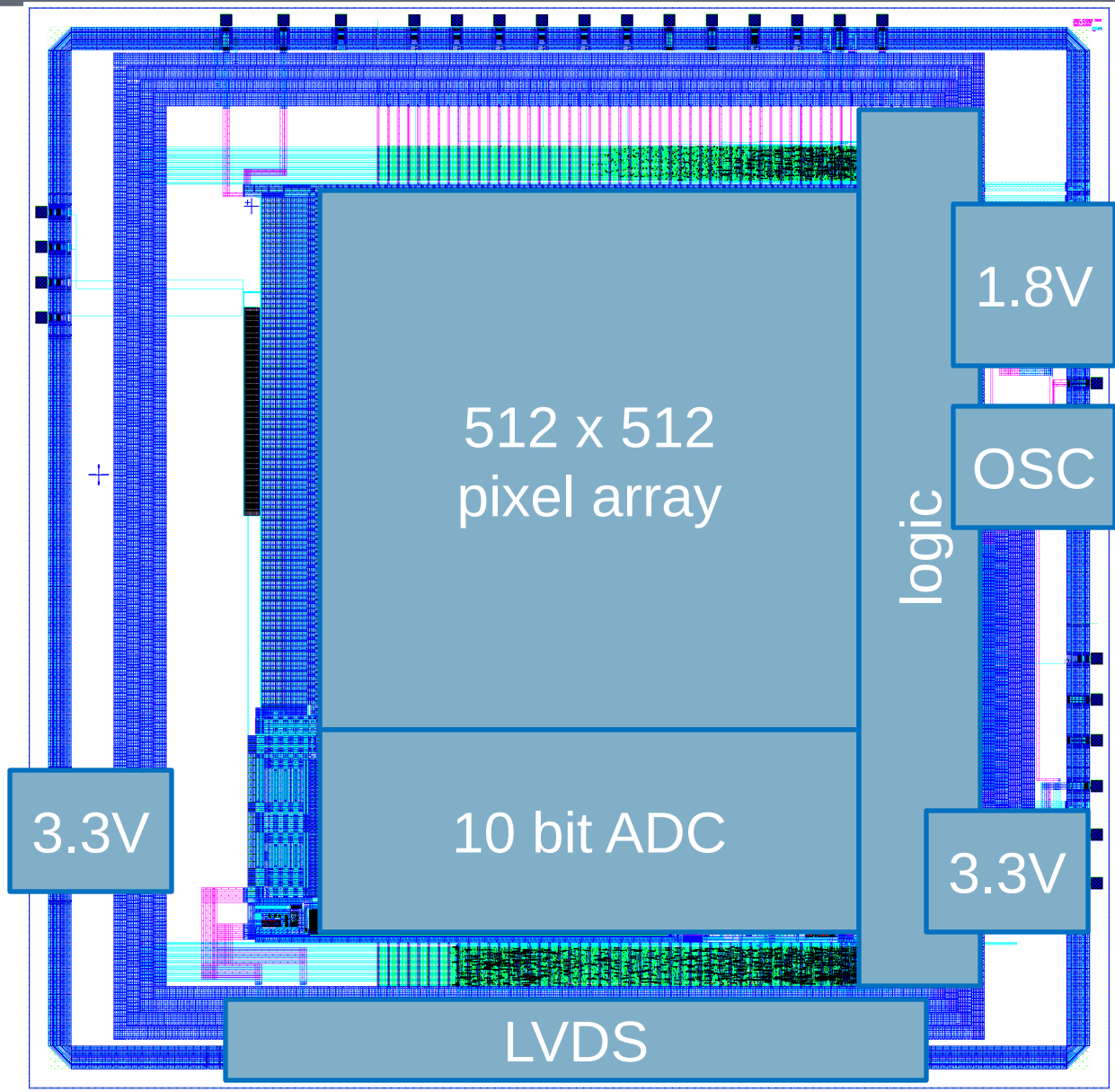
- Low-power design
  - Unused analogue blocks are dynamically switched off
  - Logic clocks are dynamically gated by actual image / data contents
- Performance
  - Designed to Sun sensor performances but with Star TRacker in mind (de-risk future developments)
  - Low-noise low-dark current buried diode pixels

- Robustness
  - Radiation
    - All hardened for gamma (layout techniques, IMEC DARE logic cell libraries)
    - All storage elements hardened against SEUs
      - HIT cells in DARE logic
      - Triple Mode Redundancy in ADC
  - Power supply
    - Voltage regulators designed for input voltages > 5.5V
  - Sun detection
    - Advanced image processing rejects non-sun objects
    - 2D clustering of sun image, photometric centroid



Detector design /2

- All functions embedded on the same chip
- Chip connects directly to S/C secondary supply
- Internal voltages generated by on chip regulators
- On chip oscillator for clocks
- SpaceWire interface with embedded LVDS drivers
- Off chip only needs
  - 5V supply
  - Quartz crystal
  - Few resistors and capacitors



Detector design /3

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- CMOS manufacturing process selection
  - Demand for radiation robustness > 300 krad called for radiation hard logic libraries.
  - IMEC DARE libraries only existed in UMC 0.18µ 1-poly-6-metal logic process
  - Process variant: UMC 0.18µ 2-poly-4-metal Image Sensor with pinned diode pixel
  - IMEC ported subset of DARE rad-hard logic libraries to this process
    - ESA contract 20896/07/NL/JD
  - However ...
    - CMOSIS lacked all experience in this process.
    - This posed a considerable risk

Detector design /4

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- Challenges
  - Pixels, electro-optical performance
    - Commercial 180 nm image sensor processes are optimised for ‘small’ pixels (mega-pixel race).
    - Sun Sensor pixel size = 10 µm, ‘large’.
    - Hard to predict (and design for) dark current, full well, image lag, yield, ...
    - Poor foundry support for low-volume projects.
    - Normally such risks are controlled through a preparatory experimental phase with a pixel test chip and full process characterisation.
    - This phase was skipped (budget, schedule!).
    - Fueled by (misplaced?) optimism.

Detector design /5

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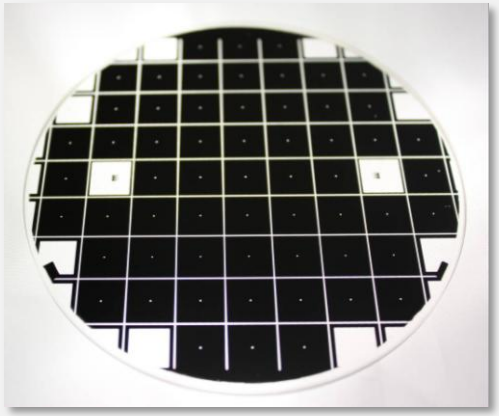
- Challenges (cont'd)
  - Analogue
    - All-new circuits in new process.
    - Entirely untried 10-bit column ADC architecture.
    - First-time clock oscilllator.
    - First-time voltage regulators.

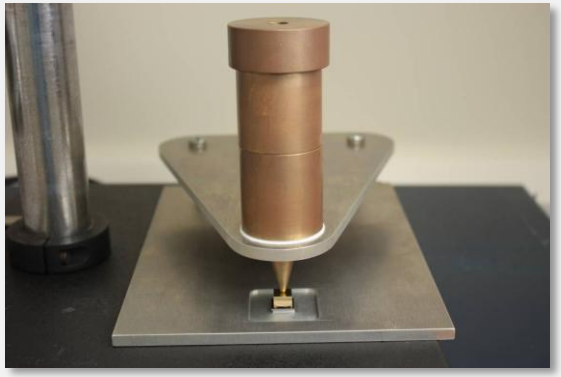
- Attempt at risk control
  - Two pixel variants: normal + rad-hard by layout
  - 3 or 4 manufacturing runs planned, each with 2 or 3 process splits (implant variations)
  - This led to a lot of characterisation work
    - This is actually still on going, under CCN4
    - Devices with optimal Electro-Optical performance will only be demonstrated by the end of 2012
    - Devices available now are good enough for sun sensor duties

Optical stack fabrication and integration

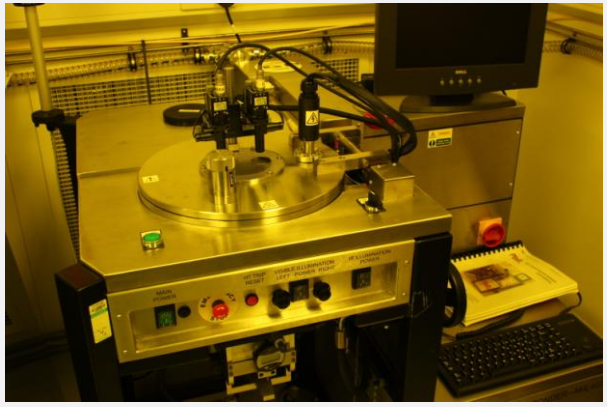
- Optical chip, glass + pinhole + glass fabricated on wafer scale
- Chip-scale integration for the prototype chip: optical chips sawn in individual pieces and bonded on already packaged sensor chips
- Wafer-scale integration for the product chip: optical chips will be aligned and bonded on the silicon wafer and then sawn and packaged



Wafer of pinhole chips, pitched to match CMOSIS wafer 44 chips/wafer



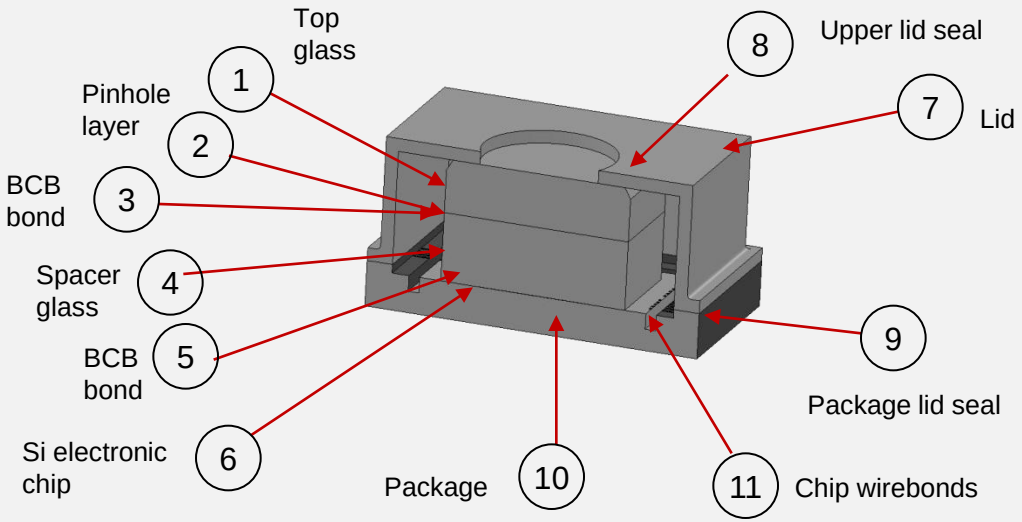
Interim Bonding jig for chip-scale bonding (bonded in vacuum chamber)



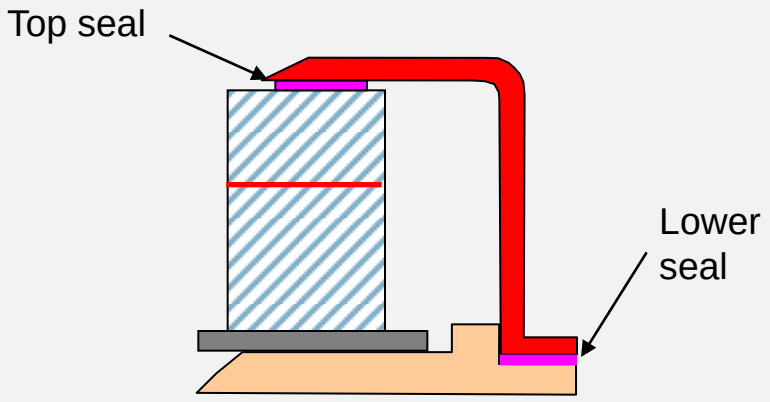
Equipment for wafer scale bonding

Custom package prototyping

- Models have been constructed with:
  - CMOSIS APS chip
  - Optical pinhole chips
  - Mock-up ceramic package
  - Stock lid
  - Additional radiation shield



- Package hermetically sealed (filled with inert gas, Ar or N)
- Conventional package seal at lower
- Additional seal at the top around the optical entrance pupil



Packaging and cover lid

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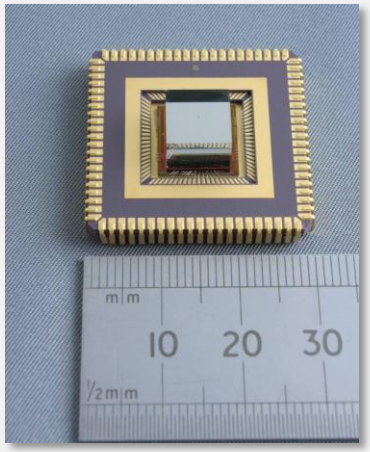
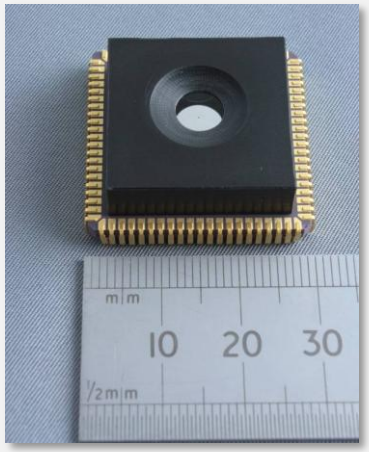
Standard (commercial) package

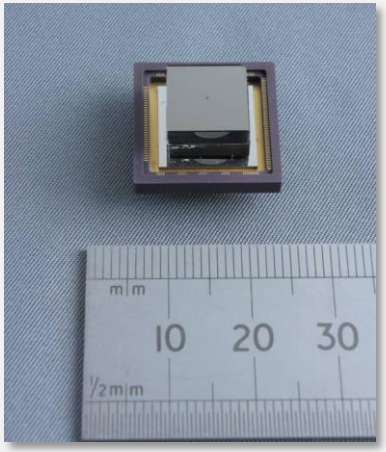


Integrated pinhole
and packaged sensor



Chip with covering lid

Custom package mockup



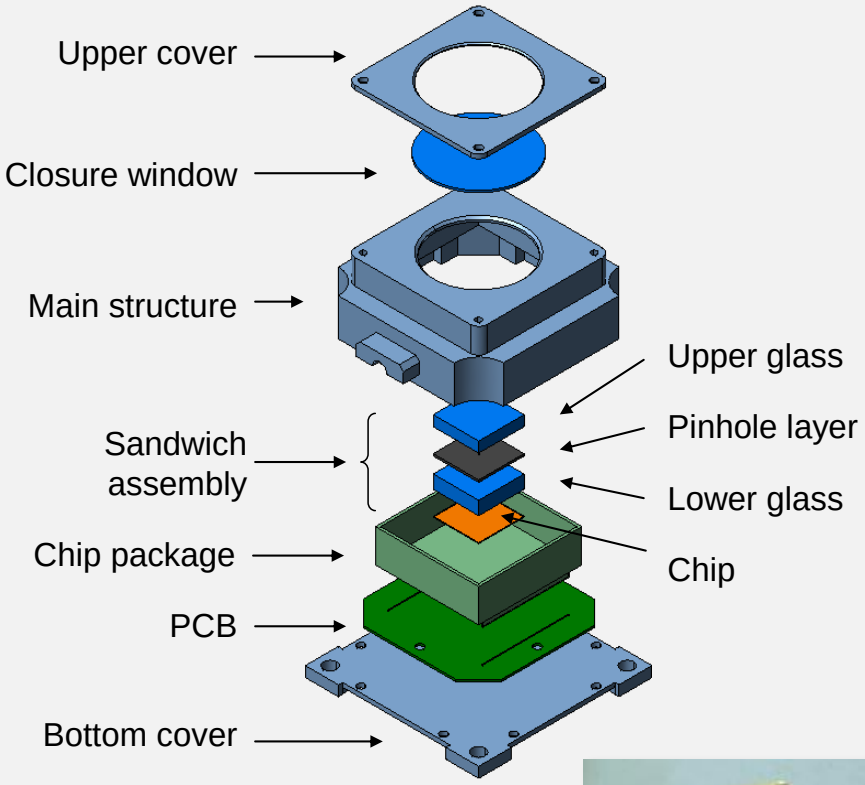
Optical chip integrated in
representative package

Mock-up package with
lid for sealing tests

- Standard (larger) commercial JLCC84 package for prototype chips
- A custom package will be designed for the final product chips → package size shrinking
- Dedicated metallic lid will provide protection from spurious light and radiation shield

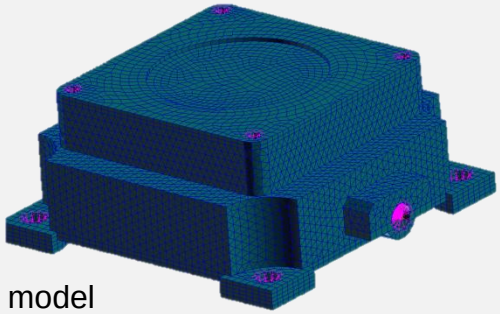
Mechanical housing design

- Main structure in Titanium alloy to offer better radiation shielding
- Compact size (~40mm cube)
- Four fixation screws
- Pigtail or miniaturized connector
- Optical glass attached to the bottom of the housing
- Ease of chip mounting and aligning
- An attenuation filter can be tailored to the mission needs
- Tiny PCB to host the few off chip components



Structural analyses

- A structural analysis of the SSoC preliminary mechanical design was carried out in terms of: free-free dynamic analysis, modal analysis, static stress analysis
- The structure presents a first natural frequency of 4070 Hz
- A Static stress analysis was performed with equivalent 26 grms PSD spectra resulting in positive Margins of Safety for the yield and ultimate stresses.



FEM model

- The thermo elastic analysis (hot and cold cases) has shown that the displacement and rotation of the package of the chip are negligible. However, the thermo elastic behaviour of the chip/pinhole itself has to be assessed with the final mechanical design of the package
- Combination of wall thickness, use of Titanium and Kovar custom package allows adequate radiation shielding to the whole chip also at GEO for 18 years mission lifetime

Thermal analysis

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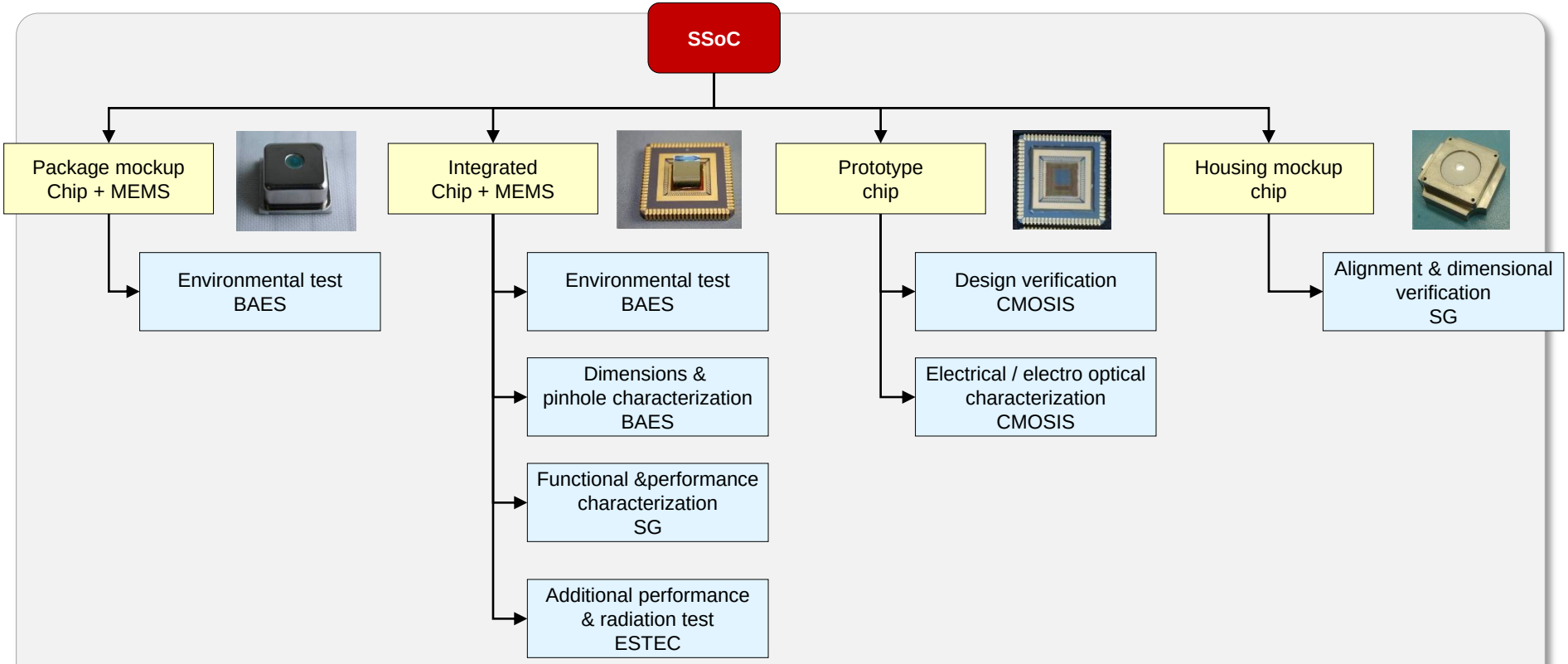
- Thermal analysis was performed assuming a qualification temp. range of -40 °C / +85 °C
- Three different thermal finishing of the housing has been considered:
  - Polished Titanium
  - VDA Kapton Tape
  - Secondary Surface Mirrors (SSM)
- In the case of isolation from the base plate the storage cold temperature must be lowered to -65 °C to allow withstanding the hibernation case (base plate at –55 °C, no Sun)
- VDA Kapton configuration with a conduction path to the spacecraft brings the minimum and maximum temperatures within storage limits of the chip even if with low margin

Test campaign



- Different items tested by SG, CMOSIS & BAES, to:
  - Prove the design concept
  - Validate the prototype manufacturing process
  - Demonstrate chip integration in the mechanical housing
  - Have a first estimate of the overall accuracy
- Additional tests performed by ESTEC to:
  - Verify additional configuration and operating modes
  - Characterize TID behaviour

Testing on packaging and optics MEMS stack

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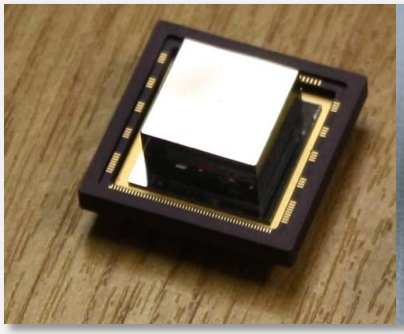
- Custom package mockup and glass MEMS stack submitted to environmental tests as per common MIL-STD standards:
  - Thermal cycling (-65°C / +120°C), vibration, rapid decompression, thermal shock, fine & gross leak, RGA
- Different cover lid to package and chip sealing variants tested:
  - Epoxy seal
  - Silicone seal
  - Soldering seal
- Final selection of the sealing method will be done in the follow on contract

Test samples

Package mockups



Glass dummy integration and dimensional check

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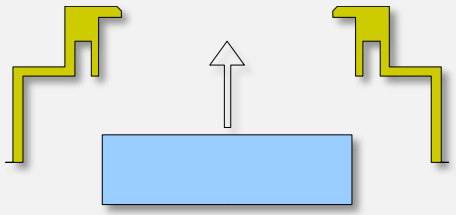
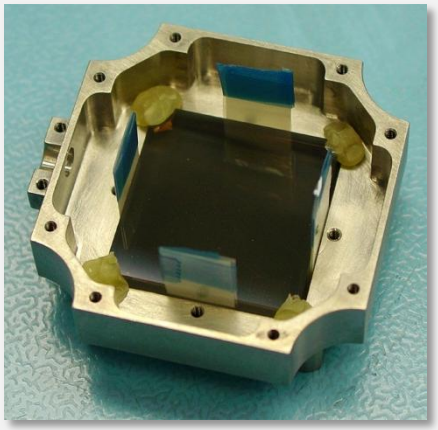
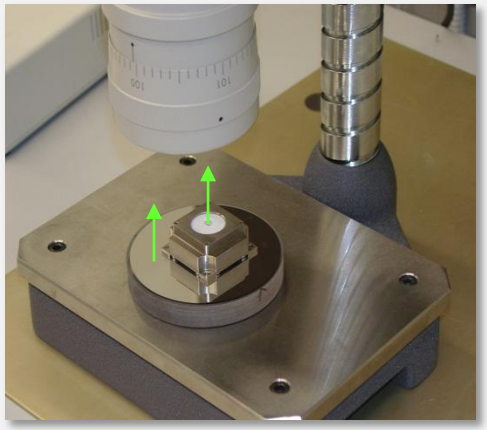
- Mass inline with expected mass budget
- Optical stack dummy attached to the top cover of the mechanical housing
- Easy glass dummy mounting process: no dedicated tool/fixtures
- Pinhole layer is reflective, can be used for alignment measurement
- Good parallelism (1.5') pinhole layer / mounting feet with no dedicated procedures
- Process will be maintained ad optimized to reduce / eliminate time consuming alignments



Chip + MEMS attachment concept



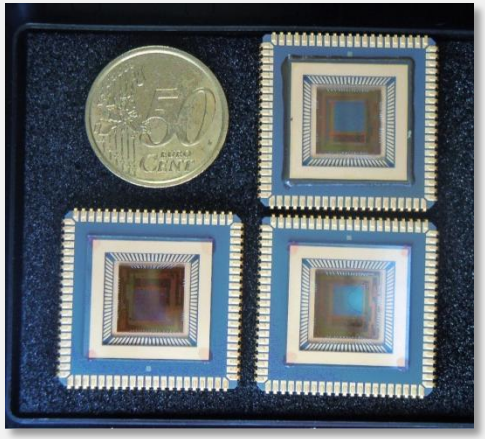
Glass dummy inside the mechanical housing



Alignment with autocollimator

Tests on Detector Chip

- Sensor chip is functional and can reliably be demonstrated
  - Image sensor
  - ADC
  - Control and processing logic
  - Regulators, power-on-reset, oscillator



Prototype sensor chip in standard package

- Issues, non-lethal
  - Bug in ADC
    - Halves input signal range
    - Causes crosstalk: PRNU, FPN, temporal noise
    - All unit tests were done with these additional noise sources
  - Excessive variance of voltage regulator output
  - Temperature sensor drifts under gamma radiation
  - Aspects of Electro-Optical performance need to be improved
    - But presently good enough for sun sensor

Tests on Detector Chip /2

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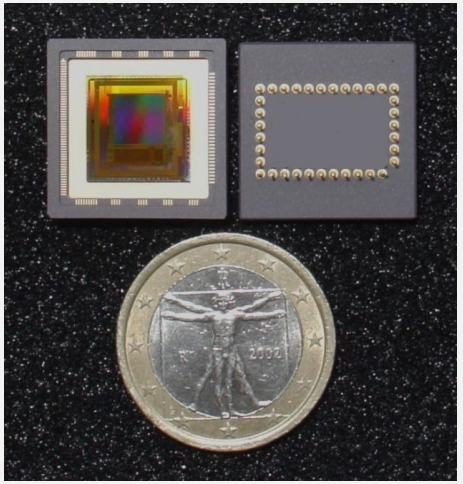
- Sensor chip is robust
  - Selective sun image processing works
  - Tracks up to 100°/s (600°/s in special mode)
  - No SEL or SEU in normal use
    - LET 67 MeV/(mg/cm^2), 15000 part./(s.cm^2)
    - LET 121 MeV /(mg/cm^2), 7500 part./(s.cm^2)
  - Supply short-term tolerant to 6.7V
  - ESD > 1800V HBM (most pins tolerate 3000V)
  - TID test by ESTEC, up to 300 kRad
  - (Proton testing deferred due to insufficient EO performance)



Mock-up of sensor chip in proposed custom µPGA package

- Sensor chip is small and with low power consumption
  - Die size < 12 x 12 mm
  - Power (design goal: < 200 mW)
    - < 186 mW at 5 V with SpaceWire/LVDS (123 mW at 3.3V)
    - < 91 mW at 5V with UART/CMOS (60 mW at 3.3V)

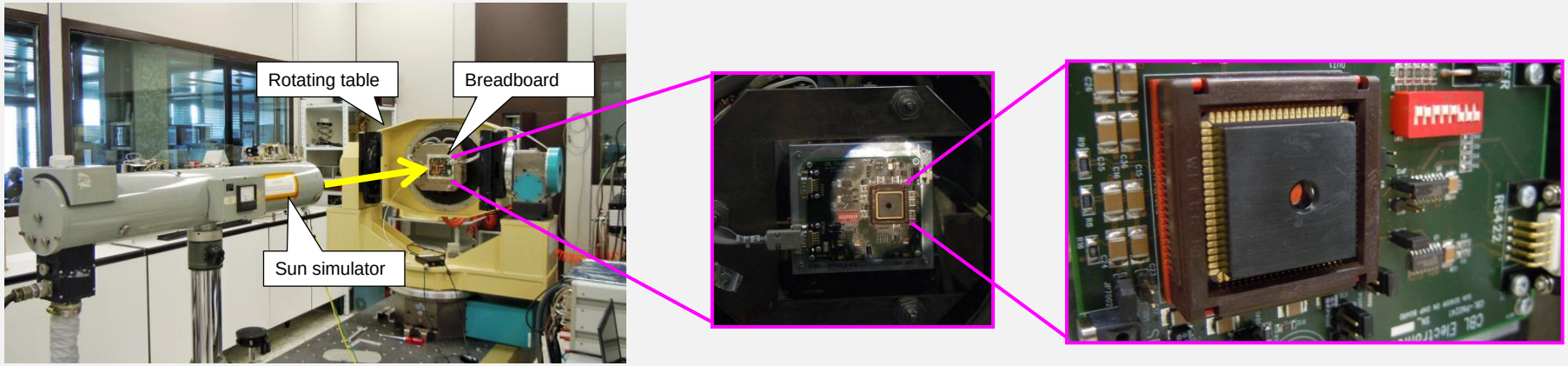
Tests on Detector Chip /3

		target	measured	
QE x FF	%	> 45	47	averaged 400-700 nm
full well charge	ke-	> 100	50-120	
read noise	e-	< 100	88	
dark current	e-/s	< 150	100-6600	RT, BOL
FPN	e-	< 50	195	(harmed by ADC bug)

- Presently no pixel + process combination that combines:
  - low dark current
  - high full well charge
  - acceptable yield
- These are required for star tracker applications.
- CMOSIS continues pixel development in CCN4 and internally-funded development.

Prototype Sun Sensing accuracy testing

- Packaged chip + MEMS mounted on a dedicated breadboard for testing purposes
- Chip protected by cover lid to prevent straylight effects

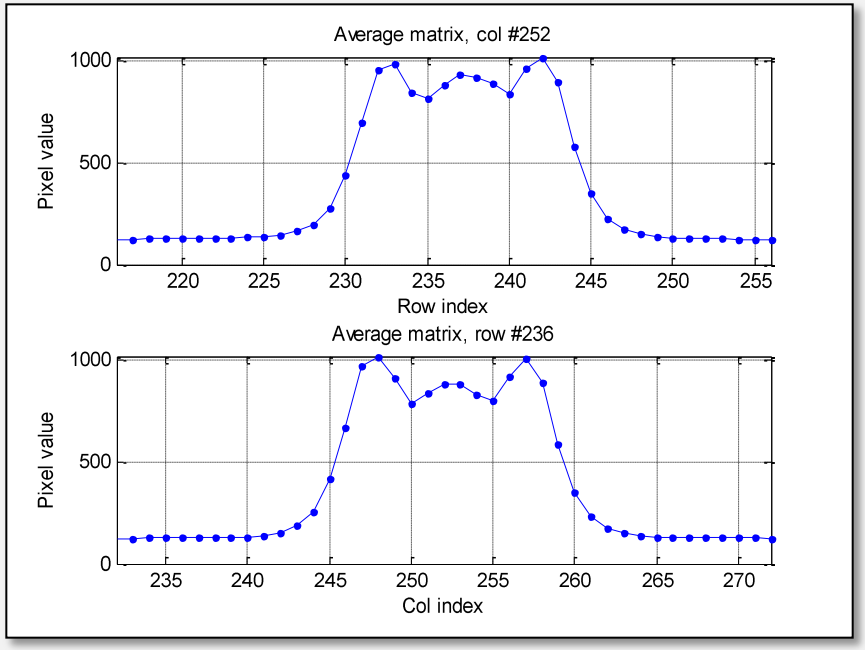


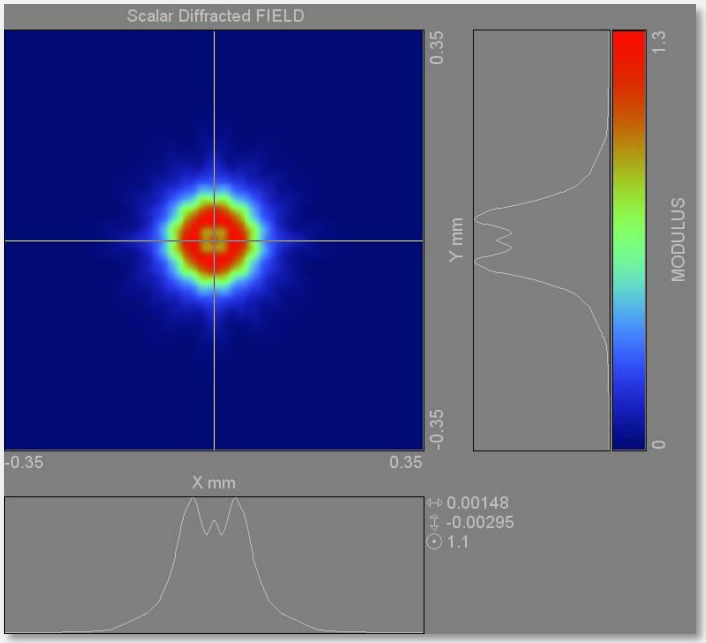
- Measured NEA within 18 arcsec
- Prior to any dedicated calibration measured bias 0.5 deg in the whole FOV, and 0.4 deg on α, β axes
- A simple focal length calibration reduces the measured bias to 0.14 deg (whole FOV) and 0.09 deg on α, β axes (5.4 arc minutes)
- Use of more complex formulas (i.e. high order polynomial) will reduce the measured bias error, to be investigated in a follow on contract

Prototype Sun spot shape verification

- Peak / valley behaviour confirmed by simulation (depending on the ratio between pinhole diameter and distance from the detector)

- Simulation details:
  - Collimated in axis source at 0.8 μm wavelength
  - 160 μm pinhole





Prototype Real Sun Test

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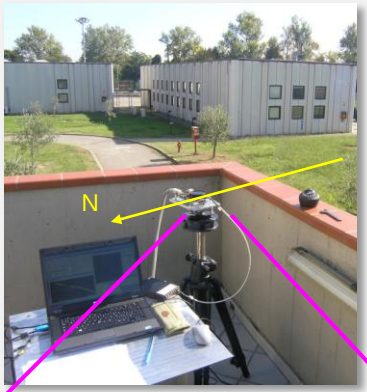
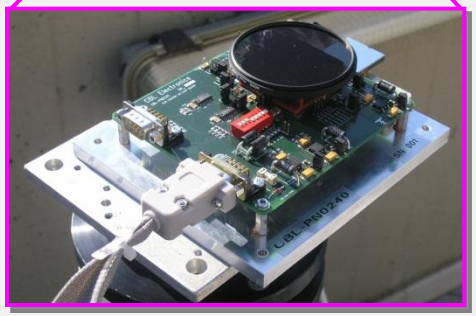
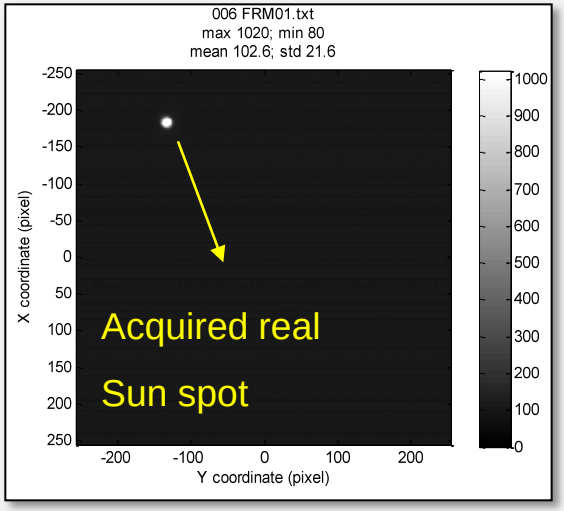
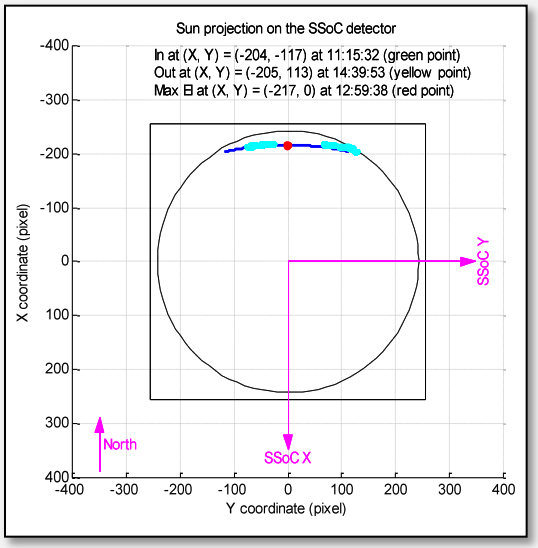
- Sensor tested in a real Sun scenario for qualitative check
- Use of attenuation filter to avoid signal saturation
- Sun acquired and tracked for ~100 minutes
- Good match expected vs measured Sun positions
- Random error 20÷25 arcsec



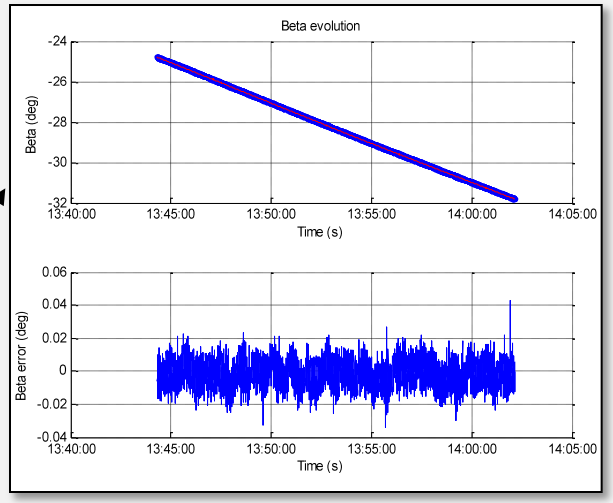






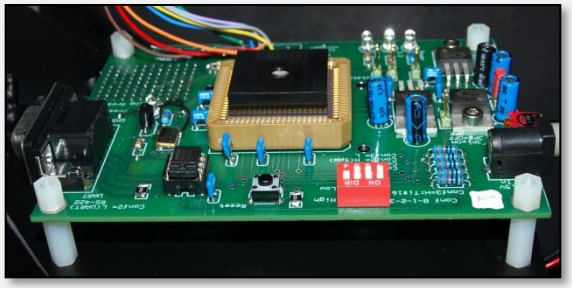
Measured β time evolution

Random error

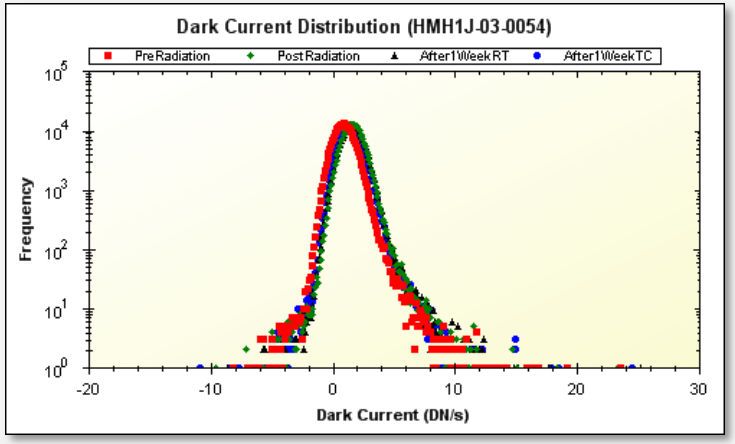


Additional tests at ESTEC

- Cross check of industrial results (noise, bias)
- Verify particular configurations and conditions not tested by the industry for schedule/cost constraints (e.g. high speed rotation)
- TID testing



- Test setup:
  - 1-axis rotating table
  - Dedicated breadboard
  - Sun simulator (Xenon Lamp)

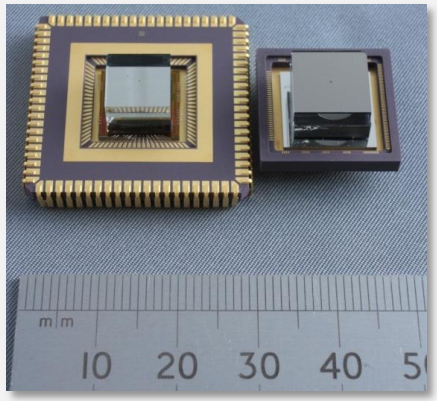


- Main results:
  - NEA < 10 arcsec
  - Bias ~2 arcmin (6th order polynomial fit, 1 axis only rotation)
  - Sun detection & Tracking up to 220 deg/second
  - Components survived and working after 300kRad TID
  - No appreciable dark current evolution (different pixel variants and TID level)

Way forward

- Contract extension (CCN4) for additional foundry spins
  - Full pixel performance, suitable also for future star tracker on chip development
  - Full characterisation, including protons
  - Repair of bug in ADC, re-spin
  - Feasibility study of DC\DC converter for future STRs

- Work planned in future development steps (EQM development)
  - Incorporation of all learning from prototype
  - Downsizing of the die
  - Off chip components configuration definition
  - Manufacturing of EQM sensor chip
  - Evaluation / qualification
  - Wafer scale optical chip process optimization
  - Full custom package design, including bonding and wire bonding methods
  - Investigation of calibration methods for direct α, β Sun angle output
  - Optimization of mounting and alignment processes at unit level to reduce AIT cost



Standard vs custom package

Summary of key results vs SSoC goals

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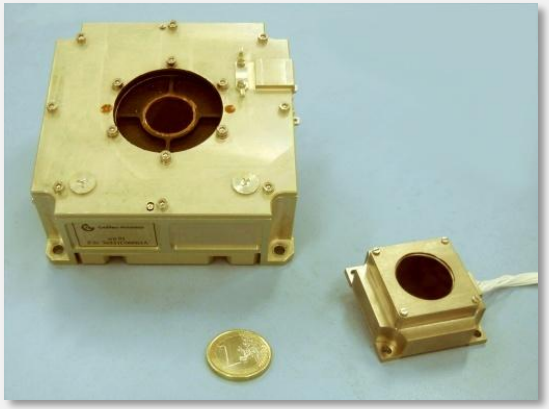
Physical characteristic	Standard SG Sun Sensor (SSS)	SSoC Prototype	SSoC Final product goal
Envelope (X, Y, Z)	(112, 110, 43) mm	(42, 45, 42) mm	(40, 40, 30) mm
Total mass	< 400gr	53.25gr measured on the mock up without off chip electronics	62 gr
APS Detector	1024x1024 15 µm	512x512 10 µm	512x512 10 µm
FOV	64 deg half cone	64 deg half cone	64 deg half cone
Accuracy, bias error (1σ)	Simple calibration 0.08 deg (whole FOV) 0.01 deg (10 deg FOV) Iterative calibration 0.02 deg (whole FOV) 0.01 deg (30 deg FOV)	No calibration: 0.5 deg (whole FOV) 0.4 deg (α, β axes) Focal length calibration: 0.14 deg (whole FOV) 0.09 deg (α, β axes)	No calibration: 0.5 deg (whole FOV) 0.4 deg (α, β axes) With dedicated calibration: 0.02 deg (whole FOV)
Accuracy, NEA (1σ)	< 15 arcsec	< 18 arcsec	< 5 arcsec
Resolution	< 0.003 deg (1/64 pixel)	< 0.002 deg (1/128 pixel)	< 0.002 deg (1/128 pixel)
Power Consumption	< 1.5 W	186mW chip only with on-chip regulators and clock oscillator	< 200mW
Data I/F	Serial Digital I/F	SpaceWire UART I/F	SpaceWire UART I/F (option)

Conclusions

- Digital Sun Sensor on Chip designed and developed
- **Challenging** design goals and specifications
- First prototype chips manufactured
- Sensor is **fully working**
- Prototype performances promising to meet **design goals**
- Coarse version with no dedicated calibration
- Accurate version with dedicated calibration
- Good **market perspectives**
- EQM ITT to be issued by ESA
- Full **qualification** in 2.5 years



SSoC comapared with current SELEX Galileo Sun Sensor