QUEENS2:EXECUTIVE SUMMARY REPORT

QUEENS2

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1. INTRODUCTION

1.1. PURPOSE

This document summarises the methodology and results obtained within the frame of the ***ESA Contract Nr. 4000128041/19/NL/AR/va "Quality Assessment of the New European Large BRA VE FPGA Software Tools (Queens)"***

1.2. SCOPE

Summary of the methodology and results developed in QUEENS2.

1.3. DEFINITIONS AND ACRONYMS

1.3.1. DEFINITIONS

Concepts and terms used in this document and needing a definition are included in the following table:

Table 1-1 Definitions

Concept / Term	Definition

1.3.2. ACRONYMS

Acronyms used in this document and needing a definition are included in the following table:

Table 1-2 Acronyms

Acronym	Definition
DFF	Flip-flop type D
DSP	Digital Signal Processor
CY	Carry
EDA	Electronic Design Automation (tools)
ESA	European Space Agency
FPGA	Field-Programmable Gate Array
GUI	Graphical User Interface
HW	Hardware
HDL	HW Description Language(s)
IP	Image processing
LE	Logic Element
LUT	Look-up Table
N/R	Not Reported
QUEENS-FPGA	QUality Evaluation of European New SW for brave FPGA
RAM	Random access memory
RAMB	RAM Block
RFB	Register File Block
SDF	Standard Delay Format
SPR	Software problem report
SW	Software
VHDL	VHSIC Hardware Description Language

2. REFERENCES

2.1. APPLICABLE DOCUMENTS

The following documents, of the exact issue shown, form part of this document to the extent specified herein. Applicable documents are those referenced in the Contract or approved by the Approval Authority. They are referenced in this document in the form [AD.x]:

Table 2-1 Applicable Documents

Ref.	Title	Code	Version	Date
[AD.1]				

2.2. REFERENCE DOCUMENTS

The following documents, although not part of this document, amplify or clarify its contents. Reference documents are those not applicable and referenced within this document. They are referenced in this document in the form [RD.x]:

Table 2-2 Reference Documents

Ref.	Title	Code	Version	Date
[RD.1]				

3. CONTEXT AND OVERVIEW

QUEENS2 project develops in the frame of the evaluation of the new European Space Qualified SRAM based BRAVE FPGAs. The main objective of this project is the evaluation of the BRAVE FPGA devices and tools (NG-LARGE and NXmap).

Due to the lack of methodologies and procedures to assess the Quality of FPGAs and its implementation tools, the consortium have proposed an assessment methodology based on benchmarking. This methodology is inherited from QUEENS1 project and updated and improvement with the lessons learnt during the previous project.

The methodology defines different metrics to be assessed during each step of the FPGA implementation flow (synthesis, place and route, netlist simulation and bitstream generation) and an objective assessment criteria based on comparison with equivalent competitors devices.

The election of the reference devices have been performed taking into account not only equivalent capabilities and FPGAs technologies, but also and more important the context of the study, Space Qualified FPGAs.

In addition to the reference devices different subsets of benchmarking circuits have been selected, from low complexity circuits to high complexity and large designs. Low complexity circuits are mandatory to assess the principal features of the implementation tools and find background errors in an easy way. On contrast high complexity designs are used to stress the EDA tool as maximum and, in this way, assess the ability of the tool to finalize the implementation of large designs and the optimization capabilities. High complexity circuits have been selected through am exhaustive trade-off of different real case designs widely used for image processing and vision based navigation systems. The selected circuits have in common the following features:

- Allocation of high percentage of the FPGA resources
- Use all type of NG-LARGE components (NRAMs, DSPs, RFBs, etc)
- High complexity
- Generic design (non-technology dependent designs)
- Easily scalable for NG-LARGE device
- Real case circuits
- Useful for demonstrations

Synthesis, place and route, interfacing with third party simulation tools and bitstream generation have been the main capabilities related with the implementation tool assessed during QUEENS2 project. In relation with the hardware, the correct behavior of the physical components inside NG-LARGE and the power consumption of the FPGA have been assessed. However, other secondary capabilities as the quality of the generated reports, the suitability of the user application interface, the user friendly graphical user interface or the quality of the user manuals have been assessed.

NXmap is a new EDA tool over continuous improvement. As a result, new versions of the tool have been released during the activity. In order to test all releases and the improvement of the tool, systematics regression tests have been performed during the whole project for synthesis, place and route and bitstream generation.

To conclude, a project and release control tool has been made available to QUEENS2 project by GMV. This tool allows the different members of the consortium to upload the SPRs (Software Problem Reports) found during the assessment of the tool in a methodical and organized manner. SPRs allows the developers of the EDA tool to discover and solve new problems in the tool without internal testing.

4. ACTIVITY SUMMARY

QUEENS2 is an 18 months duration project, during this time the consortium have relied on the consultancy and support of NanoXplore and have performed the activities described in the work packages of Figure 4-1.

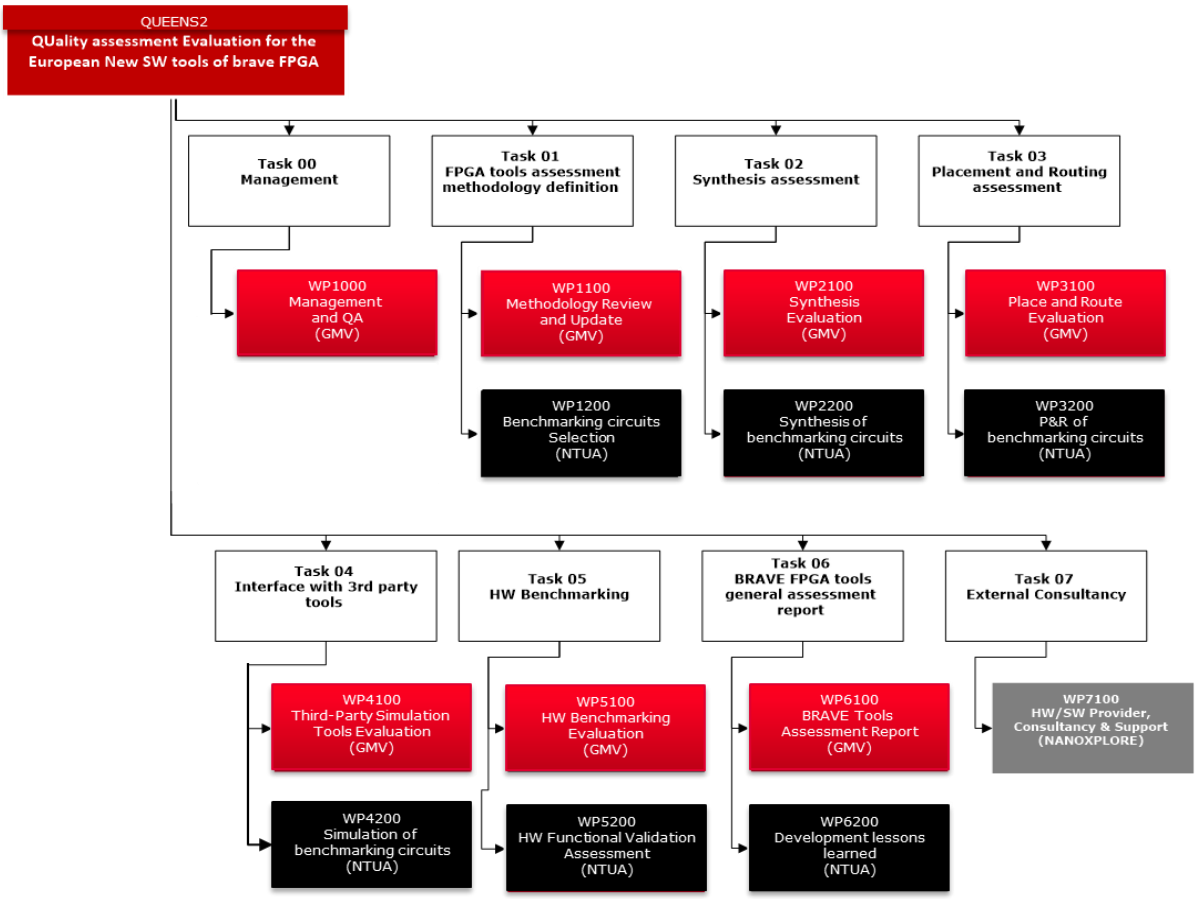

Figure 4-1: QUEENS2 Work Packages

The first work package is related with the review of the assessment methodology used in QUEENS1 project. During this activity the consortium has updated the assessment methodology with the lessons learnt during the precious project and the new capabilities of NG-LARGE FPGA. In addition, the final version of the technical note 1 (BRAVE FPGA Tool Quality Assessment Methodology) delivery at finalization of the project is updated with the lessons learnt during the current project and serves as a starting point for future BRAVE devices/tools evaluation. This activities also includes the selection of the different benchmarking circuits and FPGAs.

In the second work packages the consortium have assessed the synthesis capabilities of the implementation tool. This activities includes the benchmarking through the different complexity circuits, but also the evaluation some capabilities of the tool as the correct implementation of the synthesis options, the ability to perform an efficient mapping of NG-LARGE components and the ability of the tool to understand different syntaxes or HDL coding techniques.

The next step in the FPGA implementation flow is Place and Route. In the third work package the benchmarking is repeated for place and route step. It is important to notice that metrics for synthesis and place and route are significantly different (e.g. in synthesis the total number of allocated flip-flops, which is a non-architecture dependant metric is evaluated. However in Place and Route, in addition to the number of flip-flops, the number of Logic elements, which is an architecture dependant metric, is also assessed. Other specific metrics close related with place and route, as maximum clock frequency achieved for each circuit, is assessed in this benchmark). The correct implementation of place and route options and mapping directives, the ability of the tool to reduce the places resources, the ability of the tool to perform an efficient routing achieving the maximum clock frequency and the ability of the tool to finalize the implementation of large and complex designs is evaluated in addition to the benchmarking.

EDA tools should be able to generate understandable netlists for simulation tools. This netlist, in combination with the simulation libraries provided by the implementation tool for a specific device (NG-LARGE), makes the interfaces with third party simulation tools. In the fourth work package the generation of post synthesis, post place and post route netlist are assessed. In addition, a functional verification of each primitive inside the NG-LARGE simulation library have been performed. To conclude, the timing information included on Standard Delay Format (SDF) files is assessed and compare with the timing information provided by the Static Timing Analyser (STA) of the tool. The correct behaviour of the netlist generated for the benchmarking circuits have been also verified trough simulation.

The last step of the implementation flow is the functional verification of the designs on the hardware (NG-LARGE). In the fifth work package the correct functioning of the benchmarking circuits on NG-LARGE has been assessed. I addition, a more deep inspection of each of the physical component on NG-LARGE FPGA has been performed through unitary and general test. This evaluation implies the evaluation of the correct bitstream generation. Power consumption benchmarking is also assessed in this activity.

To conclude all this information have been collected, joined and interpreted to perform a general assessment of NG-LARGE FPGA and its implementation tool, NXmap.

5. CONCLUSIONS

QUEENS2 project is not only the assessment of an FPGA and its implementation tools, but also the evaluation of a new standard for FPGA assessment methodology. During QUEENS2 this methodology have been reviewed and improved. The following conclusions related with the assessment methodology are described below:

- The consortium realize the great importance of the low complexity designs to find and solve fundamental problems on the tool. More than 60% of the SPRs uploaded during synthesis and placed and route assessment correspond to low complexity circuits.
- Even when some EDA tool can present a wider set of configuration options, it is important to choose this options correctly in order to perform an objective comparison between tools.
- It is really important to have different procedures to create projects and collect data automatically in order to avoid human errors and safe engineering time.
- When reference values of some metrics are calculated it should be taken into account the unexpected higher or lower values. In this case the reference device which is corrupting the metric should be removed of the comparison.

After the finalization of QUEENS2 activities the consortium has collected the following conclusions and lessons learnt:

- The benchmarking for synthesis and place and route steps shown comparable results in terms of resources allocation with more mature EDA tools. In general, the number of BRAMs, DSPs and DFFs are similar or even better than reference values. However the number of LEs is higher than reference values due to the use of those to accommodate the inputs and outputs of other specialized elements, especially as DFF buffers.
- The tool is able to understand different syntaxes and HDL coding stiles.
- In relation to interfacing with third party simulation tools, the toll generates properly post synthesis, post place and post route netlists. The timing information provided in the netlist it is also correct and correspond to timing information provided by the Static Timing Analyser tool.
- In relation to the hardware assessment, the general and unitary verification of NG-LARGE physical components are successful. However, the hardware evaluation through large and complex designs has shown unexpected behaviours in some circuits.
- NXmap has experimented a great improvement from NXmap2 to NXmap3. This improvement includes more flexibility to configure the effort of the tool, more scalability and freedom to place the designs through placing constraints as focus, aperture or obstruction. In addition, the new release of the tool allows multithreading which results in a significant decreasing of the time needed to complete synthesis, place and route and generate bitstream.
- The graphical user interface the quality of the reports and the user manuals has also experimented a great improvement in NXmap3.

To conclude, some aspect of NXmap as thoroughness in the generated reports, clarifications on User manuals, compatibility with other Operating Systems (Windows) and the implementation of mapping attributes inside HDL code have to be still improved.

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