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NG RIU De-risking

Executive Summary Report

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CHANGE HISTORY

Issue	Date	Description of Change
0	Ref. to p. 1	First issue

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LIST OF ACRONYMS

ADC	Analogue-to-Digital Converter
ADHA	Advanced Data Handling Architecture for Earth observation satellites study
AOCS	Attitude and Orbit Control System
ASIC	Application-Specific Integrated Circuit
CAN	Controller Area Network
CBH	Cat Bed Heater
COTS	Commercial Off-The-Shelf
cPCI S-S	Compact PCI Serial Space; backplane standard for space applications
DCDC, DC/DC	Switched mode power converter
FCG	Failure Containment Group
FCV	Flow Control Valve
FPGA	Field-Programmable Gate Array
HPC	High Power Command
HW	Hardware
I2C	Inter-Integrated Circuit bus
ISD	Input Serial Digital
IF, I/F	Interface
LCL	Latching Current Limiter
LV	Latch Valve/ Low Voltage (HPC)
LVDS	Low-Voltage Differential Signalling
MCU	Micro Controller Unit
MDM	Micro-D Metal
MIL-1553	MIL-STD-1553B bus
OBC	On-Board Computer
OBDH	On-Board Data Handling
PCB	Printed Circuit Board
PCDU	Power Control and Distribution Unit
PDO	Process Data Object
PT	Pressure Transducer
RIU	Remote Interface Unit
µRTU	micro Remote Terminal Unit
RW	Reaction Wheel
SAVOIR	Space Avionics Open Interface architecture
SDO	Service Data Object
SPI	Serial Peripheral Interface bus
SpW	SpaceWire bus
SW	Software
TBC	To Be Confirmed
TC	Telecommand
TM	Telemetry

1 SCOPE

This document summarizes the findings of the “Next Generation Remote Interface Unit Architecture” activity.

1.1 Applicable Documents

Ref. ID	Document Name	Ref	Issue
AD1	Requirement Document	67597	1
AD2	Architecture Design	67893	1
AD3	Demonstration Design Report	68194	0
AD4	NG IO Design, Development and Verification Plan	68253	0

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2 STUDY OVERVIEW

RUAG Space Finland will, subject to separate analysis, plans and decisions, initiate a major product development project to define and implement Next Generation Remote Interface Unit ("NG RIU development" later in this document). Before starting this project, possible risks must be mitigated. For this purpose ESA GSTP "Assessments to Prepare and De-Risk Technology Developments - Next Generation Remote Interface Unit Architecture" activity ("De-risking: NG RIU architecture" later in this document) has been identified to be conducted prior to "NG RIU development" project start.

The core technical architecture of existing RIU was to large part developed from 2006 to 2009. It is heavily influenced by Airbus D&S´s specific requirements. Resulting architecture is not sufficiently flexible and modular, which leads to high non-recurring engineering (NRE) costs in each new customer case and development project. Due to high NRE costs, the competitiveness of the RIU solution is deteriorating.

The de-risking NG RIU activities were divided in three main tasks:

1) Requirement survey
2) Architecture survey
3) Demonstration

The next chapters more detailed present the how the main tasks were divided for smaller tasks.

3 REQUIREMENT SURVEY

Requirement Survey was divided in three activities:

1) Analysis of Current Generation
2) Requirement Survey
3) NG RIU Requirements

In the Analysis of the current generation, two main existing RUAG RIU concepts were studied:

- Sentinel-2 based,
  - FPGA based OBC IF
  - External Mil-Bus communication circuit
  - FPGA based front end modules
  - LVDS internal interface
  - Centralized AD converter

- MetOp SG
  - FPGA based OBC IF with MIL-BUS communication
  - ASIC based front end modules, with AD-converter
  - OBDH internal interface

In the Requirement survey task, already existing RIU requirements from two main primes were studied to gather high level requirement information as a basis for architectural selection.

Also, general SAVOIR requirements and contemporary ADHA interface requirements were studied.

In the final task, high level requirements for Next Generation RIU were generated considering:

- Environment
  - Life time and reliability
  - Radiation
  - Thermal
  - Mechanical
  - Primary power
  - Electromagnetic
- Interfaces
  - Control Interface
  - Communication interfaces
  - Command interfaces
  - Acquisition interfaces
  - AOCS interfaces
  - Mechanism drive interfaces
  - Reaction wheel interfaces
  - Propulsion interfaces
- Internal communication

4 ARCHITECTURE SURVEY AND ANALYSIS

Architecture Survey was divided into two main activities:

1. Presentation of the architecture concepts and analysis of those.
2. Filtering and selecting the most promising ideas for trade-off analysis and presenting the recommended RIU architecture according to trade off results.

Different architecture concepts were evaluated from different point of views:

- Integration level
- Mechanical concept
- Backplane Motherboard
- Redundancy Concepts
- Configurability
- RIU Internal communication
- Module Control Functions
- Analogue acquisition
- Power distribution

4.1 Integration Level

Three architecture concepts were identified, see Figure 4-1, Figure 4-2 and Figure 4-3:

- Highly integrated, one big box including all RIU functions.
- Shared concept, RIU functions shared in several small µRTU units, located close to the end users.
- Mixing the previous two concepts.

Smaller µRTU gives a lot of flexibility and provides possibility to decrease mass of the cabling, but on the other hand smaller units will weigh more in total. One big box might provide smaller mass, but on the other hand flexibility, placement of the big unit in the spacecraft and harness may be drawbacks together with thermal control. Consequently, it seems that electronic function design which supports both sizes would provide the best solution.

The analysis outcome was that the baseline is to implement the “Standard” IFs into a Main RIU (big box) and most of the “Non-standard” interfaces into smaller, more flexible µRTUs. This would easily lead to a concept in which:

The Main RIU most probably provides:

- OBC RIU IFs
- Standard User IFs
- RIU internal secondary voltages

The µRTUs most probably provide:

- Propulsion functions
- Secondary voltage outlets distribution
- Mechanism Drive Electronics
- Extension to any RIU functions

The rest of the functions (RWs and AOCS) could be located in either Unit.

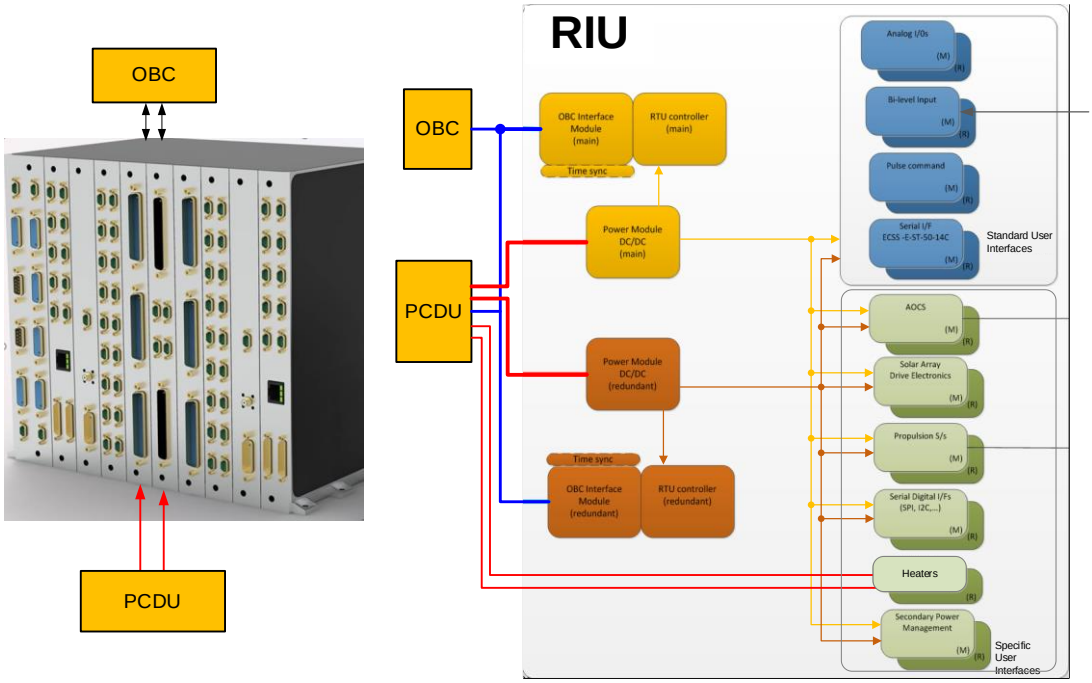

Figure 4-1 One big box RIU concept

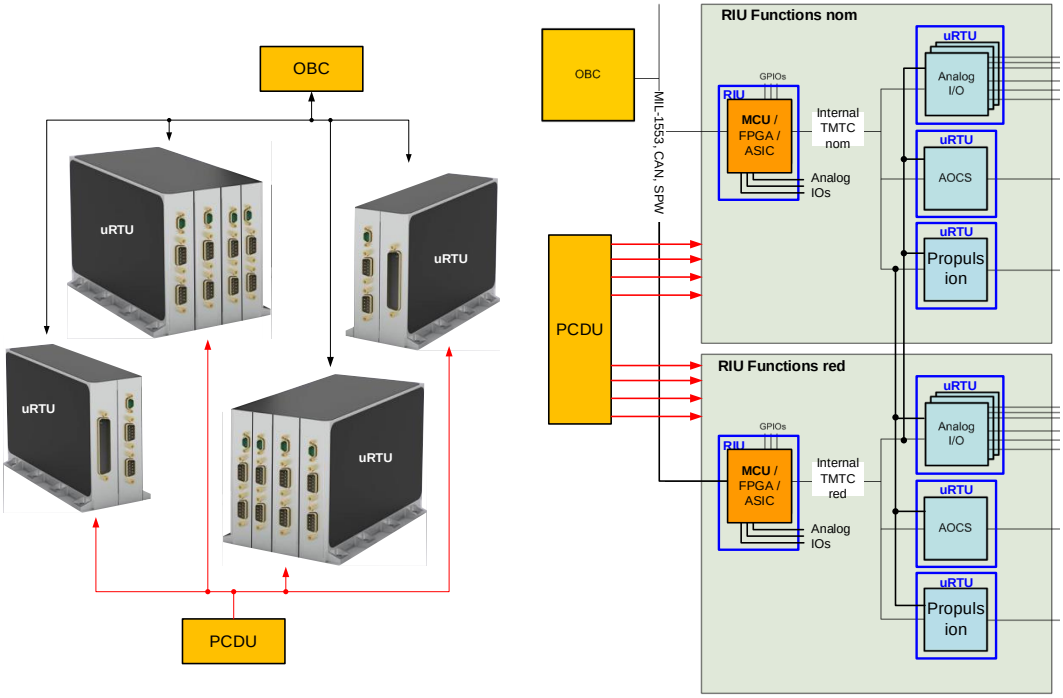

Figure 4-2 Several small µRTUs concept

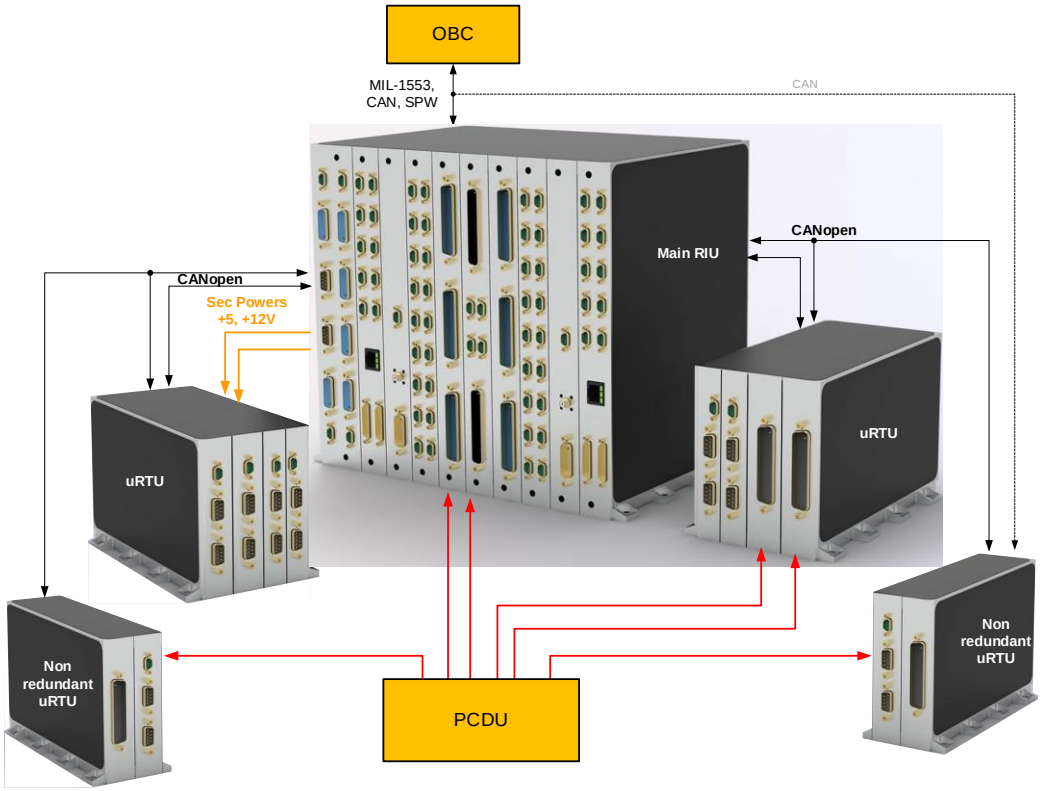

Figure 4-3 Mixed concept

4.2 Mechanical Concepts

The basic idea was to compare concepts and understand the relationship between the IF count and the mechanical size. The effect of the location of IF connectors, both on front and back sides versus only on front side was presented.

Another perspective was to see the differences between custom and industrial standard designs.

Also, the possibility to use smaller MDM-type D-connectors was presented, MDM connectors seem to be acceptable as indicated in the ADHA study.

As a reference also very modular small module concept was evaluated, with a conclusion that an ASIC would be needed to achieve the required integration level.

The cPCI Serial Space standard, with 6U and 3U PCB size concepts, was found to be one of the most promising standards, having strong support in Europe.

The present RUAG custom mechanics would provide the strongest heritage in terms of mechanical or thermal qualification.

4.3 Backplane Motherboard

Four possible motherboard solutions were identified:

- Custom rigid PCB
- Custom flex PCB
- cPCI-SS backplane
- SpaceVPX backplane

The features, benefits and drawbacks of different solution were evaluated, and the best standardized solution is the cPCI S-S Backplane. The cPCI S-S backplane concept supports both

3U and 6U solutions, and also Advanced Data Handling Architecture (ADHA) study seems to prefer the cPCI S-S over SpaceVPX.

4.4 Redundancy Concepts

Different solutions were presented from redundancy, cross-coupling, Failure Containment Group (FCG) and single failure free point of view.

- Single FCG Module
- Internally Redundant Module
- Cross coupling inside Unit through backplane
- Single failure free design

6U size modules could include 1 to 6 Failure Containment Groups, and they can be cross coupled either internally or through backplane.

3U size µRTU modules, due to smaller size, are non-redundant modules and cross coupling between sides can be implemented only through backplane.

4.5 Configurability

Configurability of the RIU functions was divided into software (SW) configurability and hardware (HW) configurability. SW configurability mainly means that typically MCU based module control may change the parameters, even during flight.

RIU configurability design would be a combination of SW and HW configuration.

The parameters which finally define the configuration method are:

- IO types
- Core control
  - FPGA, MCU or ASIC
- Available PCB area, 3U, 6U
- Failure mechanism of the functions and between functions

4.6 Internal Communication

One of the key topics of the RIU architecture is the internal communication bus (ICB). Present designs of the RIU and RIU-like units are based on SPI, OBDH, LVDS or fully customised serial/parallel bus implementations. To achieve a higher degree of standardization, some common and known solution should be selected.

Controller Area Network (CAN) is a robust, differential, asynchronous, vehicle bus standard designed to allow microcontrollers and devices to communicate with each other's which provides good change to use CANbus in RIU units.ADHA study favours CANbus, and also several COTS projects seem to plan to use CAN. There is also lot of CANopen activities on ESA side.

Internal bus was also investigated from reliability and cross coupling point of view to providing basic input and understanding of the failure propagation and reliability for the final selection of internal communication.

Again, to be able to support the Main RIU and µRTU concepts the most optimized solution would be such that the internal communication bus could also support the external communication i.e. communication between Main RIU and µRTUs.

One benefit in selecting the CAN bus is that many microcontrollers include the CAN bus interface. Also the testability of standardized bus would give some advantages. But the foremost reason to select CAN is that it is a standardized bus.

4.7 Module Control Functions

There are three relevant options for implementing the core control functions of the modules: FPGA, MCU or ASIC.

FPGA based Core would have the strongest heritage and well-known reliability and radiation aspects. FPGA would also provide the most efficient and compact way to provide the needed core interface types. The disadvantage is the long and costly development phase.

ASIC solution development costs are so high that the volumes of the RIU products are too low to cover the investment.

Microcontroller based core would provide a flexible way to use the same component in several functions. The MCU including ADC would also minimize the number of the components.

4.8 Analogue Acquisition

The Analogue acquisition architecture was separated from internal communication, because of its special nature and because of RIU requirements which may require high accuracy and high acquisition sampling rate, which may limit the possible solutions.

The analogue acquisition and AD-conversion (ADC) can be approached in two ways:

- Centralized ADC
- Distributed ADC

The ADC itself may be integrated to an MCU or be a part of ASIC, or it can be an external part controlled by an MCU or an FPGA.

4.9 Power Distribution

Power distribution aspects can be divided basically to the main cases: Primary input voltage, RIU Secondary voltages, Propulsion Power needs and Primary side control of the voltage regulation.

To be able to cover those different areas, the power system of the RIU must be quite flexible and configurable. To achieve that level of flexibility, the power system of the RIU must be modular. Even the power module itself must be divided into functional blocks in such a way that it can be configured to support different input voltages and also different outlet voltage requirements.

5 ARCHITECTURE TRADE-OFF

The full trade-off with scoring details is quite extensive, and is not repeated here. The best overall score was obtained for the solution comprising:

- Mixed Modular RIU Architecture
- 6U module size (Main RIU)
- cPCI S-S backplane, dual star redundancy
- CAN command interface
- MCU based control core
- Decentralized microcontroller ADC
- Mixed power distribution
- OBC interface baseline CAN, optionally Mil-Bus or SpW

6 DEMONSTRATION

The purpose of the NG RIU de-risking demonstration was to evaluate the data transfer capability of the selected Internal CANopen communication protocol, following CiA 301 and ECSS-E-ST-50-15C specifications.

6.1 Demonstrator Overview

Demonstration consist of:

1. Laptop PC 1
   - OBC Interface simulator
   - PEAK IPEH 002022 CAN-USB Adapter
2. Laptop PC 2
   - CAN bus logger
   - PEAK IPEH 002022 CAN-USB Adapter
3. Power supply
   - Laboratory Supply for Evaluation boards
4. CAN bus nodes
   - CTR, SAMRH71F20-EK evaluation kit
   - 5 Slaves, 5 x SAM V71 Xplained Ultra evaluation kit for
     - 4 x STD configuration + Dummy
     - 3 x STD + 1 x PROP configuration + Dummy
     - 4 x STD + 1 x PROP configuration
5. CANopen bus
   - 1Mbit/s bit rate
   - Non redundant
6. Software
   - Lely CANopen stack

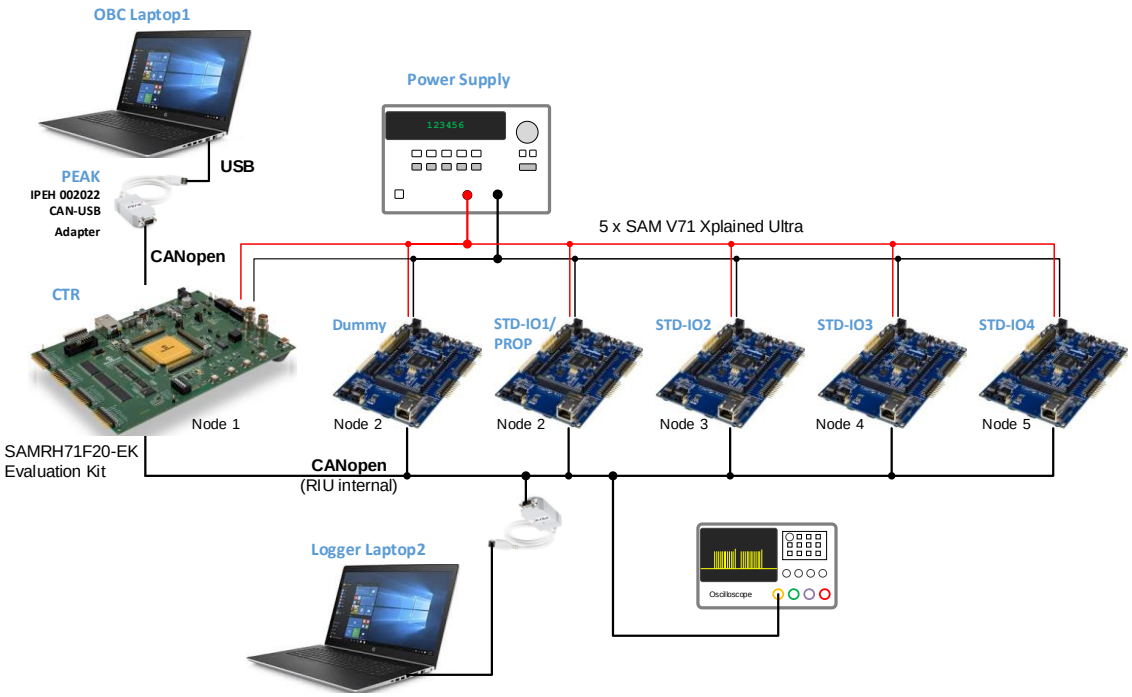

Figure 6-1 Demonstrator system principle

To verify the CANopen bus capability, the cases listed below were identified to be most challenging and covering all other data transfer requirements in the RIU system:

- Configuration of 254 long list of channel acquisition for modules
- Acquisition of data from the maximum number of RIU telemetry channels during one SYNC period 10Hz/100ms
- Acquisition of data from the maximum number of RIU telemetry channels, configure and command all 20 FCVs during one SYNC period.

Table 6-1 Demonstrator Test cases

Case	Description	To be tested	Target
Acquisition list configuration to STDs	CTR configures for all STDs the acquisition list, including totally 254 analogue channels	SDO configuration Time	254 long list, configuration during one SYNC period
Data acquisition from STDs • **4 STDs**	360 analogue channels from 4 STDs Maximum 1440 channel data by 4 STDs, each having 90 PDOs Slaves provide Heartbeat messages every 100ms	Time needed to provide the maximum analogue data, worst case data is 0xF0F0	All analogue data from the maximum number of RIU channels during one SYNC period
Data acquisition and FCV configuration • **3 STDs** • **PROP**	360 analogue channels Totally 1080 channel data provided by 3 STDs, each having 90 PDOs 20 FCVs configured by SDOs FCV IO activation timing vs SYNC message Slaves provide Heartbeat messages every 100ms	Time needed to get 1080 channel data and configure 20 FCVs SYNC -> FCV outlet timing stable	All analogue data from the maximum number of RIU channels and 20 FCVs configured and fired during one SYNC period Fire activation time vs SYNC message stable

6.2 Acquisition List Configuration

With this test setup, the acquisition list for 4 STDs takes 783ms. With 10Hz acquisition frequency, requirement was not met. By improving MCU firmwares the typical RIU requirement 8Hz/125ms could be achieved, but this might become a constraint. As this configuration time requirement is not fully clear, it shall be clarified.

6.3 Data Acquisition from 4 STDs

The needed time to provide the full set of analogue data was 45.4ms. With 10Hz acquisition frequency requirement is met with more than 50% margin.

6.4 Data Acquisition and FCV Configuration

If worst case data F0F0 is provided, the max time needed is slightly longer than 55.8ms but with 10Hz acquisition frequency requirement there is still over 40% margin.

In addition, when using the CANopen SDOs according to standards, the confirm messages do not include the data requested by master. If the later analysis shows that normal SDO request and confirm sequence is not reliable enough, the option is to add a second SDO upload sequence which reads the data from object directory and only after checking the data, the fire command is sent. This would take around another 17ms, but still could be possible inside the 100ms SYNC period.

6.5 Conclusion of the Test Results

Test results show that the CANopen protocol using PDOs and SDOs with 1Mbit/s bit rate provides feasible bit rate to transfer all the data and commands through CANbus. The configuration time of the long 254 analogue acquisition list done by SDOs may require more than 1 SYNC time 100ms, this possible “timing constraint” shall be clarified.

7 CONCLUSIONS

Study, analysis and test results of the demonstrator show that the selected internal CANopen bus is a feasible way to continue the NG RIU development.

The growing knowledge over the CANopen protocol revealed that high data traffic load between RIU and OBC may block the CANbus communication between OBC and other the devices, depending on the priority of the CANopen bus messages. One conclusion later may be that if the RIU-OBC communication is based on CANopen the RIU may need its own dedicated CANbus between OBC and RIU. Specially SDO configuration may need a long time and due to the low priority of the SDOs, other communication shall be stopped to guarantee proper SDO configuration within a reasonable time.

It is seen that even if the CANopen communication between RIU and OBC would be based on the same principles as the RIU internal one, further analysis is needed from satellite system point of view.

Also, MCU firmwares shall be optimized and developed to enable the realistically fastest and most reliable internal SDO configuration.

The test results with worst case traffic scenarios showed good results with proper margins, giving confidence over the bus and the CANopen protocol itself.

The usability of CANopen between RIU and OBC communication needs to be further studied from a satellite communication perspective.

8 FUTURE WORK

The next step in the NG RIU activities is to design and implement the Modular Micro Interface Unit, which is a subset of standardised “classical” Remote Terminal / Interface Unit in a compact form factor, 3U Compact PCI Serial Space.

The 3U µRTU provides a scalable and configurable decentralised architecture concept, optimizing the needed spacecraft harness. The modularity and configurability allow cost efficient adaptation to spacecraft and to mission specific needs.

These 3U design blocks are the basis for the foreseen development continuation with a 6U version, completing the NG IO System.