EXECUTIVE SUMMARY REPORT

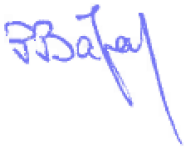
HERA-IP-ICU

Prepared by: HERA IP-ICU Team

Approved by: Paul Bajanaru

Digitally signed by Paul Bajanaru
DN: dc=es, dc=gmv, ou=Usuarios, ou=GMV-ASP, cn=Paul Bajanaru, email=pbajanaru@gmv.com

Authorized by: Paul Bajanaru



Digitally signed by Paul Bajanaru
DN: dc=es, dc=gmv, ou=Usuarios, ou=GMV-ASP, cn=Paul Bajanaru, email=pbajanaru@gmv.com

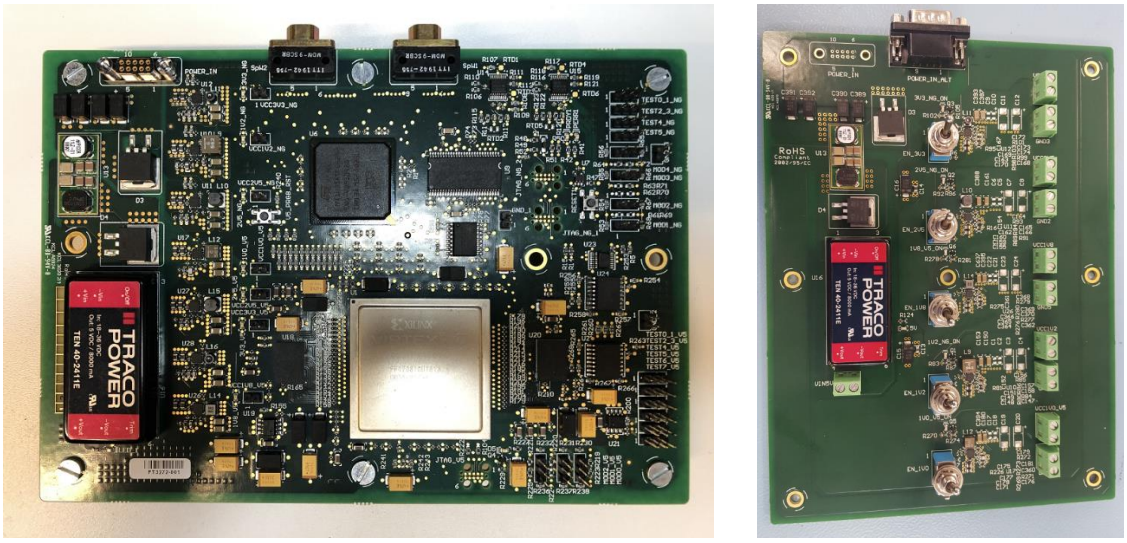
Code:	GMV-HERA-IP-ICU-ESR
Version:	1.0
Date:	17/12/2020
Internal code:	GMV 24972/20 V1/20

1. INTRODUCTION

The final goal of the HERA-IP-ICU activity has been the design, development and validation of a representative Elegant Breadboard skeleton for the Image Processing Unit (IPU) to be used in HERA mission as part of the spacecraft autonomous navigation.

The scope of the project encompassed a skeleton implementation of the breadboard model, not including high level implementation of TM/TC data Handling and neither the image processing implementation in FPGA.

The main drivers of IP-ICU design were the nominal and redundant SpaceWire I/F with the HERA S/C OBCs, and the ability to accommodate and accelerate in hardware the required image processing algorithms having as input images taken by a navigation camera. Additionally, during the activity, the necessity of IP-ICU reconfiguration was identified, to be correlated to the chosen image processing approach during mission.



(a) IP-ICU EBB **(b) IP-ICU PSU BB**

Figure 1: Hardware designed and manufactured in the framework of HERA IP-ICU activity

The following terminology (which in fact determines the name of the equipment) is adopted with respect to the functionalities of the unit:

- IP: Image Processing, as main driver for the Spacecraft Autonomous Navigation, two main typologies being baselined for HERA: (1) maximum correlation with a lambertian sphere – the position of the asteroid in the FoV of the camera is determined, (2) relative navigation system which captures images from a navigation camera, and significant points/ features are extracted, and afterwards compared with features extracted in the previous image in order to find their correspondence.
- ICU: Interface Control Unit, including I/Fs management with OBC and in-flight reprogramming functionality

2. HERA-IP-ICU DESIGN

The architecture of the equipment (fully representative in terms of interfaces and on-board processing capabilities for the actual flight hardware of IPU) is relying on an architecture with 2 separate FPGAs communicating by means of an InterFPGA link:

- UIF (Unit Interfaces FPGA, NanoXplore NG-Medium)
- UPF (Unit processing FPGA, Xilinx Virtex-5 VFX130T)

The two FPGAs have allocated external volatile and nonvolatile memories, and temperature monitoring is provided through and RTD (for the UIF) and the Xilinx SYSMON (for the UPF).

UIF is responsible for the management of the entire unit, including the SpaceWire communication with the OBC. For the fully functional higher TRL models of the unit, for reusability and unit integration, the recommended communication protocol will rely on CCSDS/PUS. In HERA mission, IP-ICU communication to OBC uses the CCSDS packet transfer protocol over SpaceWire. The Unit is providing 2 SpaceWire I/Fs for communication with the HERA OBC, allowing the accommodation of the unit to different redundancy schemes, or interconnecting to different equipment. Besides the Spacewire I/Fs management, the Interfaces FPGA of the IP-ICU can handle also the in-flight reprogramming of the Processing FPGA. Thanks to this feature, the unit can allow different image processing approaches in different phase missions, so different computer vision accelerators which are not used in the same moment of time can be accommodated by replacing bitstreams in the processing FPGA to save a potentially needed second FPGA unit.

The implemented layout corresponds to an EBB, with several components compliant to a fully scaled EM TRL 6. The PCB is designed according to the PCB and PCBA ECSS standards ECSS-Q-ST-70-60C – "Qualification and procurement of printed circuit boards", ECSS-Q-ST-70-38 – "High-reliability soldering for surface-mount and mixed technology" and ECSS-Q-ST-70-12C – "Design rules for printed circuit boards" and is manufactured at sites that have proper qualifications. The electronic components are COTS, each of them having a correspondent conterflight part, also for allowing the migration to higher TRLs.

The partial/ full compliance of the IP-ICU EBB PCB design and assembly allows the adaptation of the unit to higher TRL models and it is important to note that the board was not manufactured according to ECSS standards, nor it was tested for such purposes.

The smallest footprint used is a 0402 case size and the routing and placement of the components is by following – in most of the cases – the Design rules for printed circuit boards as defined by ECSS-Q-ST-70-12C.

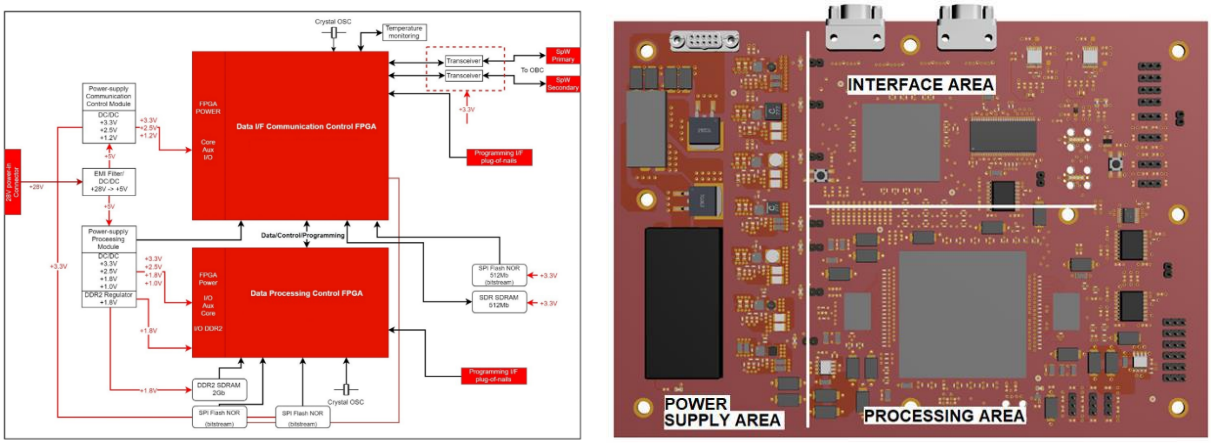


Figure 2: IP-ICU EBB Architecture

The PCB is split in 3 area: a power supply area, the interface area and the processing area.

The power supply is composed of the primary and secondary stage DC/DC converters as well as the power input connector and filter.

The interface area is composed of the NG-Medium FPGA and the adjacent parts while the processing area is composed of the Virtex-5 FPGA and its adjacent parts.

3. HERA IP-ICU VALIDATION

An EGSE unit was assembled for the purpose of validating the IP-ICU EBB skeleton, including equipment for representative validation of SpaceWire interfaces of the unit and overall functionality.

A safe approach for the validation of the IP-ICU unit was represented by the prior validation of the electrical power tree. The power tree of the IP-ICU EBB unit is implemented in a standalone breadboard (Power Supply Unit Breadboard – IP-ICU PSU BB) and validated with a commercial variable load. The tests shown stable and constant output voltage for the outputs of the DC/DCs for loads varying from miliamps up to few Ampers.

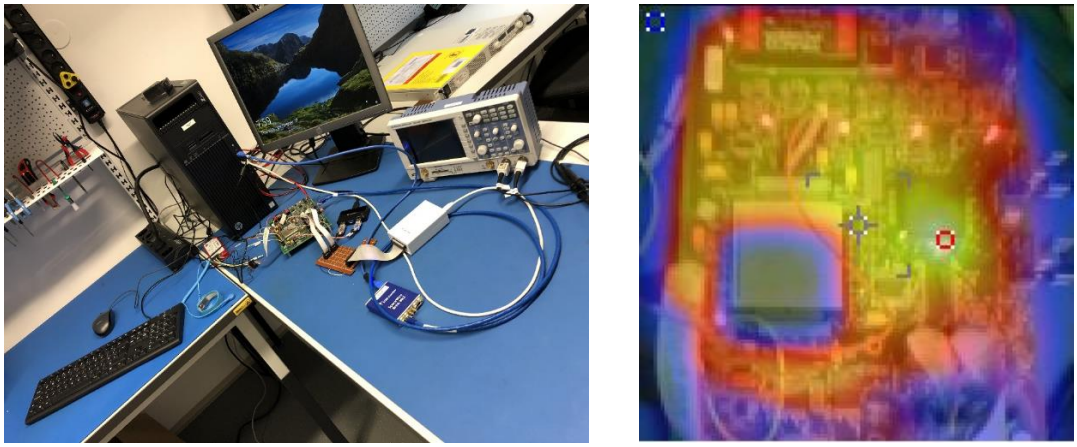


Figure 3: IP-ICU EBB Validation Set-up & Thermal Infrared Measurement

The validation of the interfaces included the validation of the correct programming of FPGAs (flash and JTAG), the SpaceWire Interafces, external volatile memories allocated to the FPGAs (SDRAM for Interfaces FPGA and DDR II for Processing FPGA), the InterFPGA link and the correct reprogramming of the processing FPGA Virtex-5.
The maximum achievable data rate of SpaceWire interfaces reached 94 Mbps, but for large sized and continuous data packet sent to IP-ICU (not the case of HERA) the median value of data rate is slower, due SpaceWire flow control.

SDRAM memory is working properly, accepting a maximum data rate of 380 Mbps for both read and write operations, while the DDR II was able to perform read and write operations at 133 MHz memory clock (higher frequencies can be easily reached).

The InterFPGA link using LVCMOS allowed data transfer between the two FPGAs at data rate of 6.25 MBps, while for LVDS lines, a maximum of 20 MBps was achieved.

Housekeeping functionality is working nominally for both FPGAs. In the case of NG-Medium, the acquisition of data from sensors was working correctly reading data from external sensors. In the case of Virtex-5, Housekeeping is relying on SYSMON functionality. The data acquired via SYSMON was consistent with the one read using the iMPACT tools (with a margin of 4 degrees Celsius)

A critical functionality of Virtex-5 that needed validation for the purpose of HERA mission is the reprogramming capability (making use of the 2 flash memories allocated), so 3 scenarios were tested:

- Selection of Virtex-5 nominal flash from NG-Medium
- Selection of one bitstream by Virtex-5 from one of the external flashes
- Programming of Virtex-5 with a bitstream written by NG-Medium in one of the Virtex-5 external flash memories

All reprogramming tests were successfully passed, but in the case of the third scenario, further features can be implemented (order to have full control over the flash memory) as Software Reset (Required for the final design to reset the Physical Memory without interrupting the power) and Block Erase (Optional, used to reduce the time lost before programming the memory)

Overall functionality and power consumption assessment of the unit was tested also using representative bitstreams for both FPGA in terms of data flow, device resource utilization, interfaces load. Power consumption of the board when loading the bitstreams was around 8.5 W and during the tests the outputs of the DC/DCs were measured within tolerances.