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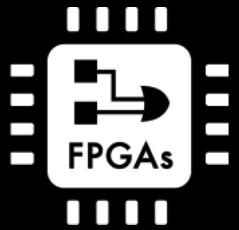
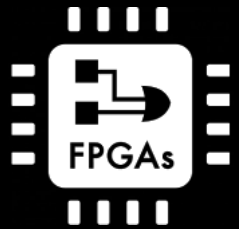
DE-RISK ASSESSMENT: HERA IP-ICU



HERA IP-ICU
Final Review Meeting

Teleconference 14/12/2020



gmv BLOG

Final Review Meeting

HERA IP-ICU

Monday, the 14th of December, 2020

gmv INNOVATING SOLUTIONS

AGENDA

Project Overview

Requirements & Architecture

Testbench Preparation

As-Built Status

IP-ICU PSU BB Validation

IP-ICU EBB Validation

IP-ICU EBB Thermal Analysis & Measurements

Roadmap to EM & EQM

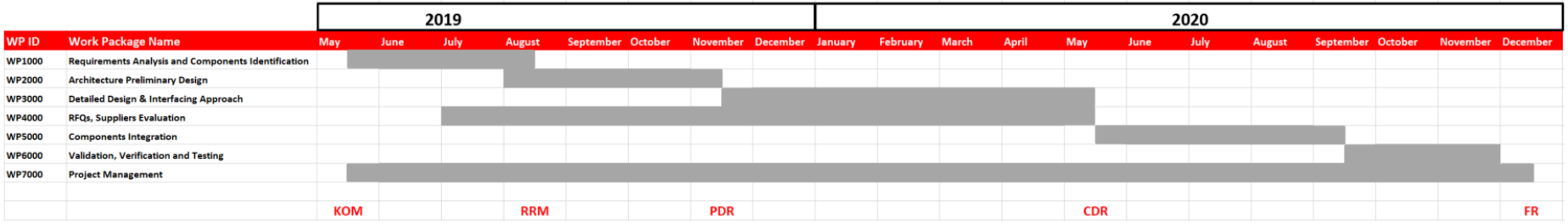
Conclusions & AoB

HERA IP-ICU
PROJECT OVERVIEW

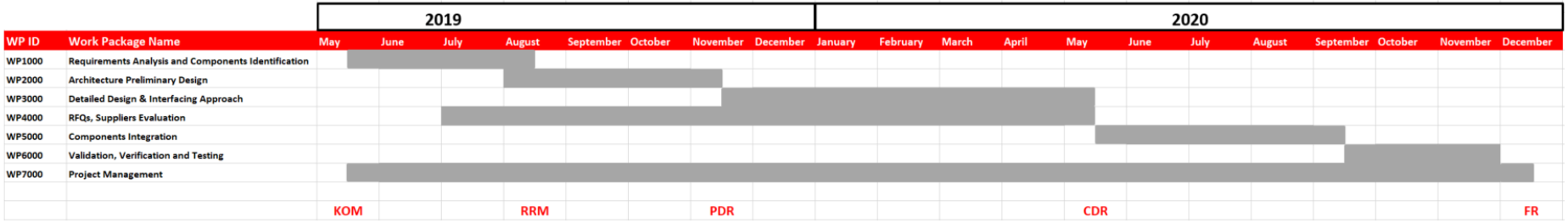
SCHEDULE

- **Negotiation Meeting Successfully Closed (25/04/2019)**
- **Kick-Off Meeting (14/05/2019)**
- **Requirements Review Meeting (09/08/2019)**
- **Preliminary Design Review (15/11/2019)**
- **Critical Design Review (18/05/2020)**
- **Final Review (14/12/2020)**
  - IP-ICU EBB As-Built Status
  - Facilities Preparations
  - Validation Campaign Reports
  - Conclusions

Estimated shift for FR: 10 months w.r.t. Project Proposal



PROJECT STATUS



- **WP1000**
  - Closed (Requirements frozen at PDR)
- **WP2000**
  - Closed (Preliminary design closed at PDR)
- **WP3000**
  - Closed (Detailed Design and Preliminary design accepted at CDR)
- **WP4000**
  - Closed (All Purchases finished)
- **WP5000**
  - Closed (Testbench assembled and IP-ICU EBB manufactured)
- **WP6000**
  - Closed (Validation Campaign finished)

HERA IP-ICU

REQUIREMENTS AND ARCHITECTURE

GENERAL

Develop and validate an Elegant Bread Board model skeleton to be used in HERA mission as:

- **Image Processing Module**
- **Interfaces Control Unit**

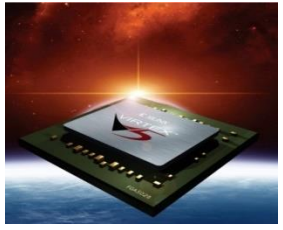
- The scope of the project encompassed a skeleton implementation of the BB, not including:
  - High-level implementation of TM/TC Data handling
  - Image Processing implementation

- In addition, the activity developed the required test bench to validate the IP-ICU BB:
  - Ground support equipment to power, operate and stimulate the IP-ICU BB

Target TRL for IP-ICU skeleton: 4/5

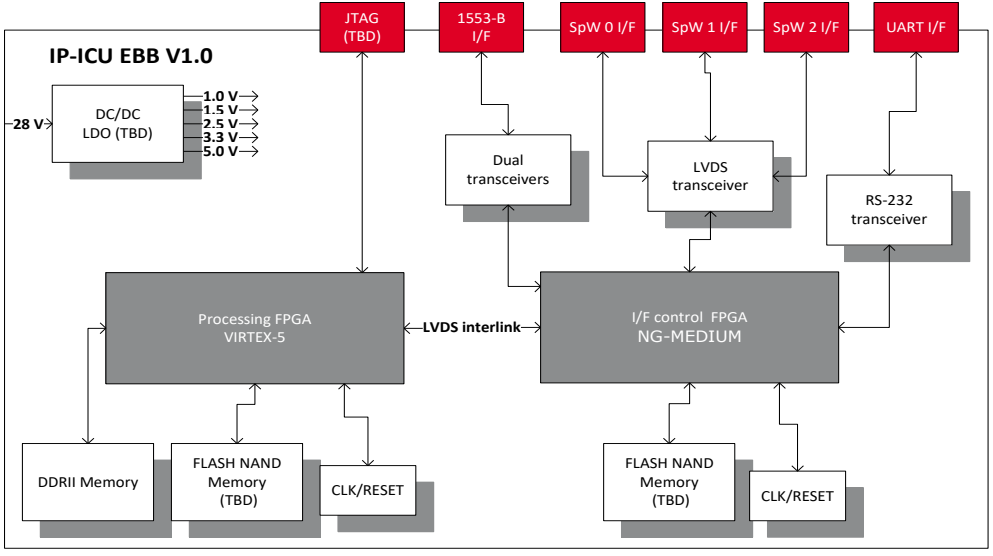
FIRST ARCHITECTURE

- Preliminary assessment regarding PCB:
  - ❑ Dimensions: 1U x 2U
  - ❑ Material: FR4 High Tg
  - ❑ Number of Layers: 8-12
  - ❑ SMD components on both sides



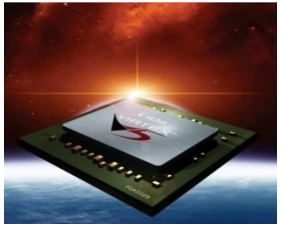
- 2 FPGA module:
  - ❑ Interfaces FPGA (IFF)
    - Deals with the interfaces of the IP-ICU to the external world
    - Master FPGA-FPGA parallel communication
  - ❑ Processing FPGA (PRF)
    - Memory controller (TBD)
    - Slave FPGA-FPGA parallel communication

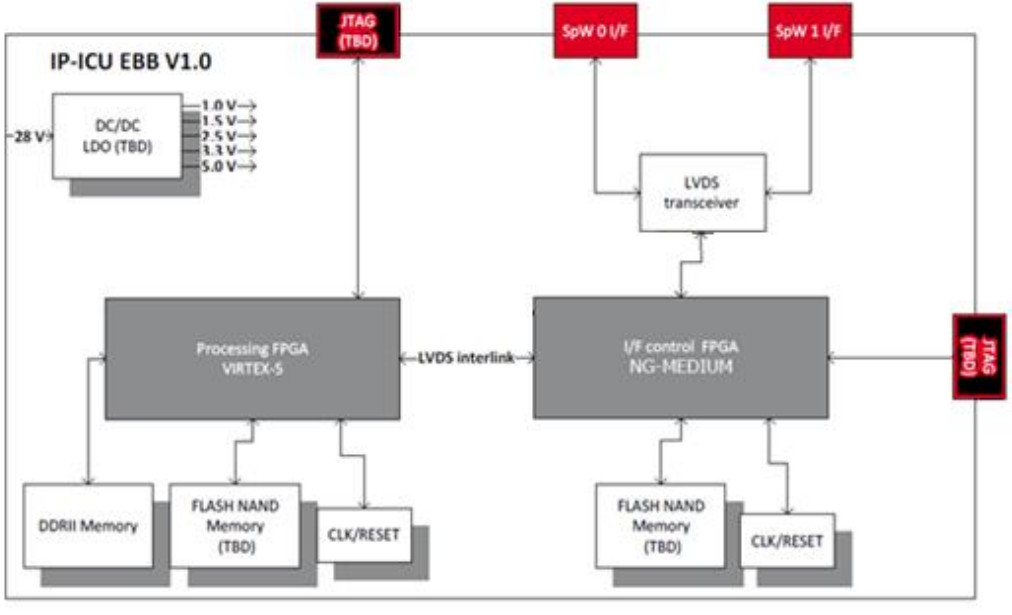
- Interfaces:
  - ❑ Power in: +28V
  - ❑ 3 x SpaceWire
  - ❑ UART
  - ❑ MIL-1553B
  - ❑ JTAG (TBD)



NEW ARCHITECTURE

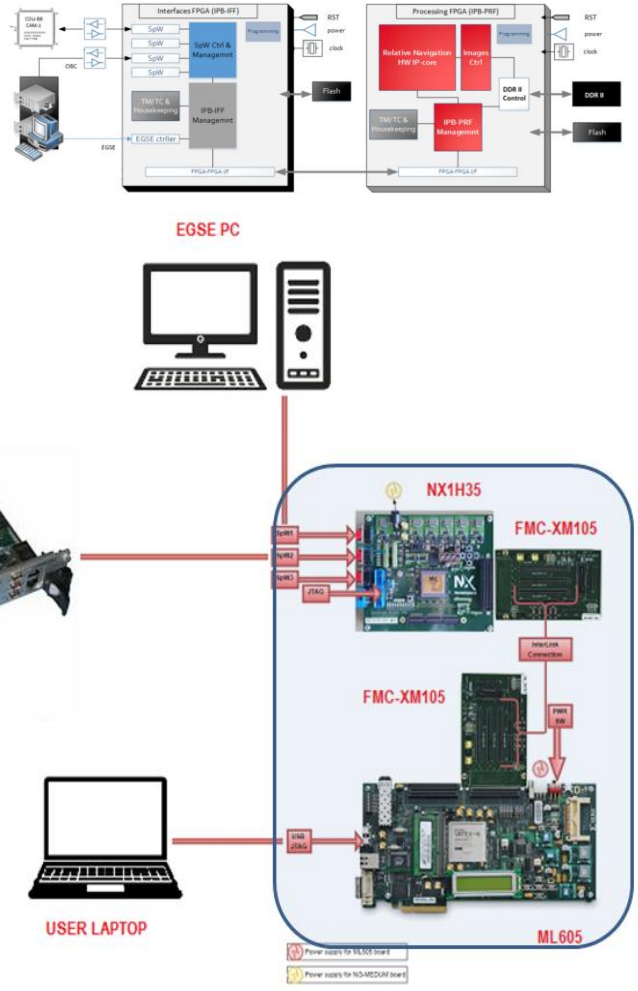
- **2 FPGAs Architecture**
  - Interfaces FPGA
  - Processing FPGA
- **I/F with OBC**
  - 1 x Nominal SpaceWire
  - 1 x Spare SpaceWire
- **28 VDC Unregulated Power Supply**
- **IP-ICU Requirements Drivers:**
  - *Connectivity (OBC: TMTC Datahandling)*
  - *Data Processing (Image Processing*
    - *Centroid HW IP (LAMB & COB)*
    - *RelNav HW IP*





HERITAGE: CAMPHORVNAV

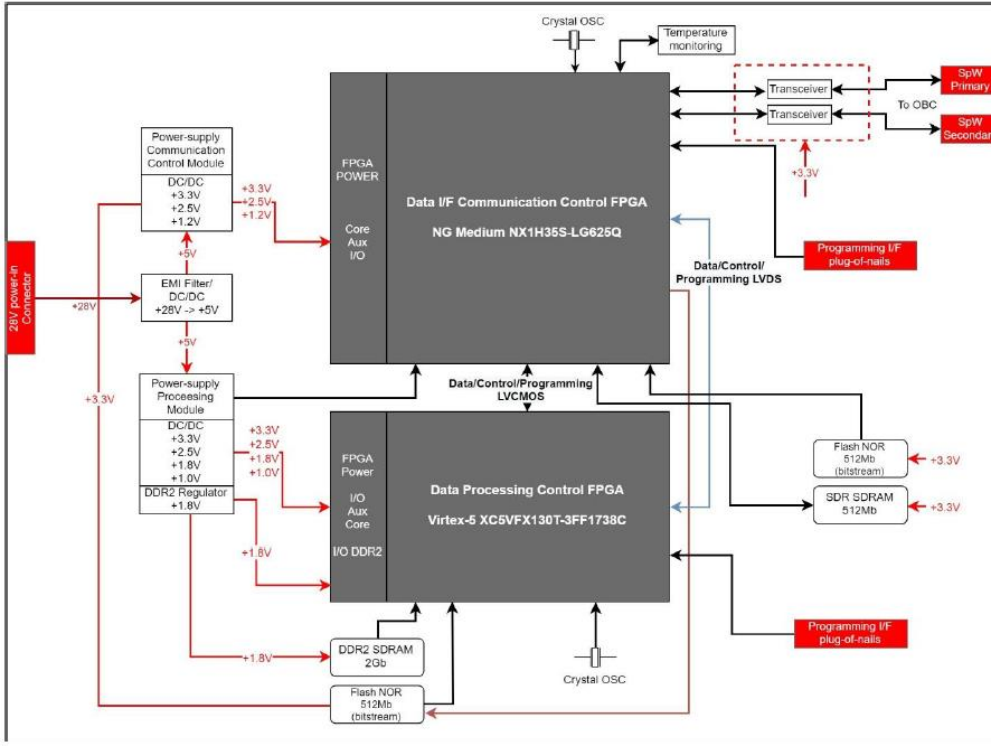
- Project within MREP Program
- Part of the Phobos Sample Return Mission (PhSR)
- VBNC used in the Descent & Landing Phase to Phobos
- **IPB-BB** for Image Processing & Data Handling fully designed, assembled and validated by GMV (ES, RO)
- **EGSE** designed, assembled and validated by GMV



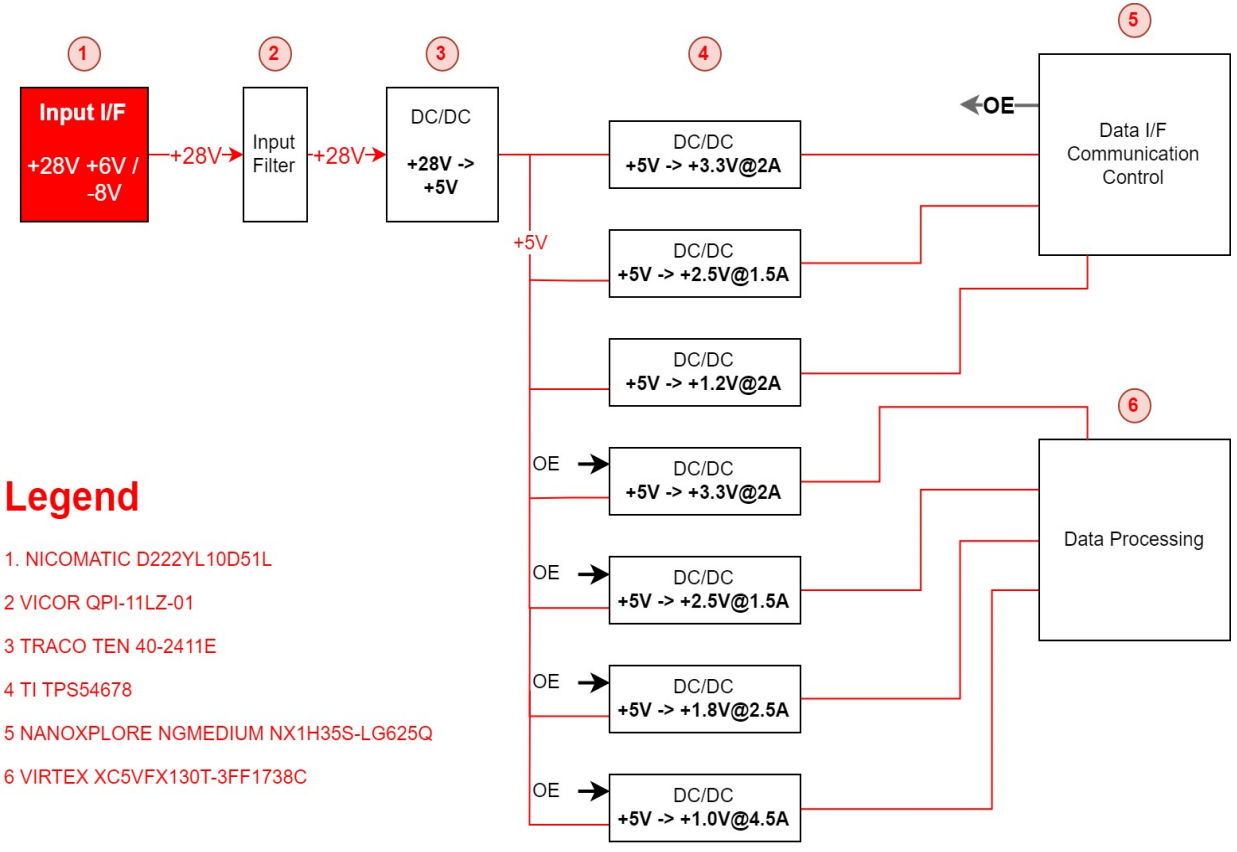
FINAL ARCHITECTURE

General Requirements of IP-ICU EBB Electrical Design

- Co-processor for Autonomous Navigation:
  - NanoXplore NG-Medium
  - Xilinx Virtex5
- Input power: **28V, 16W**
- External DDR2 devoted to Virtex5
- External **SDRAM** devoted to NG-Medium
- 2 x **SpaceWire** ports – connected through transceivers
- **Reconfigurable** Processing FPGA
- Interlink between the two FPGAs

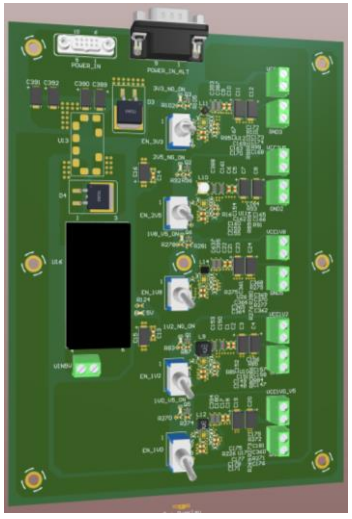


POWER TREE

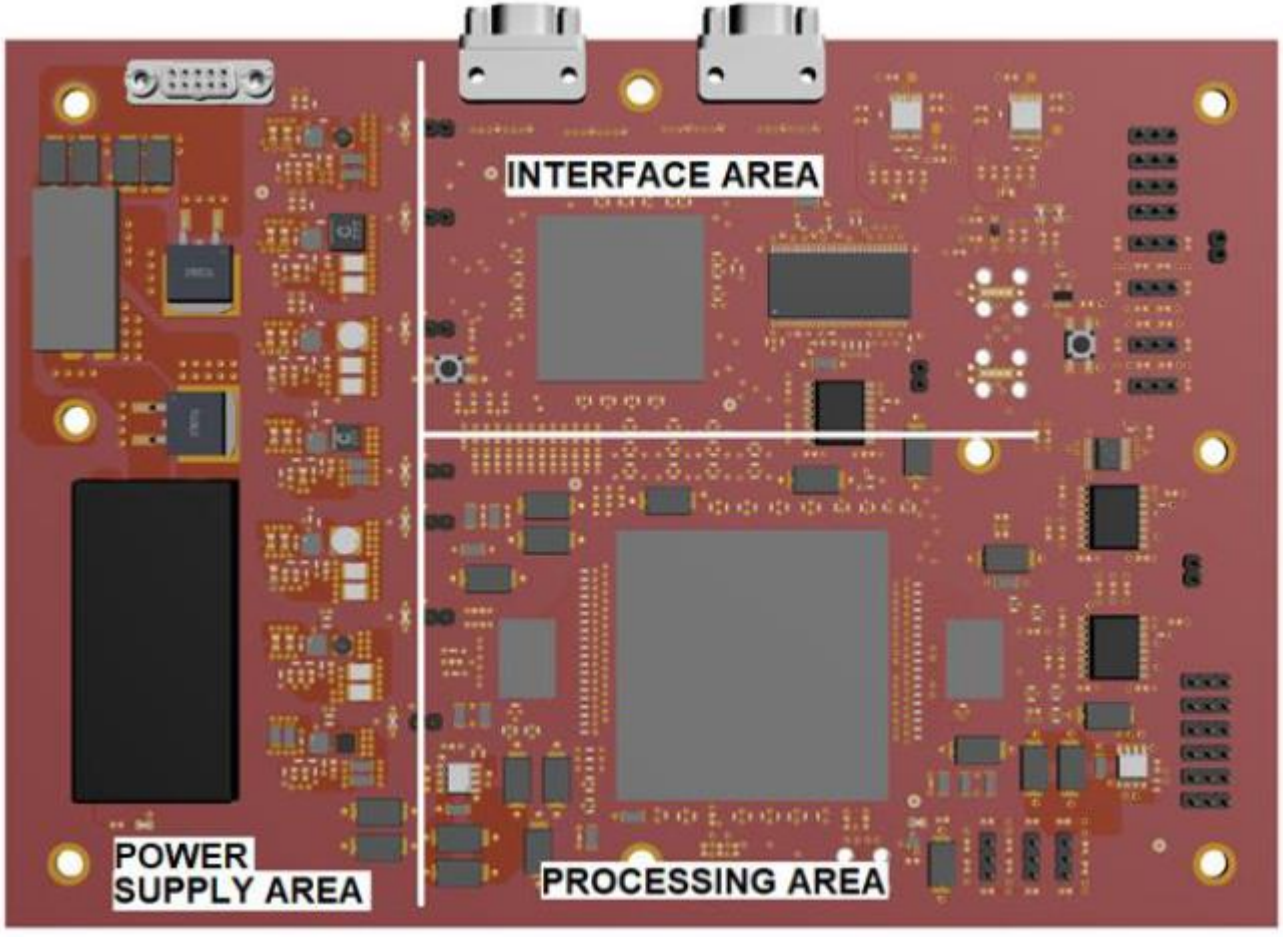


Legend

1. NICOMATIC D222YL10D51L
2 VICOR QPI-11LZ-01
3 TRACO TEN 40-2411E
4 TI TPS54678
5 NANOXPLORE NGMEDIUM NX1H35S-LG625Q
6 VIRTEX XC5VFX130T-3FF1738C

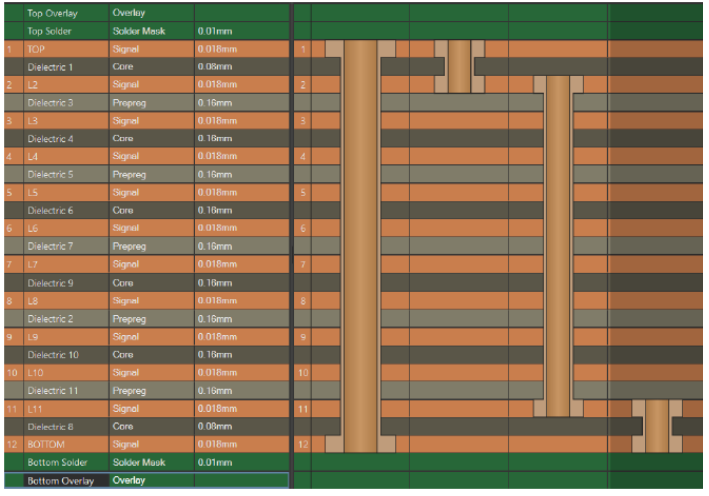


PCB AREAS



PCB & STACK-UP

- 140x200mm large
- 12 layers stack-up
- Polyamide Arlon 35N, designed for sequential lamination
- Manufacturers identification prior to layout
- Constraints faced:
  - 1mm pitch BGAs allow for only limited options in design minimum 0.8mm pitch BGA as well for the DDR2
  - Solutions: via-in-pad – blind via used – low AR – and buried via
  - All identified manufacturers recommend this solution
- Due to the constraints, using group test validation might be needed for the PCB
- Target to maintain the same stack-up and layout
- DDR2 is replaced with a side-pins part – no more uncompliant VIAs
- Iterations with the manufacturer during the manufacture of IP-ICU for improvements needed for being fully ECSS compliant



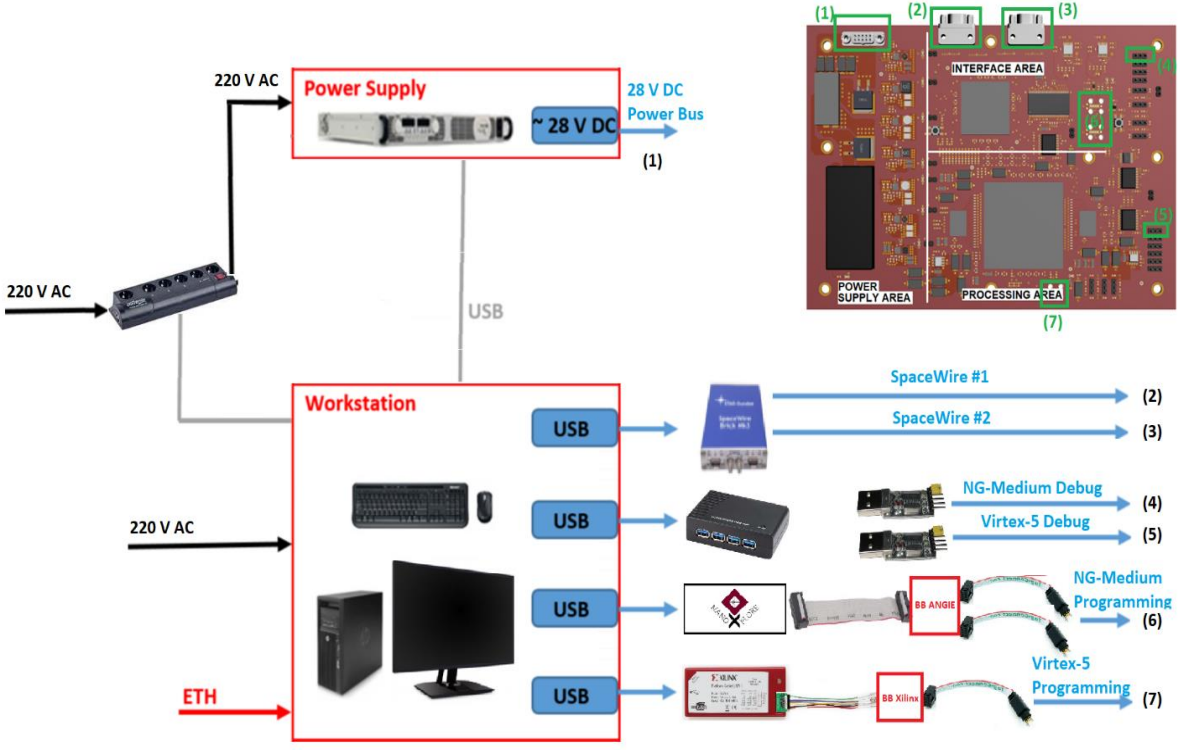
HERA IP-ICU

TESTBENCH PREPARATION

IP-ICU TEST BENCH

Set-up description

- 28 V DC Power Bus
- Remote Control Power Socket
- Workstation
- SpW USB brick
- NG-ANGIE
- JTAG Xilinx programmer
- USB HUB
- UART TTL Interfaces



EGSE WORKSTATION

Configuration:

- Intel(R) Xeon(R) Silver 4114 CPU @2.20 GHz 2.19 GHz
- 32 GB RAM Memory
- Windows 10 Pro for Workstations, 64 bit Operating System
- 512 GB SSD, 2 TB 7200 SATA 3.5”
- 1000 Watts Power Supply

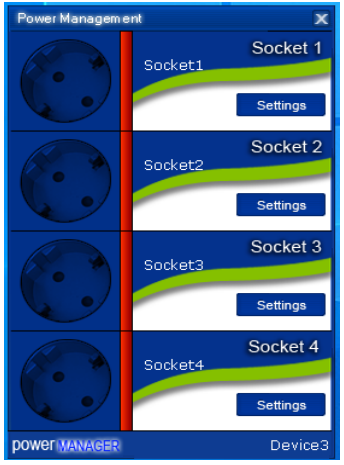
Software:

- Xilinx ISE 13.2
- Ubuntu Virtual Machine for NanoXmap
- Anaconda 2.9.7
- Power management
- SpaceWire StarDundee application

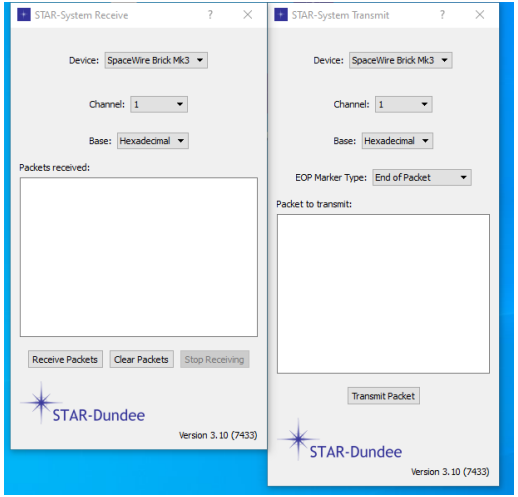
POWER SUPPLY

Configuration:

- Keysight N5767A Power Supply
- Nicomatic Power Cable
- Energenie Remote Control Power Socket
- Power Management Windows Application



SPACEWIRE BRICK & UART TTL

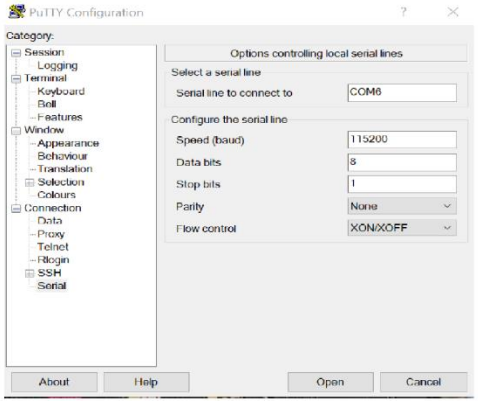


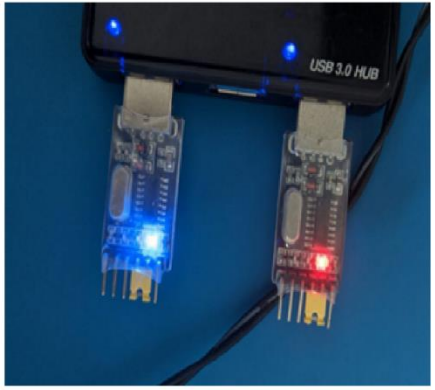
SpaceWire Brick Mk3:

- Loop Test Between TX SpaceWire#1 and RX SpaceWire#2
- Star Dundee SpaceWire Application

UART TTL:

- Loop Test between 2 units on same USB 3.0 Hub
- Putty Tool for serial communication

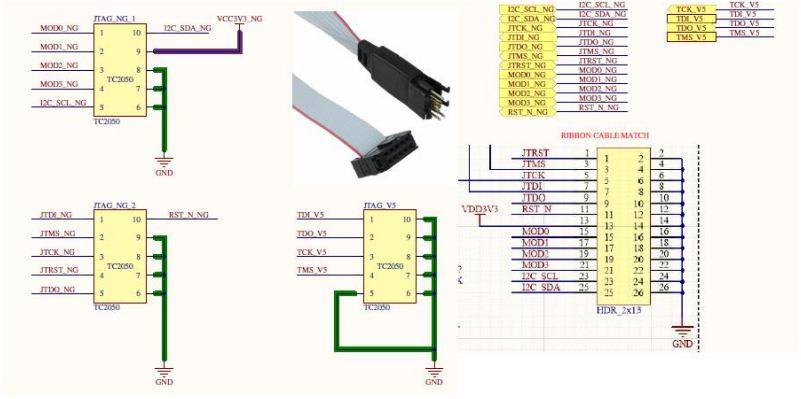




FPGA PROGRAMMING CABLES

Configuration:

- BB ANGIE
  - Custom Breadboard
  - EBB UIF Prog I/F – ANGIE Programmer
- BB Xilinx
  - Custom Breadboard
  - EBB UPF Prog IF – Xilinx USB Platform Cable II



HERA IP-ICU
AS-BUILT STATUS

BOM CHANGES

There are some minor differences from the proposed components detailed in Detailed Design frozen at CDR Level and the actual components used in the manufacturing and assembly of the HERA IP-ICU EBB.

Reasons span from availability of component in market, flexibility of design, datasheet recommendations for usage of part.

Resistors and capacitors were affected.

Most changes required a replacement with 1:1 counterpart.

Few parts were added.

One resistor was removed.

BOM part modifications Proposed vs. Assembled

Proposed		Assembled		
MFR	MFR PN	MFR	MFR PN	Part type
TDK	C2012X5R1A476M125AC	TDK	C2012JB1A476M125AC	Capacitor
YAGEO	CC0402KRX7R8BB103	KEMET	C0402C103J8RACTU	Capacitor
KEMET	T520B476M006ATE070	AVX	TRJD476K025RRJ	Capacitor
KEMET	T520B336M006ATE040	KEMET	T520V336M016ATE045	Capacitor
Samsung	CL05C181JB5NNNC	KEMET	C0402C181J5GACTU	Capacitor
Vishay	CRCW040220K0FKEDC	ROHM Semiconductor	SFR01MZPJ203	Resistor
Vishay	CRCW0402140KFKED	Stackpole Electronics	RMCF0402FT140K	Resistor
Panasonic	ERA2AEB2870X	Panasonic	ERA-2AEB2870X	Resistor

BOM Parts added

Assembled Part		
MFR	MFR PN	Part type
Panasonic	ERA-2AED103X	Resistor
Panasonic	ERJ-2RKF1000X	Resistor
Panasonic	ERJ-3EKF4421V	Resistor
KEMET	C1206C105K5RAC	Capacitor
STMicroelectronics	STPS10H100CG-TR	Diode

BOM Parts removed

Proposed Part		
MFR	MFR PN	Part type
Vishay	CRCW06034M22FKEA	Resistor

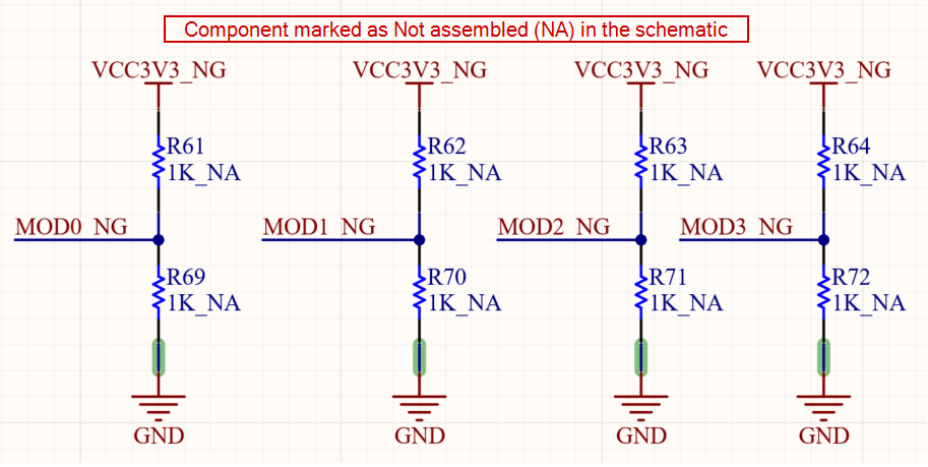
COMPONENT CHANGES ON BOARD LEVEL

The assembly house responsible for mounting the components on the Hera IP-ICU had soldered components which were declared in our documentation as not fitted.

In order to save time, it was decided to remove the originally not fitted parts from the board in the GMV RO laboratory.

Most of the components targeted were resistors which affected certain signals default logic level.

The unsoldering was a success and validation tests could continue normally.



FLASH MEMORY FOR VIRTEX-5

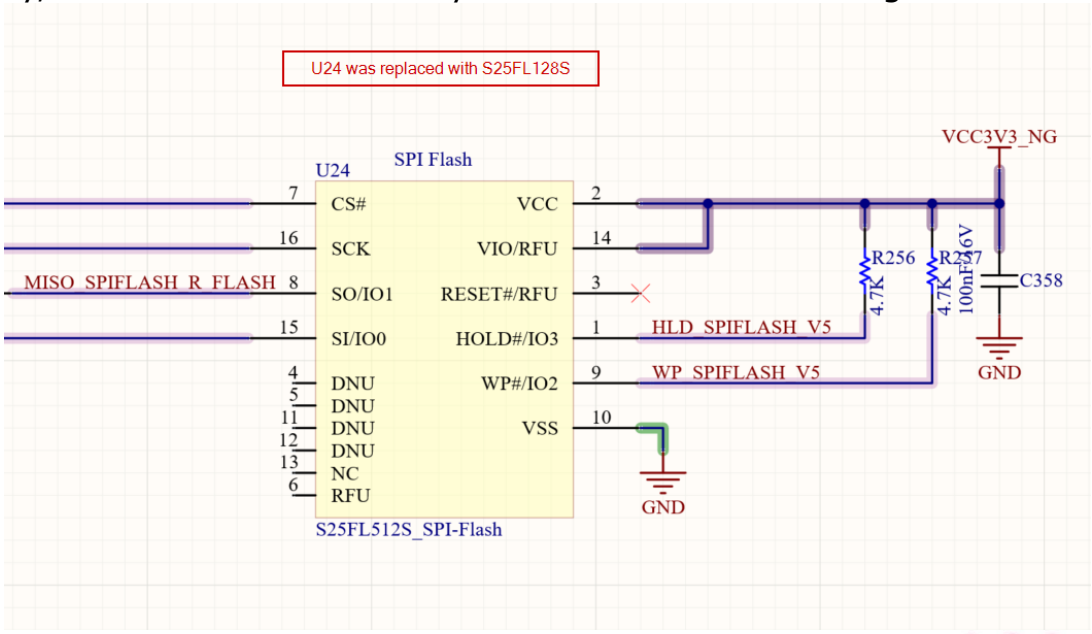
As per architecture of the design, there are two 512 Mbit flash chips connected to the Virtex-5 FPGA.

When testing the readability and writability of the flash, it was decided to replace one 512 Mbit flash chip with a 128 Mbit counterpart from the same manufacturer.

Reason for this change was incompatibility, how the internal memory of the 512Mbit flash is organized and how Virtex-5 is able to access it partially.

The change to a lower memory was possible, as the 128 variant had the same package and pinout.

The 128 Mbit flash has been soldered with success and tests re-ran were now consistent with expected output.



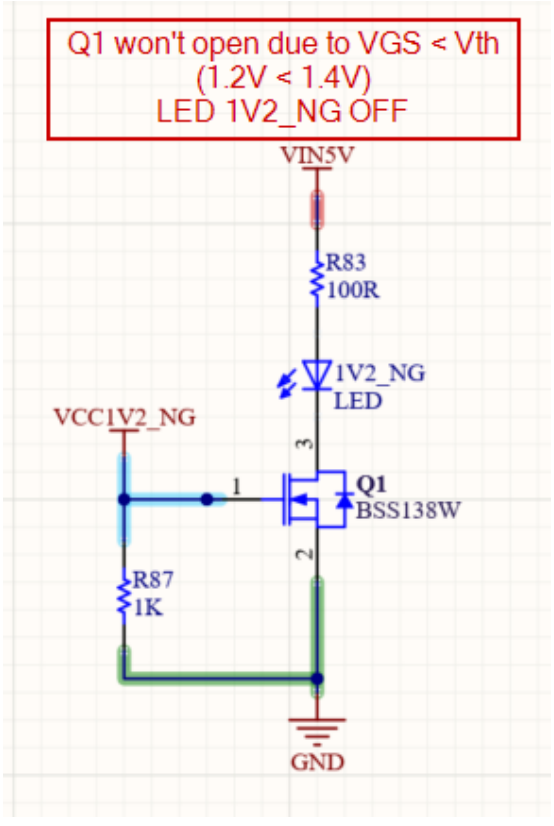
POWER STATUS LEDS OFF: 1.0V & 1.2V

Due to a schematic design error when dimensioning the LED circuit, the 1.0V and 1.2V LEDS are not lighting red as expected during power up of the board

This does not need to be associated with a absence of the supply itself but has roots on the circuit which should enable the LED to light.

Because both 1V and 1.2V are below the Vth of the transistor [0.8V-1.4V] , Q1 will not open and allow a GND path for the current to sink and allow the LED to turn on.

No fix was done for this issue as was considered minor.



UNBOXING & INSPECTION

Delivery and unboxing

Box was delivered appropriately, damage to content being avoid by taking several measures: Absorbing foam surrounding the , ESD bag and markings etc.

Manufacturing process inspection

The manufacturing of the board was done with high quality, respecting GMV set requirements.

The surface layers have good finishes, with evenly distributed soldermask, clear silkscreen, respecting target dimensions and thickness.

Assembly process inspection

The assembly of components on board was done as well with high quality.

Apart from the confusion for assembling not fitted parts, the component soldering was done correctly, as later interconnectivity tests proved.

FIRST POWER VALIDATION

The IP-ICU EBB was successfully powered up from the laboratory power source at +28V.

The current consumption of the board indicated by the supply was 240 mA for this voltage.

For the primary DC-DC converter, we measured 4.94V RMS where 5V was the target voltage.

For the secondary DC-DC converters, we measured within tolerance values for target 1V, 1.2V, 1.8V, 2.5V and 3.3V.

Note that all readings were done with no load at this stage.

Presence of various active supplies is indicated by red LEDs on board.

UIF & UPF PROGRAMMING

Basic programming was performed at this stage on the board.

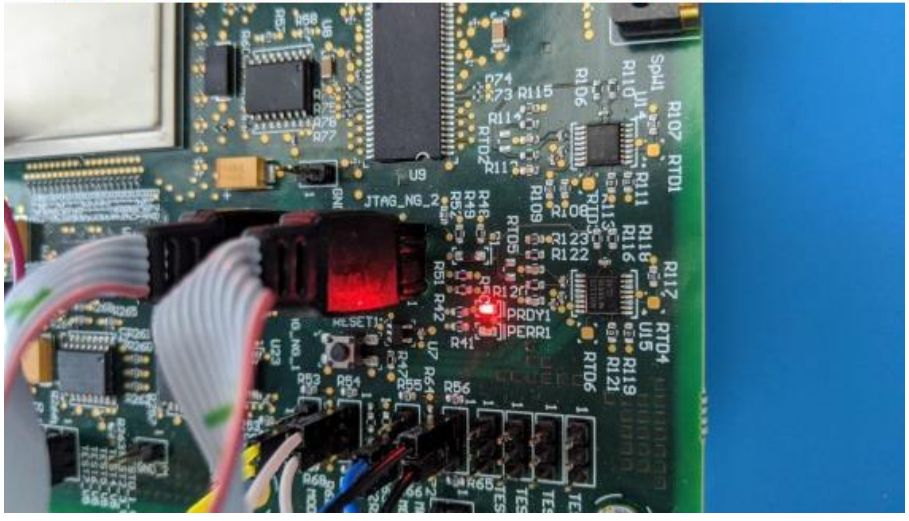
Simple bit streams were succesfully loaded into the NG and Virtex-5 via each JTAG interface.

The same bit streams are being written into respective flashes for NG and Virtex-5 via each JTAG interface.

JTAG programmers are removed and upon a new power-up, successful reads are done by NG and respective V5.

No issues were reported.

PRDY LED from NG medium indicating succesful programming



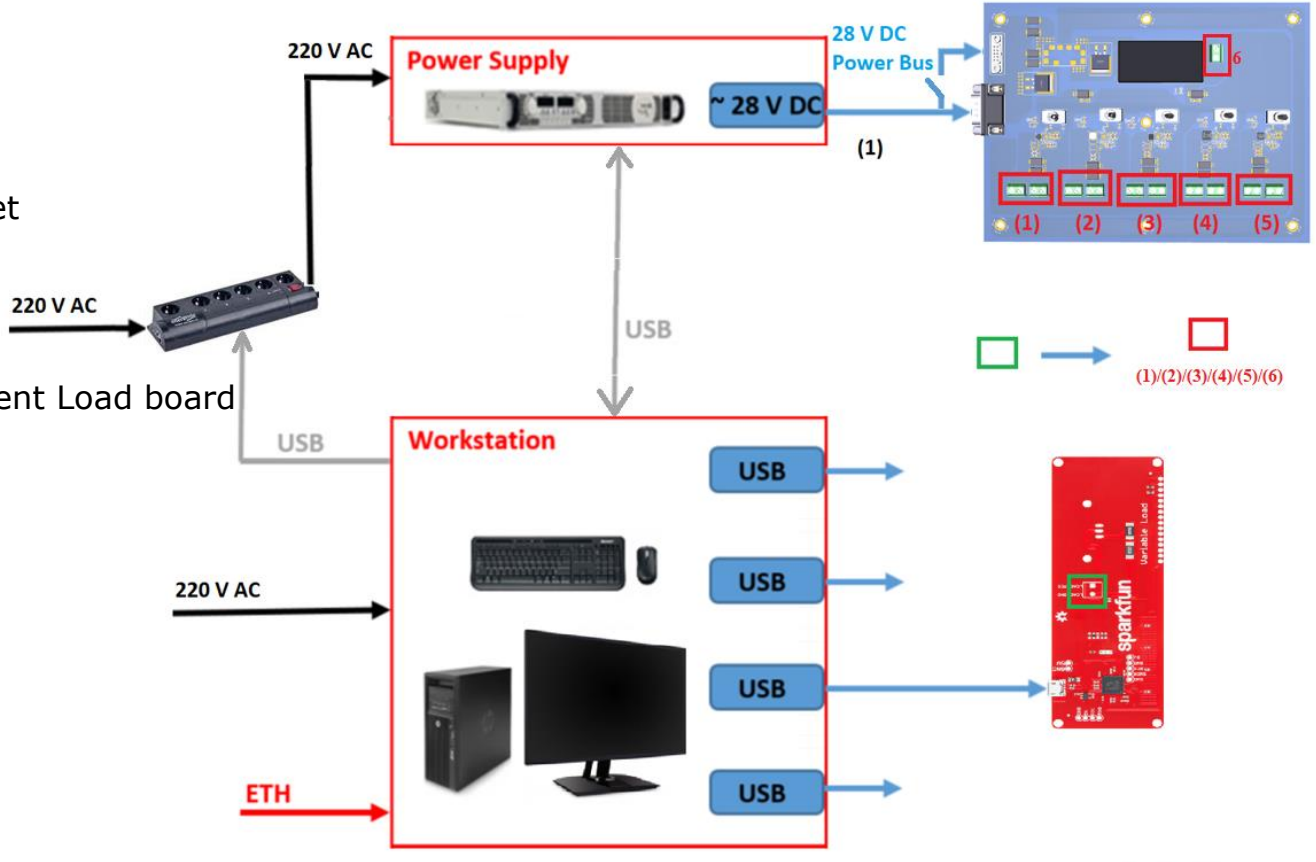
HERA IP-ICU

IP-ICU PSU VALIDATION

PSU TEST BENCH

Power tree validation

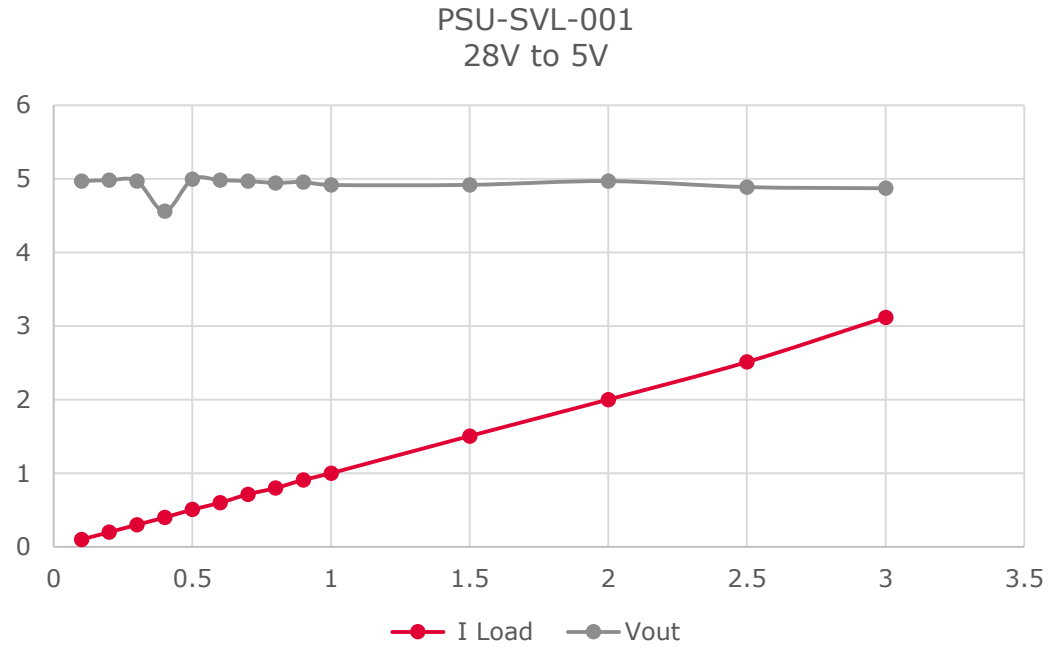
- 28 V DC Power Bus
- Remote Control Power Socket
- Workstation
- UART TTL Interfaces to Current Load board
- USB to Power supply
- USB to Power Socket
- Power supply custom cable
- Power output custom cable



POWER TREE OUTPUT (6)

Power tree validation

Iload max = 3 A
Vin = 28V
Vout = 5V
Vout pp= 0.433 V

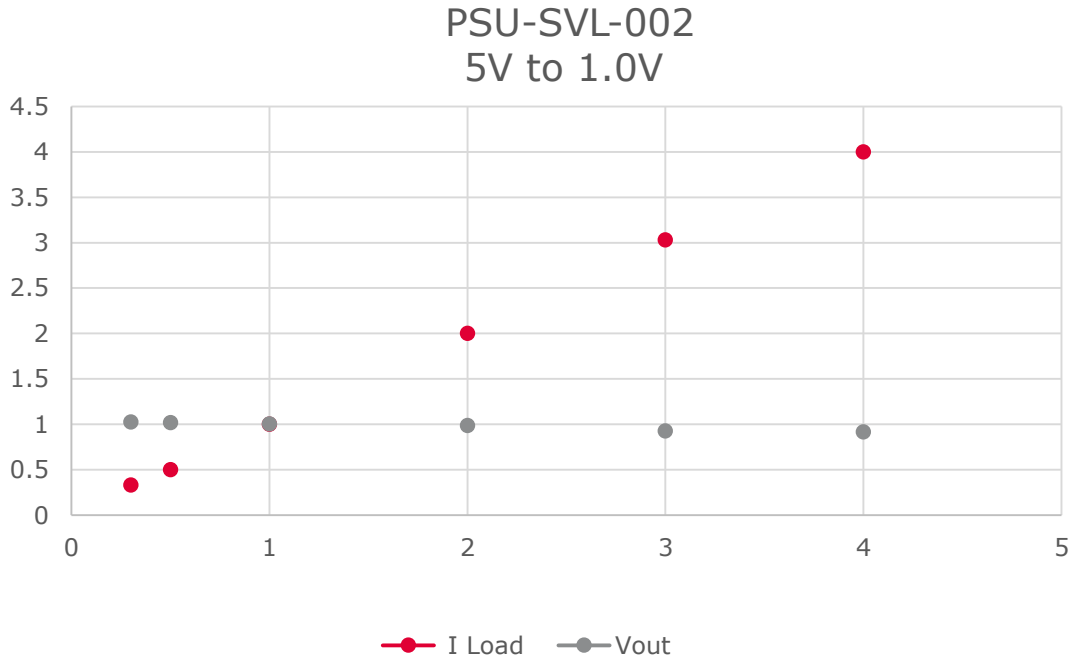


POWER TREE OUTPUT (5)

Power tree validation

RID-04

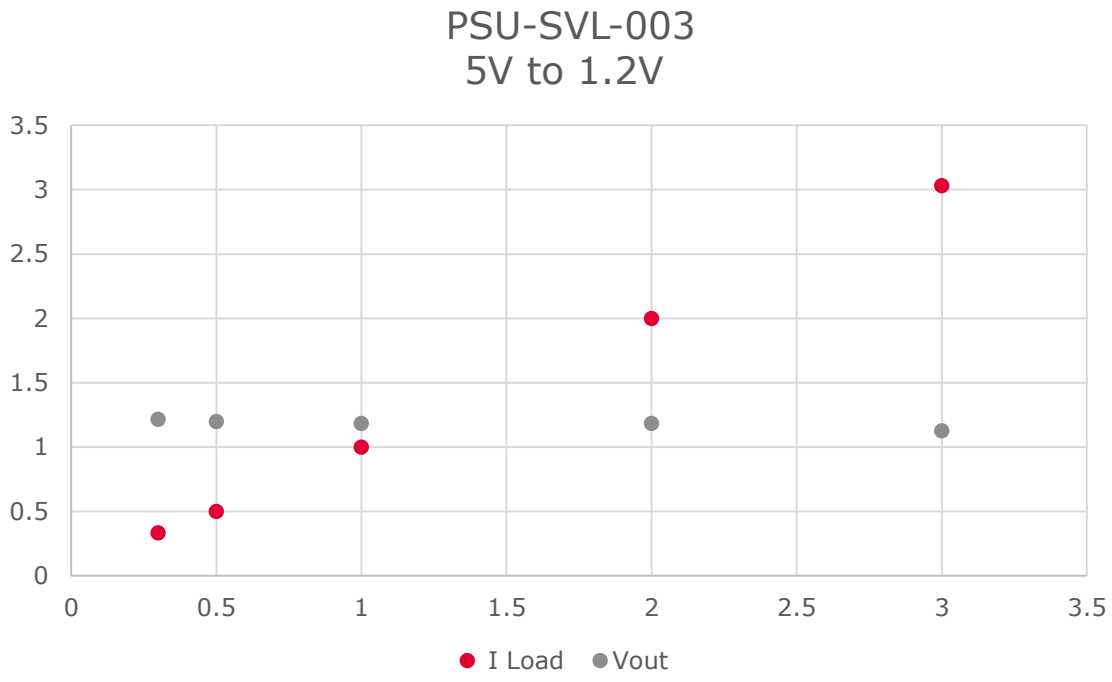
Iload max = 4 A
Vin = 5V
Vout = 1V
Vout pp= 0.108 V



POWER TREE OUTPUT (4)

Power tree validation

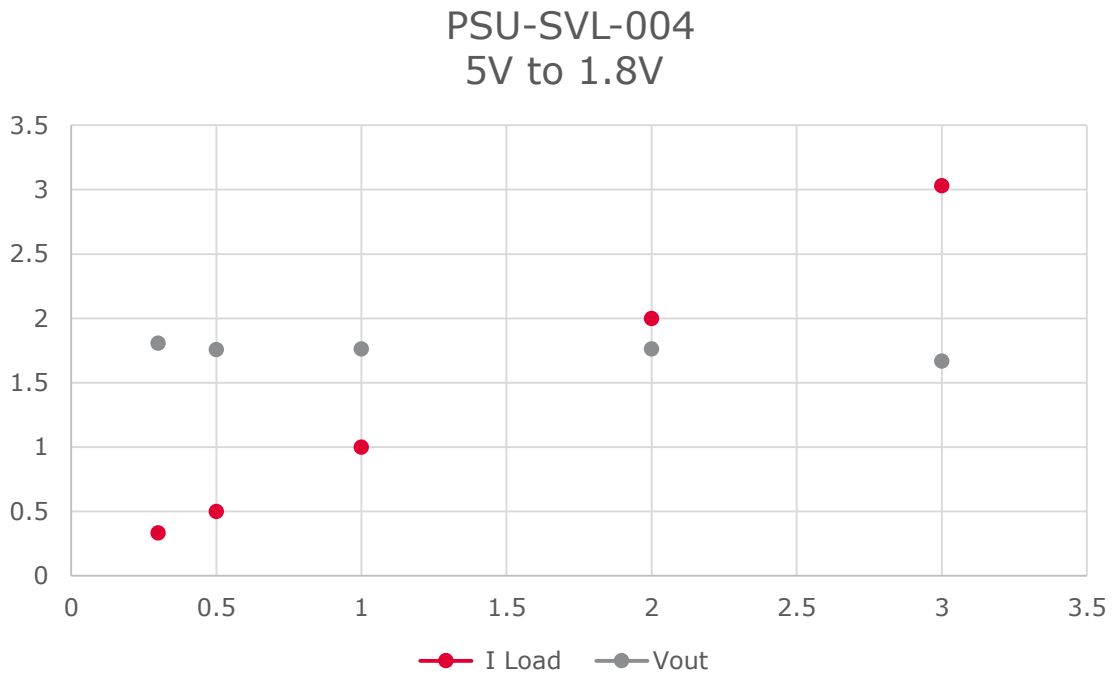
Iload max = 3 A
Vin = 5V
Vout = 1.2V
Vout pp= 0.09 V



POWER TREE OUTPUT (3)

Power tree validation

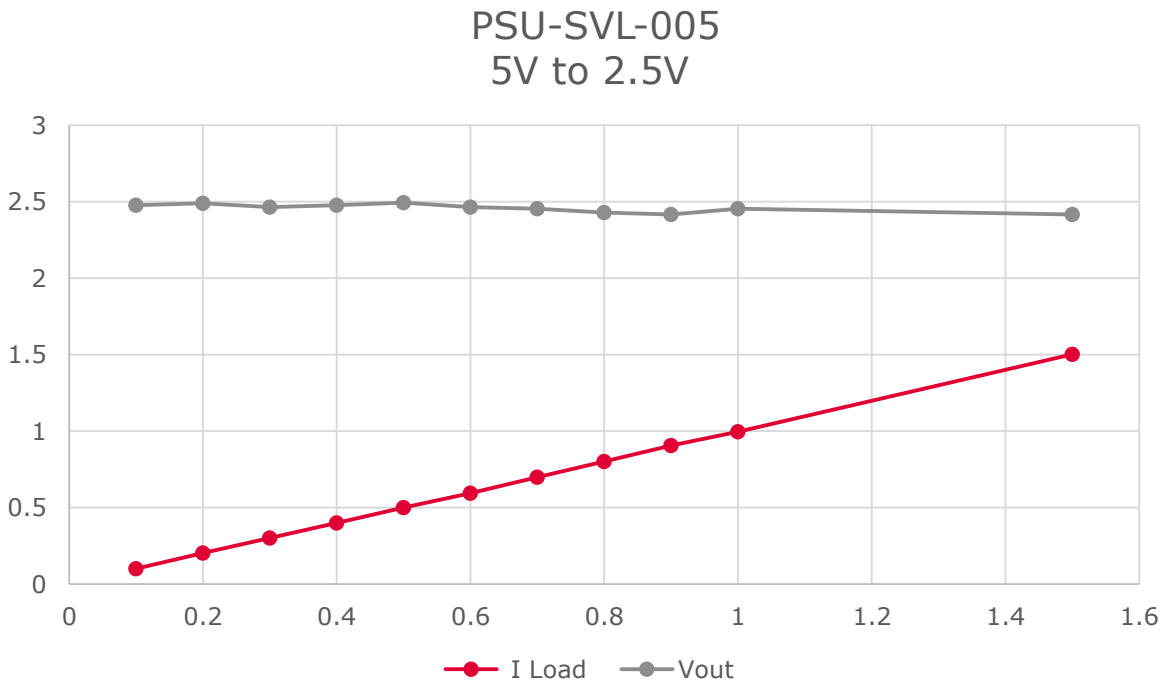
Iload max = 3 A
Vin = 5V
Vout = 1.8V
Vout pp= 0.14 V



POWER TREE OUTPUT (2)

Power tree validation

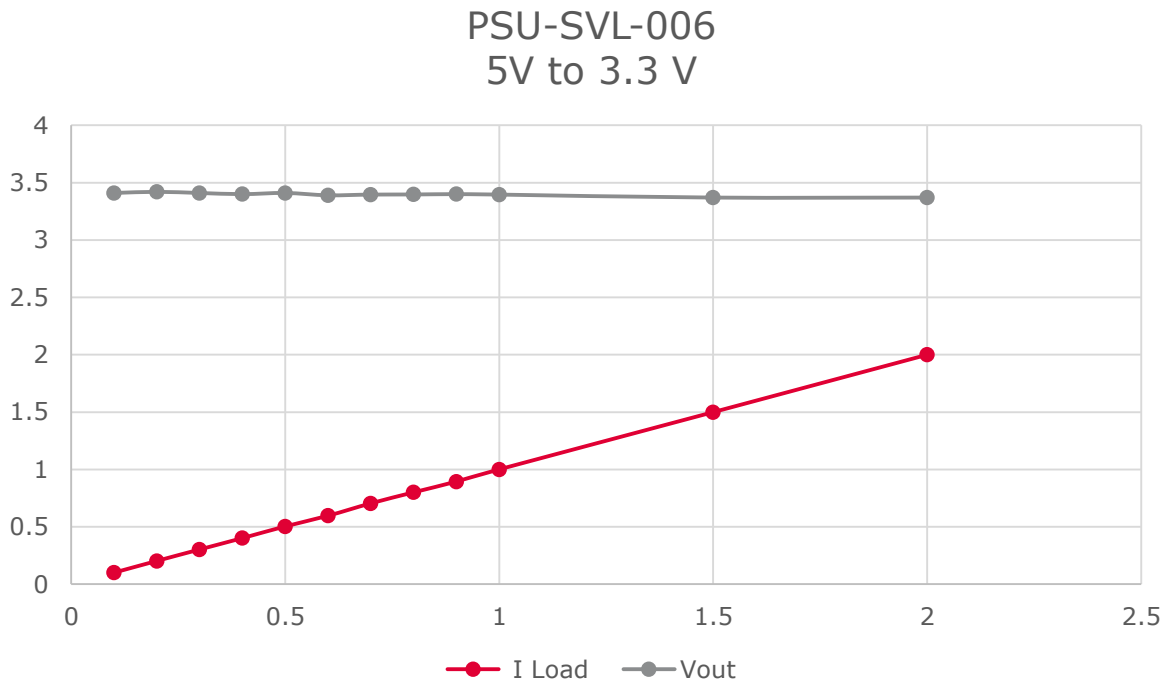
Iload max = 1.5 A
Vin = 5V
Vout = 2.5V
Vout pp= 0.077 V



POWER TREE OUTPUT (1)

Power tree validation

Iload max = 2 A
Vin = 5V
Vout = 3.3V
Vout pp= 0.05 V



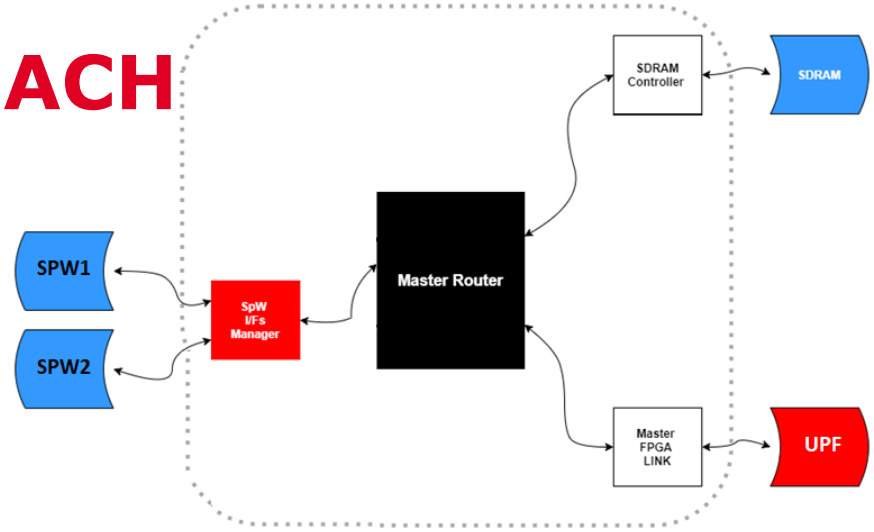
HERA IP-ICU

IP-ICU EBB VALIDATION

UIF : SPW TEST APPROACH

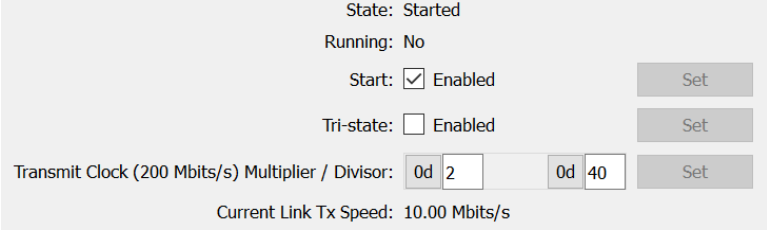
UIF Functional Architecture:

- **Master Router tasks**
  - routs all the commands received from SPW
  - decodes data received from SPW
  - choose the route of the data received from the SPW
  - routes data to SDRAM
  - routes data to UPF via Interlink

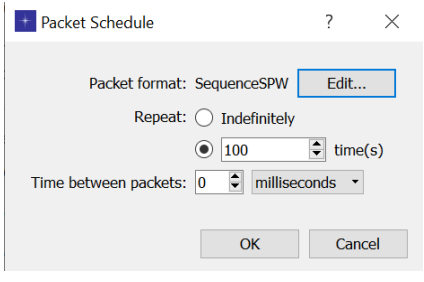


UIF SPACEWIRE Validation:

Step1. Set the connection, configure the speed of the link, select the PORT



Step2. Choose one image of 1024x1024 pixels and sent it for 100 times

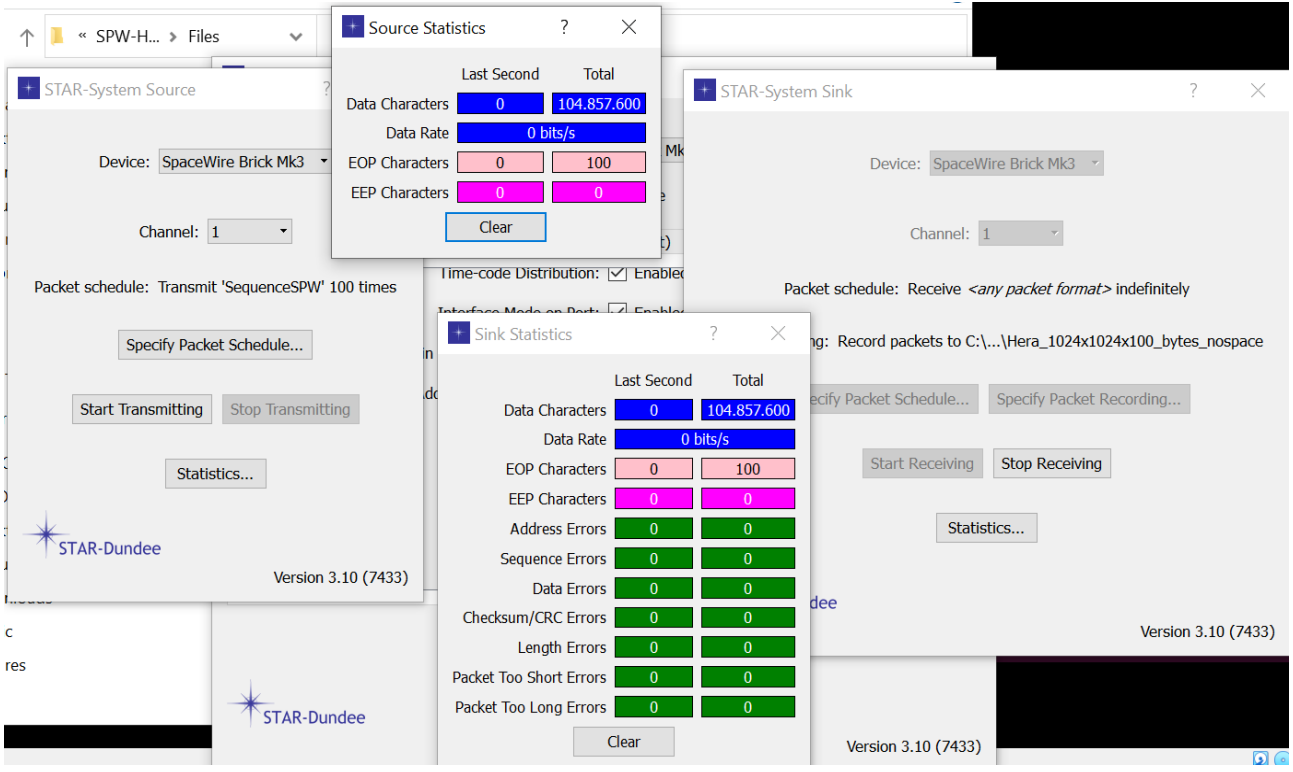


UIF : SPW TEST

RID-05

UIF SPACEWIRE Validation:

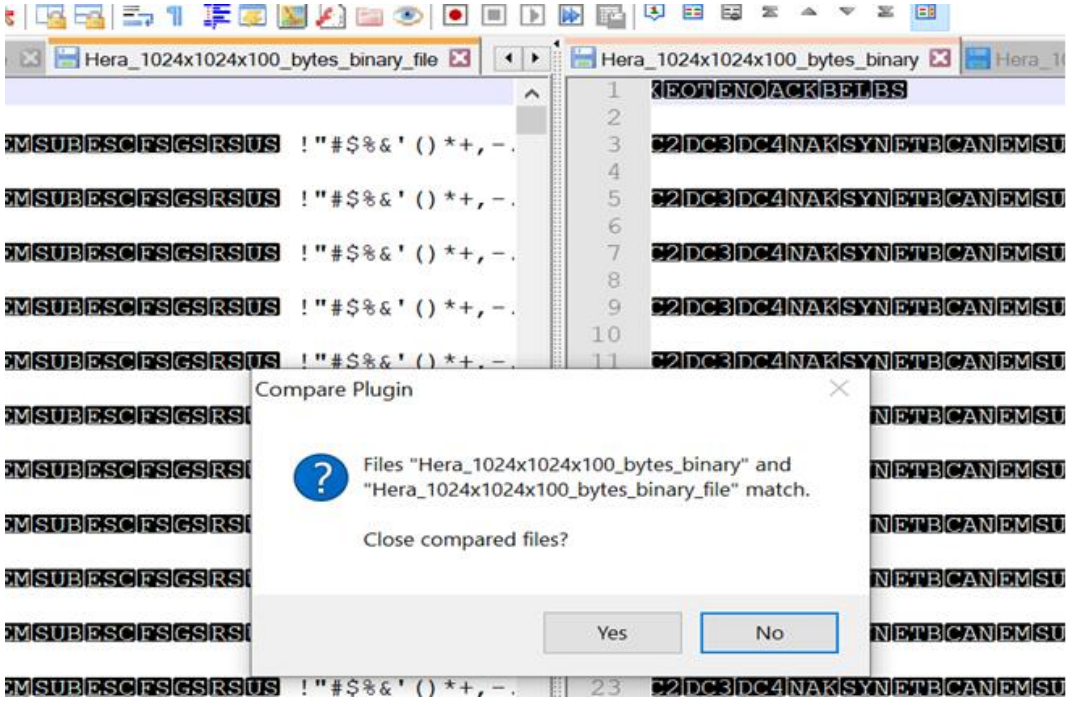
Step3. Prepare the sending and receiving application and start the transmission



UIF : SPW VALIDATION

UIF SPACEWIRE Validation:

Step4. Compare the files with a proper tool to compare the files. After comparison it was concluded that the files were identical and all the data matched after sending and receiving 100 images of size 1024x1024 pixels.



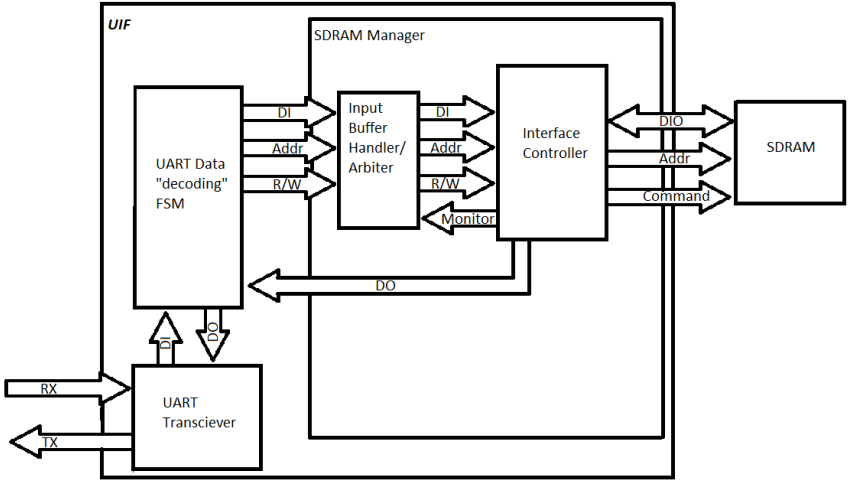
UIF : BOOTING & SDRAM CONTROL

UIF Boot Validation:

- A selected bitstream is successfully loaded into the external Flash memory using ANGIE programmer
- The loaded bitstream is successfully verified using ANGIE programmer
- UIF successfuly reads the bitstream from the external Flash after the power up sequence is complete and if the ANGIE programmer is disconnected

UIF SDRAM Validation:

- Random Address Access
- Large Data sequences using .bin files
- 50 MHz Operating Frequency
- Data Rate up to 380 Mbps

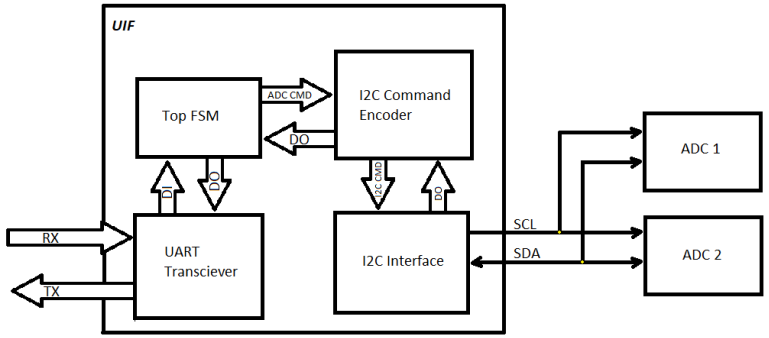


Simplified Architecture Overview

UIF : HOUSEKEEPING

UIF Housekeeping Validation:

- The ADCs are successfully responding to basic commands via I2C
- The conversion result is successfully returned to EGSE



Simplified Architecture Overview

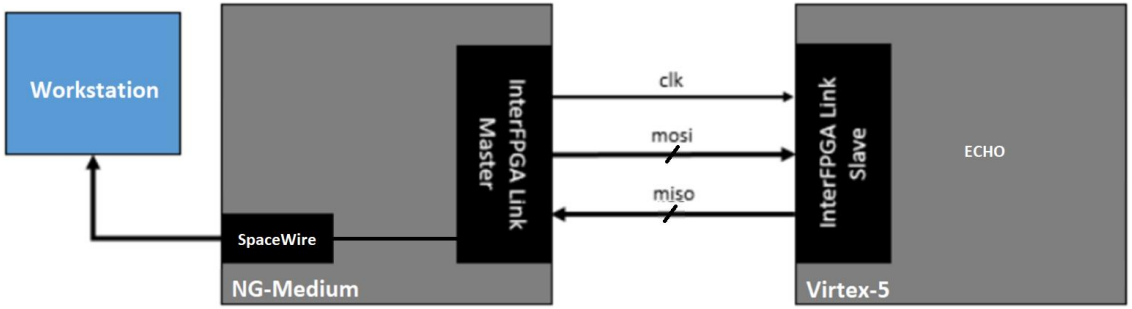
INTERFPGA LINK : SINGLE LINES

Implementation:

- Inherited from CAMPHORVNAV
- LVCMOS single lines
- Parallel communication bus (8 bits of data, 1 bit for control), bidirectional (miso, mosi signals)

Tests Results:

- Maximum clk frequency: 6.25 MHz
- Achievable data-rate (without parity bit error) 6.25 MBps
- metastability problems for clk frequencies greater than 6.25 MBps



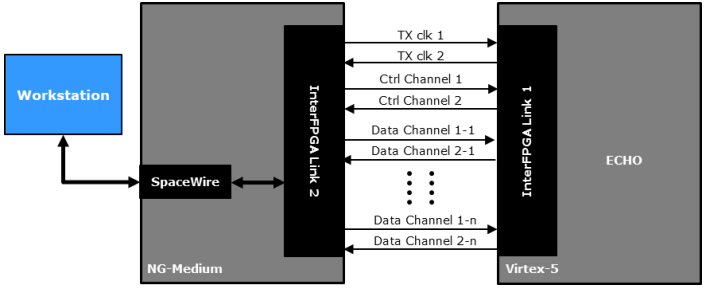
INTERFPGA LINK : LVDS LINES

Implementation:

- Tailored for HERA IPU
- LVDS lines
- scalable/ configurable (up to 8 channels)
- Serial bus
- FDIR
- Flow Control

Tests Results:

- Clk frequency: 100 MHz
- Achievable data-rate (without errors) 20 MBps (using 2 channels)
- Communication fails for HW-in-the-loop tests with 3 channels, probable causes:
  - Longer delay paths in INTERFPGA_LVDS7 and/or INTERFPGA_LVDS8 that avoid correct sampling of received bits at 100 mbps
  - INTERFPGA_LVDS7 and/or INTERFPGA_LVDS8 are damaged and there is no continuity between both FPGAs in these paths



UPF : BOOTING

UPF Boot on Virtex-5 FPGA:

- UPF successfully turns on after UIF is enabling the power tree without sequential power-up
- UPF successfully turns on after UIF is enabling the power tree with sequential power-up
- UPF successfully turns on after being shut down by the UIF and after a brief delay the power tree is enabled

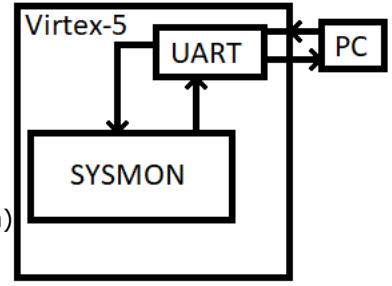
*Note: The UPF will not boot until “V5_Reset” signal is asserted by UIF after the power tree is enabled

UPF : SYSMON

UPF System monitor on Virtex-5 FPGA:

Methods to compare the result:

1. IMPACT application status
2. Proprietary firmware measurement using SYSMON primitive in the following architecture:



(The aimed values requested were for Temperature and Power Consumption)

Values on CHIP:

02 70	01 56	03 4F	-> T: 32,76 C; Vccint: 1.002 V; Vccaux: 2.481 V
02 72	01 55	03 4F	-> T: 33,74 C; Vccint: 0.999 V; Vccaux: 2.481 V
02 71	01 56	03 51	-> T: 33,25 C; Vccint: 1.002 V; Vccaux: 2.487 V

Values on IMPACT:

```
):iMPACT - Current time: 19.10.2020 12:15:44
'** BATCH CMD : readTemperatureAndVoltage -p 1
)evice Temperature: Current Reading:   34.63 C, Min. Reading:   29.70 C, Max. Reading:   35.12 C
'CCINT Supply: Current Reading:   1.002 V, Min. Reading:   0.996 V, Max. Reading:   1.005 V
'CCAUX Supply: Current Reading:   2.484 V, Min. Reading:   2.473 V, Max. Reading:   2.493 V
):iMPACT - Current time: 19.10.2020 12:17:24
'** BATCH CMD : readTemperatureAndVoltage -p 1
)evice Temperature: Current Reading:   35.12 C, Min. Reading:   29.70 C, Max. Reading:   35.61 C
'CCINT Supply: Current Reading:   0.999 V, Min. Reading:   0.996 V, Max. Reading:   1.005 V
'CCAUX Supply: Current Reading:   2.481 V, Min. Reading:   2.473 V, Max. Reading:   2.493 V
):iMPACT - Current time: 19.10.2020 12:17:34
'** BATCH CMD : readTemperatureAndVoltage -p 1
)evice Temperature: Current Reading:   35.12 C, Min. Reading:   29.70 C, Max. Reading:   35.61 C
'CCINT Supply: Current Reading:   0.999 V, Min. Reading:   0.996 V, Max. Reading:   1.005 V
'CCAUX Supply: Current Reading:   2.484 V, Min. Reading:   2.473 V, Max. Reading:   2.493 V
```

Values obtained on chip corresponded to the ones from IMPACT console (including the measurement errors).

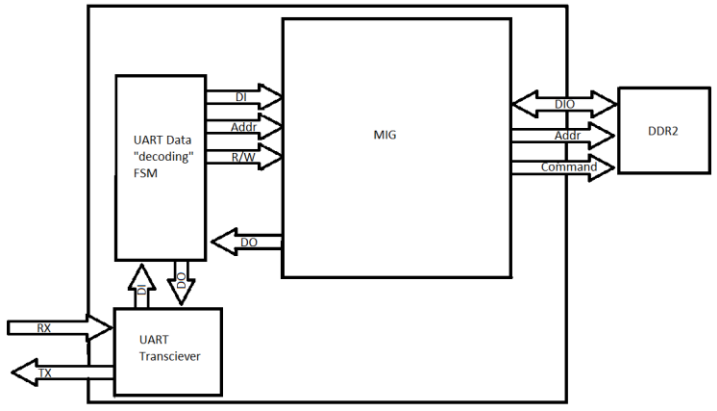
UPF : DDR II CONTROL

UPF DDR2 (1) on Virtex-5 FPGA:

- MIG 3.6.1 Virtex-5 Compliant connection V5 - DDR II
- Used the basic and latest MIG for Virtex-5
- 133 MHz Operating Frequency (250+ Achievable)
- Random Address Access without data corruption

UPF DDR2 (2) on Virtex-5 FPGA:

- MIG 3.6.1 Virtex-5 NonCompliant connection V5 - DDR II
- Used the latest MIG for Virtex-5 with several modifications, especially on initialization process and DCI pins
- 133 MHz Operating Frequency (200+ Achievable)
- Random Address Access without data corruption

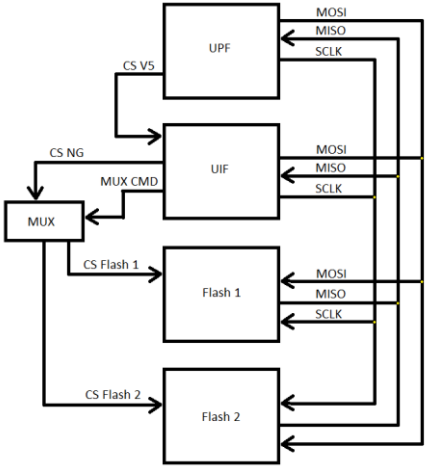


Simplified Architecture Overview

UPF : REPROGRAMMING

UPF Reprogramming Validation:

- The Flash memories can be correctly switched using UIF MUX Command
- The MUX output can be either an output commanded by UIF or a route-through of the UPF's CS
- UIF can successfully access both Flash memories if the correct bitstream generation settings are made for UPF in order to let it's programming pins (corresponding to the SPI lines) on a floating state after successfully loading a bitstream
- UPF bitstreams can be successfully loaded via JTAG on both Flash memories
- When the SPI lines are left by UIF in a floating state (using 3-state pin definition), UPF can successfully read a bitstream from the Flash memory selected by UIF
- UPF can successfully switch between two bitstreams loaded in the same Flash memory

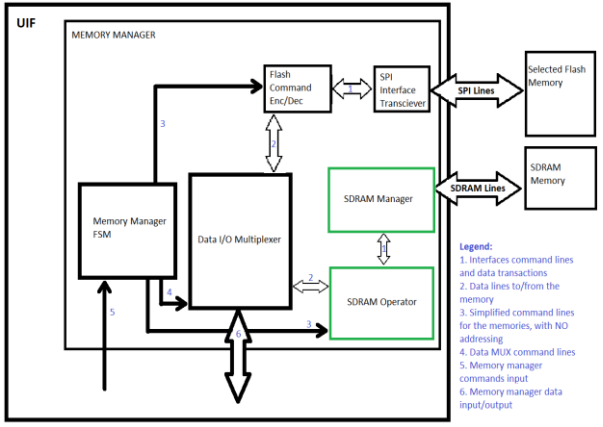


SPI Flash Implementation

UPF : REPROGRAMMING

UPF Reprogramming Validation:

- UIF can successfully write a received bitstream (via UART or SpaceWire) on a selected flash memory, using the architecture presented in the figure
- UPF bitstreams MUST have the settings made in the generation process in order to let the programming pins (corresponding to the SPI lines) on a floating state after the bitstream reading process is completed
- Due to the Flash memory's low data rate on the programming process, the received bitstream (by UIF)will be first saved into UIF's external SDRAM before sending it to the selected Flash memory
- UPF can successfully read an UIF-written bitstream from the selected Flash memory



Simplified Architecture Overview

POWER CONSUMPTION

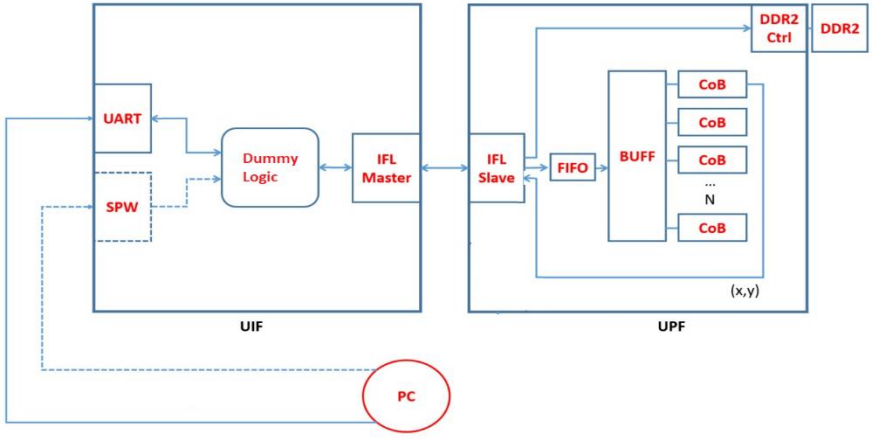
Resources/ Processing:

- 10 x 1024x1024 pixels images (8 bits per pixel)
- 72 parallel HERA Center Of Brightness IP
- UART, IFL, DDR II
- Around 40-50% resource utilization

Tests:

- 28 V, 22 V, 31 V
- 28-31-22 V

Power Supply [V DC]	Current [mA]	Power [W]
28	306	8.56
22	377	8.29
31	281	8.71



Device	
Family	Virtex5
Part	xc5vfx130t
Package	ff1738
Grade	Commercial
Process	Typical
Speed Grade	-1

Environment	
Ambient Temp (C)	30.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	None
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.531	151	---	---
Logic	0.178	42970	81920	52
Signals	0.246	62136	---	---
BRAMs	0.005	4	298	1
PLLs	0.126	1	6	17
IOs	0.521	69	840	8
Leakage	1.832			
Total	3.440			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.1	76.8	37.3

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	2.310	0.969	1.341
Vccaux	2.500	0.330	0.034	0.296
Vcco33	3.300	0.008	0.000	0.008
Vcco18	1.800	0.405	0.000	0.405

		Total	Dynamic	Quiescent
Supply	Power (W)	3.890	1.053	2.836

THERMAL CONSIDERATIONS & DC/DCS

Component	Temp Measured
Virtex5	40
NG-Medium	43
DC/DC 28 a 5	38
DC/DC 1 V5	41
DC/DC 1.2 NG	39
DC/DC 1.8 V5	37
DC/DC 2.5 V5	37
DC/DC 2.5 NG	36
DC/DC 3.3 V5	35
DC/DC 3.3 NG	35

DC/DC [V]	PP_{28V} [V]	PP_{22V} [V]	PP_{31V} [V]	PP_{28Vi} [V]
1.2	1.11 – 1.31	1.19 – 1.23	1.19 – 1.23	1.21 – 1.25
2.5	2.49 – 2.45	2.49 – 2.45	2.45 – 2.49	2.51 – 2.57
1.0	0.99 – 1.03	0.99 – 1.03	0.99 – 1.03	1.01 – 1.05
2.5	2.45 – 2.49	2.45 – 2.49	2.45 – 2.49	2.47 – 2.51
1.8	1.81 – 1.83	1.79 – 1.83	1.79 – 1.85	1.81 – 1.85
3.3.	3.25 – 3.29	3.27 – 3.31	3.27 – 3.31	3.29 – 3.33

HERA IP-ICU

THERMAL ABALYSIS & MEASUREMENTS

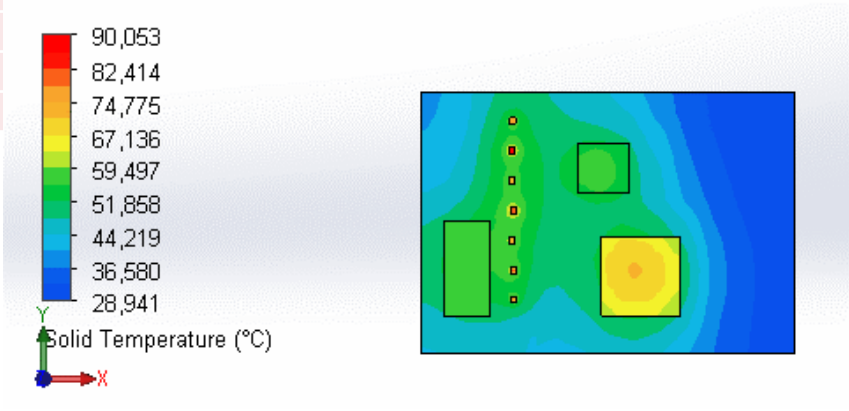
THERMAL ANALYSIS: WCA GROUND

Worst Case Analysis @ Ground Condition (25ºC & 101325 Pa)

Component	Numb	Power Dissipated	Temp at ambient with radiation
Virtex5	V5	6	69,2
NG-Medium	NG	3	57,6
DC/DC 28 a 5	DCDC_1	3,2	58
DC/DC 1.2 V5	4	0,945	80
DC/DC 1.2 NG	6	0,405	89,8
DC/DC 1.8	1	0,7245	79,226
DC/DC 2.5 V5	3	0,48	73
DC/DC 2.5 NG	5	0,48	72,6
DC/DC 3.3 V5	2	0,66	79,261
DC/DC 3.3 NG	7	0,66	76,9

Considerations for Worst Case:

- Max. Power dissipation achievable by the component taking into account the voltages and the efficiency of the components.



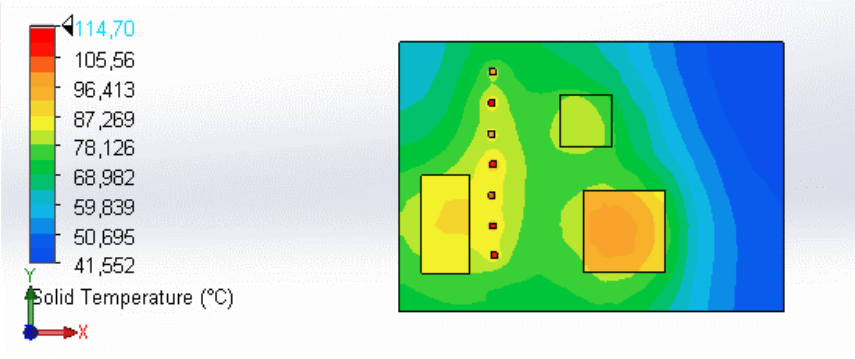
THERMAL ANALYSIS: WCA VACUUM

Worst Case Analysis @ Vacuum Condition (25ºC & 0 Pa)

Component	Numb	Power Dissipated	Vacuum condition
Virtex5	V5	6	99,21
NG-Medium	NG	3	82
DC/DC 28 a 5	DCDC_1	3,2	86,8
DC/DC 1.2 V5	4	0,945	107,45
DC/DC 1.2 NG	6	0,405	114,6
DC/DC 1.8	1	0,7245	109,1
DC/DC 2.5 V5	3	0,48	101,6
DC/DC 2.5 NG	5	0,48	98,6
DC/DC 3.3 V5	2	0,66	108,92
DC/DC 3.3 NG	7	0,66	99,8

Considerations for Worst Case:

- Max. Power dissipation achievable by the component taking into account the voltages and the efficiency of the components.

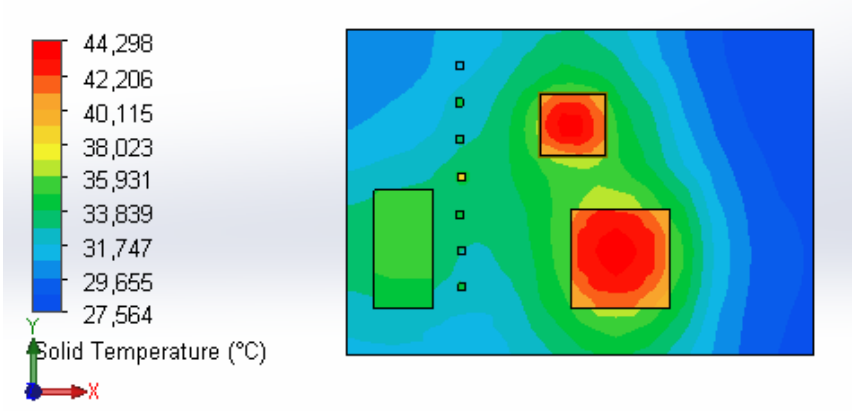


THERMAL ANALYSIS: RCA GROUND

Real Case Analysis @ Ground Conditions

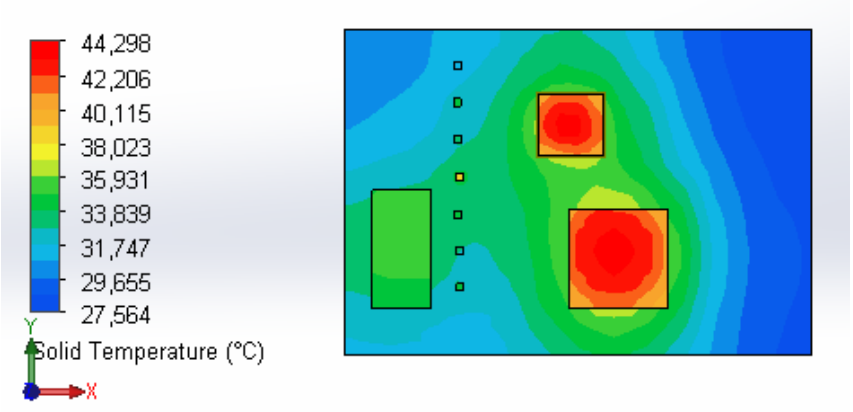
Considerations:

- Power consumption obtained from simulations
- Efficiency of the DC/DC converters
- T=25ºC
- P=101325 Pa



Component	Numb	Power Dissipated	Temp at ambient with radiation
Virtex5	V5	2,4	44,038
NG-Medium	NG	1,4	43,83
DC/DC 28 a 5	DCDC_1	1	35,351
DC/DC 1 V5	4	0,1507	39,085
DC/DC 1.2 NG	6	0,07535	34,685
DC/DC 1.8 V5	1	0,056	34,381
DC/DC 2.5 V5	3	0,0444	34,78
DC/DC 2.5 NG	5	0,0259	33,45
DC/DC 3.3 V5	2	0,001188	32,9
DC/DC 3.3 NG	7	0,000693	31,4

THERMAL MEASUREMENTS



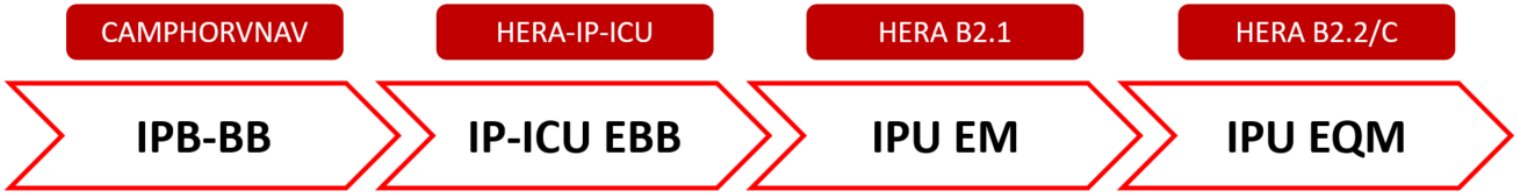
Component	Numb	Power Dissipated	Temp at ambient with radiation	Temp Measured
Virtex5	V5	2,4	44,038	40
NG-Medium	NG	1,4	43,83	43
DC/DC 28 a 5	DCDC_1	1	35,351	38
DC/DC 1 V5	4	0,1507	39,085	41
DC/DC 1.2 NG	6	0,07535	34,685	39
DC/DC 1.8 V5	1	0,056	34,381	37
DC/DC 2.5 V5	3	0,0444	34,78	37
DC/DC 2.5 NG	5	0,0259	33,45	36
DC/DC 3.3 V5	2	0,001188	32,9	35
DC/DC 3.3 NG	7	0,000693	31,4	35

RID-02

HERA IP-ICU

ROADMAP TO EM & EQM

IDEAL SCHEDULE



- NG-Medium Devkit + ML605
- IP: RelNav HW
- 2 SpaceWire I/Fs
- TRL 4/5

- Single Board EBB
- NG-Medium & Virtex-5
- No Image Processing
- 2 SpaceWire I/Fs
- TRL 4/5

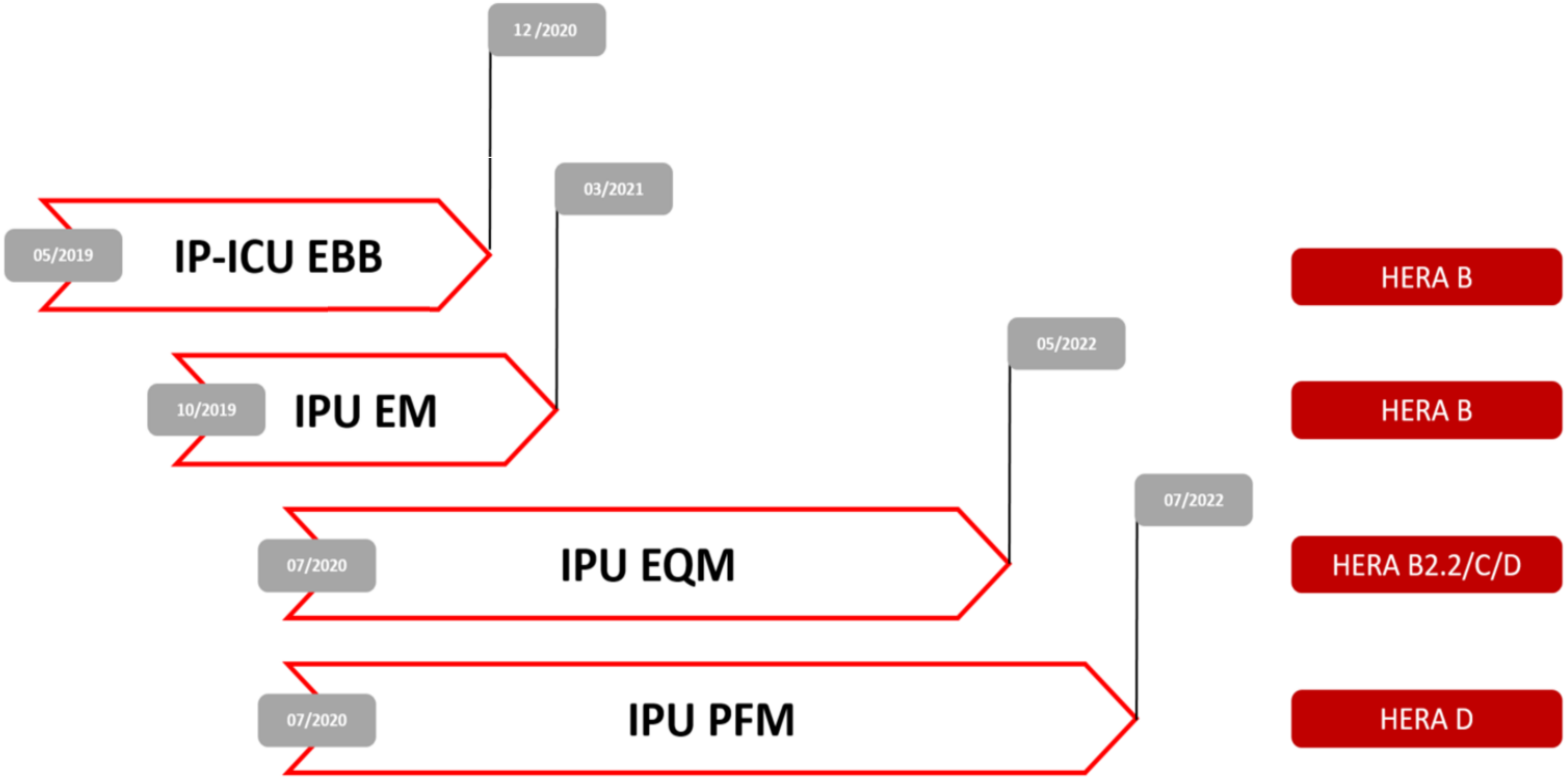
- Higher TRL Model of IP-ICU
- IP1: Centroid HW
- IP2: RelNav HW
- Reconfiguration capability
- 2 SpaceWire I/Fs
- TRL 6

- Higher TRL Model of IPU EM
- Space Components
- TRL 7

- Higher TRL Model of IPU EQM
- Space Components
- TRL 8

REAL SCHEDULE

RID-06



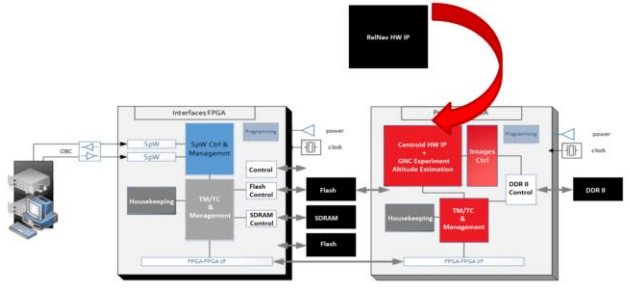
IPU EM

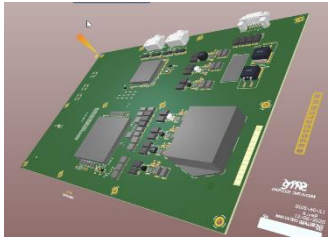
Evolution of IP-ICU EBB Skeleton into fully functional EM

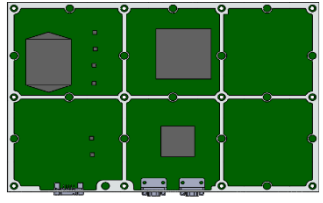
- Electronics
  - Replacement of passive components. There will be chosen similar packages in dimensions and weight for the EM model based on the target space graded components.
  - The purpose is the full compliance to ECSS of the PCB design.
  - Some critical electronic components will be maintained components (FPGAs, memories, secondary DC/DCs, Xceivers), only main DC/DC will be replaced with ArcPower 28V/ 5V component (representativeness for space grade components)
  - Removal of jumpers, switches, push-buttons
  - Removal of LEDs and transistors that drive the LEDs
  - Some uncompliant VIAs and update the design based on manufacturer recommendations (some vias dimensions associated to BGA components, some traces widths associated to DDR II memories and copper balancing on layers)
  - Update and keep only the conclusion of the SPI Flash reprogramming for Virtex5. On IP-ICU an IC MUX has been used for SPI flash selection. This components should be physically removed and the functionality to be implemented in NG-Medium VHDL Code

- VHDL Code Integration & Updates to CAMPHORVNAV heritage
  - CoB/ LAMB (Center of Brightness) Image Processing Algorithm
  - RelNav Modifications tailored for HERA mission
  - SpaceWire management for only one VHDL Router
  - PUS 5, PUS 17
  - SDRAM Controller for the external volatile memory allocated to UIF
  - Virtex-5 Reprogramming
  - LVDS InterFPGA Link
  - MIG-5 DDR II Controller for the external volatile memory allocated to Virtex-5

- Mechanical Integration
  - Replacement of connectors with ones which will be integrated into the mechanical enclosure design
  - Metallic enclosure box with stiffeners







LAYOUT FOR EM

Small changes in placement of main components compared to Hera IP-ICU design.

Due to mechanical design and integration, the primary side (where most components will be placed) is now the bottom side.

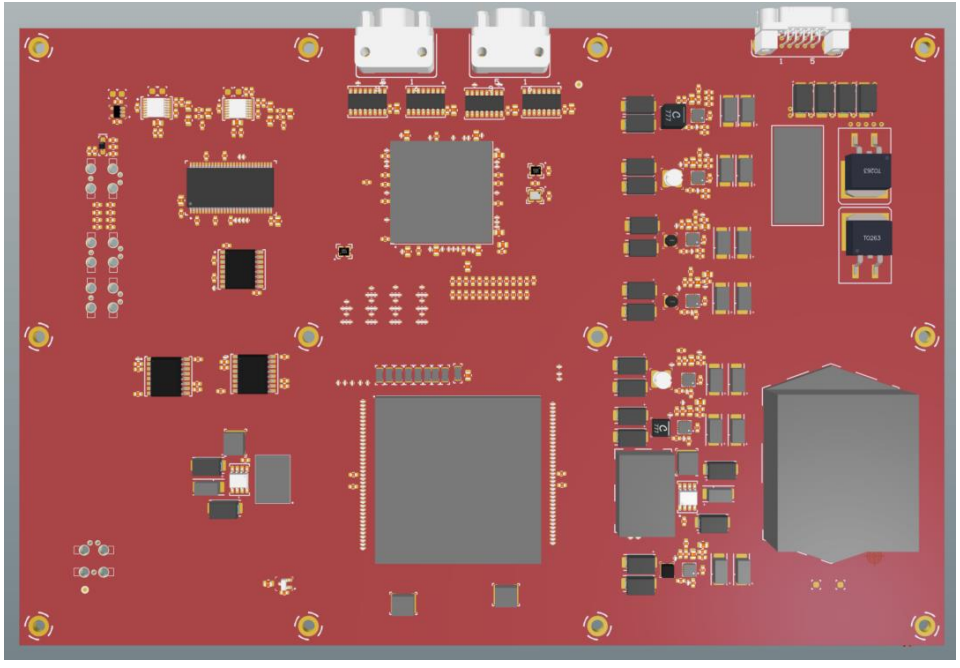
Board size increased slightly to 240 mm x 160 mm.

Mounting holes will be redistributed and added to accommodate stiffener design.

Targeting 12 layers with 1.6mm overall thickness, same as in HERA IP-ICU design.

Layout design will follow ECSS standards

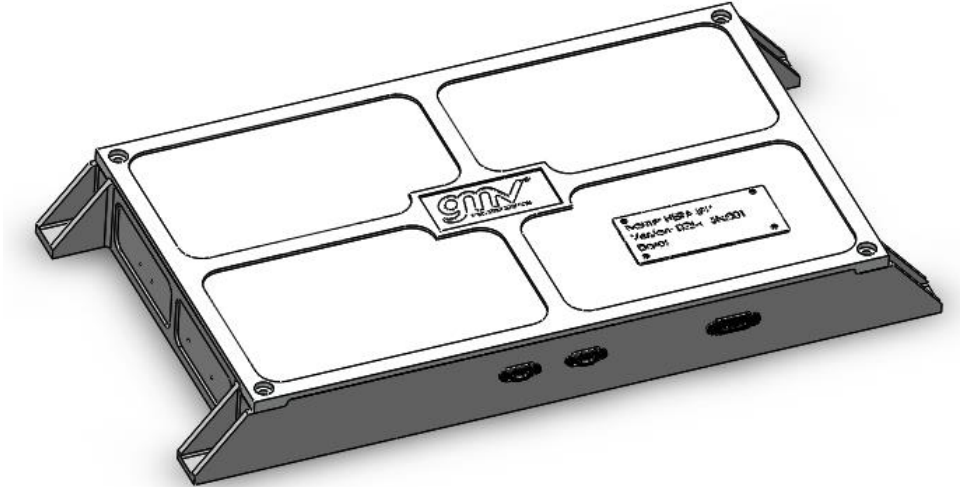
EMC, Signal integrity and thermal dissipation layout practices will be applied.

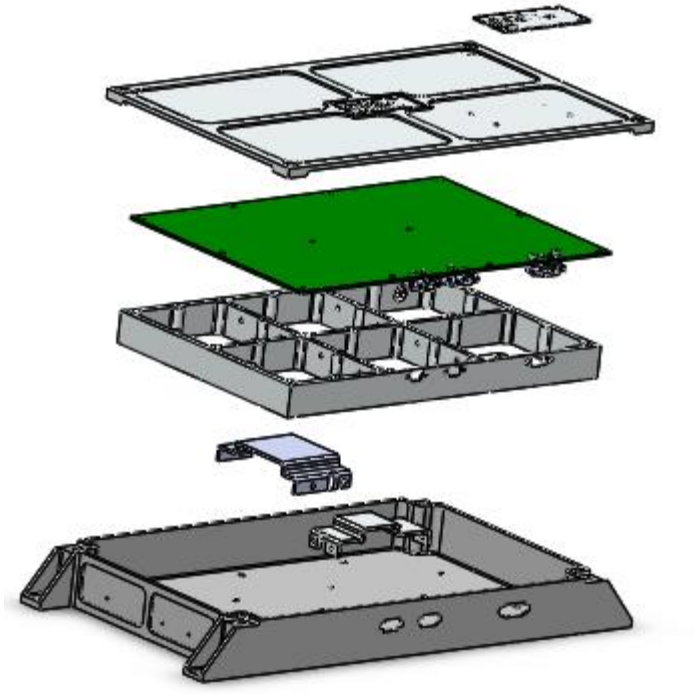


MECHANICAL DESIGN OVERVIEW

The mechanical enclosure has been designed in order to increase:

- Thermal Dissipation creating direct thermal dissipation paths to the bottom plate
- Mechanical Stiffness of the PCB
- Increase Electrical conductivity





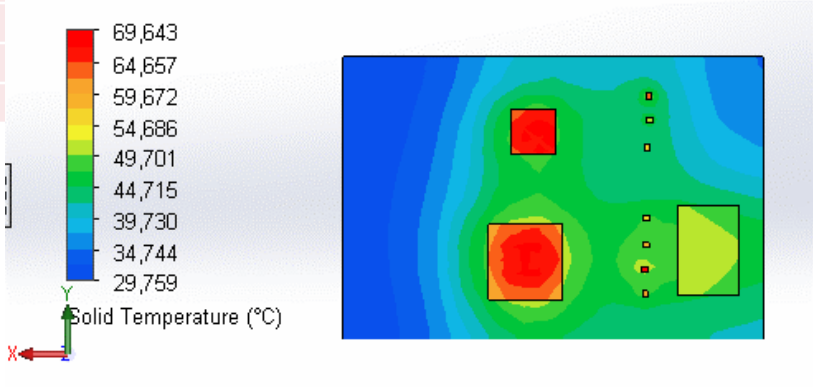
THERMAL ANALYSIS: IPU WCA GROUND

Worst Case Analysis for Ground Conditions (T=25ºC – P=101325 Pa)

Component	WCAnalysis	Error Margin (20%)	Ground Environment
Virtex5	6	7,2	67,8
NG-Medium	3	3,6	67,3
DC/DC 28 a 5	3	3,6	50
DC/DC 1.2 V5	0,531953125	0,63834375	69,5
DC/DC 1.2 NG	0,531953125	0,63834375	64
DC/DC 1.8	0,36	0,432	60,1
DC/DC 2.5 V5	0,225	0,27	55,25
DC/DC 2.5 NG	0,225	0,27	51,9
DC/DC 3.3 V5	0,297	0,3564	59,6
DC/DC 3.3 NG	0,297	0,3564	55,2

Considerations for Worst Case:

- Max. Power dissipation achievable by the component taking into account the voltages and the efficiency of the components.

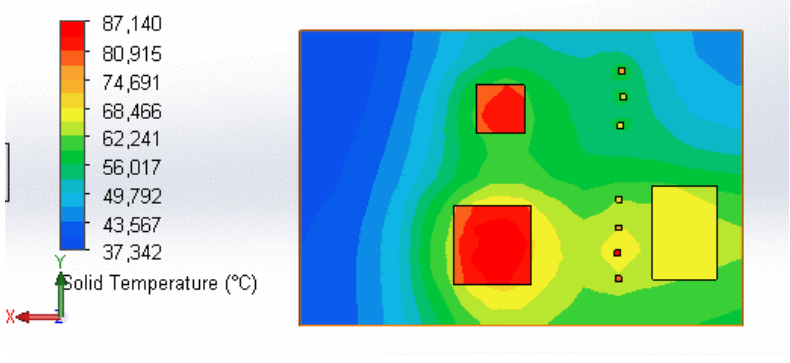


THERMAL ANALYSIS: IPU WCA VACUUM

RID-03

Worst Case Analysis for Vacuum Conditions (T=25ºC – P=0 Pa)

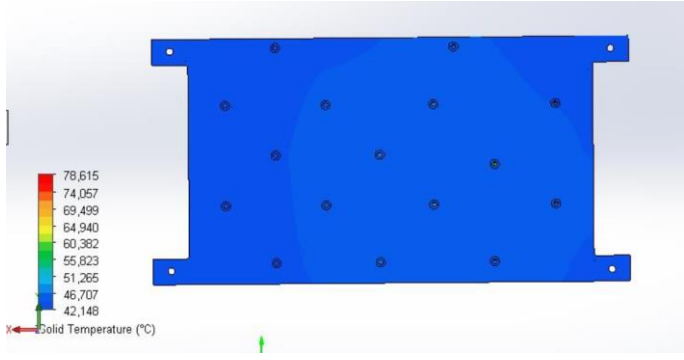
Component	WCAnalysis	PC with 20% Margin	Temp. Raised
Virtex5	6	7,2	90,25
NG-Medium	3	3,6	86,71
DC/DC 28 a 5	3	3	68,33
DC/DC 1 V5	0,532	0,638	88,51
DC/DC 1.2 NG	0,532	0,638	77,55
DC/DC 1.8	0,360	0,432	79,07
DC/DC 2.5 V5	0,225	0,270	70,89
DC/DC 2.5 NG	0,225	0,270	64,29
DC/DC 3.3 V5	0,297	0,356	77,64
DC/DC 3.3 NG	0,297	0,356	68,63

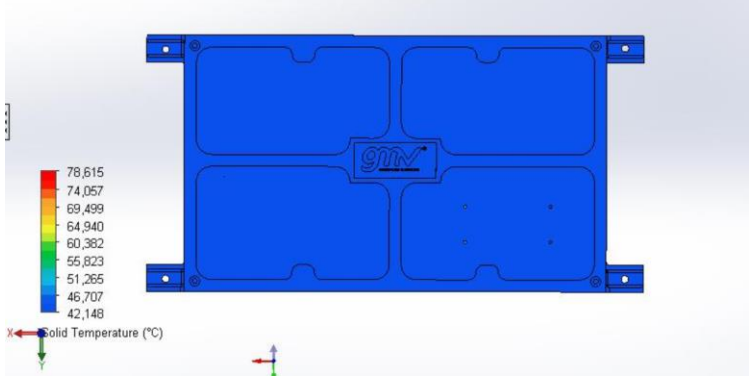


THERMAL ANALYSIS: WCA VACUUM ALL

Worst Case Analysis for Ground Conditions (T=25ºC – P=0 Pa)

Component	WCAnalysis	PC with 20% Margin	Temp. Raised
Virtex5	6	7,2	62,4
NG-Medium	3	3,6	63,7
DC/DC 28 a 5	3	3	60,9
DC/DC 1 V5	0,532	0,638	81,23
DC/DC 1.2 NG	0,532	0,638	77,33
DC/DC 1.8	0,360	0,432	70,47
DC/DC 2.5 V5	0,225	0,270	62,9
DC/DC 2.5 NG	0,225	0,270	62,38
DC/DC 3.3 V5	0,297	0,356	70,28
DC/DC 3.3 NG	0,297	0,356	64,82
PCB	-	-	68,6
Stiffener	-	-	46,5





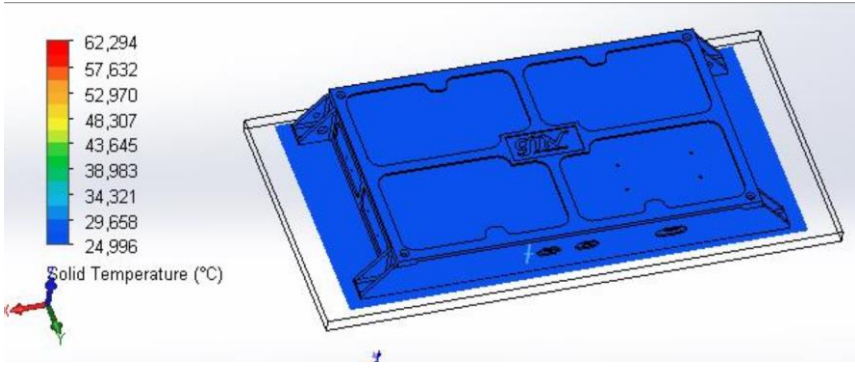
Considerations:

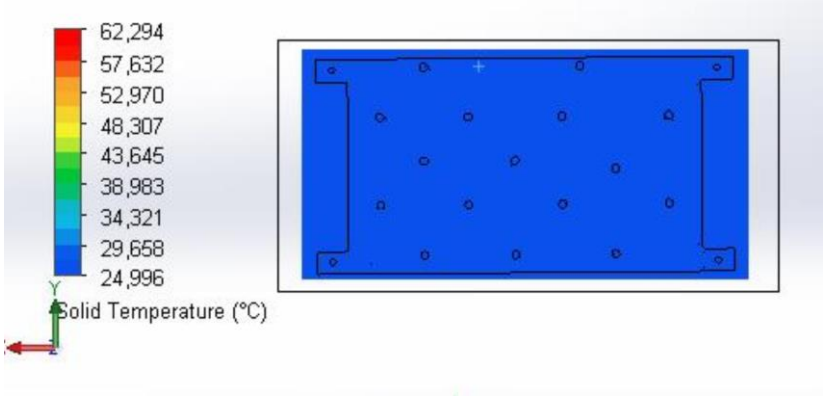
- Includes all the mechanical enclosure described.

THERMAL ANALYSIS: WCA REAL ENVIRONMENT

Worst Case Analysis for Ground Conditions (T=25ºC – P=0 Pa)

Component	WCAnalysis	PC with 20% Margi	Temp. Raised
Virtex5	6	7,2	42,2
NG-Medium	3	3,6	44,3
DC/DC 28 a 5	3	3	41,19
DC/DC 1 V5	0,532	0,638	63,5
DC/DC 1.2 NG	0,532	0,638	59,2
DC/DC 1.8	0,360	0,432	51,74
DC/DC 2.5 V5	0,225	0,270	43
DC/DC 2.5 NG	0,225	0,270	43
DC/DC 3.3 V5	0,297	0,356	50,7
DC/DC 3.3 NG	0,297	0,356	46,4
PCB	-	-	50
Stiffener	-	-	26





Considerations:

- Includes all the mechanical enclosure described.
- Includes also a panel in the bottom plate at constant temperature as in the satellite.

THERMAL ANALYSIS: COMPARISON

Comparison Table with all the results obtained:

Component	Ground Environment	Vacuum	Vacuum Enclosure	Vacuum Enclosure Satellite Case
Virtex5	67,8	90,25	62,4	42,2
NG-Medium	67,3	86,71	63,7	44,3
DC/DC 28 a 5	50	68,33	60,9	41,19
DC/DC 1 V5	69,5	88,51	81,23	63,5
DC/DC 1.2 NG	64	77,55	77,33	59,2
DC/DC 1.8	60,1	79,07	70,47	51,74
DC/DC 2.5 V5	55,25	70,89	62,9	43
DC/DC 2.5 NG	51,9	64,29	62,38	43
DC/DC 3.3 V5	59,6	77,64	70,28	50,7
DC/DC 3.3 NG	55,2	68,63	64,82	46,4
PCB	-	-	68,6	50
Stiffener	-	-	46,5	26

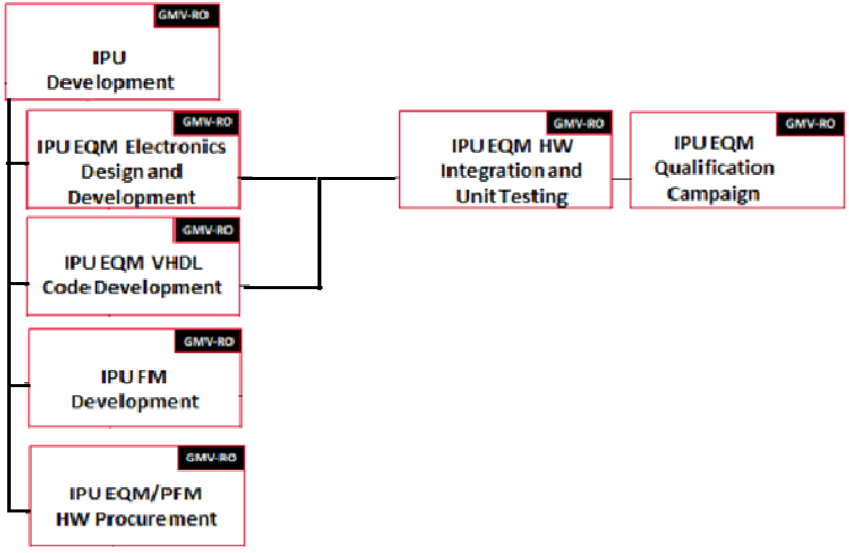
THERMAL ANALYSIS: NEXT SIMULATIONS

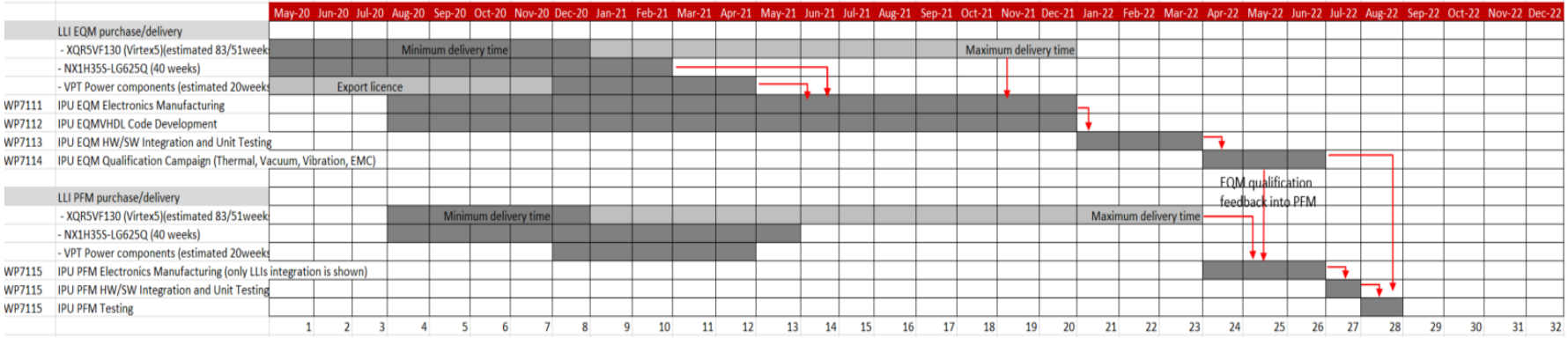
Next Simulations to be performed:

Sim. Numb	Description	Radiation	Temp Baseplate
1	Vacuum with refrigeration in baseplate.	No	25
2	Vacuum with refrigeration in baseplate.	Si	-30
3	Vacuum with refrigeration in baseplate.	Si	0
4	Vacuum with refrigeration in baseplate.	Si	50
5	Vacuum with refrigeration in baseplate.	Si	70
6	Vacuum with refrigeration in baseplate.	No	25
7	Vacuum with refrigeration in baseplate.	Si	-30
8	Vacuum with refrigeration in baseplate.	Si	0
9	Vacuum with refrigeration in baseplate.	Si	25
10	Vacuum with refrigeration in baseplate.	Si	50
11	Vacuum with refrigeration in baseplate.	Si	70

IPU EQM & PFM

- Parallel development EQM & PFM
- Qualification Campaign in 2022
  - Thermal, Vacuum, Vibrations, Shock, EMI, EMC tests
  - Radiation Analysis





ROADMAP

ECSS SOLDERING

RID-07

- For EQM & PFM
- 3 companies evaluated with Rfi
- Analysis for entire EQM BOM
- Full ECSS qualification not available for soldering of some components

Option 1	Option 2	Option 3
➢ CGA-625 (no capability of soldering it) ➢ CGA-1752 (no capability of soldering it) ➢ other 31-37 packages	➢ Chip cap 0402 AVX BME flex ➢ Nicomatic Connector ➢ SOP20 ➢ SOP24 ➢ SOP74 ➢ CFP20 metal base (but full ESA verification for the for CFP16 Metal base) ➢ QFP84 with metal base ➢ VPT through hole components (5 pin and 10 pin) ➢ 1752 CCGA (at project level data a full ESA verification in progress but with an ENIG substrate finish) ➢ 625 CCGA (project level verification on a similar component) ➢ 4J lead Q-Tech (D29recommend "flip and wire" for this component shape)	➢ C0402 II BME (but CNC19 qualified at ECSS level) ➢ C1206 II BME (but CNC12 qualified at ECSS level) ➢ C2220 II BME (but CDR35BX qualifeid at ECSS level) ➢ SOP-20 ➢ SOP-24 ➢ BGA-95/ SOP-74 ➢ 5 PIN THT (but STF28-461 qualified at 350 TC) ➢ 10 PIN THT (but SMHF2805D qualified at 350 TC) ➢ C0603 II BME (qualified at project level, -55/100 Celsius, 68 TC) ➢ C0805 II BME (qualified at project level, -55/100 Celsius, 68 TC) ➢ SESI-14SR (qualified at project level, -55/100 Celsius, 200 TC) ➢ C0805 I (qualified at project level, -55/100 Celsius, 350 TC) ➢ LCC-2D (qualified at project level, -55/100 Celsius, 350 TC) ➢ FP-8 (qualified at project level, -55/100 Celsius, 350 TC) ➢ SOP-54 (qualified at project level, -55/100 Celsius, 350 TC) ➢ SOP-84 (qualified at project level, -55/100 Celsius, 350 TC) ➢ CGA-625 (full qualifiecation on-going) ➢ CGA-1752 (full qualification on-going, but for NanoXplore NG-Large component)

HERA IP-ICU

CONCLUSIONS & AoB

CONCLUSIONS

- IP-ICU EBB Skeleton Validated
  - Power Tree (IP-ICU PSU BB)
  - Interfaces
  - Power Consumption & Overall functionality

- IP-ICU EBB Fully compliant to HERA mission needs
  - 2 x SpaceWire I/Fs providing >10 Mbps (autostart/ autodetect functionality included)
  - External volatile memory (SDRAM) allocated to UIF for Navigation Image Reconstruction/ Pre-Processing
  - Processing Capabilities by means of UPF Virtex-5 & allocated external volatile memory (DDR II)
  - Reprogramming Capabilities (Centroid & RelNav IPs can be stored prior launching into one flash memory; second flash memory allocated to Virtex-5 can be let for in-flight reprogramming with bitstreamm received from ground)
  - Counterflight parts identified for IP-ICU EBB electronic components

- ESR, TAT, WAT, CCD To be delivered

- FR Minutes of Meeting to be sent by GMV for review and signing

AoB

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THANK YOU

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