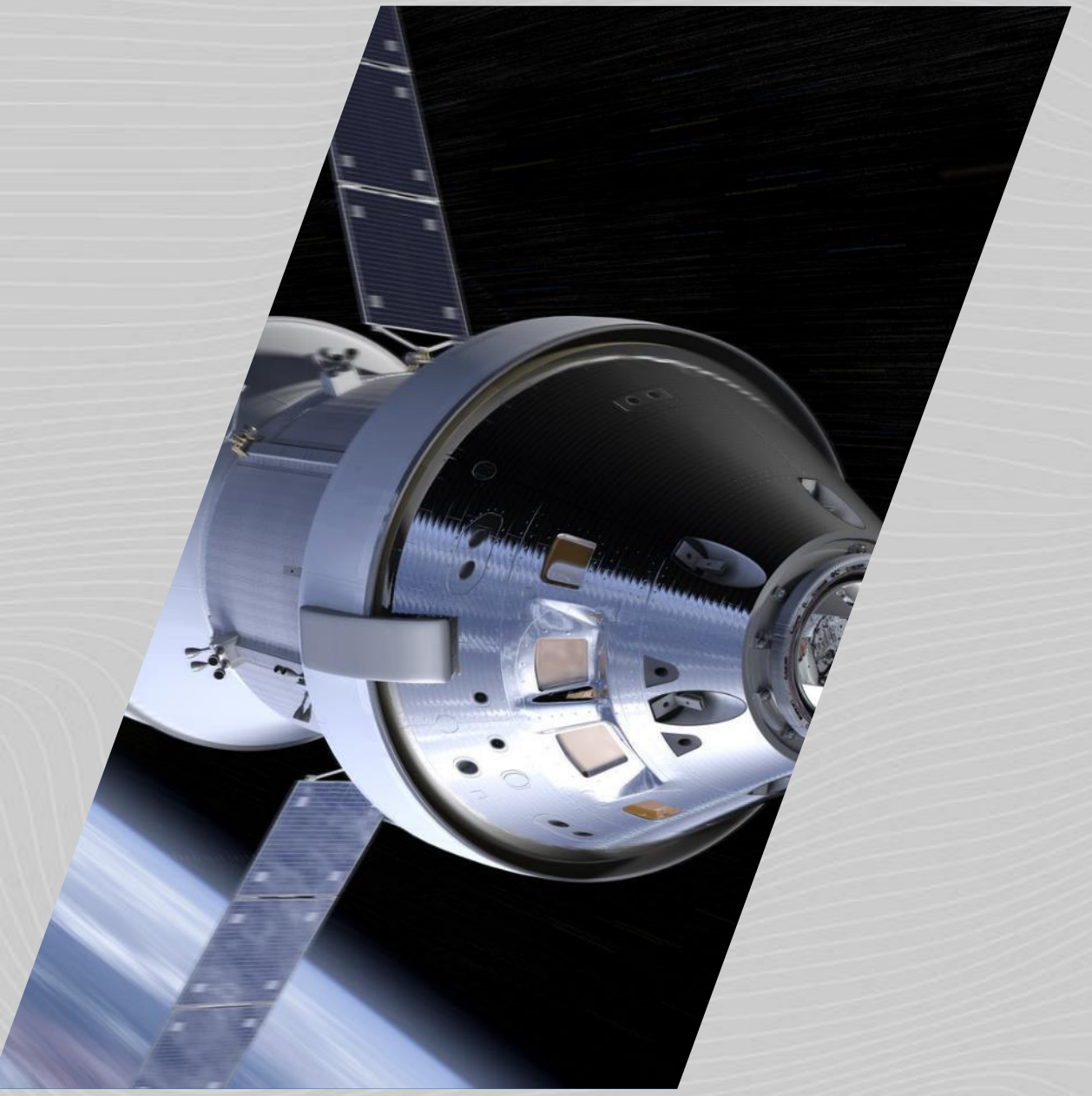
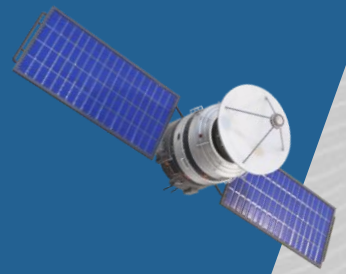


CAES PIONEERING ADVANCED ELECTRONICS

GR740 Next Generation Microprocessor Flight Models

TEC-ED & TEC-SW Final Presentation Day

June 2021



Abstract

- The **GR740** microprocessor has been developed within ESA's NGMP (Next Generation MicroProcessor) initiative in TRP, GSTP and EOP programmes, accompanied also by several activities to consolidate the SW ecosystem.

- The Phase 3 contract dedicated to the production of GR740 Flight Models has now been completed. Screening / qualification tests per MIL-PRF-38535L / MIL-STD-883K and delta-evaluation per ESCC-2269000 have been passed successfully.

- QML-V & QML-Q equivalent flight parts can now be ordered, and first users have already designed GR740 into their equipment.

- QML-V and QML-Q qualified parts will be offered once the certification is granted by the DLA.

Agenda

- **About Cobham Gaisler**
- **Start at the finish line**
  - Where are we now?
- **Back to the beginning**
  - When, why, what, where?
- **Hurdles along the way**
  - Package development
  - Over Pad Metallisation
  - Wire bonding
  - Selection of columns
  - Design changes
- **We have made it**
  - GR740 qualification results
- **And now what?**
  - RoadMap

CAES PIONEERING ADVANCED ELECTRONICS

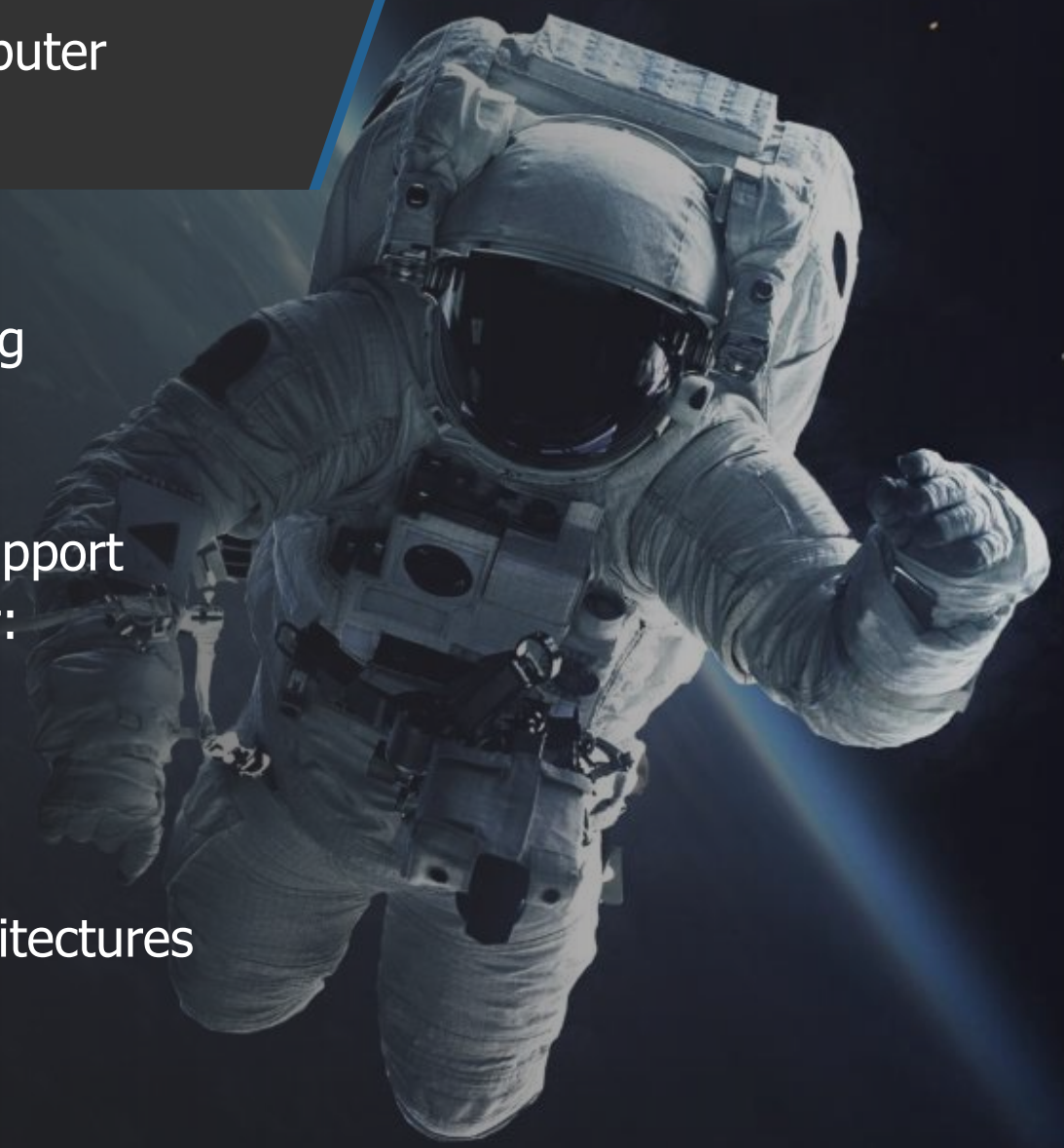
A world leader in embedded computer systems for harsh environments

Experts in fault-tolerant computing

We provide a full ecosystem to support hardware and software design for:

- Standard components
- Semi-custom FPGA
- Full custom ASIC

Based on SPARC and RISC-V architectures



CAES PIONEERING ADVANCED ELECTRONICS

Established 2001, 20-year anniversary!

- Acquired by Aeroflex in 2008
- Acquired by Cobham in 2014
- Acquired by Advent in 2020

Main office located in Gothenburg, Sweden

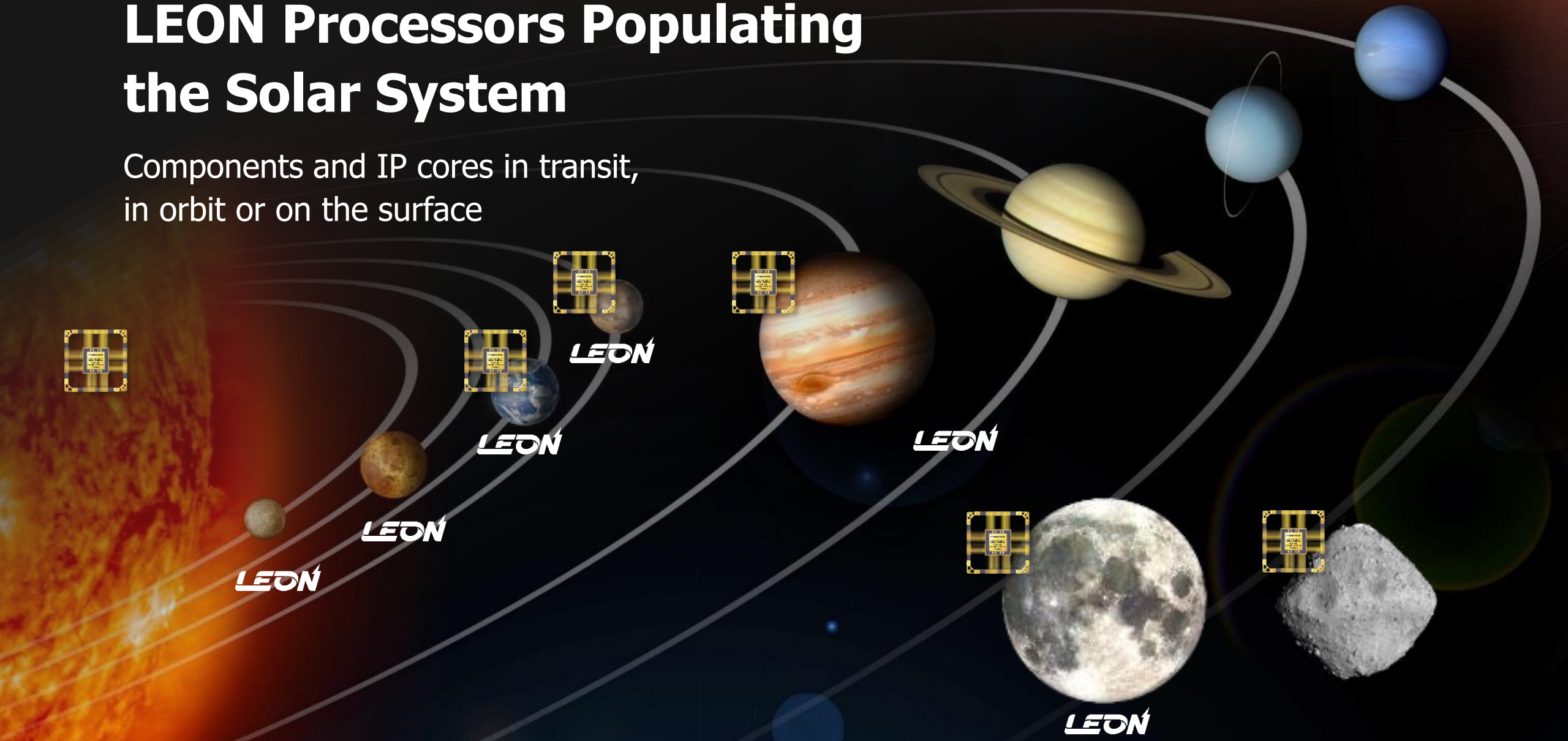
48 staff + 10 consultants + 6 students

In-house facilities

- ASIC and FPGA design
- Software
- Component lab

LEON Processors Populating the Solar System

Components and IP cores in transit, in orbit or on the surface



9 out of 10 instruments in Solar Orbiter use the LEON3FT

Launched February 2020

Components

High-reliability

- **Radiation hardened**
- **Space qualified**
- **Fault-tolerant**

NOEL Processor Family

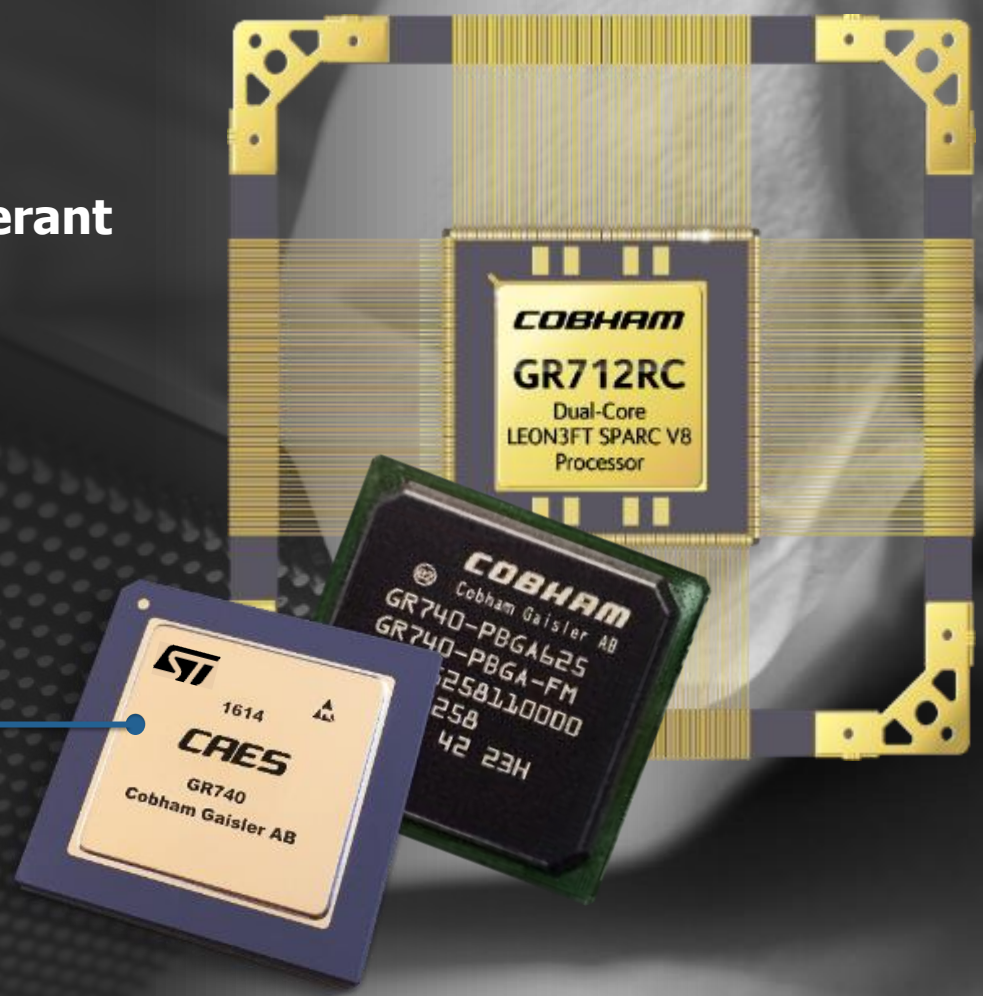
- GR7xv, NOEL-V, 16-Core, in development

LEON Processor Family

- GR765, LEON5FT, in development
- GR740, LEON4FT, quad-core, 250 MHz, QML-V approval exp. Q2 2021
- GR740 PBGA, LEON4FT, quad-core, 250 MHz, prototypes Q2 2021
- GR716A, LEON3FT, single-core, 50 MHz, ESCC 9000 screening exp. Q2 2021
- GR716B, LEON3FT, single core 100 MHz, in development
- GR712RC, LEON3FT, dual-core, 100 MHz, Vendor class S
- UT700, LEON3FT, single-core, 166 MHz, QML-Q, QML-V
- UT699E, LEON3FT, single-core, 100 MHz, QML-Q, QML-V
- UT699, LEON3FT, single-core, 66 MHz, QML-Q, QML-V

Interconnect

- GR718B, Vendor class S



Start at the finish line

TEC-ED & TEC-SW Final Presentation Day

Why start at the finish line?
Because the finish line for this project is today

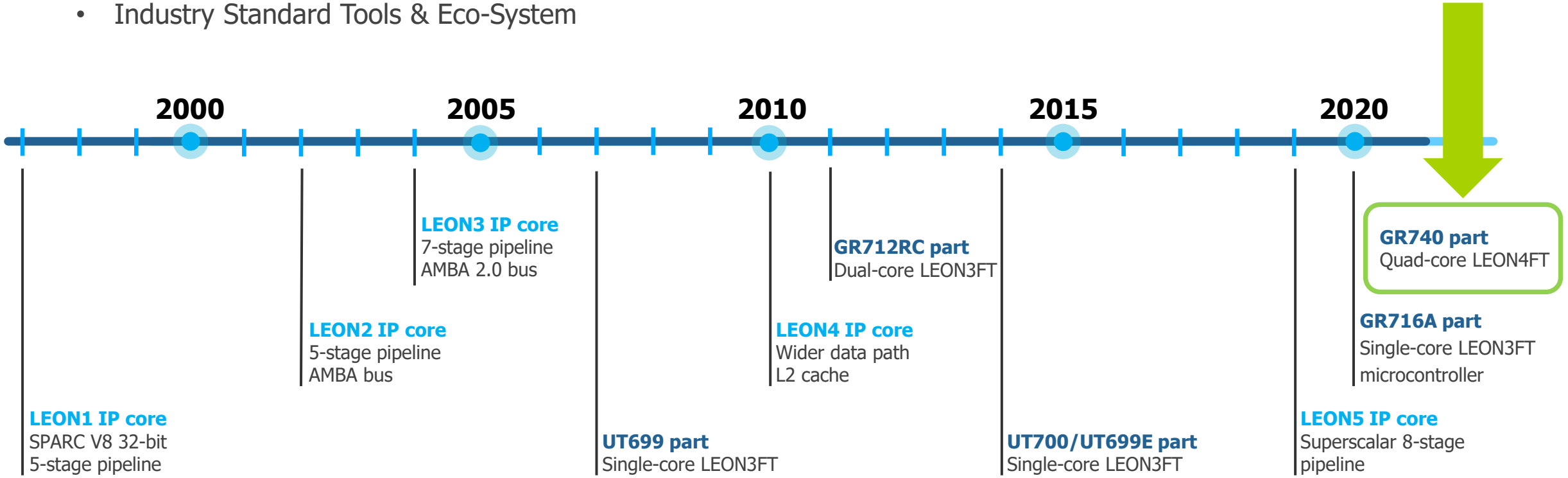
So let us talk about:

- 20 years of LEON processors
- Where we are now with the GR740
- How we got here

The finish line, is it?

LEON Technology – over 20 years of space success

- Five generation LEON SPARC V8 processors
- Space proven technology
- Industry Standard Tools & Eco-System



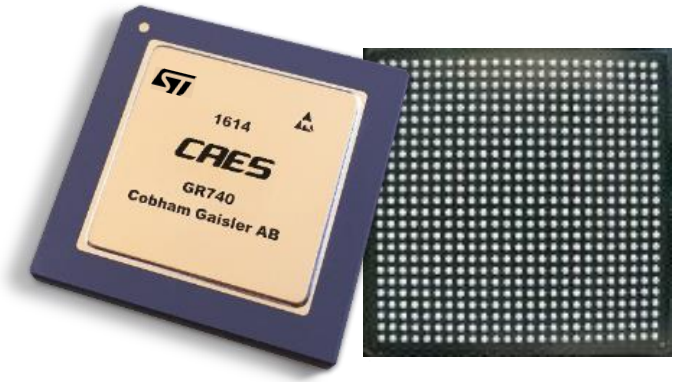
Where are we now

Part no.	Processor core	Clock freq. (MHz)	Perf. (DMIPS)	TID krad (Si)	SEL LET (MeV-cm^2/mg)	Power cons.	Package	Temp. range	Qualification status	Availability	Development board
GR740 SMD: 5962-21204	Quad-Core LEON4FT	250	>1700 *	300	> 125	< 2W at 40 °C*	625-Pin Ceramic **Land** Grid Array	-40°C / +125°C (junction)	• QML-Q/V qualification tests completed in 2020 • QML-Q/V approval expected in Q2 2021	• Components available	
GR740 SMD: 5962-21204	Quad-Core LEON4FT	250	>1700 *	300	> 125	< 2W at 40 °C*	625-Pin Ceramic **Column** Grid Array	-40°C / +125°C (junction)	• QML-Q/V qualification tests completed in 2020 • QML-Q/V approval expected in Q2 2021	• Components available	GR-CPCI-GR740 GR-VPX-GR740
GR740P BGA	Quad-Core LEON4FT	250	>1700 *	300	> 125	< 2W at 40 °C*	625, **PBGA**	-40°C / +105°C (case)	ESCC-Q-60-13C class 2 evaluation ongoing	• Prototypes in Q2 2021 • Flight Models in Q4 2021	

Complete software toolchain and debuggers are available

QML-V equivalent and QML-Q equivalent parts are currently available!

* For more information:
https://www.gaisler.com/doc/gr740/GR740-VALT-0010.pdf

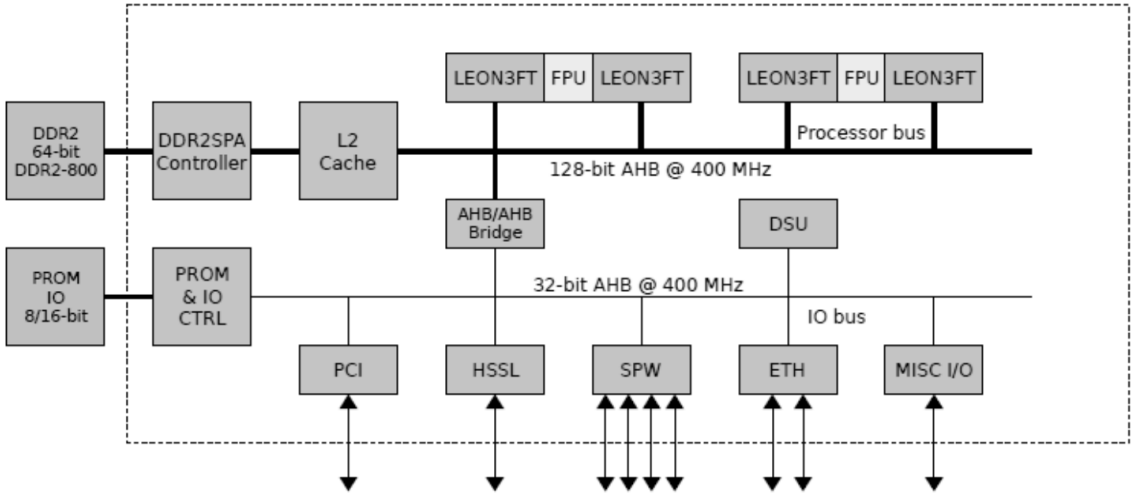


How did we get here

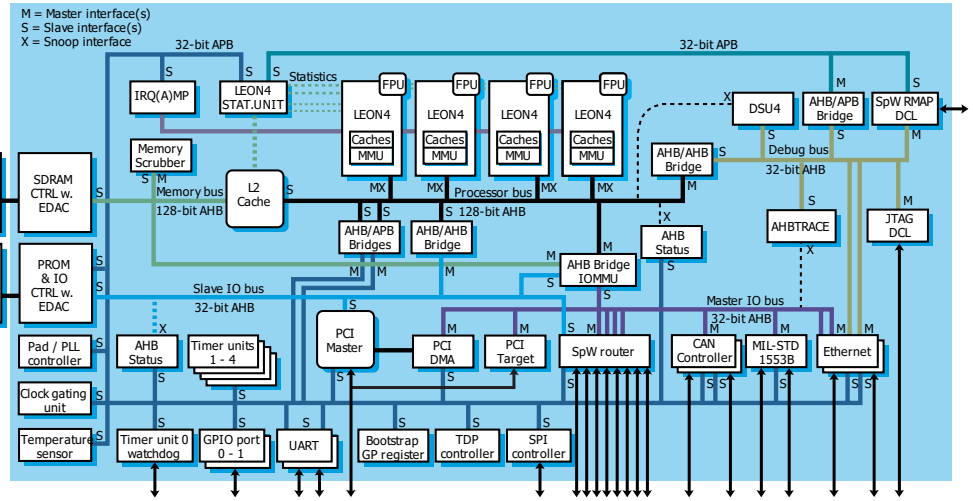
- Technical officer **Roland Weigand**
- STMicroelectronics (France)
  - Rennes
  - Grenoble
  - Crolles
- Micross Components, Crewe (UK)
- Pender Electronic Design (Switzerland)

Back to the beginning

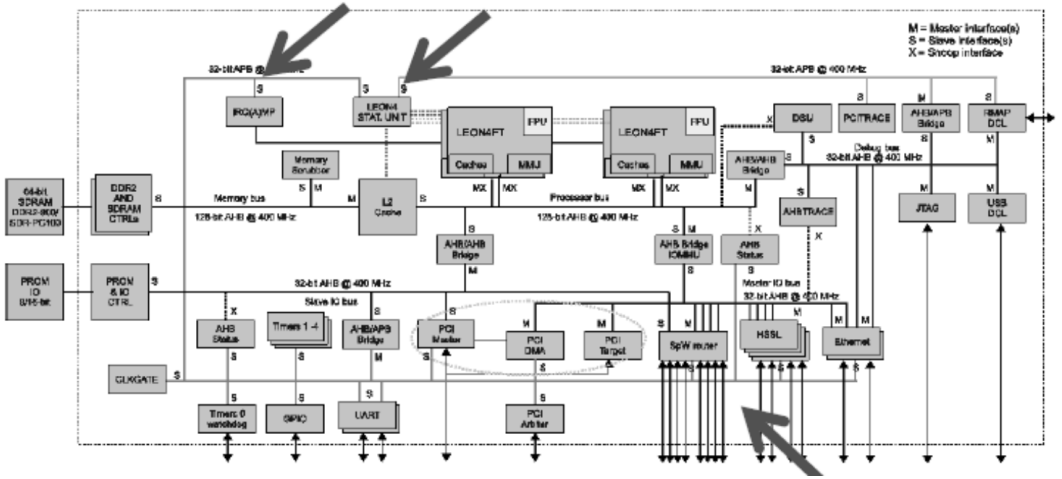
NGMP proposal 2008



Final GR740 Product



PDR proposal 2010



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When

ESA's next generation Microprocessor (NGMP) development time-line:

2009

Start of the development under a TRP contract with ESA (VHDL design and verification by simulation on FPGA).

2014

Implementation of NGMP into a space chip technology (C65SPACE).

2016

Engineering models of the GR740 were evaluated.

2018

Flight Silicon manufactured and validated (including radiation).

2020

All QML-V related qualification tests successfully completed.

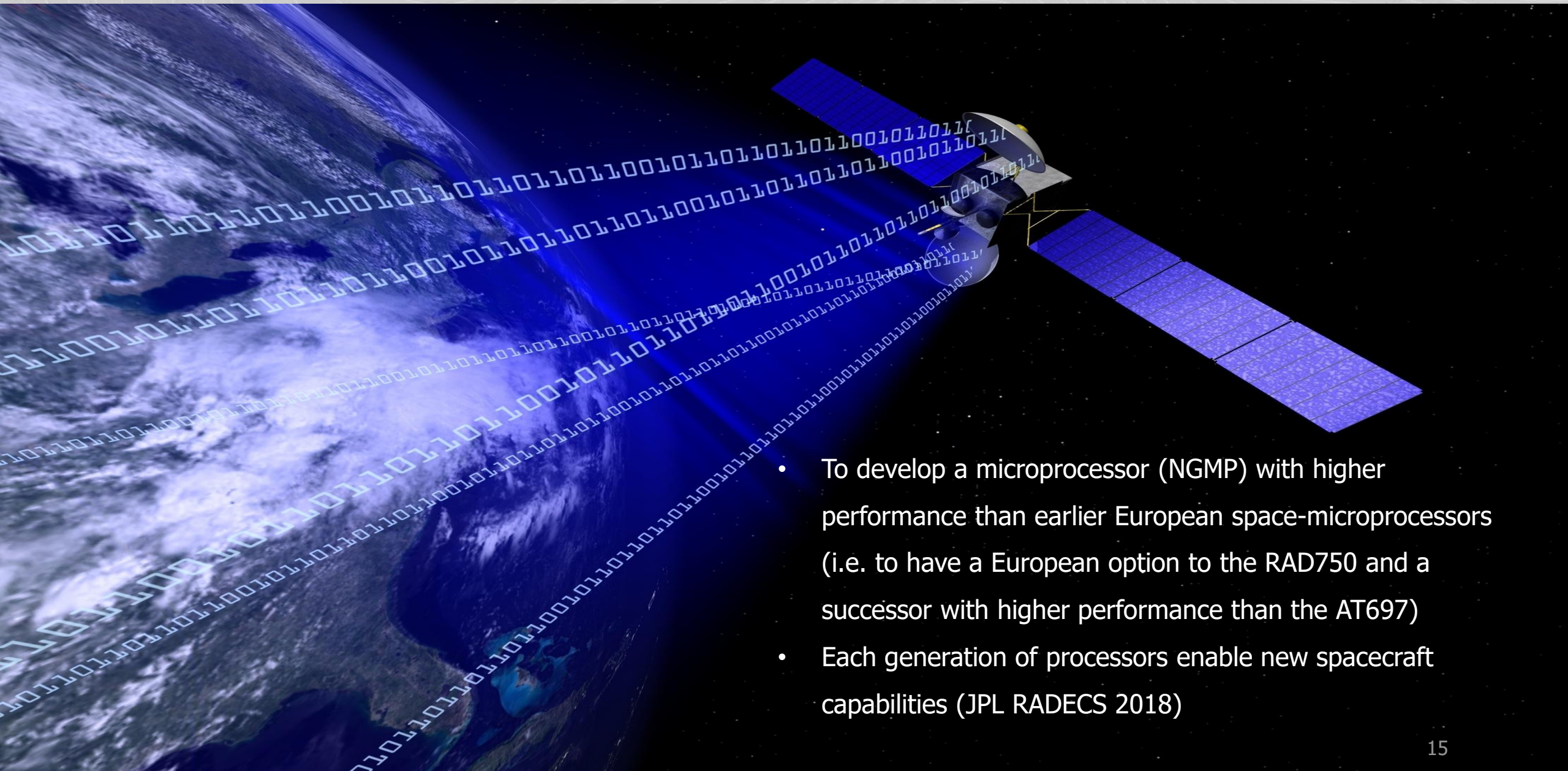
2021

2021-Q1 -> All complementary tests (Delta ESCC) successfully completed.

2021-Q1 -> QML-V / QML-Q equivalent flight parts made available.

Expected 2021-Q2 -> Constructional analysis on CLGA & CCGA package by ESA.
Expected 2021-Q2 -> QML-V and QML-Q certification by the DLA.

Why

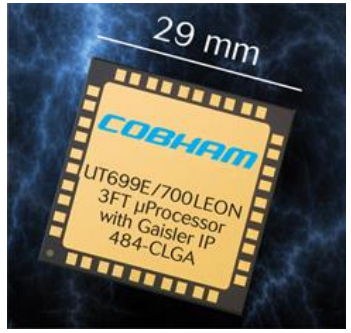


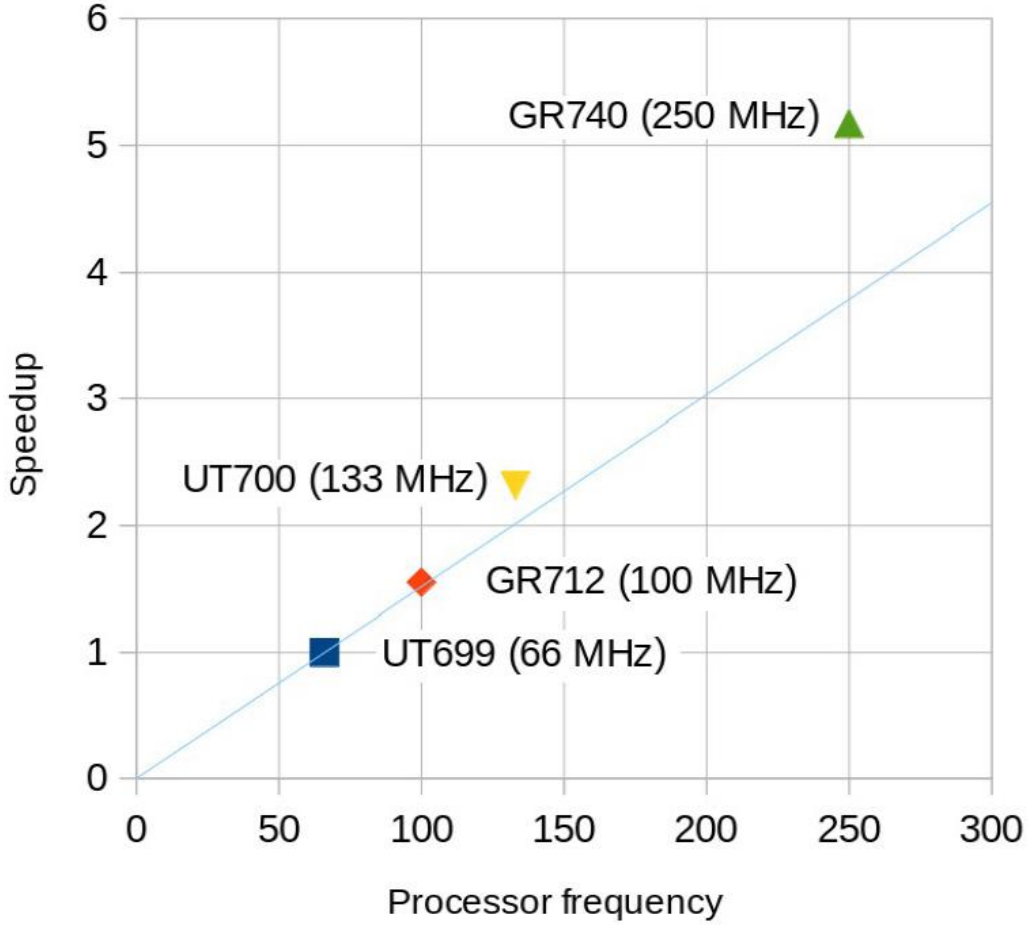
- To develop a microprocessor (NGMP) with higher performance than earlier European space-microprocessors (i.e. to have a European option to the RAD750 and a successor with higher performance than the AT697)
- Each generation of processors enable new spacecraft capabilities (JPL RADECS 2018)

Success

GR740 - the successor of UT700

- GR740 can replace UT700 when more powerful processing is demanded
- GR740 can operate in single core mode, almost doubling performance vs UT700
- GR740 offers three additional cores for more processing, providing a 7x performance increase over UT700
- GR740 is software compatible with UT700
- GR740 requires same real estate as UT700



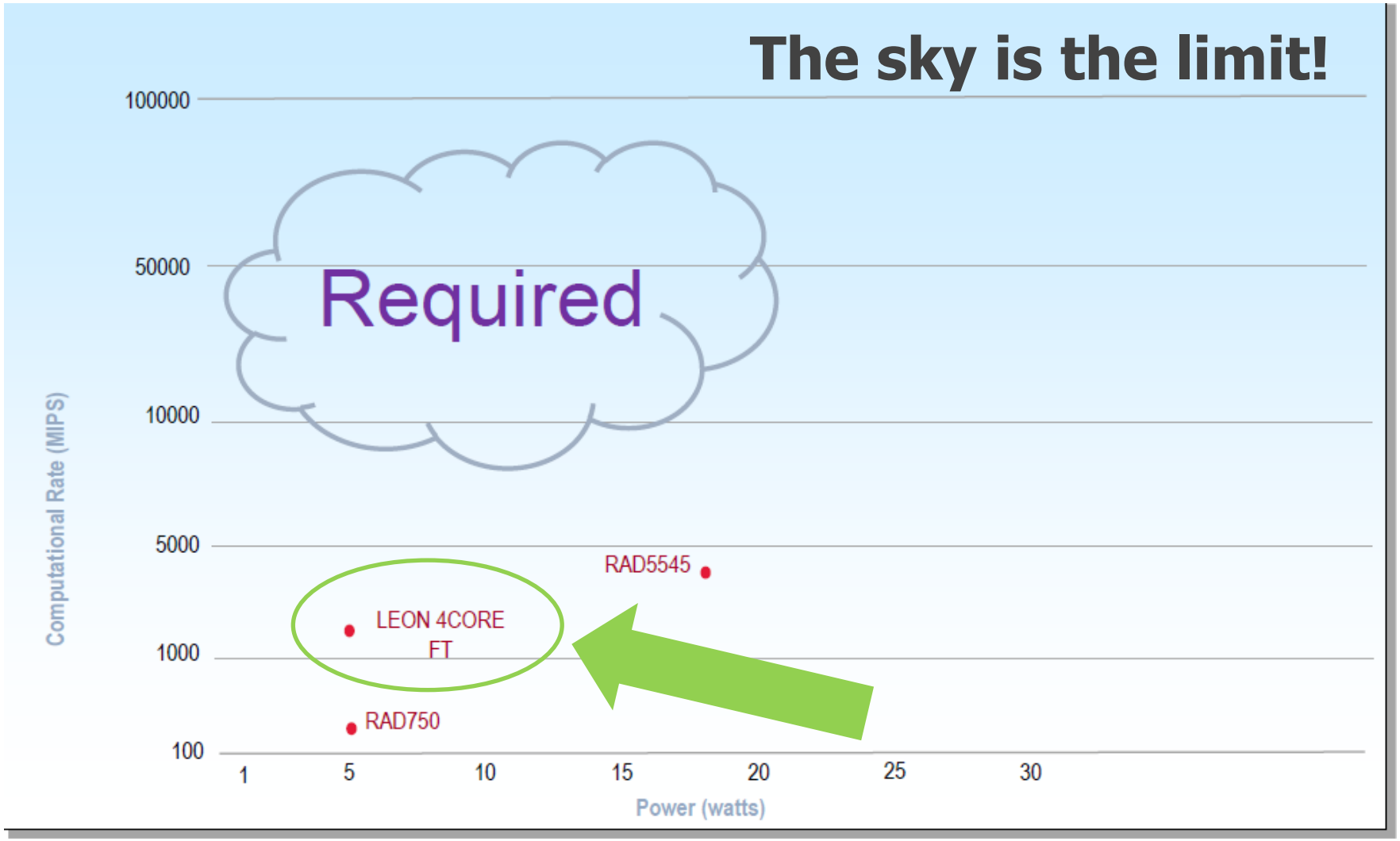


Success

Part Number	GR716A	GR716B*	UT699	UT699E	UT700	GR712RC	GR740
Processor	LEON3FT Single Core 32-bit SPARC V8	LEON3FT Single Core 32-bit SPARC V8	LEON3FT Single Core 32-bit SPARC V8	LEON3FT Single Core 32-bit SPARC V8	LEON3FT Single Core 32-bit SPARC V8	LEON3FT Dual Core 32-bit SPARC V8	LEON4FT Quad Core 32-bit SPARC V8
Foundry	UMC (180)	UMC (180)	TSMC (250nm)	TSMC (130nm)	TSMC (130nm)	TowerJazz (180nm)	ST (65nm)
Operating Voltage (core/IO)	1.8V/3.3V	1.8V/3.3V	2.5V/3.3V	1.2V/3.3V	1.2V/3.3V	1.8V/3.3V	1.2V/2.5&3.3V
Clock Frequency	50 MHz	100 MHz	66 MHz	100 MHz	166 MHz	100 MHz	250 MHz
DMIPS/Core, total	98	196	92	140	230	140, 280	425, 1700
Cache L1 I/D (KiB)	192 KiB TCM	192 KiB TCM	8/8	16/16	16/16	16/16	16/16
Cache L2 / L3 (KiB)	No	No	No	No	No	No	2048KB
MMU	No	No	Yes	Yes	Yes	Yes	Yes

*Products under development, Values can be changed without notice

Are we there yet?



Next Generation Processing for space applications (JPL RADECS 2018)

What?

Value proposition

- High performance, wide range of interfaces
- SPARC V8 compliant, Radiation-hard and Fault Tolerant
- LEON Technology – re-use of Development and Software ecosystem
- Excellent performance/watt ratio
  - Very low power, < 3 W (core typical)
  - Performance 1700 DMIPS

Applications

- High-performance general-purpose processing
- Symmetric and asymmetric multiprocessing
- Shared resources can be monitored to support mixed-criticality applications

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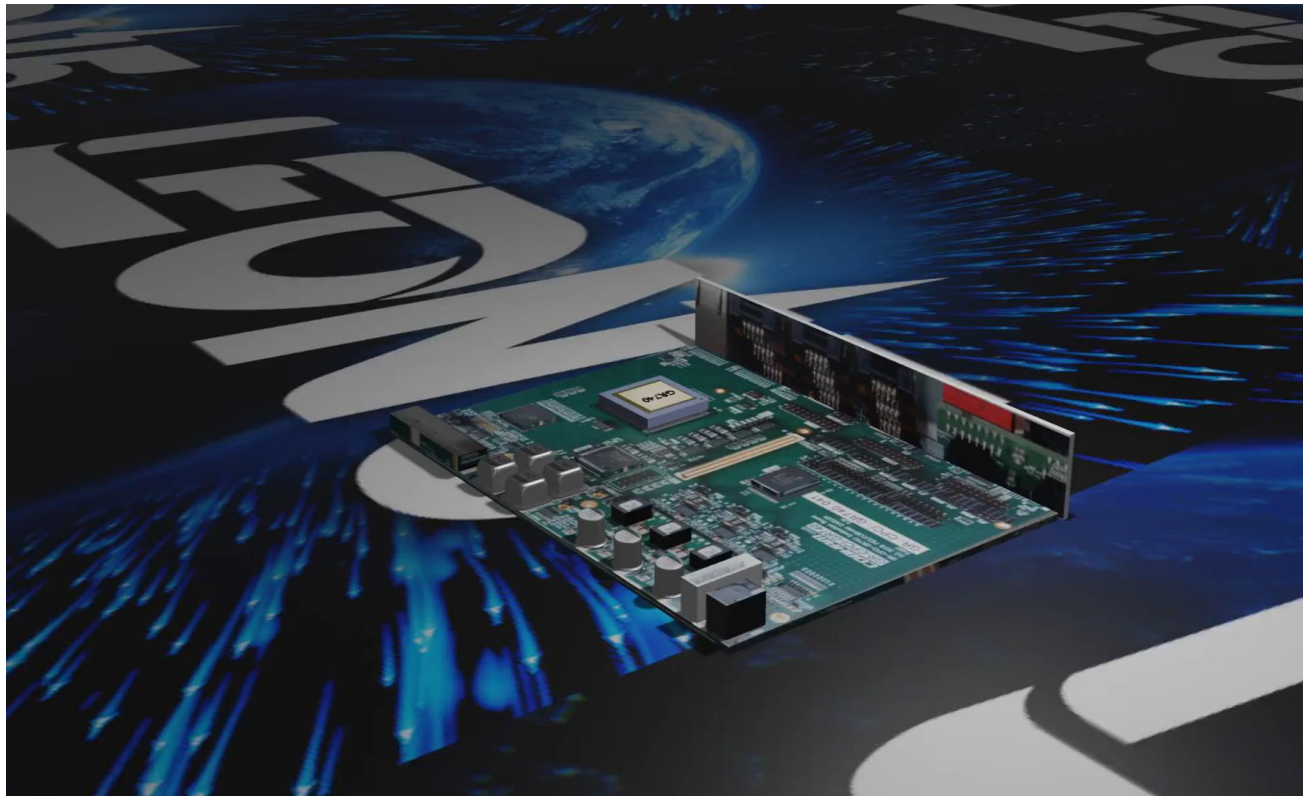
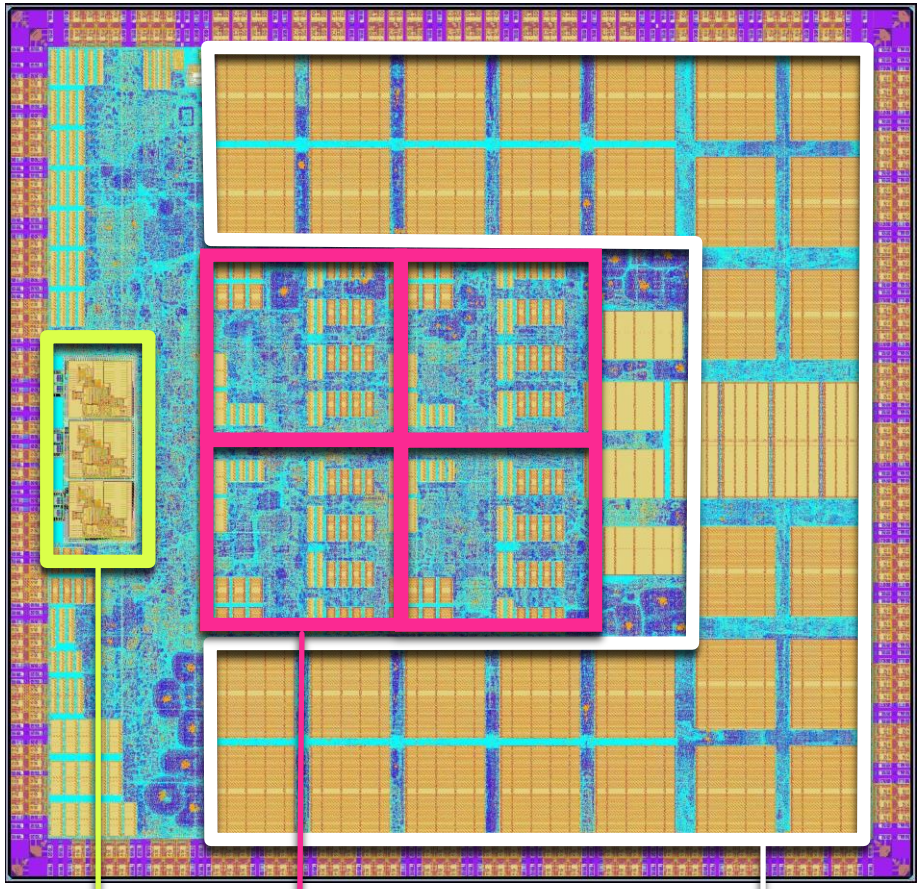
What?

Let’s see what is under the surface



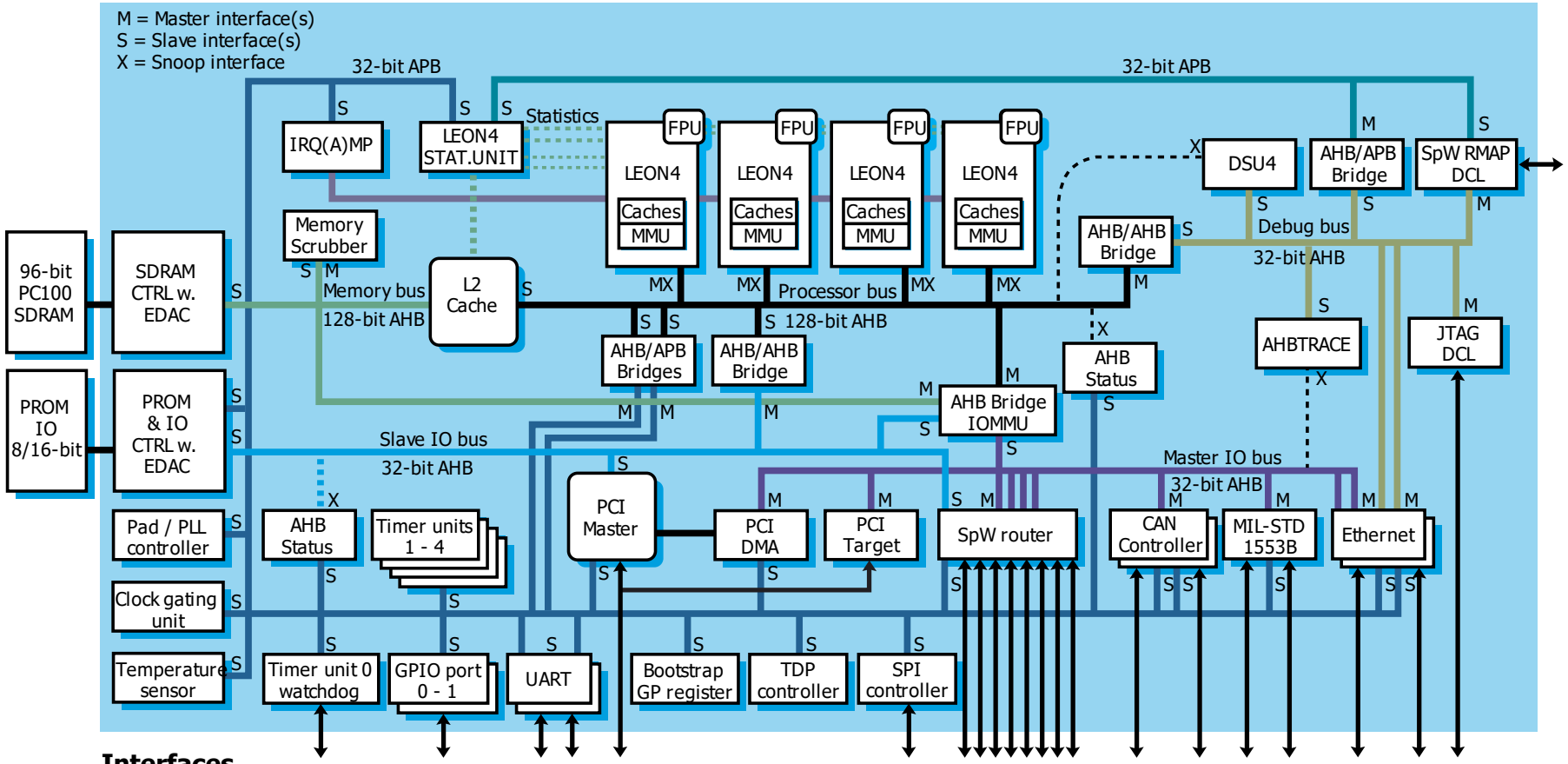
65nm CMOS Technology
ST C65SPACE Library



What?

Features

- Fault-Tolerant Quad-processor SPARC V8 integer unit with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches.
- Double-precision IEEE-754 FPU (1 FPU/Core)
- 2 MiB Level-2 cache
- 64-bit PC100 SDRAM memory interface with Reed-Solomon EDAC
- 8/16-bit PROM/IO interface with EDAC
- CPU and I/O memory management units
- Multi-processor interrupt controller with support for asymmetric and symmetric multiprocessing
- SpaceWire TDP controller and support for time synchronisation



Interfaces

- SpaceWire router with 8 SpaceWire links (200 MHz)
- 2x 10/100/1000 Mbit Ethernet interfaces
- 2x MIL-STD-1553B interface
- 2x CAN 2.0 controller interface
- 2x UART, SPI, Timers and watchdog, 16+22 pin GPIO
- PCI Initiator/Target interface
- JTAG

GR740 Software Ecosystem

Operating Systems

OS	Real Time	SMP	AMP	MMU	Toolchain	License
BCC bare-metal	Y	N	*	N	GCC/LLVM	BSD
RTEMS-5 **	Y	Y	Y	N	GCC/LLVM	BSD/GPL
Linux 4.9	N	Y	*	Y	GCC	GPL
VxWorks 7	Y	Y	Y	Y & N	GCC/LLVM	COM
Zephyr RTOS 2.5	Y	N	*	N	GCC	APACHE

*) single-core and/SMP support, no dedicated AMP mode

**) ESA RTEMS SMP qualification package released 2021/2022

Hypervisor and memory protection support via Partners

- Para-virtualization or processes interface for mixed criticality, protection using MMU
- WindRiver VxWorks 7 Real-Time Processes (RTP) w/wo Time Partition Scheduler
- FENTISS Xtratum Next Generation (XNG)
- SysGo PikeOS

Software ecosystem support from Cobham Gaisler

- Software Life-cycle webpage
- Software Overview webpage
- Updated continuously as part of LEON device support and LEON5

  Upcoming releases Q2 and Q3: Linux 5.10 LTS and Zephyr 2.6 LTS

GR740 Software Ecosystem

CAES PIONEERING ADVANCED ELECTRONICS

Toolchain support

- GCC-7 and GCC-10 (GPL)
- LLVM Clang-8 (MIT)
- C/C++11 or later depending on environment

Boot loaders

- MKPROM2 (GPL)
- GRBOOT (COM)
  - ECSS quality development flow, Criticallity B
  - Flight Computer Initialisation Sequence (SAVOIR-GS-002)
  - Unit/validation test-suite
  - Optional STANDBY SpW/PUS remote terminal

GRMON-3 hardware debugger

- Assembly and C/C++ via GDB
- JTAG and Ethernet debug-link
- GR740/LEON4 drivers, AMP and SMP system support
- Instruction trace, AHB bus traces, I/O register inspection, etc.

Simulator (GR740 specific support)

- TSIM3 multi-core simulator
- Wind River Simics simulator (partner)

ECSS

SAVOIR
space avionics open interface architecture

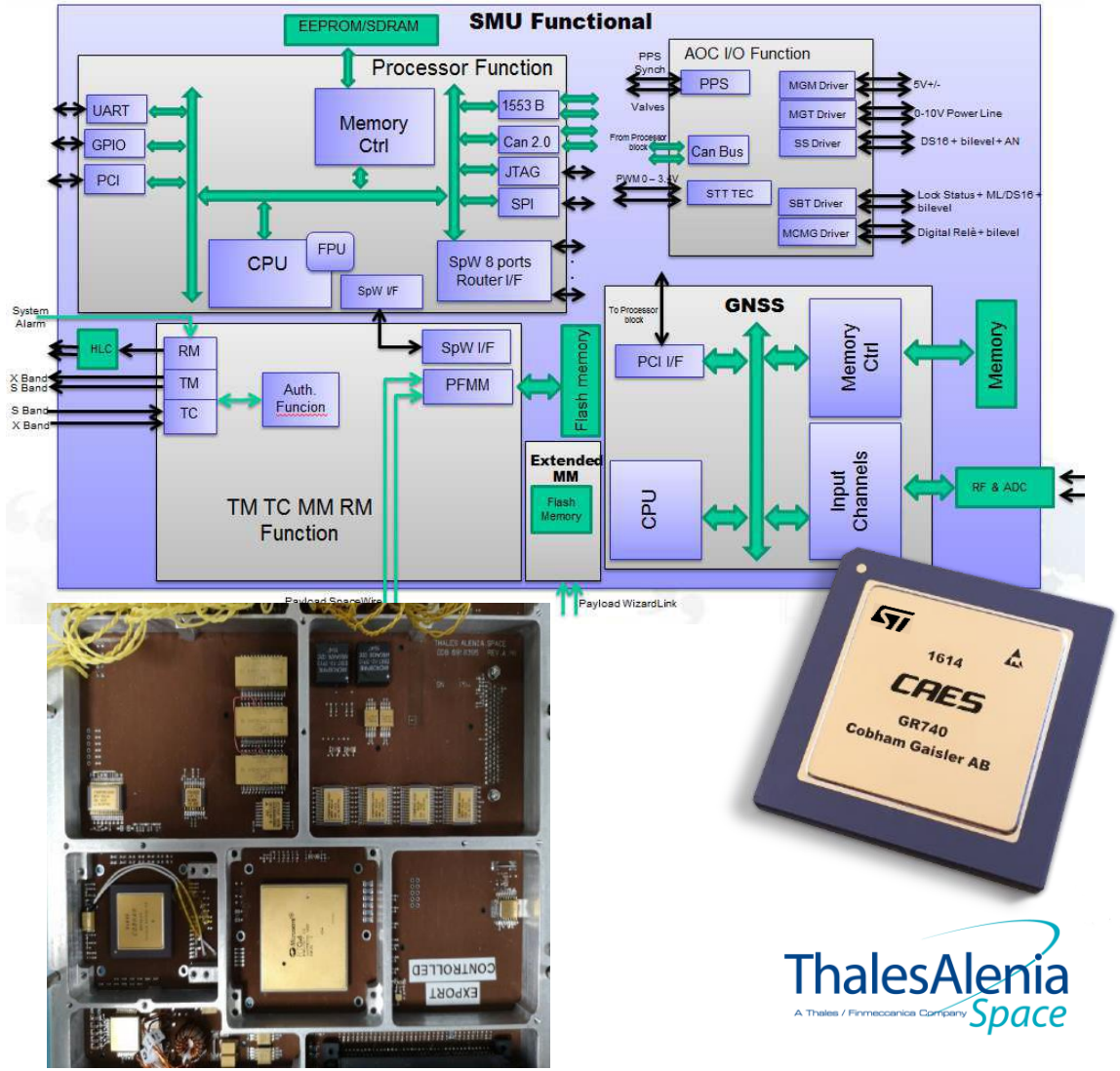
GRMON3
debugging made easy

TSIM3
Instruction-level simulator

Application example:
GR740 - IPAC Computer for the Platino mission

IPAC is an innovative avionic based on an integrated and modular approach, which essentially consolidates all the DHS units typically present in EO missions (e.g. OBC, PDH, GNSS, RTs) in a unique box.

One example of this approach is related to On Board Processors: in fact in previous platform architectures (e.g. Sentinel-1C/D) there were on-board as many as 8 CPUs (2 x SMU, 2 x GNSS, 2 x Star Trackers, 2 x DSHA), whereas in IPAC all the processing for these functions is consolidated on the two LEON4 GR740 quadcore processors, with the possibility to host also payload processing if required.



Source: Presented by Alessandro Marini at ADCSS 2018,Noordwijk, The Netherlands

Application example:
GR740 – Roman Space Telescope (WFIRST) Processor Board

Quad-Core LEON4 GR740 (MUSTANG + size module form factor) - board size 6U-220

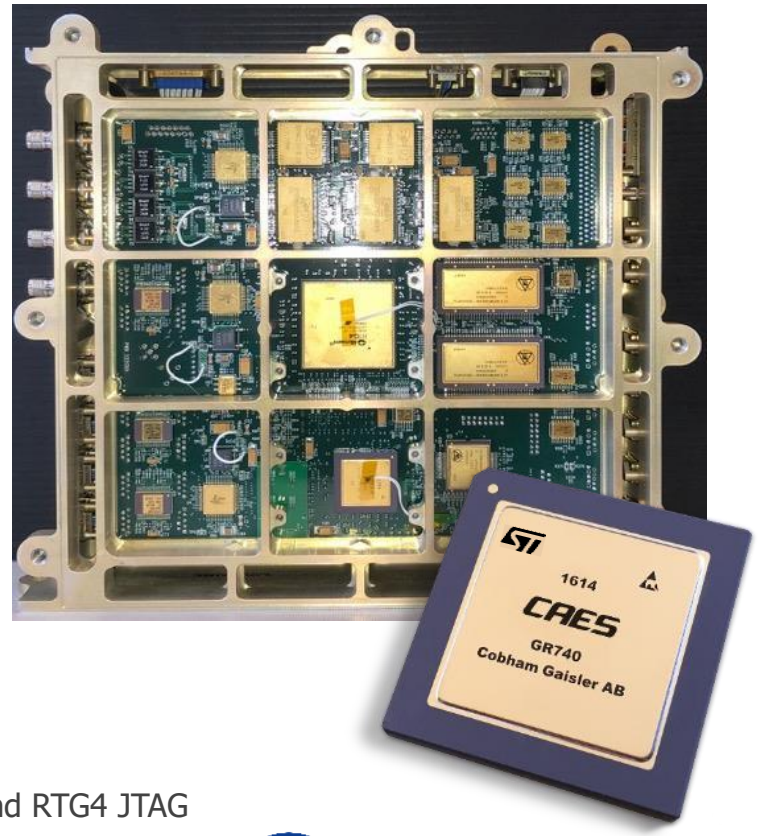
3x Engineering Board assembled tested

- 1x delivered to the JPL Coronagraph Team to be used in the instrument for a tech demo on WFIRST Observatory
- 2x more deliveries planned for JPL

MUSTANG Team is planning on lifting the Quad–Core LEON4 design/layout and create an upgraded version of MUSTANG Processor Card

WFIRST Processor Board features:

- GR740 Quad-Core LEON4 SPARC V8, 250MHz
- FPGA RTG4
- SUROM 64KB
- SDRAM 256MB(+128MB FEC)
- DDR2 4GB(+2GB FEC)
- MRAM 2X16MB
- Oscillator QT194(50MHz)+QT2020
- Peripherals:
  - SpaceWire: 20 (8 GR740, 12 RTG4)
  - 1553B: 1 (1 GR740)
  - RS422: 16 TX and 16RX
  - UART: 3 (2 GR740, 1 RTG4)
  - Debug-ports: GR740 SPW debug-port and RTG4 JTAG



Source: Presented by Art Azarbarzin at the IEEE Space Computing Conference, Pasadena, CA, July 30 to August 1, 2019

Application example: GR740 – CORA-RDHC activity

Compact Reconfigurable Avionics – Reconfigurable Data Handling Core Module

ESA

- Technical Officer: Jørgen Ilstad, TEC-EDD –> EOP-PPE

Cobham Gaisler AB, Sweden (prime)

- Responsible for the development of hardware, VHDL design, boot software and drivers

Thales Alenia Space France

- Responsible for middleware software design

Thales Alenia Space España S.A., Spain

- Responsible for FPGA reconfiguration code

Airbus Defence & Space, France

- Contribution to the systems analysis and trade-off, requirements and system architecture

External service providers

- Responsible for breadboard development

Development of an Elegant Bread Board

- A compact reconfigurable data-handling core module
- High performance microprocessor and high-capacity reconfigurable FPGAs
- Clear path to space qualification
- Accompanied by I/O interface modules

Development of board support package

- FPGA communication and reconfiguration
- Communication interfaces towards external sensors and actuators

Development of SW platform and Boot SW

Installation of hardware at ESTEC's avionic laboratory

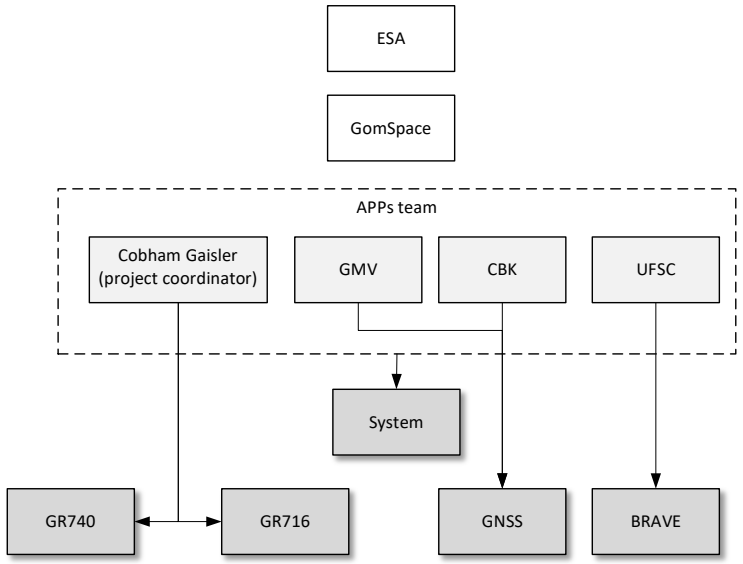
GR740 Quad-Core LEON4 SPARC V8 Processor

- Controller and high-performance processing

Application example: GR740 – GOMX-5 cubesat

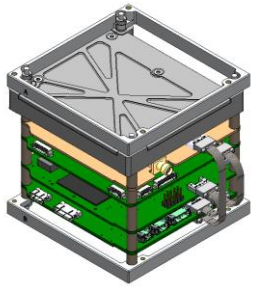
APPs Team

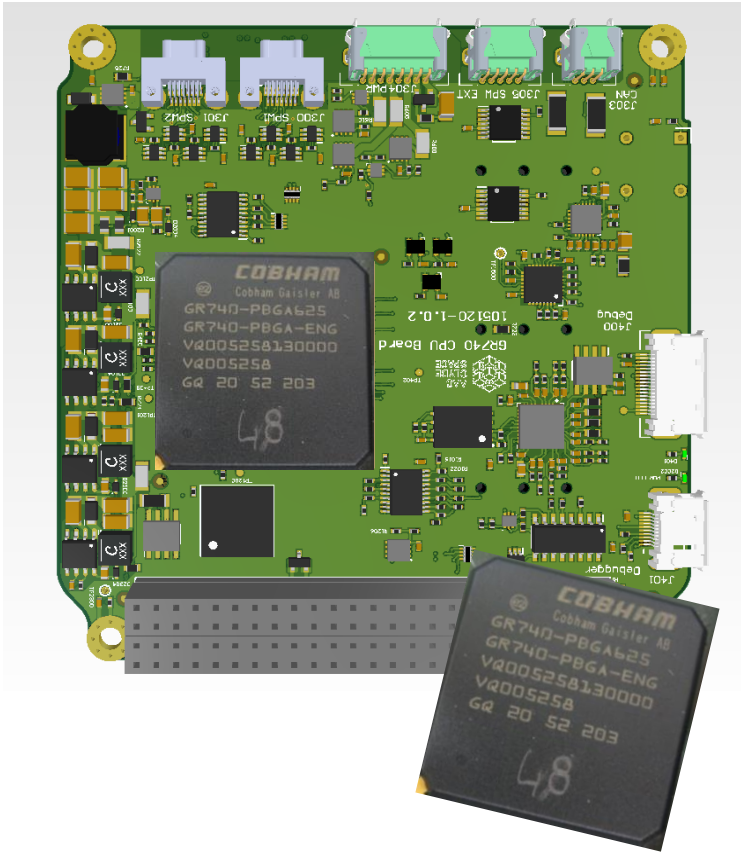
- Cobham Gaisler AB, Göteborg, Sweden
- Centrum Badań Kosmicznych Polskiej Akademii Nauk, Warsaw, Poland
- GMV Innovating Solutions Sp, Warsaw, Poland
- Space Technology Research Laboratory, UFSC, Florianópolis, Brazil



Objective

- Demonstrate multiple processing technologies developed within ESA activities and acquire flight heritage from related components





Applications

- APPs management
  - Communications routing (S/C CAN to/from local APPs SpW)
  - Board and application control (GPIO I/F to APPs boards)
- Memory error detection and correction
- Processing and memory resource for off-board experiments via SpW
  - Mono-frequency receiver for GNSS SDR experiments (with GMV)
  - BRAVE board reconfiguration (with UFSC)
- Power distribution from S/C to APPs boards (passive)

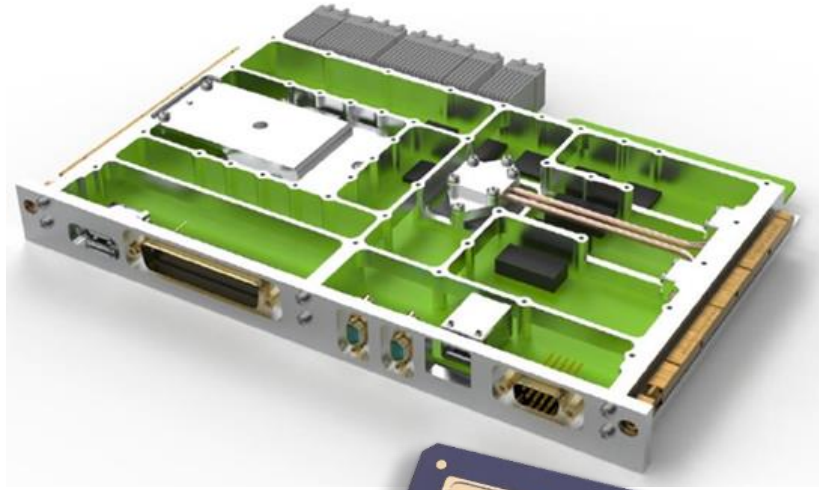
Source: Presented by

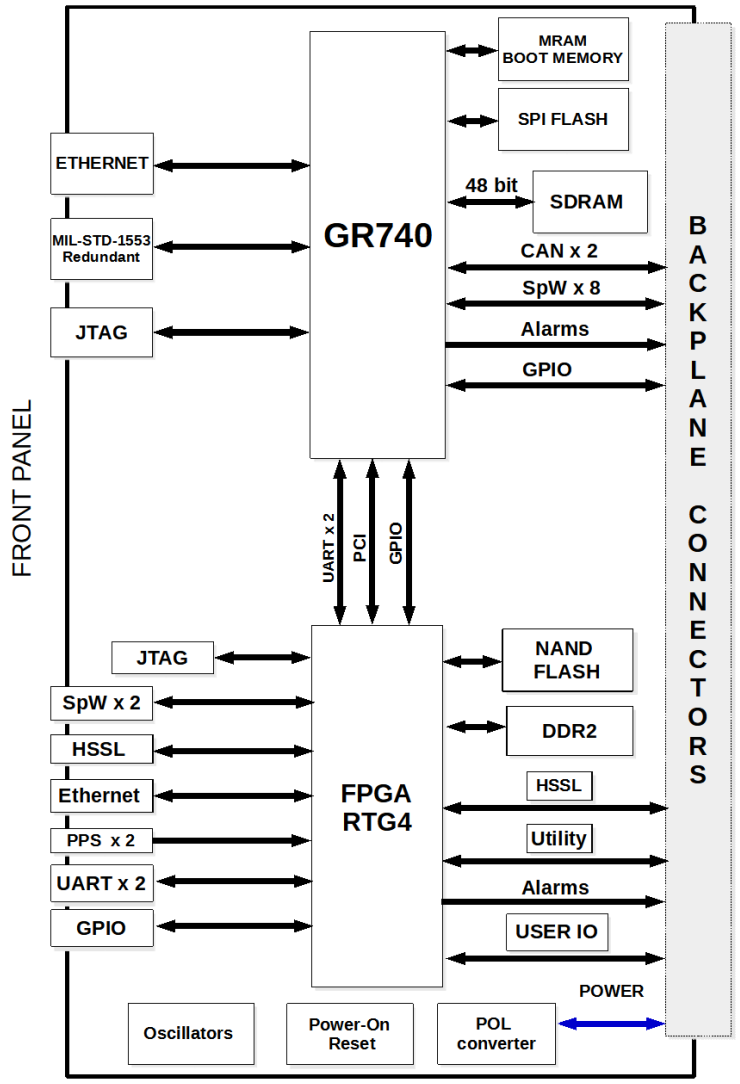
Application example: GR740 – Single Board Computer

The SBC provides an extensive set of memories and redundant interfaces to support the needs of current and future OBC and Data Handling platforms.

Features

- **Interfaces**
  - Redundant MIL-STD-1553B
  - 2 x SpaceWire
  - HSSL (SpFi)
  - 2 x UART
  - Gigabit Ethernet
  - 8 x General purpose I/O's
  - PPS (Pulse Per Second) input for synchronization
  - JTAG debug interface
  - Dual star, eight SpaceWire interfaces from the GR740 SpaceWire router
  - Multi drop bus, redundant CAN from GR740
  - Full mesh, 3.125 Gbit/s HSSL (SpFI) from RTG4 **
  - Multi drop bus, I2C from RTG4
  - Alarms and other utility signals
- **Form factor**
  - 6U (233.5 mm x 160 mm), 5 HP, Mass 1.2 kg (estimate)





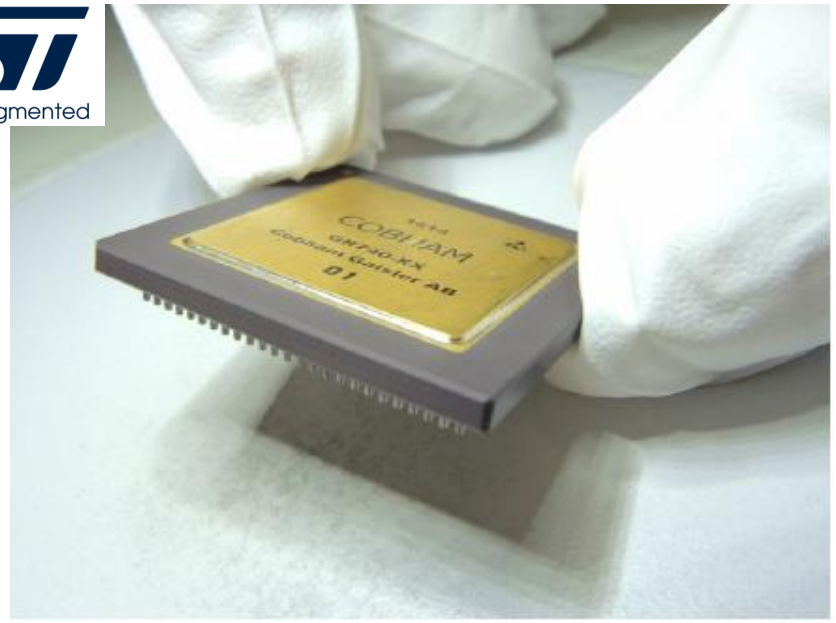
*Product under development, options can be changed without notice

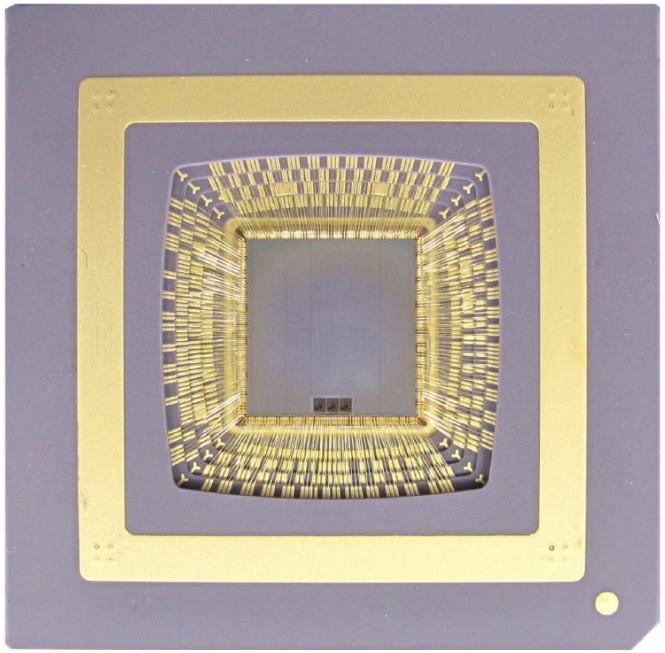
Hurdles along the way

No development is free of technical challenges:

- Technology platform was not available
- Package development
- Over Pad metallization
- Wire bonding
- Selection of column type for CCGA package
- Design changes

Package development

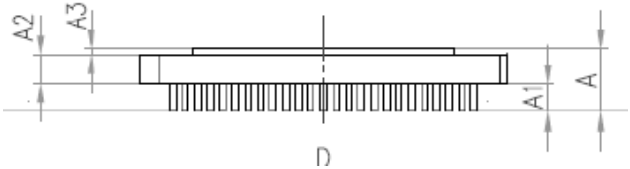


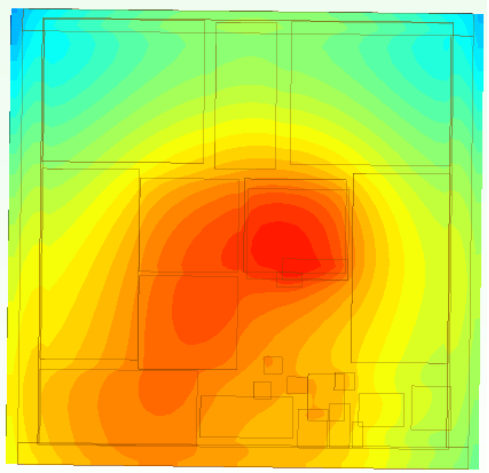


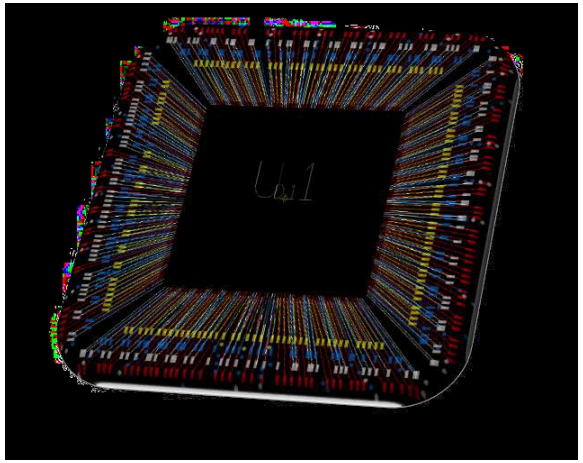
625 pins Package:

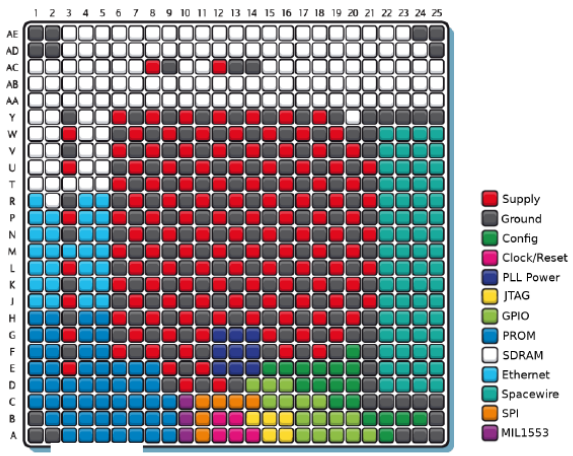
- CLGA

- CCGA



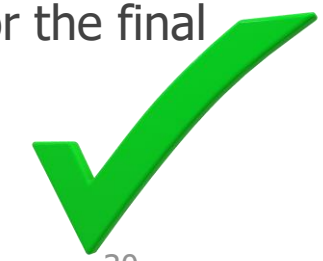






...gure 77. Placement, bottom view

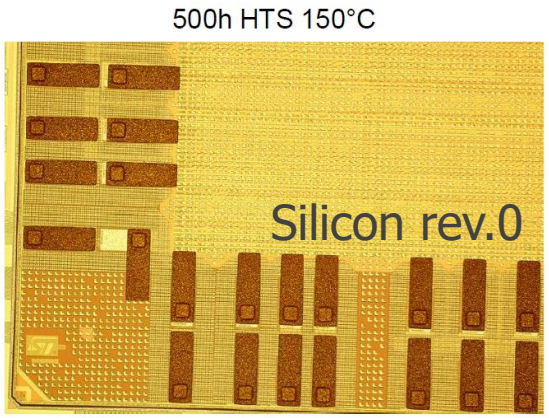
- Flip-Chip was not available to project
- This led to development of functional prototypes and, in the end, additional design improvements for the final product



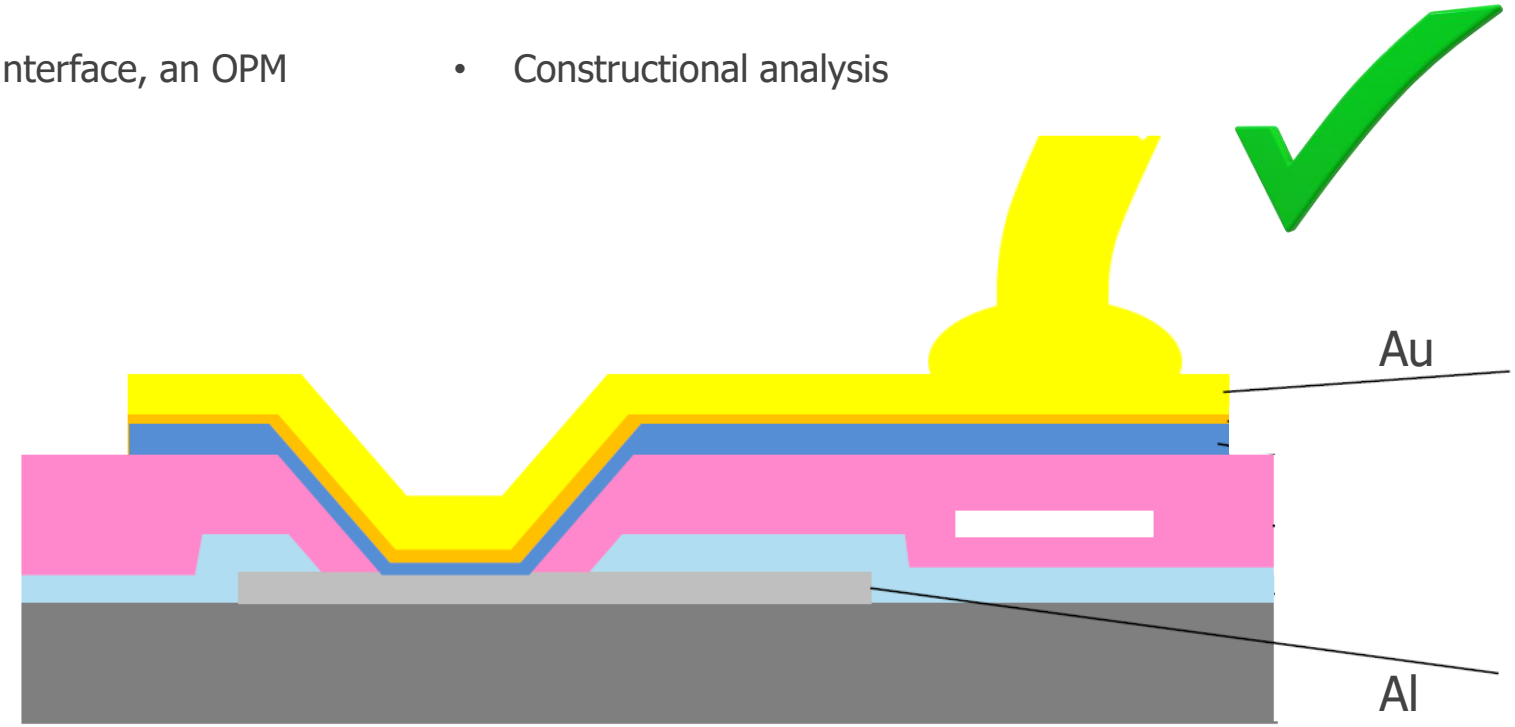
Images courtesy of ST Microelectronics

Over Pad Metallisation (OPM)

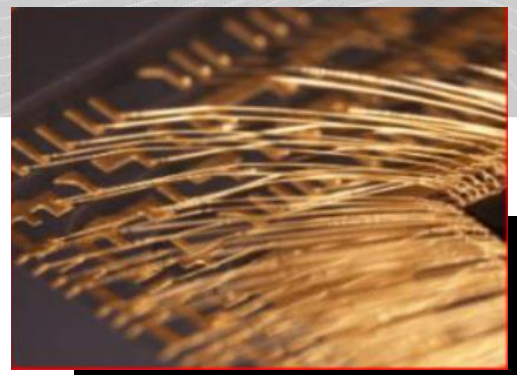
- Al wedge bonding was not possible for the C65SPACE library due to pad size compatibility and the complexity of the GR740. Au wire had to be used instead.
- Because of the Al pad – Au wire metal interface, an OPM layer was implemented
- Wire bonding validation after die aging on corner case (500h 150C / 500h 85C/85%RH) was performed with metallisation integrity check after aging
- Constructional analysis



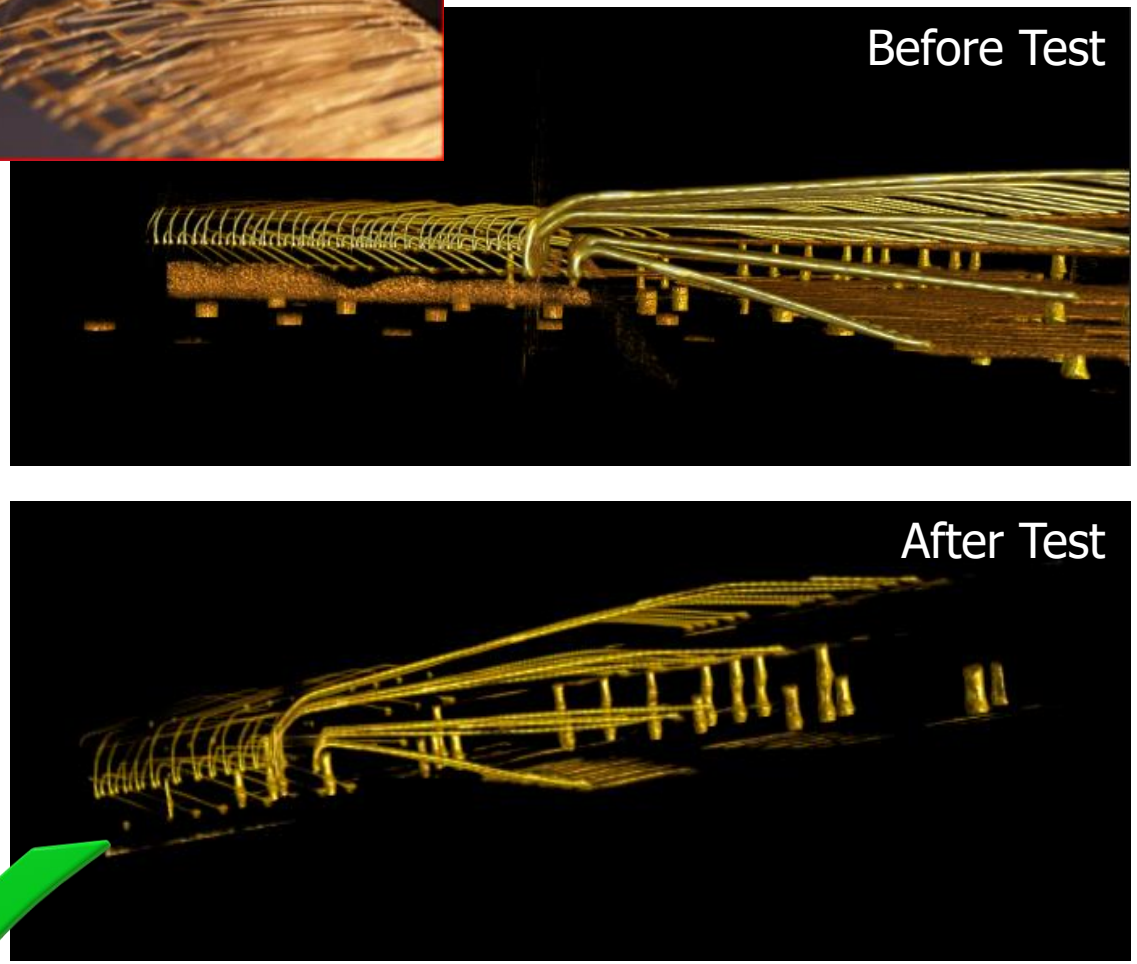
Images courtesy of ST Microelectronics



Wire Bonding



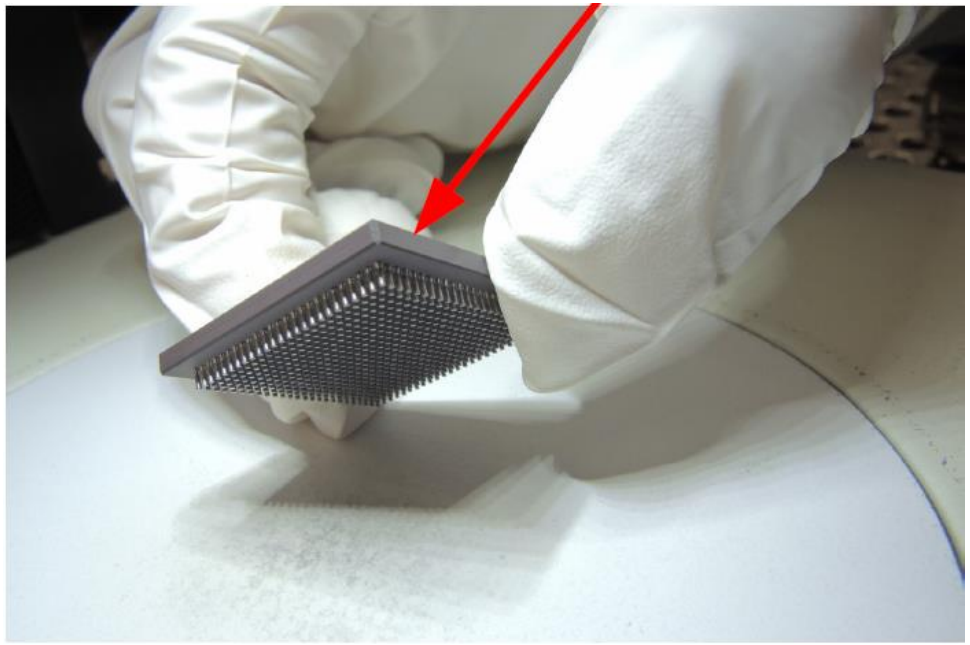
- C65SPACE library imposed the used of Au ball bonding
- Device complexity imposed the use of thin bond wires, 20µm in diameter
- 4 decks were necessary to accommodate all bond wires. Package validation included:
  - Vibration, TM 2007 Condition A
  - Mechanical Shocks, TM 2002 Condition B
  - Constant acceleration, TM 2001 Condition D
  - PIND test, TM 2020 Condition A.
  - Electrical test & X-ray before and after each test.

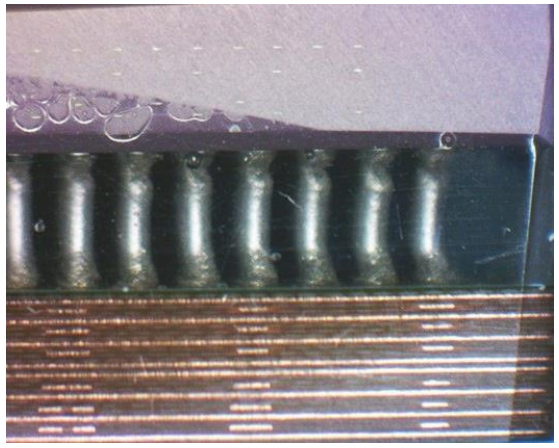


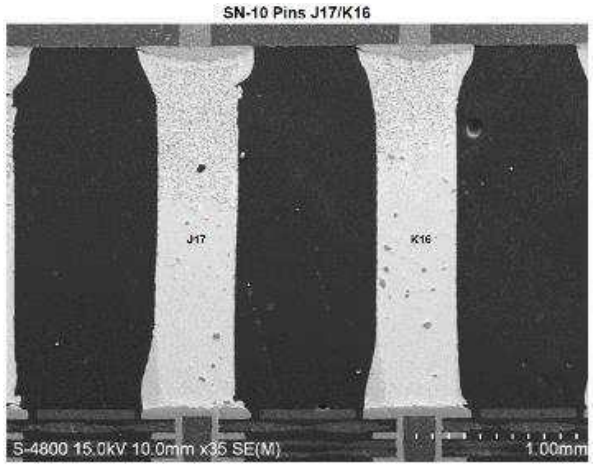
X-ray based 3D reconstruction of the GR740 bonds.

Images courtesy of ST Microelectronics.

Selection of column for the CCGA package







Images courtesy of ST Microelectronics

- The GR740 package is compatible with various columns types:
  - Sn/Pb IBM type (Micross Crewe UK)
  - Sn/Pb copper wrapped (e.g. Serma, SixSigma)
- The QML qualification has been run with Micross IBM type columns
- Micross Crewe UK is currently QML-Q/V/Y certified by the DLA
- A board level reliability study of the IBM columns has been completed by ST & Micross.
  - FIT FOR PURPOSE
- A comparison study between Micross and Serma type columns has been carried out by ESA/Thales I.

Design Changes

- Corrections of issues with functional impact
  - Level-2 cache fault-tolerance
- Improvements of functional impact
  - Extensions of logging
  - Time synchronization
- Improvements without functional impact
  - Correction of ring oscillator
  - Removal of unused RAM bits
  - Pipelining to reduce backend effort
  - LVDS driver ESD sensitivity at low voltage (HBM)
  - On-chip temperature sensor fixed

Die & Package revision 1

Description	Reference	Level
HBM	JS-001-2017	2000 V
CDM	JS-002-2014	500 V

All GR740-CP/MP/MSxx components have die revision 1

We have made it

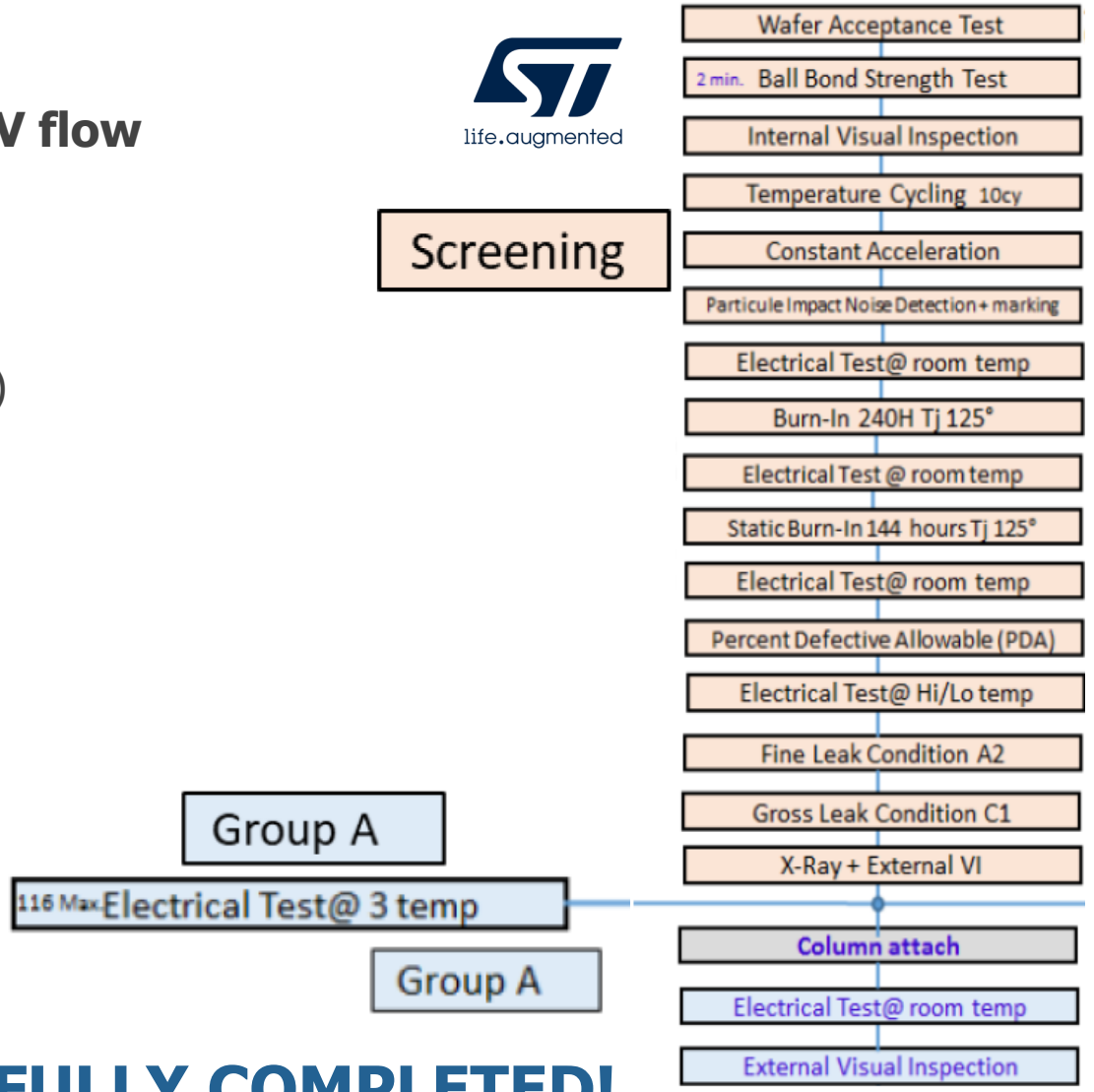
- Qualification testing has been successfully completed
  - Screening / qualification tests per MIL-PRF-38535L / MIL-STD-883K
  - Delta-evaluation per ESCC-2269000

- The qualification data package to the DLA includes:
  - Draft SMD 5962-21204
  - Results of qualification tests
  - Reliability data
  - Technology support data

GR740 qualification results

GR740 qualification performed following QML-V flow

- QML-V Screening (MIL-PRF-38535)
- Group A (Electrical tests)
- Group B (Mechanical and Environmental tests)
- Group C (Life test)
- Group D (Package related tests)
  - CLGA
  - CCGA (IBM type columns)
- Group E (Radiation tests)



ALL TESTS SUCCESSFULLY COMPLETED!

GR740 qualification results

Solder column pull test for CCGA performed in Group D

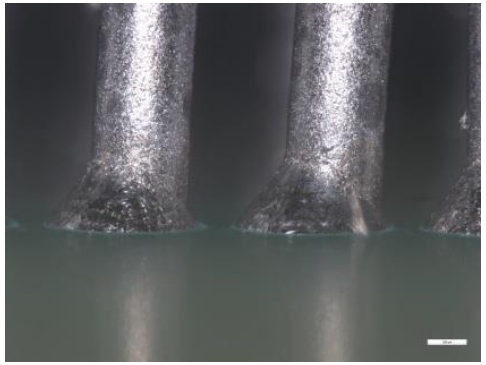
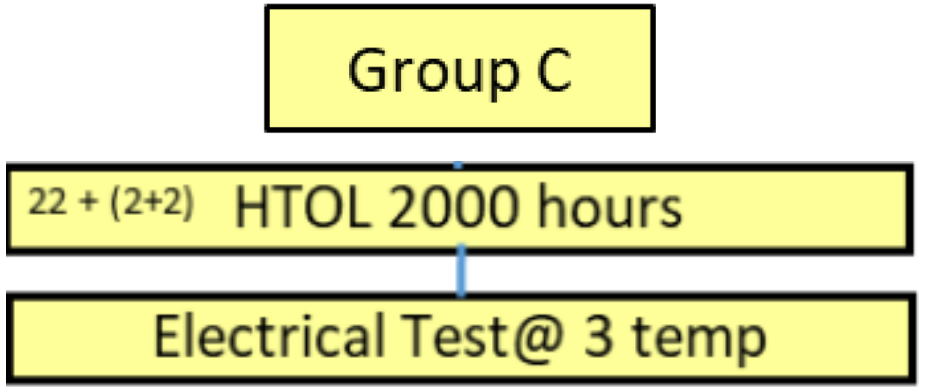


Image of solderability test
courtesy of ST Microelectronics and Micross Crewe UK



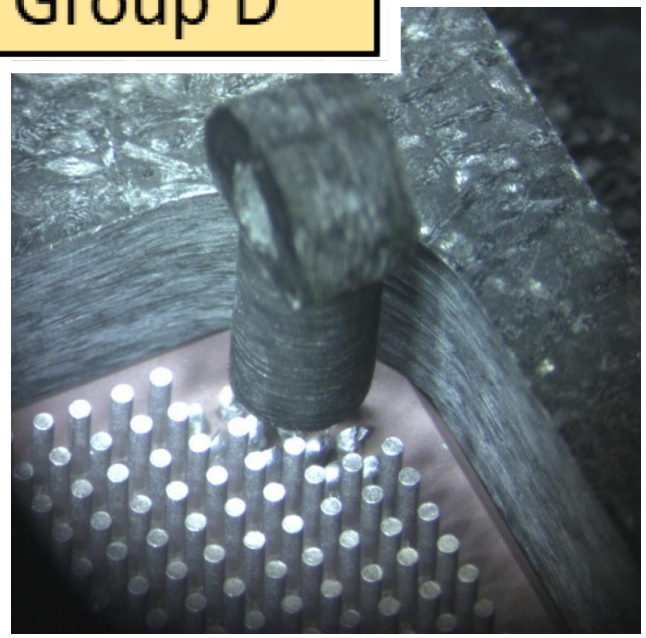
Extensive Life test data has been collected by ST for test vehicles manufactured with same library to calculate the failure rate of the GR740 silicon.

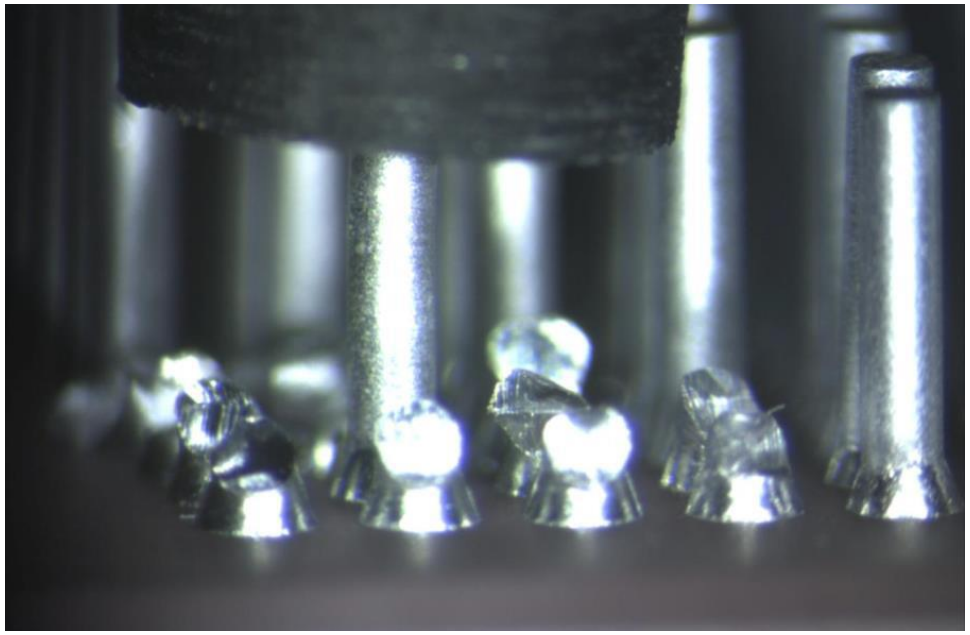
Mission profile	FIT result
Tjunction in use: +125°C, Vuse= Vmax (1.32V)	17
Tjunction in use: +125°C, Vuse= Vnom (1.2V)	3

ALL TESTS SUCCESSFULLY COMPLETED!

GR740 qualification results

Group D





Images of solder column pull test
courtesy of ST Microelectronics and Micross Crewe UK

Group D

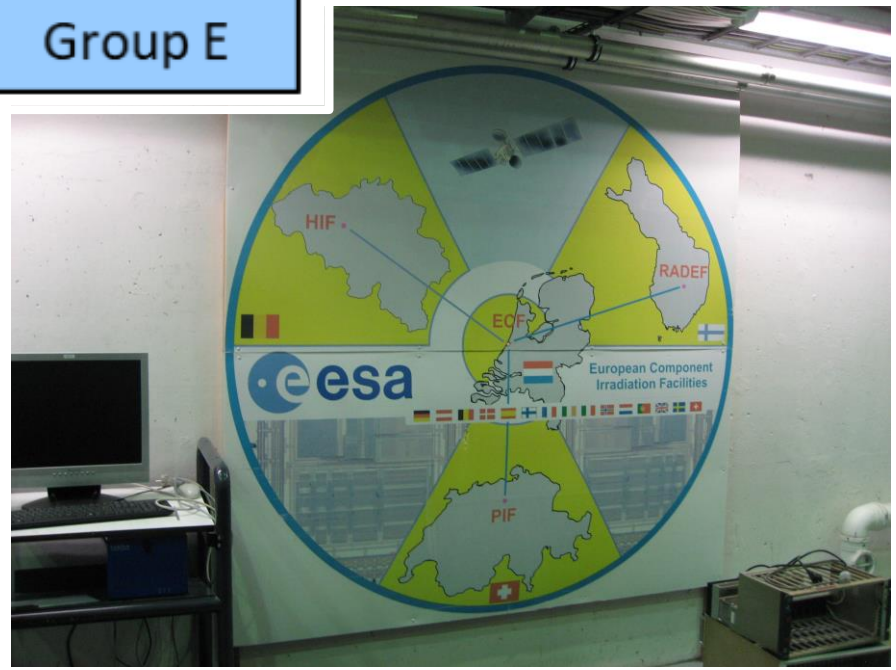
- 3 Internal Water Vapor Test
- 15 Thermal Shock 15 shocks
- Temperature Cycling 100 cy
- (15) Moisture Resistance
- Electrical Test@ room temp
- Visual Inspection
- Seal Test (fine & Gross)
- 15 Mechanical Shock 5 shocks
- Vibration 12 sweeps
- Constant acceleration
- Seal Test (fine & Gross)
- Visual Inspection
- Electrical Test@ room temp
- 15 Physical Dimension
- (15) Physical Dimension
- (15) Salt Atmosphere
- Visual Inspection
- Seal Test (fine & Gross)
- 2 Solder Column Pull Test
- 3 Soldering Heat
- Seal Test (fine & Gross)
- External Visual Inspection
- Electrical Test@ room temp

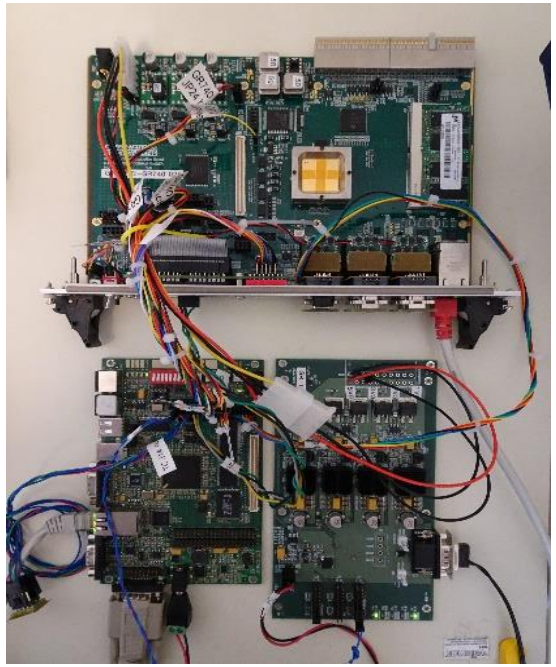
Resistance to soldering heat (subgroup D9)
performed under both conditions I and J

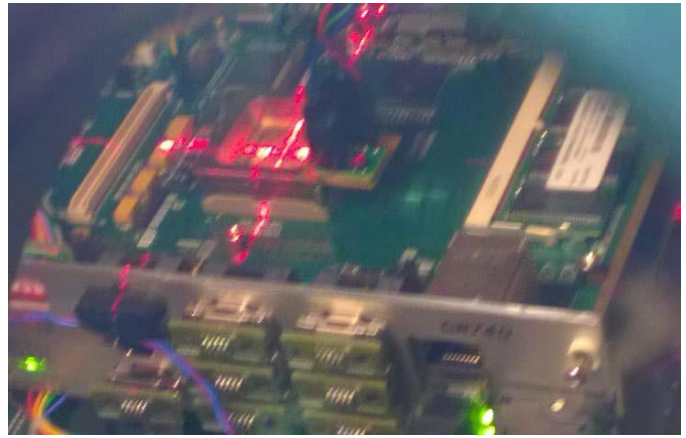
ALL TESTS SUCCESSFULLY COMPLETED!

GR740 qualification results

Group E





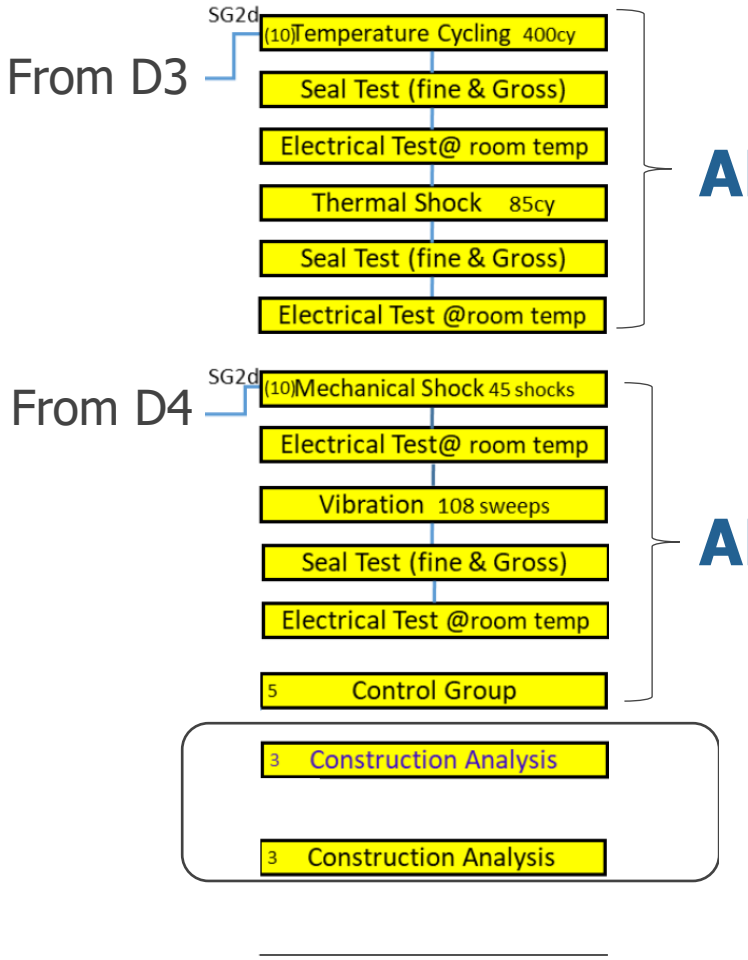


- TID tolerance of 300 krad(Si)
- Overall SEE rate below $1x10^{-5}$ events/device/day (GEO)
- SEL > 125 MeV.cm^2/mg (T>85ºC & max supply)

ALL TESTS SUCCESSFULLY COMPLETED!

GR740 qualification results

Delta ESCC



ALL TESTS SUCCESSFULLY COMPLETED!

ALL TESTS SUCCESSFULLY COMPLETED!

Expected in Q2 2021

Lessons Learnt

- In every development obtaining requirements and feedback from users is difficult but very valuable

- It is important to release prototypes early for:
  - Functional validation
  - Radiation characterisation
  - Allow customers to test and design-in the device

- Hardware/Software Co-engineering is critical to make sound design decisions. The GR740 has benefited from backward compatibility with earlier generation LEONs and a large software ecosystem for development available at an early stage

Leaning tower of Pisa in 2013 (Wikipedia)

What's next

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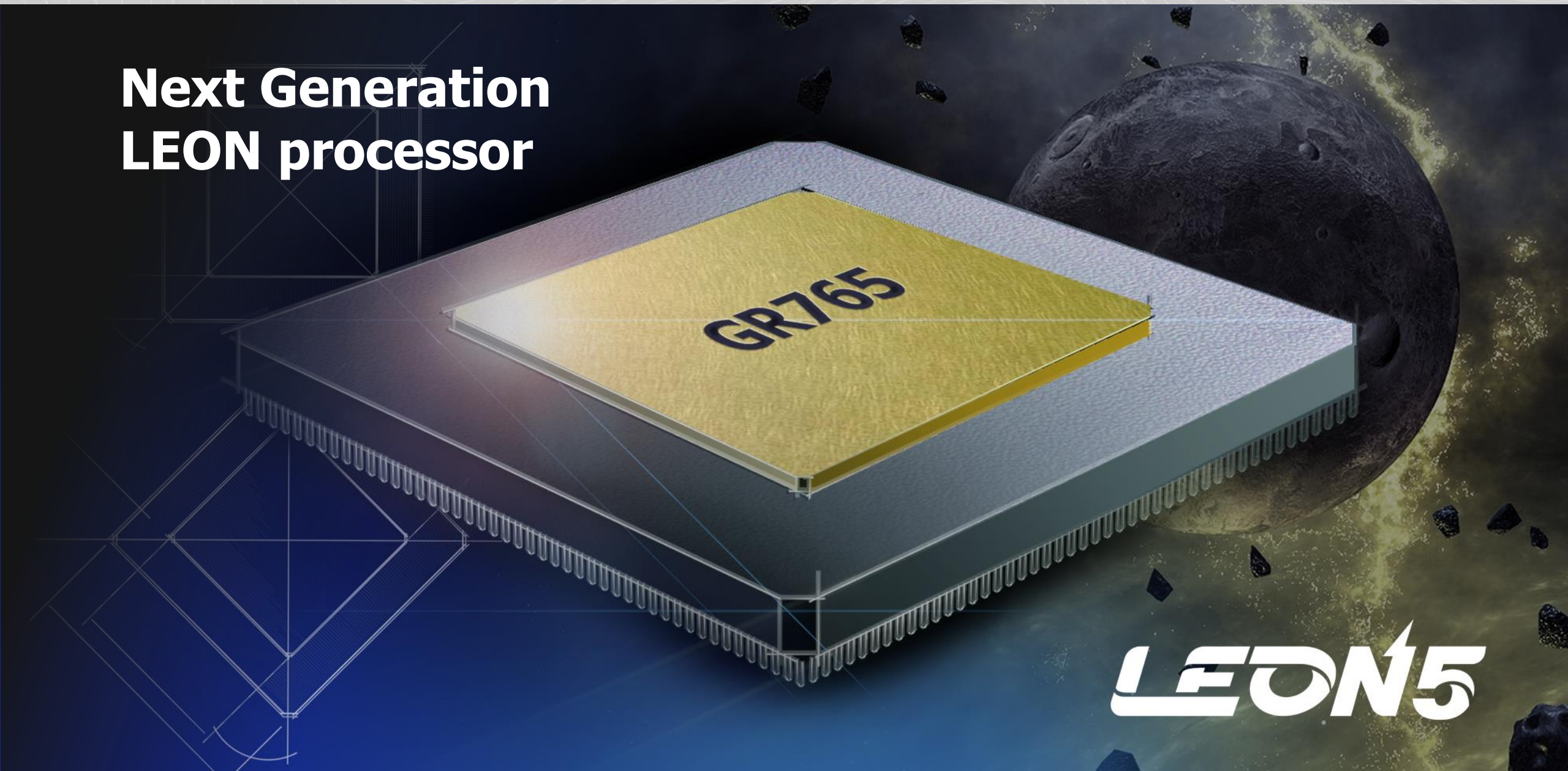
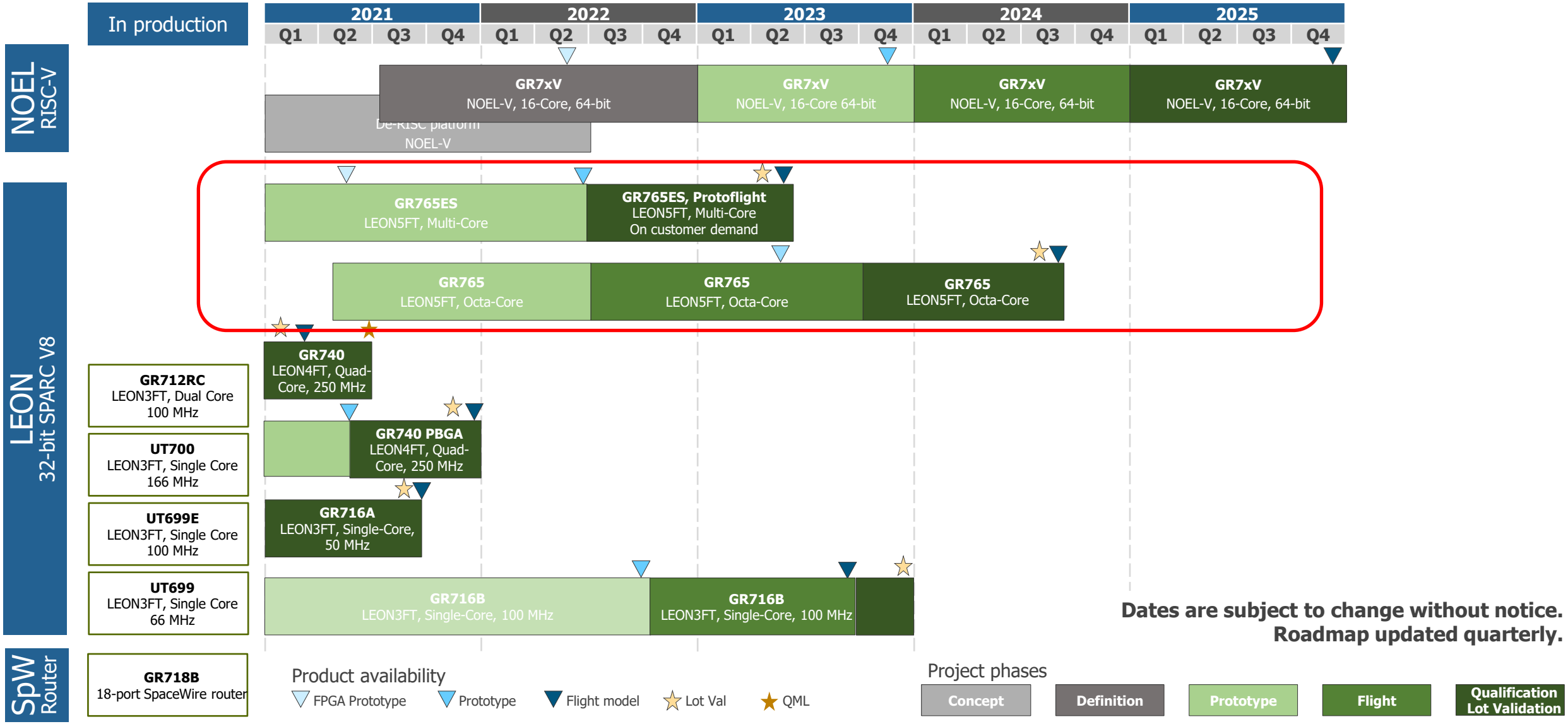
Next Generation LEON processor



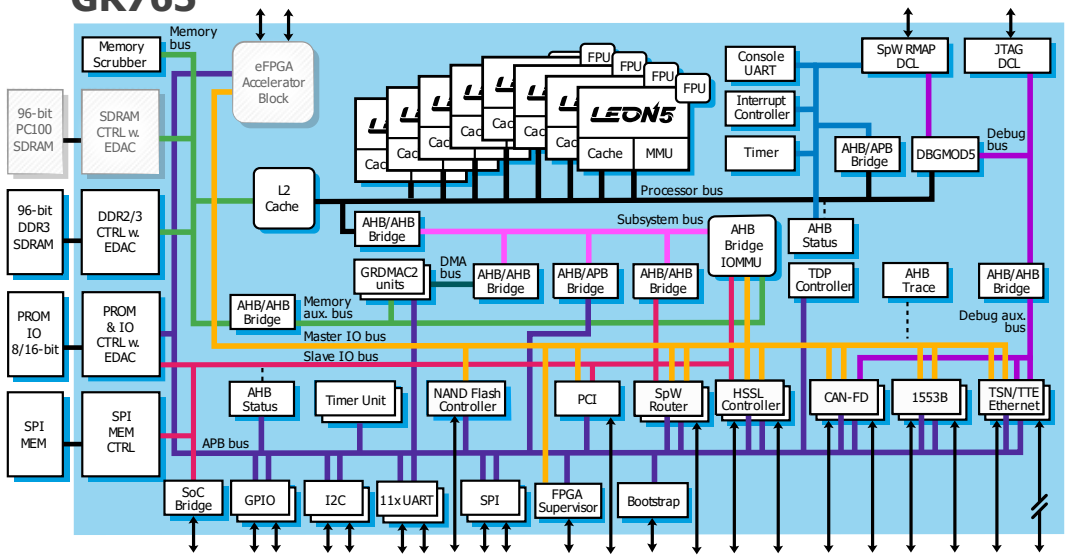
What's next



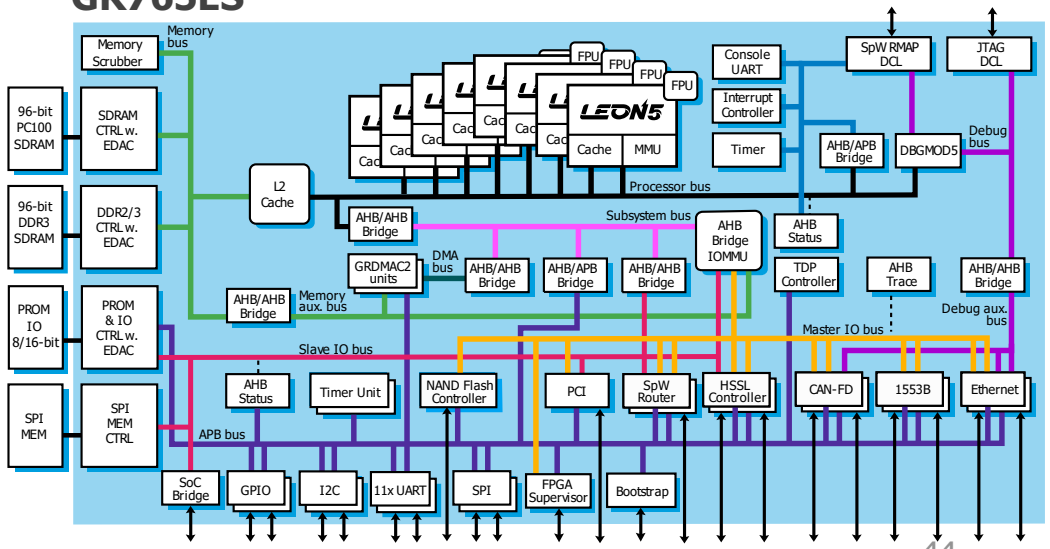
What's next

- The GR765 development builds on the successful GR740 quad-core LEON4FT component and maintains backward compatibility with it.
- The GR765 includes a octa-core LEON5FT, support for DDR3 SDRAM, high-speed serial link controllers and several other extensions.
- GR765ES is planned to be available on development boards mid-2022
- The GR765 SoC implementation starts in parallel with the manufacturing of GR765ES, GR765-XX (prototype) components are planned to be available Q2 2023.
- The GR765 development puts emphasis on computational performance, power efficiency, and support for mixed criticality application.
- The GR765 is being defined and implemented with focus on the space industry. Feedback can still be addressed, and your input is most welcome.
- GR765/ES user's manual will be posted during June 2021 at www.Gaisler.com/GR765

GR765



GR765ES

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