Radiation-Hardness Components at Scaled Technology Nodes (UTBB FDSOI28)

Test of Single-Events Effects in ARM Cores

Executive Summary

Authors: R. Liu[1], X-T. Li[1], L. Chen[1], J. Cunha[2], L. Summerer[2]

Affiliation:
[1] University of Saskatchewan, SK, Canada
[2] Advanced Concepts Team, European Space Agency (ESA)

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Contacts:

Li Chen (Professor)
Tel: 306-966-2507
Fax: 306-966-5407
e-mail: lic900@mail.usask.ca

Leopold Summerer (Technical Officer)
Tel: +31(0)715654192
Fax: +31(0)715658018
e-mail: act@esa.int

Available on the ACT website
http://www.esa.int/act

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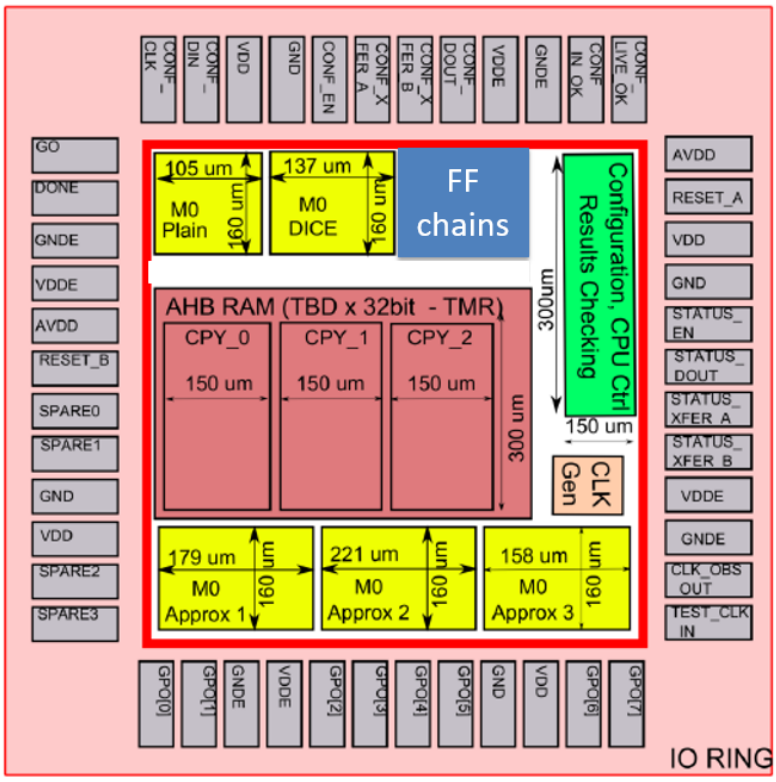
Picture:



Motivation:

The main goals of this Ariadna study was to determine the radiation hardness of potential future space processors. The AR0 test-chip was used to study the impact of SEUs and SETs on different versions of a hardened processor on UTBB-FDSOI 28nm technology, including DICE flip-flops, and three different hardening level of combinational logic.

Methodology:

Two chips especially designed to study the operation of complex circuits in ST Microelectronics 28 nm UTBB-FDSOI technology under radiation environments were developed and tested. The first test chip was designed for Single Event Transient (SET) pulse characterization using (1) a Pulse Capture detector, (2) a Vernier detector, and (3) a Pulse Filter detector. To study SET event rate vs. clock frequency, a high-speed Circuit for Radiation Effects Self-Test chain with 4096 stages was embedded in the chip. The second chip was used to to study the impact of SEUs and SETs on complex circuitry, namely different customized variants of an ARM microprocessor. For this, five variants of the ARM-Cortex-M0 are implemented on the die. A reference M0 microprocessor variant is implemented with regular flip-flops and normal logic. A second variant is implemented using custom-designed DICE flip-flops. Three other variants are implemented with different levels of redundant logic.

Results:

- We measured the single event pulse width of the 28nm UTBB-FDSOI due to irradiation particles, and found the pulse widths of the SET pulses significantly smaller than those of bulk technologies with similar feature size.
- We noticed from the experiments that the error rate contribution from SET is at least one order of magnitude smaller than that of the SEU.
- The 28nm UTFDSOI has a relatively high total dose tolerance. It shows a small leakage increase below 300 krad(SiO2), and the circuit is functional up to 1Mrad (SiO2).
- 5 ARM core processors have been developed on a single die and the test chip has passed functional testing.

Publications:

Please list here the complete references to the papers published or submitted for publication during the study.

- R. Liu, A. Evans, L. Chen, Y.-Q. Li, M. Glorieux, R. Wong, S.-J. Wen, J. Cunha, L. Summerer, and V. Ferlet-Cavrois, "Single Event Transient and TID Study in 28 nm UTBB FDSOI Technology," *IEEE Transactions on Nuclear Science,* Vol. PP, Issue 99, Nov. 9, 2016.
- H.-B. Wang, J. S. Kauppila, K. Lilja, M. Bounasser, L. Chen, M. Newton, Y.-Q. Li, R. Liu, B. L. Bhuva, S.-J. Wen, R. Wong, R. Fung, S. Baeg, and L. W. Massengill, "Evaluation of SEU Performance of 28-nm FDSOI Flip-flop Designs," *IEEE Transactions on Nuclear Science*, Vol. PP, Issue 99, Nov. 19, 2016.
- H.-B. Wang, R. Liu, L. Chen, Y.-Q. Li, J. S. Kauppila, B. L. Bhuva, K. Lilja, S.-J. Wen, R. Wong, R. Fung, and S. Baeg, "An Area Efficient Stacked Latch Design Tolerant to SEU in 28 nm FDSOI Technology," *IEEE Transactions on Nuclear Science,* Vol. PP, Issue 99, Nov. 9, 2016.

Highlights:

Additional laser and proton testing on the ARM test chip, to further evaluate the tolerance of the various ARM cores. Results published in 2018 NSREC/RADECS conferences