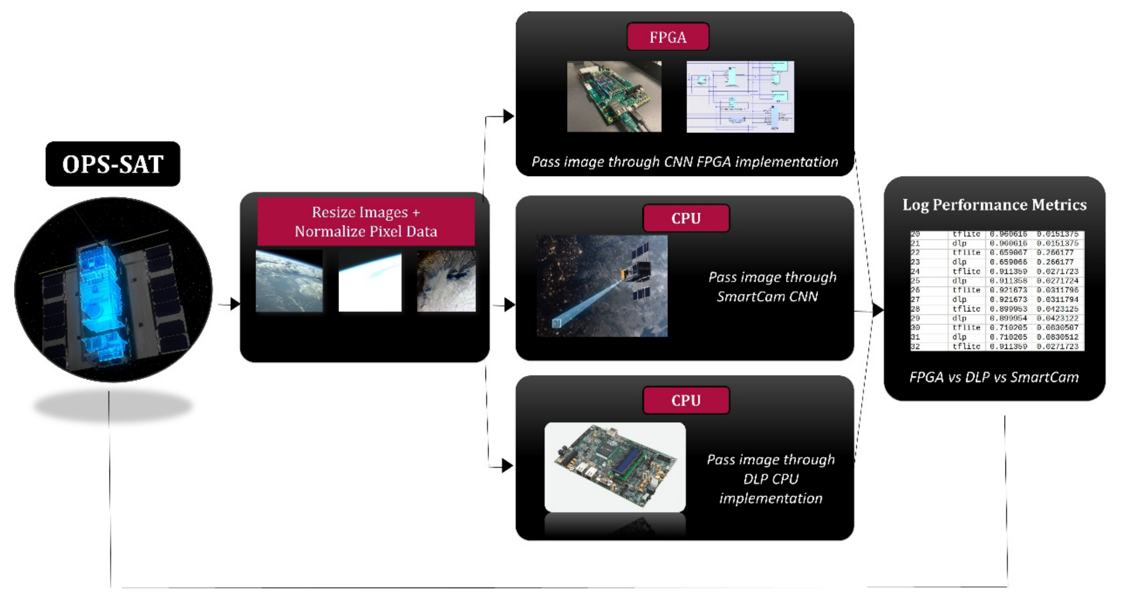

A Comparative Study of High-Level and Low-Level Implementations of Deep Learning Models for Spacecraft

Executive Summary Report (ESR)

Study

Campaign: OPS-SAT
Idea: I-2021-03755
MCSS.2112

Affiliation: Mission Control Space Services Inc.

Activity summary:
Mission Control deployed a low-level implementation of the OPS-SAT SmartCam model using a Field Programmable Gate Array (FPGA), comparing against a high-level CPU model using Tensorflow Lite. Experiments showed that the FPGA implementation reproduced the precision and accuracy of the high-level model, while running at a slower speed. Further optimizations of the FPGA are expected to close the gap in timing and unlock new methods for deploying deep learning on spacecraft.

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Executive Summary

Artificial intelligence (AI), in the form of deep neural networks, is a key enabler for space mission autonomy, performance, and functionality. The deployment of AI algorithms onboard spacecraft is an emerging capability currently limited to a handful of demonstration missions. Onboard AI holds the promise of empowering a new generation of more productive, autonomous spacecraft adaptable to new, complex, and unknown environments quickly. Several demonstrations of deep learning onboard EO satellites in orbit have been conducted and shown the utility of deep learning for EO in space, in particular the European Space Agency (ESA's) OPS-SAT [1] and Φ-Sat-1 [2]. OPS-SAT uses a CNN called SmartCam [3] to ingest data from an optical sensor onboard and classify incoming imagery as "Earth", "Edge of Space", or "Bad" to give an indication whether an image should be prioritized for downlink or whether it is oversaturated due to the presence of clouds. In the Φ-Sat-1 mission the Hyperscout-2 sensor by cosine feeds hyperspectral data to a Movidius Myriad 2 VPU which uses a neural network to segment clouds in the hyperspectral imagery, reducing the need for downlink for the large hypercube files since the sensor cannot see the earth's surface through cloud cover.

For remote sensing satellites neural networks are well-suited to deliver computer vision solutions using autonomous observation and data-filtering [4, 5] that enable human operators to maximize use of limited bandwidth. A crucial factor in the successful implementation of deep neural networks on space platforms is the embedded nature of such systems. The performance of onboard space processors lags that of their terrestrial counterparts due to the additional effort required to make circuitry that can operate in extreme radiation, thermal, and vacuum conditions [3]. The spaceborne processors available in the OPS-SAT Satellite Experimental Processing Platform, including the reconfigurable Field Programmable Gate Array (FPGA), address this performance gap and are the ideal test bed to develop new deep learning architectures for implementing neural networks on embedded space platforms.

Mission Control reports results of an experiment to use its Deep Learning Processor (DLP) compiler and run-time (See Figure 1) to hybridize the SmartCam model across the CPU and FPGA of the Cyclone V System-on-a-Chip (SoC) onboard OPS-SAT. FPGAs offer a balance of reconfigurability, generalizability, and utilization efficiency but FPGA deep learning frameworks are still in their infancy [4, 5]. Our FPGA implementation advances how AI can be deployed on spacecraft using the Neural Network Exchange Format (NNEF), an open and standard data format for exchanging information about trained neural networks. We perform the first comparative study to make use of NNEF for deep learning on a spacecraft by comparing our low-level implementation of the OPS-SAT SmartCam model against the existing high-level model that uses the Tensorflow Lite C API. The software developed as part of this study will explore the operational performance of SmartCam with a hybridized neural network and provide a modular scaffold for future space-based deep learning FPGA technology.

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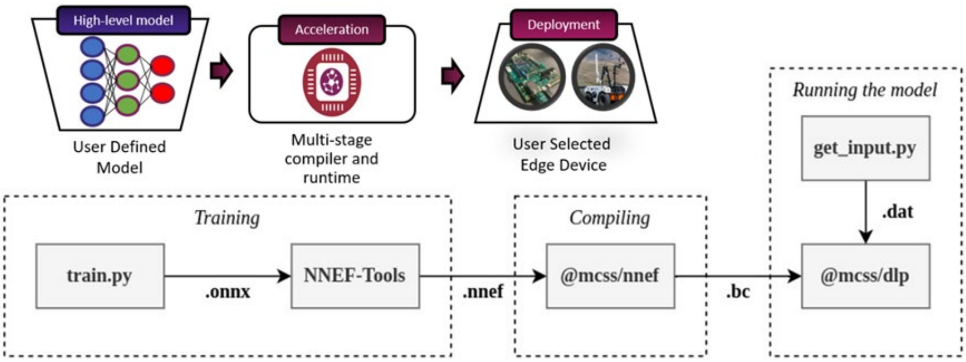

Figure 1 Mission Control's Deep Learning Accelerator deploys deep learning models on spaceflight hardware using the NNEF format [6].

Technical development to execute OPS-SAT Experiment 177 was broken down into a series of development milestones and smaller experiments using development boards. Initial FPGA development focused on successfully packaging a joint FPGA-CPU adder experiment to run first on MitySOM development boards and then the ESA Engineering Model (EM). This was supplemented by additional FPGA tests including streaming data directly to DDR through FIFO. Metrics reporting software was developed to report on a representative test set of SmartCam imagery, both for the TensorFlow Lite and DLP implementations. Features were added to the underlying DLP architecture to support the SmartCam network layers. Orbital path planning calculations analyzed when and where to acquire imagery during the Flight Model experiment.

The Software Architecture was written to begin the process of iteratively capturing RAW images using the onboard camera utility once the initial application was successfully uploaded to the FM. Flatsat testing concluded that the process of capturing an image, converting it from RAW to PNG, resizing and saving it takes around 20 seconds. The trade-off space for the FPGA implementation was explored, including toolchain evaluation like High Level Synthesis (HLS). The FPGA component was designed and is depicted in Figure 2.

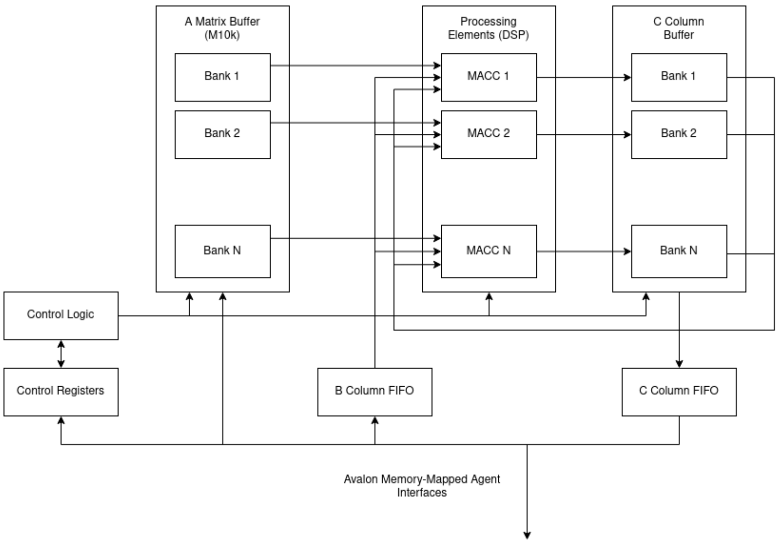

Figure 2 FPGA Component Design.

Mission Control ran multiple versions of the experiment, adding features and complexity with each step. Test versions, such as the FPGA adder were captured in Version 0.1. CPU-based experiments 0.2-0.5 advanced on the EM, overcoming problems with memory consumption to achieve a model that ran SmartCam with a simulated camera app embedded in the installation package. Release 1.0 included the first FPGA-based version to accelerate inference operations, while continuing to use test data. This release was validated on the MitySOM boards, with Version 1.1 using images from the camera on the FM. MitySOM testing and evaluation showed that the DLP and Tensorflow Lite (TFLite) implementations were equally accurate, precise, and sensitive, elapsed time showing that the TFLite CPU run was more efficient than a strictly CPU implementation of DLP, with average CPU time of 1599 ms for TFLite and 8644 ms for DLP. Future work will focus on the FPGA hybridization steps required to outperform the elapsed time criteria of the TFLite model. Detailed optimization of the FPGA optimization is expected to produce clear performance gains, particularly the use of Direct Memory Access that can decrease bottlenecks related to interfacing between the CPU and FPGA during computation. Mission Control will continue to mature the technology required to deploy deep learning on FPGA, advancing the Machine Learning Technological Readiness Level [7] required for future autonomy capabilities for the Earth, Moon, and Mars.

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