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Subject: **ESA RFP/3-15927/19/NL/FE/hh**

Title: **“For In-Flight Artificial Intelligence Proof-of-Concept Experiments”**

Document: **ESR - Executive Summary Report**

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Reference UB_3-15927_ESR
Issue/Revision 1.0
Date of Issue 30/11/2020
Status Release

Approval

Title	
Issue Number 1	**Revision Number** 0
Author Javier Parra, Álvaro Guerrero, Léonie Buckley, Aubrey Dunne	**Date** 30/11/2020
Approved by Aubrey Dunne	**Date of Approval** 30/11/2020

Change Log

Reason for change	Issue Number	Revision Number	Date
Initial version	1	0	12/10/2020

Change Record

Issue Number 1	Revision 1
Reason for change	Date

Distribution

Name/Organisation
Dr. Gianluca Furano/ESA
Dr. Antonios Tavoularis/ESA

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2 Acronyms

AI Artificial Intelligence
API Application Programming Interface

C&C Command & Control
CNN Convolutional Neural Network
COTS Commercial Off The Shelf
CV Computer Vision

DPE Dynamic Pipeline Engine

EM Engineering Model
EOT Eyes of Things
ESA European Space Agency

FM Flight Model

GPIO General Purpose Input/Output

IOD In-Orbit Demonstrator
ISP Image Signal Processor

MDK Movidius Development Kit

NCSDK Neural Compute Software Development Kit
NN Neural Network

OBC On-Board Computer

PC Personal Computer
PCE Pipeline Configuration Editor
PCIe Peripheral Component Interconnect express
PFM Proto Flight Model

ROM Read-Only Memory

SEE Single Event Effects
SIPP Streaming Image Processing Pipeline

TID Total Ionising Dose
TVAC Thermal VACuum

USB Universal Serial Bus

3 Executive Summary Report

3.1 Overview

Five different tasks were executed as part of the "For In-Flight Artificial Intelligence Proof-of-Concept Experiments" project. Together these tasks enable effective Artificial Intelligence (AI) inference and Computer Vision (CV) pipeline deployment on a dedicated hardware platform, and simultaneously demonstrated AI inference on an In-Orbit Demonstrator (IOD) cubesat platform. This report summarises the achievements of the project within each of the five tasks.

3.2 CV extensions

Before implementing and running complex applications, and understanding of embedded software development and of the underlying architecture of the Myriad 2 is typically required. In order to facilitate an alternative and more user-friendly application development approach, a set of tools, called CV extensions, was developed with one objective: expose a subset of the CV and Image Signal Processor (ISP) capabilities of Myriad 2 in an easy-to-use manner. Furthermore, they also maintain the performance of bare metal implemented applications.

In the Movidius Development Kit (MDK), image processing tasks are typically implemented via the Streaming Image Processing Pipeline (SIPP) framework. The approach used by this framework involves a graph of connected filters in which data is streamed from one filter to the next one on a line-by-line basis. However, the graph and the parameters of each filter, which usually must be configured before use, have to be implemented manually using code. This is an error-prone process in which errors are difficult to track and where minor, single-filter changes lead to the modification of several lines of code.

The **CVAI Toolkit**™ provides a solution to the previous problems, by implementing a tool that allows to construct and use arbitrary SIPP pipelines at runtime by using the already existing SIPP framework and calls, and a separate tool that allows to more easily generate SIPP pipelines.

Furthermore, the **Dynamic Pipeline Engine (DPE)** was developed, which is a tool that allows the construction and use of ISP and CV pipelines, which are previously serialized as Pipeline Configuration Data (*.pcd*) files. Pipelines can be destroyed and reconstructed as required at runtime.

Finally, the **Pipeline Configuration Editor (PCE)** was created, which is a graphical tool that allows the user to design image processing pipelines, by representing the Hardware and Software SIPP filters as nodes whose parameters and connections can be configured.

In order to verify the implemented solutions, two DPE constructed SIPP pipeline were analysed to check that the output when using said pipelines matched with the output obtained when manually coding the same equivalent pipelines. The developed workflow can be seen in Figure 1.

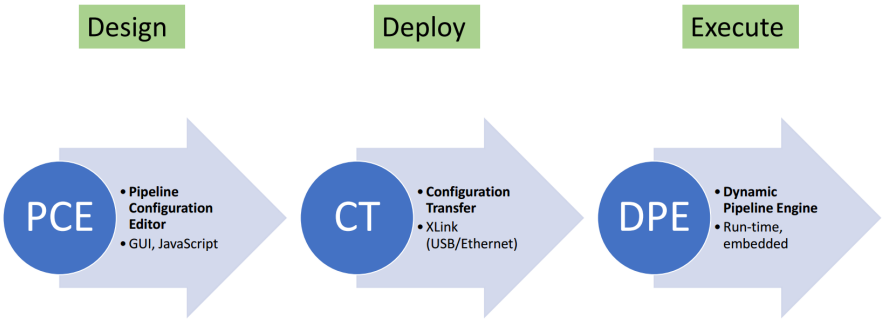

Figure 1: Image processing substeps

3.3 Ethernet Software Stack

The XLink component handles all the communications in the host (Personal Computer (PC)) and in the external device (Myriad 2) through a set of generic Application Programming Interface (API) functions. With them, it allows communication between the host and the Myriad 2 over different physical channels. The XLink software layer sits between the application and the drivers, so that the user does not need to be aware of the particular communication channel used.

The goal of this task was to add Ethernet to the list of protocols handled by XLink, by default only composed by the Universal Serial Bus (USB) and the Peripheral Component Interconnect express (PCIe) protocols. As part of the task, several characteristics were developed and configured at different layers within the protocol:

- **Different required clocks**. All clocks and attributes were configured to enable selection of the communication protocol to be used to perform the inference, providing the required functionalities to run AI inference over USB, PCIe or Ethernet.
- **Myriad 2 Discovery process**. The Ethernet protocol includes the special feature of not requiring to be physically connected to the PC, in contrast to USB or PCIe. For this reason, a specific protocol was implemented for performing the Myriad 2 discovery on the PC.
- **Add XLink with Ethernet to the NCSDKUB and to the FathomKey**. The NCSDKUB is a custom Ubotica™ developed version of the Neural Compute Software Development Kit (NCSDK) from Intel Movidius that includes different features and improvements. FathomKey is the name of the of the MDK AI inference firmware module.
- **Build the boot process**. The Myriad 2 is designed to boot from a number of different sources, such as USB or PCIe. It "'pre-boots" using code in its internal Read-Only Memory (ROM) which reads a specific set of General Purpose Input/Output (GPIO) pins, configures itself to load a boot image (custom binary firmware) from the GPIO-pin-specified source, and then runs this image once this boot image has been downloaded. Originally, the ROM bootloader could not download boot images over Ethernet. A two-stage Ethernet boot process was developed, utilising a custom primary boot image that resides in flash memory.

Finally, the Ethernet integration was tested using different Convolutional Neural Networks (CNNs), demonstrating the capability of using the Myriad 2 as an AI inference engine through Ethernet connectivity.

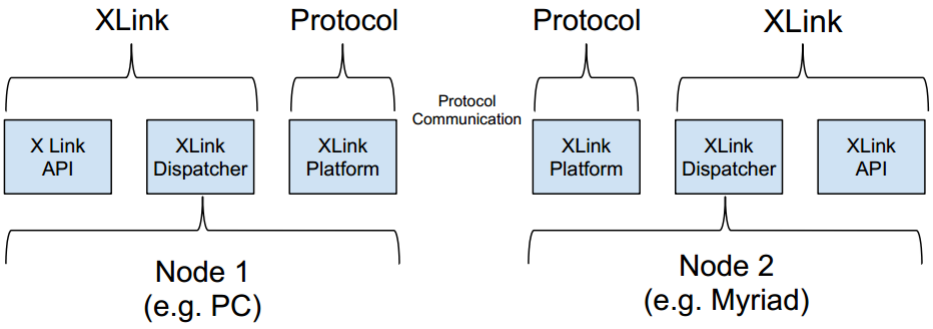

Figure 2: XLink component used by the PC and Myriad

3.4 HyperScout-2 Myriad 2 software integration

The PhiSat-1 satellite is an IOD whose payload integrates a novel hyperspectral sensor (the HyperScout-2) with a Myriad 2 AI engine. This task addressed the AI engine build and the software integration of the AI engine with the HyperScout-2 2 payload processor.

An pre-existing Myriad 2 processing board, termed the Eyes of Things (EOT) board, was used as the base design for the AI engine, due both to its ready availability and its suitable form factor. All active components on the EOT board were analysed for inclusion in the PhiSat-1 build, both in terms of their functional necessity, and their operational temperature range. Components that either had debug use or were associated with functionality not essential to AI inference were identified, and removed from the final custom board build. Four custom builds were completed, and basic USB connectivity and Myriad 2 operation was verified on each board. Three of these boards were shipped to cosine for integration with the payload and environmental testing (see subsection 3.5).

Several steps were required in order to enable AI inference from the payload processor using the EOT board, and to run the IOD verification tests on the HyperScout-2 payload processor.

- **Libusb** Libusb-1.0.so.0, compatible with the HyperScout-2 2 was required to enable communication with the Myriad device. On the HyperScout-2 2 device, Libusb-1.0.so.0 is placed in the usr/local/lib directory so that it can be found when compiling the applications.
- **MVNC** The installation for the mvnc library was altered to install only a minimal version. The installation of libraries such as OpenCV was removed. To ensure that the mvnc library is compatible with the HyperScout-2, this modified version of the mvnc library is compiled on the HyperScout-2. The location of the compiled mvnc library is then linked when compiling the host side applications.

  The modified install does the following:

  1. Delete any existing version of the NCSDK
  2. Download the NCSDK
  3. Remove unnecessary files
  4. Copy across custom install file
  5. build libmvnc.so

6. Run the install script
7. Run a test application to make sure it is working

- **Myriad Boot Images** The boot images for the tests run must be copied over to the HyperScout-2 device. No Myriad-side code is required to run on the HyperScout-2. When a test is run, the corresponding boot image is loaded onto the Myriad 2 through the host side application.
- **Compiling Host Side Application** When compiling host side applications on the HyperScout-2, the compiler resident on the device must be used: /opt/x-tools/x86_64-multilib-linux-gnu/bin/x86_64-multilib-linux-gnu-g++.
  Compiling on the HyperScout-2 using the resident compiler ensured that the application was compatible with the device requirements.
- **Recording Results** Results can be recorded on the HyperScout-2 in two different ways. Results can be saved locally in a files, or to the syslog on the device. When messages are written to the syslog they are timestamped automatically.
- **Syslog** Before running the tests, writing to the syslog must be enabled. This is done through running the following command: sudo syslogd -s 0 -O /var/log/messages.

3.5 HyperScout-2 Myriad 2 hardware integration

A series of functional testing was performed on the EOT board installed on the HyperScout-2 Proto Flight Model (PFM), in addition to testing of the HSMP-10 protection board and the APACER Secure Digital (SD) card. Three test types were performed on the EOT board for each test in the functional test campaign, specifically communication, diagnostic, inference and storage tests. Testing was carried out with the EOT installed on the HyperScout-2 PFM. The EOT functional tests consisted of the following tests:

- PFM dry assembly
- PFM wet assembly
- Installation in vibration structure
- Pre and post vibration campaign
- Pre and post Thermal VACuum (TVAC)
- Pre-shipment to TYVAK
- Post shipment
- Flight Model (FM) interface test
- Post S/C vibration
- Post S/C TVAC

All of these tests passed. TVAC testing was also conducted as part of the acceptance level environmental testing (conducted at payload level). Interface temperature, Myriad 2 temperature, and Myriad 2 power draw were recorded for each test. Diagnostic Myriad 2 self-tests were conducted during the functional test of Myriad 2 interfaced with the PFM On-Board Computer (OBC), and no critical issues were identified. The test was conducted at payload level. Finally, function tests of the EOT were conducted post vibration and post TVAC, all of which were successful.

3.6 CubeSat-grade board design

The board design task was to design and develop a Myriad 2-based processing board suitable for CubeSat integrations - a CubeSat-grade AI inference and processing engine. The design requirement was for a Commercial Off The Shelf (COTS) board that is suitable for flight. The CubeSat-grade board was designed from scratch, but using many of the design features of the EOT board. The design adheres to the European Space Agency (ESA) PC104 form-factor cubesat board requirements. All processing on the board is performed by the Myriad 2, including all communications and peripheral management. The board is designed for application to image processing, AI inference, and combinations of these two operations. Data to be processed can be on-boarded via one of two primary data interfaces, or can alternatively be captured directly from an interfaced image sensor (over either serial or parallel interfaces).

The CubeSat-grade board has been designed to provide a level of flexibility and configurability to the end user, both via hardware and software options, enabling configuration of the board in both Engineering Model (EM) and FM versions. All board components are COTS devices (with the exception of the Dosimeter which has partially undergone radiation qualification). Where possible, components were chosen that either have space heritage from previous missions, or that have radiation characterisation results available (Total Ionising Dose (TID) and/or Single Event Effects (SEE)). Neither failure of passives nor indirect propagation of voltages as a result of regulator failures were considered during the design process.
The CubeSat-grade board is designed such that either Ethernet or USB is used as the data transfer and Command & Control (C&C) interface to the board in the standard AI/CV engine operating paradigm. CV processing is performed via the Ubotica™ DPE firmware module. In this paradigm, the CubeSat-grade board operation is completely controlled by Ubotica™ software running on a host OBC, which communicates with Ubotica™ firmware executing on the board. The software manages the transmission of the firmware (boot image) to the board via the chosen primary interface, and subsequently sends Neural Network (NN) blobs and/or DPE configurations to the board over this interface to configure the engine. Thereafter, images/input tensors can be continuously transmitted to the board over the primary interface, with processed results returned over the same interface. In this way the CubeSat-grade board acts as a server to the client application running on the OBC. A power cycle of the board requires a re-transmission of the firmware (boot image). The CubeSat-grade board is designed to accommodate a variety of different operational modalities, and in line with this it offers a range of physical input/output interfaces. Certain interfaces are designed for utilising when performing specific functionalities, while others are more generic.

Key design features of the CubeSat-grade board are:

- On-board integrated latch-up protection

- Operates from single 5V supply
- Serial NOR flash for boot
- 3.3V I/O voltage
- Parallel and MIPI camera interfaces for direct sensor connection
- microSD card for non-volatile data storage
- Additional integrated satellite-oriented peripherals
  - Floating Gate Dosimeter for radiation sensing
  - IMU (3D accelerometer and gyroscope)
- Targets sub 5W power envelope (application dependent)
- Stackable 2x dual row board-edge headers for power delivery and platform/payload communications

A functional overview of the CubeSat-grade board is shown in Figure 3.

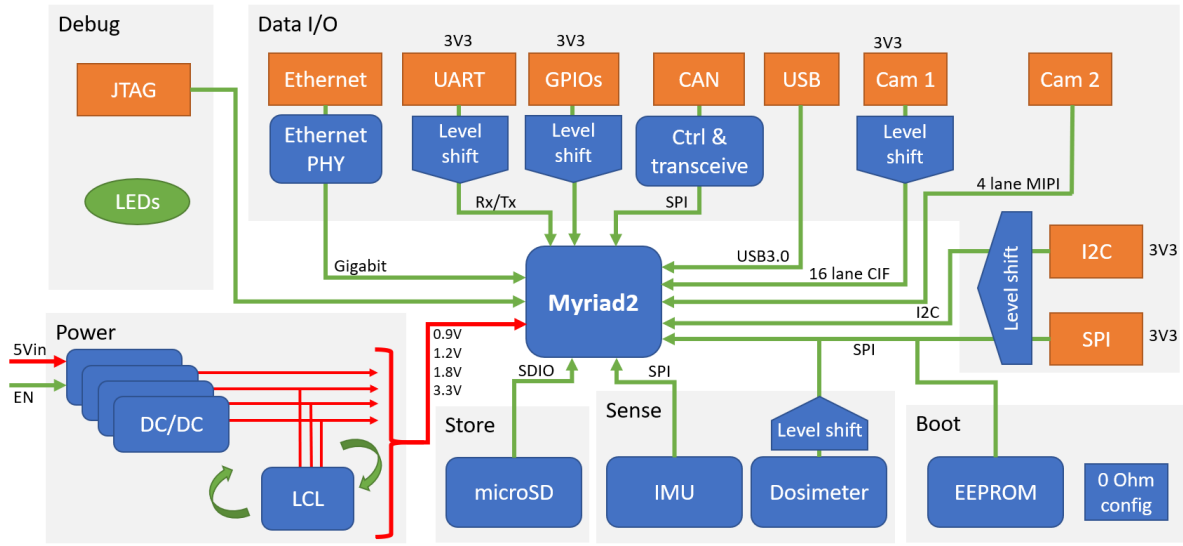

Figure 3: CubeSat-grade board functional block diagram

3.7 Summary

The work conducted under the "For In-Flight Artificial Intelligence Proof-of-Concept Experiments" project covers a range of activities that together further the goal of enabling in-orbit AI inference. Software solutions to both extend the range of operations that can be executed on the Myriad 2 via a host API, and enable these operations to be requested over an Ethernet link, were developed and validated. In parallel, the software and hardware integration of a Myriad 2-based AI engine with a CubeSat hyperspectral payload was conducted and verified. This subsequently enabled the first ever accelerated AI inference on an orbiting satellite, which was achieved aboard ESA's PhiSat-1 satellite in September 2020. Finally, and in order to facilitate other satellites to replicate and build on PhiSat-1's feat, a PC104 form-factor CubeSat-grade board was designed as a Myriad 2-powered CV and AI processing engine that is software-integratable with the Ubotica™ CVAI Toolkit™.