Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications Executive Summary Report

Prepared by:	SITAEL S.p.A. LF15A Team	Date:	26/01/2024
Verified by:	M. Bacci (SITAEL S.p.A., deputy Technical Manager)	Date:	26/01/2024
Approved by:	G. Piscopiello (SITAEL S.p.A., Project Manager)	Date:	26/01/2024

ESA STUDY CONTRACT REPORT

ESA CONTRACT No.	SUBJECT	CONTRACTOR
4000117048/16/NL/P	Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications	SITAEL S.p.A. Via San Sabino 21 70042 Mola di Bari (BA) - ITALY Tel.: +39.080.53.21.796 - Fax: +39.080.53.55.048 E-mail: info@sitael.com
ESA CR () No.	No. of volumes 1 This is volume No. 1	CONTRACTOR'S REFERENCE SIT-LF15A-RP-0101

ABSTRACT

The objective of the project is to perform the radiation and reliability characterisation of LFoundry S.r.l. 150nm MS CMOS process (LF15A) in order to provide a first necessary step in the roadmap of evaluating its adoption for space applications.

This document establishes a concise summary of the findings of the contract.

The work described in this report was done under ESA contract. Responsibility for the contents resides in the author or organisation that prepared it.

Names of authors

G. Piscopiello (SITAEL S.p.A.)
M. Bacci (SITAEL S.p.A.)
SITAEL S.p.A. Design Engineering Team

NAME OF ESA STUDY MANAGER	ESA BUDGET HEADING
Mr. Juergen Beister DIV: ESTEC/ TEC-EDC DIRECTORATE: ESA Data Systems and Microelectronics Division, Components Section	

Distribution List

Document title: Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications Executive Summary Report

Distribution	Type	Copies
ESA	E	1*
IMT	E	1*
LFoundry	E	1*
RedCat	E	1*
TAS-I	E	1*
UniPD	E	1*
SITAEL	I	1*

I = Internal
E = External
* = Electronic Copy

Change Document Record

Document title: Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications Executive Summary Report

Issue	Date	Total pages	Modified pages	Notes
1.0	26/01/2024	22	None	First issue of the document

List of acronyms

Abbreviation	Meaning
AD	Applicable Document
ASIC	Application Specific Integrated Circuits
CAD	Computer-Aided Drafting
EDA	Electronic Design Automation
ELT	Early Life Test
ESA	European Space Agency
ESCC	European Space Components Coordination
ESD	Electric Static Discharge
FPGA	Field Programmable Gate Array
HTOL	High Temperature Operating Life
HV	High Voltage
IMT	Ingegneria Marketing Tecnologia S.r.l.
LET	Linear Energy Transfer
LF15A	"Evaluation of LFoundry mixed-signal 150nm CMOS process for Space Applications" Project
LFoundry	LFoundry S.r.l.
LV	Low Voltage
MOS	Metal Oxide Semicontiuctor
PDK	Process Design Kit
RD	Reference Document
RHBD	Rad Hard Data Base
RedCat	RedCat Devices Srl
SEE	Single Event Effect
SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
SITAEL	SITAEL S.p.A.
SOW	Statement Of Work
STI	Shallow Trench Isolation
SRAM	Static Random Access Memory
TAS-I	Thales Alenia Space Italia S.p.A.
TID	Total Ionizing Dose
TV1	Test Vehicle 1
TV2	Test Vehicle 2
UniPD	Università di Padova – Dipartimento di Ingegneria dell'Informazione
VHDL	Very high speed integrated circuits HDL

TABLE OF CONTENTS

1. Scope ***7***

2. References ***8***

2.1. Applicable Documents *8*

2.2. Reference Documents *8*

3. Background of the activity and project Goal ***10***

3.1. Consortium Composition *11*

3.2. Project Tasks *11*

4. Project Overview ***14***

4.1. Test Vehicle 1 (TV1) *14*

4.2. Test Vehicle 2 (TV2) *17*

4.3. Project Outcomes *20*

LIST OF FIGURES

Fig. 4.1: TV1 layout – top view 16
Fig. 4.2: TV1 Hierarchy View. 17

LIST OF TABLES

Tab. 4.1: Implemented test structures. 15

1. Scope

The present document summarises the work performed within the framework of ESA Contract No. 4000117048/16/NL/PS - LF15A – Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications [AD - 1].

In the following pages, a concise descriptive summary of the outputs produced is provided.

2. References

2.1. Applicable Documents

[AD - 1] ESA Contract No. 4000117048/16/NL/PS - LF15A – Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications

[AD - 2] “Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications” – Statement of Work, ESA, ref. ESA-GSTP-TECQTC-SOW-125, Issue 1, 30/11/2015

[AD - 3] “Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications” – SITAEL Proposal, ref. P.15.264.01, issue 1.0, 29/01/2016

[AD - 4] “Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications” – Negotiation Meeting Minutes, ref. SIT-LF15A-MN-0001, 08/03/2016

[AD - 5] “Requirement for the Technology Flow Qualification of Electronic Component for Space Application”, ESCC 25400

[AD - 6] “Requirement for the Technology Flow Qualification of Monolithic Microcircuits”, ESCC 2549000

[AD - 7] “Evaluation Test Programme for Monolithic Integrated Circuits”, ESCC 2269000

[AD - 8] “Space Product Assurance ASIC and FPGA Development”, ECSS-Q-ST-60-02C

[AD - 9] “Total Dose Steady-State Irradiation”, ESCC 22900

[AD - 10] “SEE Test Method and Guidelines”, ESCC 25100

[AD - 11] VHDL Modelling Guidelines, ASIC/001 Issue 1, September 1994, ESA

[AD - 12] ECSS-Q-ST-60-02C, “ASIC and FPGA development”

2.2. Reference Documents

[RD 1] Radiation Hardness Assurance - EEE Components – ref. 'ECSS-Q-ST-60-15C

[RD 2] Techniques for Radiation Effects Mitigation in ASICs and FPGAs, ESA Handbook – ref. 'ECSS-Q-HB-60-02A DIR2

[RD 3] TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD – ref. 'ESCC Basic Specification No. 22900

[RD 4] SINGLE EVENT EFFECTS TEST METHOD AND GUIDELINES – ref. ' ESCC Basic Specification No. 25100

[RD 5] Requirements for the Techlogy Flow Qualification of Electronic Components for Space Application – ref. 'ESCC Basic Specification No. 25400

[RD 6] Requirements for the Technology Flow Qualification of Monolithic Microcircuits ESCC – ref. 'ESCC Basic Specification No. 2549000

[RD 7] DL1 - A-MS ASIC Technology Flow description - ref. SIT-LF15A-RP-0001)

[RD 8] DL2 - Preliminary A-MS DK specification (including gap analysis) – ref. SIT-LF15A-RP-0002

[RD 9] DL3 - LFoundry intrinsic reliability report / data package – ref. SIT-LF15A-RP-0003

[RD 10] DL4 - Intrinsic reliability assessment report including gap analysis – ref. SIT-LF15A-RP-0004

[RD 11] DL5 - Radiation effects and mitigation techniques assessment report – ref. SIT-LF15A-RP-0005

[RD 12] DL6 - Description of selected test structures, radiation and reliability test plans – ref. SIT-LF15A-PL-0006

[RD 13] DL8 - Preliminary TID test plan - ref. SIT-LF15A-PL-0008

[RD 14] DL9 - Task 2 test report: TID test report on existing structures – ref. SIT-LF15A-RP-0009

[RD 15] DL10 Split 1 - DL10A - Preliminary Test Chip Specification (Parametriic List) Part A: SITAEL Test Vehicle (TV1) – ref. SIT-LF15A-RP-0010A

[RD 16] DL10 Split 2 - DL10B - Preliminary Test Chip Specification (Parametric List) Part B: RedCat Test Vehicle (TV2) – ref. SIT-LF15A-RP-0010B

[RD 17] DL11 Split 1 - DL11A - Detailed Specification Part A: SITAEL Test Vehicle (TV1) – ref. SIT-LF15A-RP-0011A

[RD 18] DL11 Split 2 – DL11B - Detailed Specification Part B: RedCat Test Vehicle (TV2) – ref. SIT-LF15A-RP-0011B

[RD 19] DL12 - Evaluation Test Programme – ref. SIT-LF15A-RP-0012

[RD 20] DL13 Split 1 – REPORT on CONSTRUCTIONAL ANALYSIS Device LF15A TV1 (ref. RPT/2126/19/IMT-BA)

[RD 21] DL13 Split 2 – Single Event Upset Radiation Verification Test Report on LF15A TV1 (ref. RPT/2840/22/IMT-BA)

[RD 22] DL13 Split 3 – REPORT On Temperature Cycling (TC) Early Life Test (ELT) High Temperature Operating Life (HTOL) LF15A TV1 – ref. RPT/2356/20/IMT-BA

[RD 23] DL13 Split 4 – REPORT on TOTAL IONISING DOSE Radiation Verification LF15A TV1 – ref. RPT/2526/20/IMT-BA

[RD 24] DL13 Split 5 – REPORT on CONSTRUCTIONAL ANALYSIS Device LF15A TV2 SRAM – ref. RPT/2125/19/IMT-BA

[RD 25] DL13 Split 6 – REPORT on ELECTROSTATIC DISCHARGE SENSITIVITY TESTING HUMAN BODY MODEL (ESD HBM) Device LF15A TV2 SRAM – ref. RPT/2277/19/IMT-BA

[RD 26] DL13 Split 7 – REPORT on LATCH-UP Device LF15A TV2 SRAM – ref. RPT/2276/19/IMT-BA

[RD 27] DL13 Split 8 – SINGLE EVENT EFFECT Radiation Verification Test Report on LF15A TV2 – ref. RPT/115/18/IMT

[RD 28] DL13 Split 9 – REPORT on Temperature Cycling (TC) Early Life Test (ELT) High Temperature Operating Life (HTOL) LF15A TV2 – ref. RPT/2094/19/IMT-BA

[RD 29] DL13 Split 10 – REPORT on TOTAL IONISING DOSE Radiation Verification LF15A TV2 – ref. RPT/2236/19/IMT-BA

[RD 30] DL14 - Final report including proposal for recommended future work – ref. SIT-LF15A-RP-0014

[RD 31] DL15 - Design Kit for space A-MS ASICs (beta version) – ref. SIT-LF15A-RP-0015

[RD 32] LF15A Contractual Final Report – ref. SIT-LF15A-RP-0100

3. Background of the activity and project Goal

Application specific integrated circuits (ASICs) are commonly used in both spacecraft subsystems as well as payload instruments. This includes digital, analogue, and mixed signal applications. Analogue and Mixed Signal (A-MS) ASICs provide savings in volume, power, and weight versus discrete designs and often lead to a performance benefit for science accuracy or bandwidth. The concentration of functions that once were distributed on multiple PCBs into single components, also lead to an overall reliability improvement due to the reduction of components, connections, PCBs, wires, and solder joints.

Possible applications of mixed signal ASICs include the integration of discrete low/medium complexity of analogue & digital functions, such as for example:

- Sensors and Detectors signal conditioning and A to D and D to A conversion
- Telemetry acquisition, Telecommand drivers
- Power conversion, control, and distribution
- CMOS image sensors and Charge Coupled Device (CCD) detectors readout.
- High speed communication interfaces
- RF and IF down/up conversion

At program negotiation stage following several European rad-hard mixed-signal ASIC supply chains for space were existing in various maturity levels or were currently being developed:

- Atmel 150 nm SOI (wafer fab in Taiwan)
- IMEC DARE 180 (wafer fab in Taiwan)
- IMEC DARE 180X (wafer fab in Malaysia)
- IMEC DARE 65 (wafer fab in Taiwan and/or France)
- Arquimea / IHP 250 (wafer fab in Germany)
- ID-MOS/XFAB 350nm CMOS (wafer fab in Germany)
- IMEC DARE/Onsemi 350nm CMOS (wafer fab in Belgium)
- ST: Multiple process options down to 65nm (wafer fabs in Europe)

With a usage of CMOS based processes in the range of 100-200 nm owned by non-European foundries.

Therefore, an Italian based consortium consisting of SITAEL S.p.A, Redcat S.r.l., Lfoundry S.r.l., IMT S.r.l., University of Padova and Thales Alenia Space Italia S.p.A. has proposed to ESA a project for the evaluation of a mixed signal 150nm CMOS process (LF15A), owned by LFoundry S.r.l., for space applications.

This led to the starting of this GSTP-based ESA contract aiming to exploit the different skills of consortium members in evaluating for space applications LFoundry mixed-signal 150nm CMOS process (LF15A, available from Avezzano manufacturing plant) with the aim to introduce a very attractive European solution in the market.

3.1. Consortium Composition

An integrated industrial and research team has been setup combining the necessary expertise and capabilities to provide a thorough, reliable, and competitive outcome to the "Evaluation of LFoundry mixed-signal 150nm CMOS process (LF15A) for Space Applications" project (ESA RFQ/3-14429/15/NL/PS).

The integrated team is composed by:

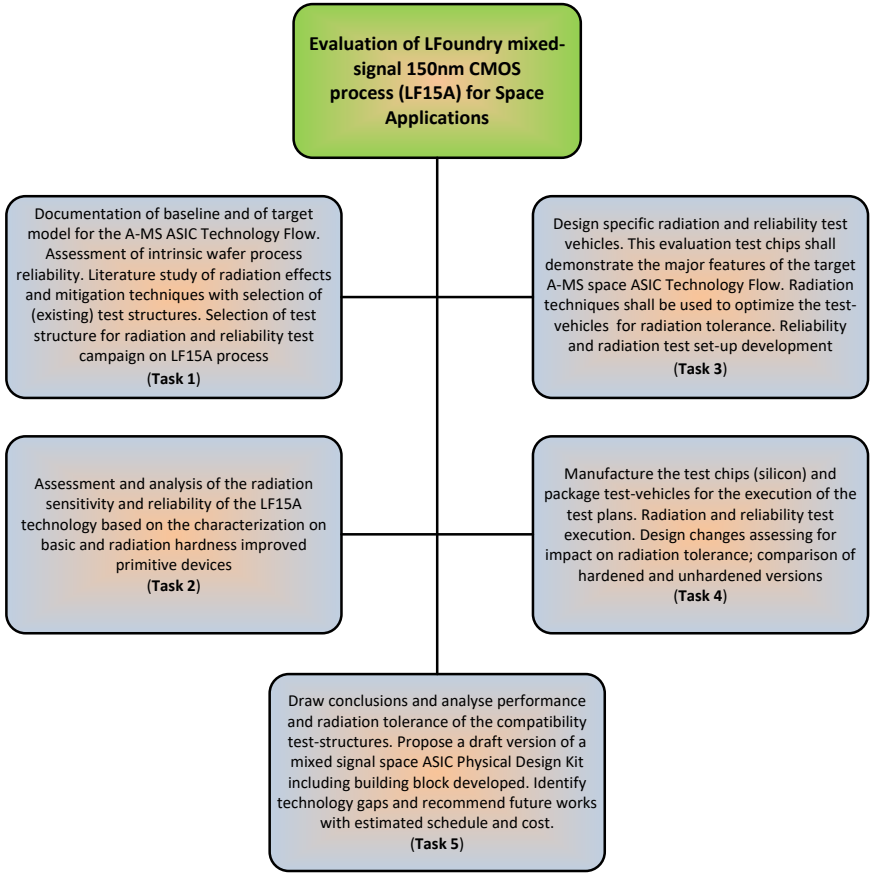
- SITAEL, acting as Prime, responsible of management, contractual and technical aspects, beyond to guarantee the execution of the development of one of the two test vehicles and its test data analysis and correlation.
- IMT, acting as subcontractor for SITAEL, responsible of the evaluation testing activity, from the definition of test plan and procedures to the test set-up development and manufacturing, to the execution of the tests and production of related test reports.
- LFoundry, acting as subcontractor for SITAEL, responsible of Test Vehicles fabrication and to provide partners with the proper support related to the process and PDK, as indicated in WBS.
- RedCat Devices (also named RedCat), acting as subcontractor for SITAEL, responsible of development of one of the two test vehicles and of the related test results analysis and correlation
- Thales Alenia Space Italy (also named TAS-I or TAS), acting as subcontractor for SITAEL, responsible of the evaluation requirement definition on the base of space user needs and of Test Vehicles packaging.
- University of Padua (also named UniPD), acting as subcontractor for SITAEL, responsible of the intrinsic reliability characterization of elemental structures and radiation-hardened elemental structures of the technology.

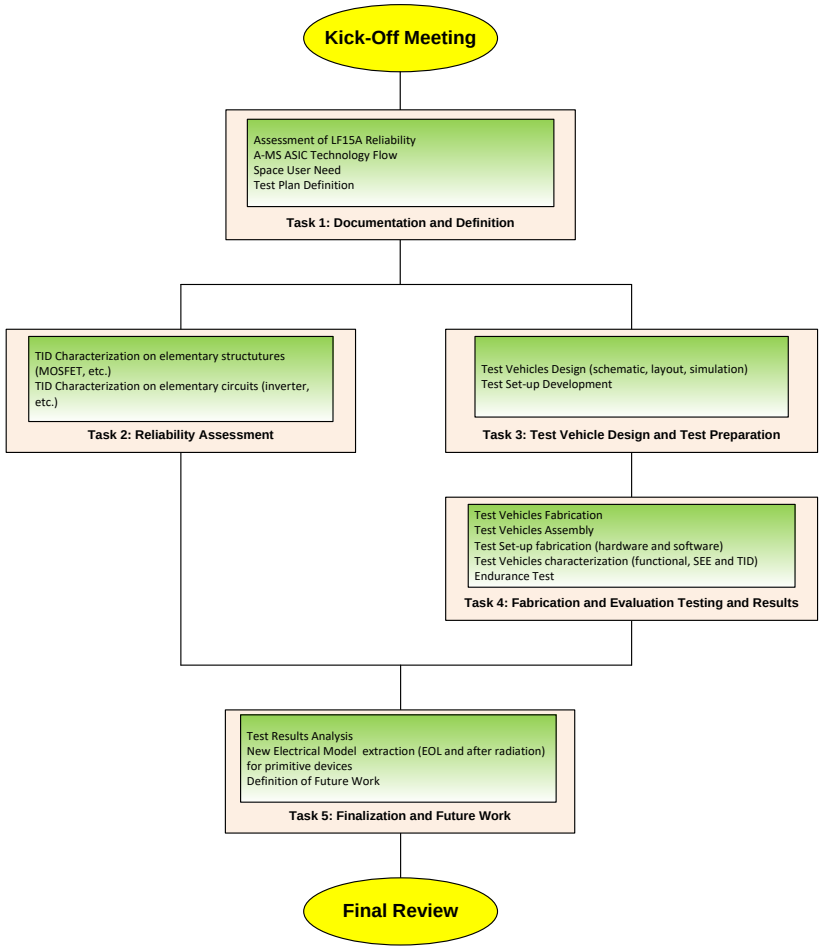
3.2. Project Tasks

Activities proposed for this work were organized in the following five tasks (with additional supporting one dedicated to project office):

- Task 1 – Documentation and Definitions
- Task 2 – Reliability assessment
- Task 3 – Test vehicle design and test preparation
- Task 4 – Fabrication and Evaluation testing
- Task 5 – Finalisation and evaluation of future required work

The project tree of the different tasks and their logical flow during the program are detailed in the following pictures:





4. Project Overview

The project started by the analysis of the needs for mixed-signal ASICs from the space community and planned space missions. Investigated space community equipment requirements on mixed-signal ASIC included payload as well as platform systems covering the instrumentation, control, power, and radio applications. Assessment of the quality, suitability and required improvement to mitigate the radiation effects of the LF15A design kit and technology flow description has then been performed together to an assessment of the intrinsic process reliability. A test plan has been defined including the radiation-tests, the reliability tests, and the acceptance test for the test-vehicles in accordance with the ESCC standards.

In parallel a characterization of total ionizing dose effects in elementary structures has been performed. MOSFETs behaviour has been experimentally assessed against TID induced degradation as a function of channel length and width. Physical modelling of the effects of leakage due to STI and spacers, short and narrow channel effects, etc. has been extracted. Small circuits (like inverter chains or other) have been also designed for experimental investigation of parametric drift in dynamic bias conditions to assess the technology potentiality for TID tolerance.

On the base of previous activities, the design of 2 test vehicles has been carried out together with the preparation of test set-up (and related test set-up control software) to evaluate the performances under radiation and endurance of the 2 test vehicles.

4.1. Test Vehicle 1 (TV1)

The Test Vehicle 1 (TV1) has been designed to evaluate the performances in terms of reliability and under radiation (TID and SEE) of the LF15A technology provided by LFoundry according to TAS selected design structures described in previous section. The exact process modules are: MOS18SL (standard 1.8V MOS module with single poly quad metal), MOS35 (3.3V and 5.0V MOS module, two additional gate oxides), MVGOX (3.3V gate oxide), HVGOX (5.0V gate oxide), M6 (6 metal layers), MIM (metal insulator metal capacitor), NISO (N isolation PWELL, additional NPN parasitic bipolar transistor).

The TV1 ASIC prototype is assembled in CPGA 256 pin ceramic package.

The TV1 contains several SET of primitive devices grouped on the basis of the measurements to be performed. Following table shows the implemented test structures including a short description:

Test Structure	Description
I-V	To measure current as function of applied voltages in straight and ELT transistor
C-V	To measure capacitances as function of applied voltages in straight and ELT transistor
MATCHING	To measure matching parameters in straight and ELT transistors
NOISE	To measure noise parameters in straight and ELT transistors
DIODE	To measure diode characteristics
BIPOLAR	To measure BJT characteristics
HV-MOS	To measure HV MOS characteristic
PASSIVE	To measure resistors and capacitors characteristics
DIGITAL	To evaluate the performances of a rad tolerant standard cell library
RING	To evaluate the effect of ageing and NTBI
SEU	To evaluate the performances of DICE flip-flop against SEE
BGR	To evaluate the performances of band-gap voltage reference

Tab. 4.1: Implemented test structures.

In most structures (I-V, C-V, MATCHING and NOISE), some service circuits have been added and they have been included in a service block.

The TV1 layout top view is shown in following picture. The physical size of the chip without scribe line is 6454.44 x 6694.44 μm^2. The location of the implemented test structures is highlighted by means of red and violet line boxes.

Low voltage test structures (I-V, C-V, Matching and Noise) contain services blocks that are mainly composed by drive logic and switches needed to select properly each primitive inside the test structure.

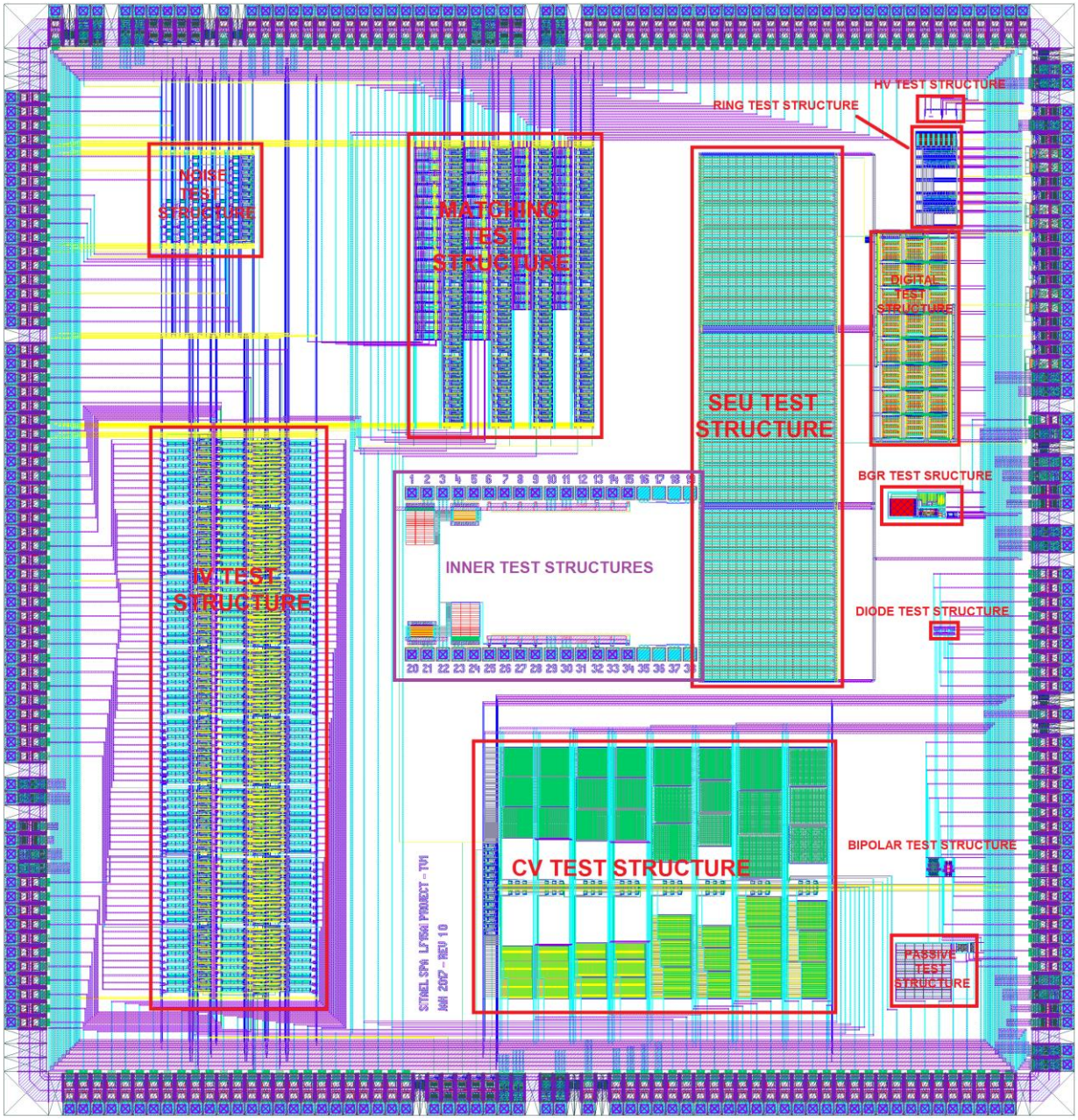


Fig. 4.1: TV1 layout – top view

In the following picture a hierarchy view of TV1 ASIC has been reported to allow an easier surfing thought the database.

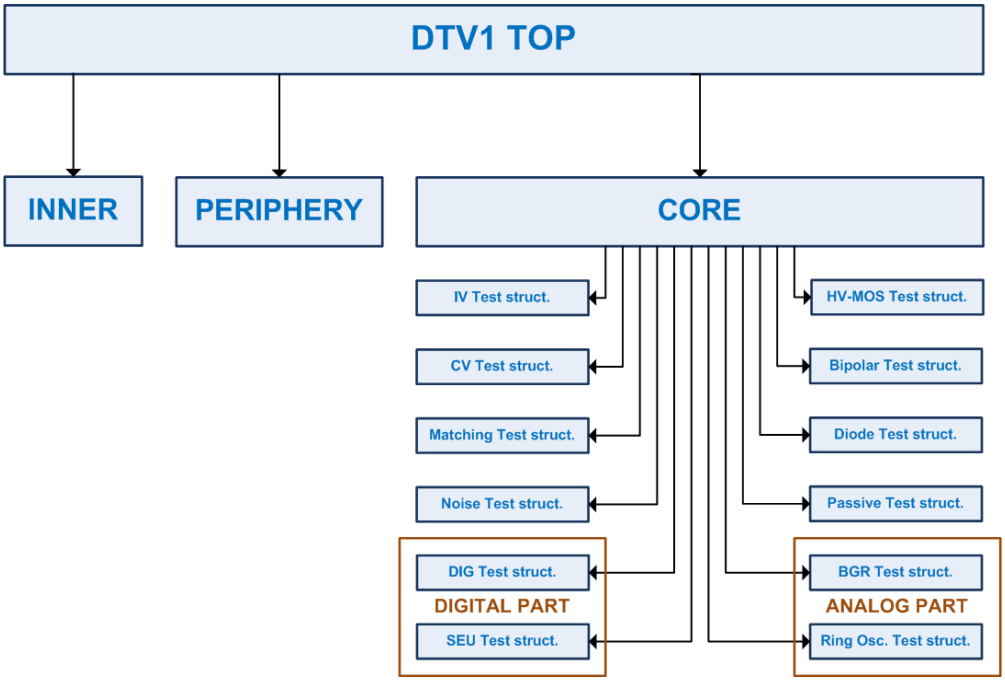
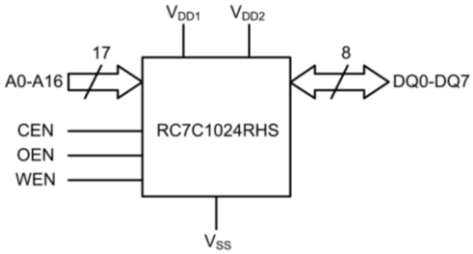


Fig. 4.2: TV1 Hierarchy View.

4.2. Test Vehicle 2 (TV2)

In the second test vehicle (TV2) a rad hard 1Mbit SRAM (RC7C1024RHSL) has been designed. The foundry gave support providing design and extraction rules files for elementary structures designed in non-conventional mode. RC7C1024RHSL is a 1024 kbit radiation hardened asynchronous SRAM memory, organized in eight 128 kbit blocks, each having 256 word lines (rows) and 512 bit lines (columns). The technology is LF15A with 1.8V as standard supply voltage. The external pins structure is as follows. First, there are eight I/O pads for data, which are inputs in writing and outputs in reading the memory. The control input pins are three: complementary write enable (WEN), chip enable (CEN) and output enable (OEN). Their truth table is described in table here below. Finally, 17 input pads are used for addressing the selected eight cells. Of these 17 input address bits, 8 are for rows and 9 for columns.

In following picture, the external pins scheme is illustrated, while in following table their function is explained.



A0-A16	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
CEN	Complementary Chip Enable
OEN	Complementary Output Enable
WEN	Complementary Write Enable
V_{DD1}	Supply Voltage (I/O)
V_{DD2}	Supply Voltage (core)
V_{SS}	Ground

Fig. 4.1: TV2 External pins names and description

Mode	CEN	OEN	WEN	DQ0-DQ7
Stand By Mode	H	X	X	Z
Read Mode	L	L	H	Data out
Write Mode	L	H	L	Data in
Output Disable	L	H	H	Z

Tab. 4.1: TV2 Control signals truth table

Bonding scheme used for the TV2 samples, is shown in following picture.

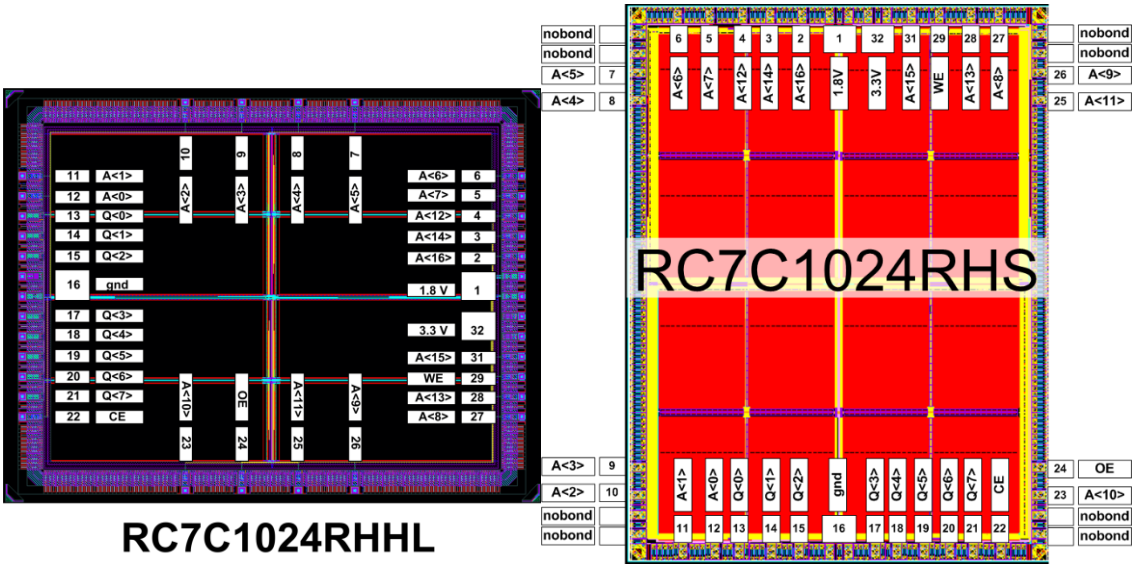


Fig. 4.2: TV2 bonding diagram and bonding pattern on CSB03202, ceramic 32DIL package

The chip core has 200mW maximum average power consumption, at maximum operating frequency of 40MHz, while the absolute maximum ratings and the recommended operating conditions are depicted in following tables.

Symbol	Parameter	Limits	Units
V_{DD1}	Supply Voltage (I/O)	-0.5 to 4.6	V
V_{DD2}	Supply Voltage (core)	-0.5 to 3.0	V
$V_{I/O}$	Voltage on any pin	-0.5 to 4.6	V
I_{IN}	Input current	±10	mA dc
I_O	Output current	20	mA dc
P_D	Device Power Dissipation	700	mW
T_{OP}	Operating Temperature Range	-55 to 125	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SOL}	Soldering Temperature	+300	°C
T_J	Junction Temperature	+175	°C
$R_{th(j-c)}$	Thermal Resistance	3	°C/W

Tab. 4.2: TV2 Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V_{DD1}	Supply Voltage (I/O)	3.3 ± 0.3	V
V_{DD2}	Supply Voltage (core)	1.8 ± 0.15	V
V_{SS}	Ground	0	V
V_{IL}	Input Low Voltage	0 ± 0.3	V
V_{IH}	Input High Voltage	V_{DD1} ± 0.3	V

Tab. 4.3: TV2 Recommended Operating Conditions

4.3. Project Outcomes

At completion of design activity, the test-vehicles (80 instances of TV1 and 80 instances of TV2) have been manufactured and packaged in accordance with the test as defined in the test-plan and the test set-ups have been manufactured, populated, and tested for verification of correct functionality and performance operation. Then the reliability and radiation tests have been performed on the selected devices according to the test plan. The reliability and radiation test data have been evaluated and analysed and consolidated into a test report. Expected and anomalous behaviour have been reported.

Finally, the results obtained have been analysed and lesson learnt for a future possible roadmap through a complete rad-hard library for this technology collected and reported.

Main LF15A feasibility study outcomes are the followings:

- TV1 test results were able to characterise primitive devices of the PDK highlighting very good performances for what regards passives, BJTs and MOS until 3.3V and up to 300 Krad. A

remodelling is needed for 5V and HV MOSFETs because VTH drift under TID irradiation without bias, and critical fails when under irradiation with bias have been experimented.

- TV2 test results and comparison with other technologies demonstrated that 1Mbit SRAM developed with LF15A PDK can represent a viable alternative to other 180nm processes. However heavy ions tests must be repeated in possible future qualification activities because some doubts on correct penetration range over 30 MeV cm2 and up to 60 MeV cm2 due to facility range or test measurements during the activity have been not solved.

Therefore, project defined a first successful step in the roadmap of having a space foundry located in Europe as alternative to Asian usual ones for what regards ASIC mixed signal business.

The initial aim of project activities in this sense was to have an Italian independent production chain. During the years, LFoundry S.r.l. remained and Italian company with autonomous R&D and production lines but from May 2022, is owned 70% by SPARC SEMICONDUCTOR HK LIMITED and 30% by WUXI XICHANWEIXIN SEMICONDUCTOR CO. LTD. At first glance this change could discourage the goal of the program.

However, Covid-19 and global geopolitical challenges, highlighted the importance of relocating and spreading worldwide as much as possible businesses too much concentrated on a single region/nation of the planet to mitigate risk of possible global unavailability of critical technologies.

In this sense, LF15A activity, opened a positive scenario not only for National but also for European and at latest world will of technological independence from Asian foundries.

In addition, the LF15A 150nm technology is still available and LFoundry is still interested in possible business opportunities on space market driven by RadHard feasibility studies developed during this LF15A ESA GSTP program.

From this point of view, it could be reasonably assessed that an important contribution has been provided by LF15A project.

For what regards the lessons learnt arisen from this activity, surely the main disadvantage of the GSTP formula and budget was the need to limit the feasibility study to an evaluation, with the impossibility to perform a real qualification program. However, data collected by LF15A project provided two main advantages. First of all, they justified the meaningfulness of possible additional activities and investments to reach qualification goal. Then produced data and indications to better drive this process if implemented.

In this context the list of main instructions produced by discussion and interaction between LF15A project consortium and ESA experts, is here below provided as input to next possible developments:

- TID approach on primitive devices: ECSS standard must be followed. For example:
  - radiation measurement must be performed first after 24h @25°, then @25° until total 168h and then annealing @100° for additional 168h.
  - TID plan more relaxed, starting from a very low dose rate for BJTs, and then going gradually to the top, must be adopted.
- TID approach on SRAM: during this evaluation activity, TV2 reached the tolerance of the technology. This must be considered for next activity.
- HI approach: ECSS standard must be followed. In particular:
  - 60um minimum HI beam range must be adopted to grant correct HI penetration in the devices.
  - the use of 5 different ions energies is recommended to give more possibilities to identify the real sensitivities of the devices.

End of Document

(Intentionally left blank)