ESA CONTRACT: 4000108445-13-NL-RA

ADC 16 BITS

ESR EXECUTIVE SUMMARY REPORT

	Name/Title	Signature	Date (yyyy/mm/dd)
Prepared by:	D. Lopez/E. Cordero		2019/10/08
Approved by:	D. López B.U. Manager		2019/10/08

ALTER TECHNOLOGY TÜV NORD S.A.U. CIF: A41990490. C/ Majada 3, 28760 - Tres Cantos (Madrid), SPAIN.
T: 34-91-804 18 93, Fax: 34-91-804 18 93, E-Mail: info@altertechnology.com

CHANGE RECORD

Issue / Revision	Change date	Affected Issue / Revision	Affected chapter or page / Change description
01	2019/07/08		Initial issue
02	2019/09/09	01	This edition includes the modifications agreed in the ESA comments in accordance with email 2019/08/13. 1.- Summary • ECI program is replaced by TRP. • "Hardering" is corrected by "Hardened" 2.- Related Task • The resolution of graph is improved. 3. Device Datasheet. • The resolution of images is improved, and the blurry text is clarified. 5.1. Electrical Performances. • The resolution and the blurry text are improved, and the datasheet is updated with Datasheet document issue 2. 5.2.1. TID • This section is modified according to comments to TID report • The typo error is corrected and a clarification about dip at 40 Mbps is included. 5.3. Life Test • This section is modified according to comments to Life test report • A clarification about dip at 40 Mbps is included. 6. Compliance Status • The operational range of temperature is increase at 125ºC in accordance with results of samples 4, 6 and 10 of the life test.
03	2019/10/08	02	This edition includes the modifications according to RID FR_18_jb & FR_32_jb 3. Datasheet • Radiation Performance are modified according to FR_13_jb and FR_32_jb. The clarification on test conditions, sensitivity at TID, SEE is included according to data sheet and test reports. 5.3 Endurance test • According to RID FR_18, The "life test" is replaced by "endurance test" and the test conditions are included.

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1 SUMMARY

An ADC 16 bits has been developed by ALTER TECHNOLOGY TÜV NORD in the frame of contract ref.: 4000108445-NL-RA I the frame of ESA TRP program.

The objective of this activity has been to design, manufacture and test a standalone high speed (20 Msps) and high resolution (16 bit) ADC being the primary use of this device shall be for CMOS image sensors and also potentially any generic analog signal data acquisition e.g. from CCD image sensors but also o-board atomic clocks are one of the key elements of GNSS systems that could be considered for use in high resolution instruments for Earth Observation or Space Science and Secure Telecom Applications. Several new types of clocks with better performances and requiring larger number of simultaneous high-resolution control channels will require mixed signals ICs and in particular high-resolution ADCs and DACs.

The 16bADC ASIC is a radiation hardened analog-to-digital converter (ADC) in a 1.8V/3.3V 0.18µm CMOS process. The base performance specification of this device is 12-ENOB for a 2Vpp differential input signal range within the input bandwidth from 1MHz to 10MHz. If needed, the analog input bandwidth is extended up to 100MHz to allow intermediate-frequency (IF) sub-sampling in communication applications.

The ADC has a SHA-less Pipeline architecture comprising seven stages with digital foreground self-calibration. Bias references are generated on-chip. A differential clock input controls all internal conversion cycles. The analogue and mixed signal section of the ASIC have been implemented exclusively with thin oxide transistors, robustly protected again latch-ups with dedicated guard rings, using a single power supply voltage of 1.8V. The digital logic section uses the 1.8V standard cells for the core and the 3.3V ones for I/O pads from the rad-hard digital library DARE (= Design Against Radiation Effects). Redundant flip-flops are used in all critical configurations and programming registers, which could be setup using a 4-wire serial interface. The ADC output bits are provided in parallel in LVDS (low-voltage differential signaling) format. To facilitate the receiving operation a data ready clock defines the proper sampling instant.

Summary of the project including main achievements are here below presented in this document.

ALTER TECHNOLOGY TÜV NORD S.A.U. CIF: A41990490. C/ Majada 3, 28760 - Tres Cantos (Madrid), SPAIN.
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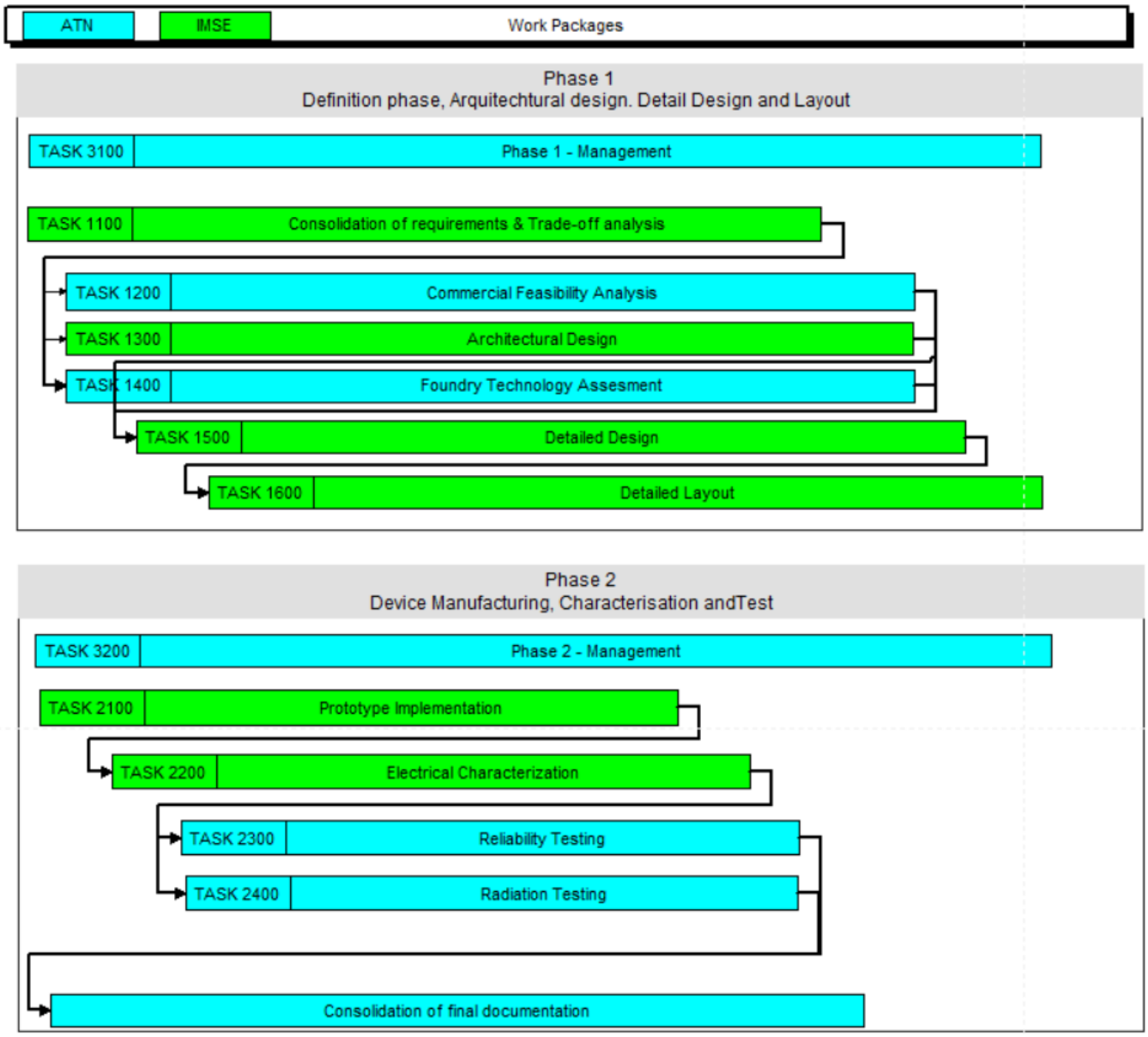
2 RELATED TASKS

Project has been developed in accordance with the following tasks flow:



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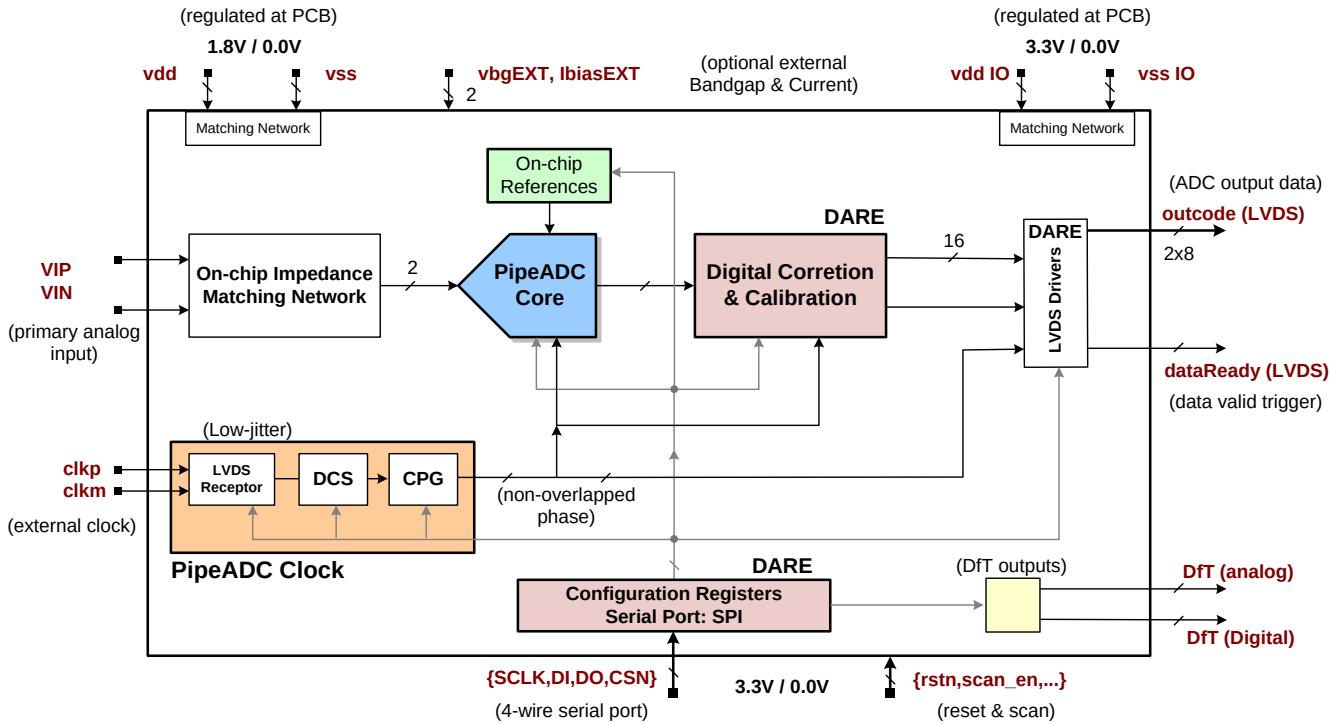
3 DEVICE DATA SHEET

Following project completion, a detailed data sheet has been prepared with full description of the part.

16bADC ASIC: A 1.8V/3.3V 16bit 83dB-SNDR 100Msps Oversampled Pipeline ADC with Digital Self-Calibration



16b ADC Block Diagram

General Description:

The 16bADC ASIC is a radiation hardening analog-to-digital converter (ADC) developed under the ESA (European Space Agency) framework in a 1.8V/3.3V 0.18µm CMOS process. The base performance specification of this device is 83dB-SNDR at 100Msps for a 2Vpp differential input signal range within the input bandwidth from 1MHz to 10MHz. If needed, the analog input bandwidth is extended up to 100MHz to allow intermediate-frequency (IF) sub-sampling in communication applications.

The ADC has a SHA-less Pipeline architecture comprising seven stages with digital foreground self-calibration. Bias references are generated on-chip. A differential clock input controls all internal conversion cycles. The analogue and mixed signal section of the ASIC have been implemented exclusively with thin-oxide transistors, robustly protected again latch-ups with dedicated guard rings, using a single power supply voltage of 1.8V. The digital logic section uses the 1.8V standard cells for the core and the 3.3V ones for I/O pads from the rad-hard digital library DARE (= Design Against Radiation Effects). Redundant flip-flops are used in all critical configurations and programming registers, which could be

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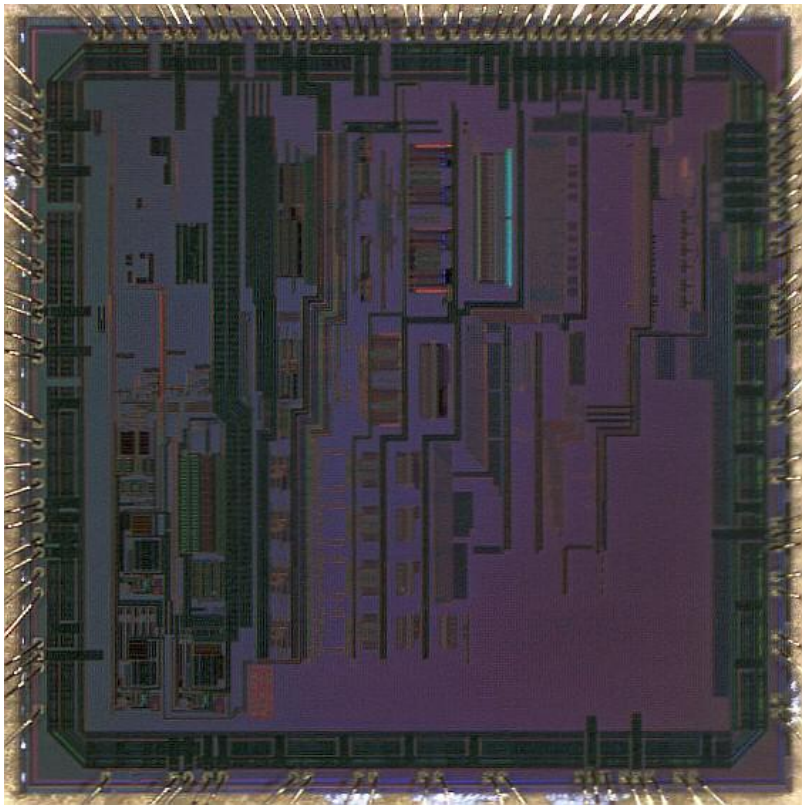
setup using a 4-wire serial interface. The ADC output bits are provided in parallel in LVDS (low-voltage differential signaling) format. To facilitate the receiving operation a data ready clock defines the proper sampling instant.

Applications:

Sampled Video signals, Band-Pass communication signals.

Chip Design:



Microphotograph of the first 16bADC prototype (Dec 2016)

Electrical Key Features:

Package: Ceramic QFN52 ([1])
Resolution: 16 bits
Control Interface: 4-wire serial port
Analog Input:
- **Range: 2.0Vpp fully differential**
- **Bandwidth**: 1MHz ≤ f_{in} ≤ 100MHz

Digital Output Code:
- **Encoding: Binary and Two's Complement**
- **Signaling: LVDS standard**
- **Bandwidth: 10 MHz (LP/BP)**
- **ENOB:** ~12.0 bits for fin ≤ 10MHz @ 27°C

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~10.0 bits for 10MHz ≤ fin ≤ 100MHz @ 27ºC

SNR: ~ 73 dB (f_{in} ≤ 10MHz @ 27°C)

SFDR: ~ 83 dBc (f_{in} ≤ 10 MHz @ 27°C)

Power supply: 1.8V for Analog and Digital Cores
3.3V for CMOS Digital I/O

Power consumption: ~ 500mW (whole ASIC)

Temperature range: -55° to +125°C Functional ([2])

Notes: ([1]) Other package solutions are also feasible, please contact us for further details. ([2]) Expected data, real values to be provided.

Radiation Performance:

TID: > 130 krad ([1])

SEL: immune > 62 MeV·cm^2/mg (tested up to 85ºC). ([1]).

SEU & SEFI: Events recorded from 10 MeV·cm^2/mg ([1]).

([1]) See radiation reports to more information.

Development Status:

The ASIC has been electrically characterized after fabrication. The core area is approximately 3.460 µm x 3.600 µm (12.43 sqmm). From this area, 10.21 sqmm corresponds to analog part and 2.2 sqmm corresponds to digital part. Radiation data available on request.

Acknowledgements

This device has been designed and manufactured as per European Space Agency Contract ref.: 4000108445/13/NL/RA

Contact:

Demetrio López Demetrio.lopez@altertechnology.com
Joaquín Ceballos joaquin@imse-cnm.csic.es
Adoración Rueda rueda@imse-cnm.csic.es

ALTER TECHNOLOGY TÜV NORD S.A.U. CIF: A41990490. C/ Majada 3, 28760 - Tres Cantos (Madrid), SPAIN.
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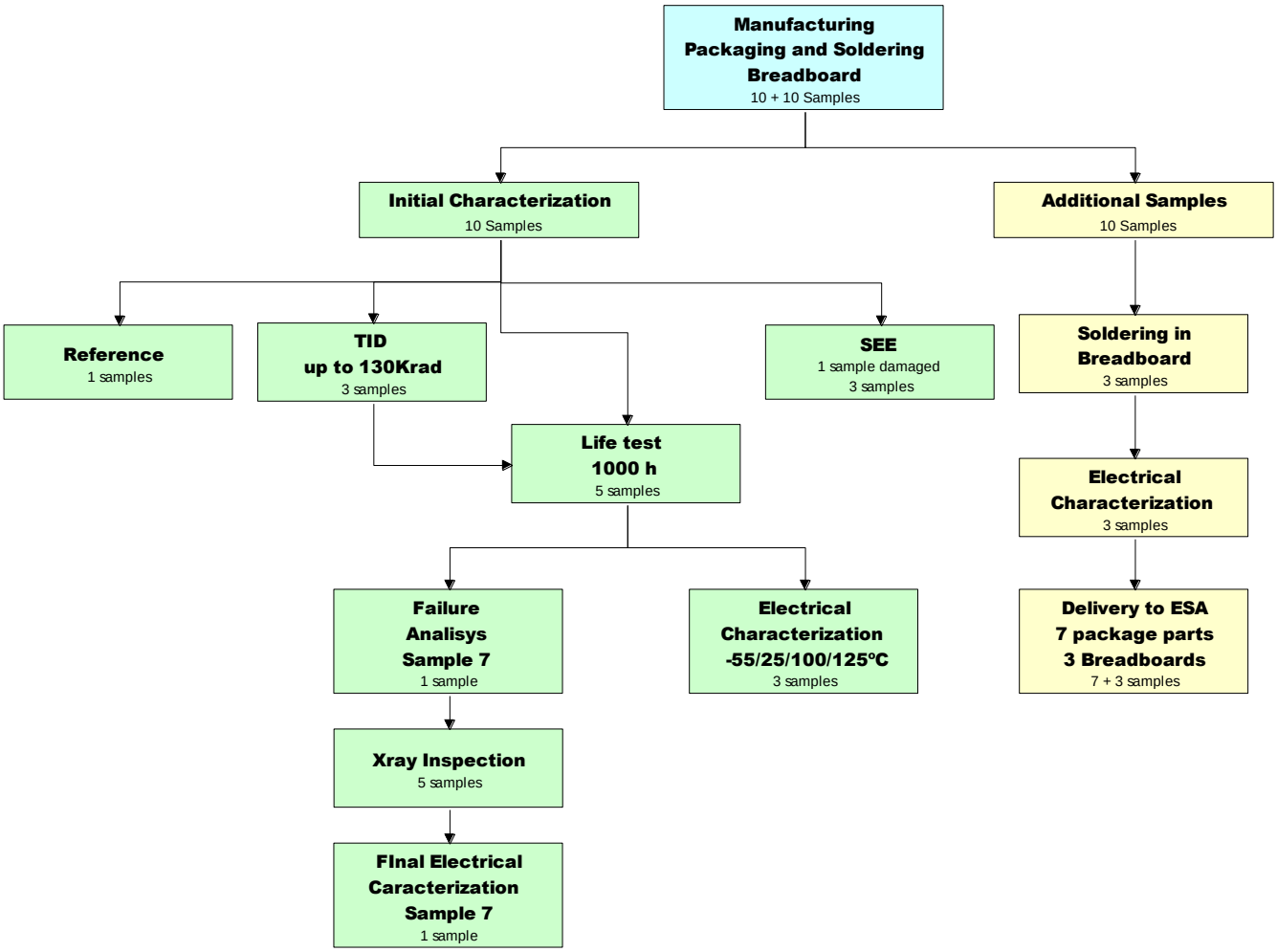
4 TEST PLAN

Full characterization, endurance, Totals dose and SEE radiation tests have been performed under ALTER TECHNOLOGY responsibility as per following chart



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5 PERFORMANCE SUMMARY

5.1 Electrical performances

Parameter	Unit	Temp = -55ºC	Temp = 25ºC	Temp = 125ºC	Conditions
Resolution	bits	16	16	16	
Power Consumption	mW	470/587	456/585	525/625	Power average Fsampling 20 Msps/80 Msps Finput = 10 MHz
Analog Input Voltage Span	Vp-p	1.99	1.97	1.94	Overload Condition

DC Accuracy

Test signal: Filtered sine wave at the available lowest frequency (2.0 MHz).
Test Input Voltage = -0.5 dBFS (~1.9 Vp-p).
Test sampling frequency: 20Msps.
Procedure: Non-overloaded Coherent Sine-Wave Histogram.
Sample Number: 3.3 M (65536 x 50).
More insight can be extracted from graphical results in next figure.

Parameter	Unit	Temp = -55ºC	Temp = 25ºC	Temp = 125ºC	Conditions
No missing codes	-	Guaranteed	Guaranteed	Guaranteed	Code@16 bits
Gain	LSB/V	0.88	0.94	0.89	Code@14 bits
DNL	LSB	[-0.32, 0.34]	[-0.34, 0.39]	[-0.32, 0.58]	Code@14 bits
INL	LSB	±1.1	±1.2	±2.0	Code@14 bits
ENOB	bits	13.2	13.2	12.6	Code@14 bits

AC Accuracy

Test signal: Filtered sine wave at five frequencies from 2.0 MHz to 25 MHz
Test Input Voltage = -1.0 dBFS (~1.8 Vp-p).
Test sampling frequency: Two cases, 20 Msps and 80 Msps.
Procedure: Coherent Sine-Wave Averaged Non-windowing FFT Spectrum.
Sample Number: 16384 x 4 x 10.
More insight can be extracted from graphical results in next figures.

Parameter	Unit	finput (MHz)	Temp = -55ºC		Temp = 25ºC		Temp = 125ºC	
			20 Msps	80 Msps	20 Msps	80 Msps	20 Msps	80 Msps
ENOB	**bits**	2	12.35	11.82	12.44	11.30	11.98	10.81
		5	12.38	11.70	12.20	11.19	11.42	10.45
		10	11.74	11.46	11.68	11.05	11.58	10.78
		25	10.64	11.17	10.64	10.68	10.48	9.85
SNR	**dB**	2	77.2	75.2	76.7	74.3	75,2	68,8
		5	75.5	75.5	75.0	74.0	74.0	67.5
		10	71.8	74.5	71.0	73.4	71.8	67,3
		25	65.1	71.9	65.1	70.9	64.9	62.9
THD	**dB**	2	79.0	74.6	81.6	70.1	77,0	68,7
Harmonics with amplitude greater than -100 dBFS. Assuming the first 65 harmonics in 20 Msps case, and the first 151 harmonics in 80 Msps case.		5	85.3	73.1	80.9	69.3	71.5	66.1
		10	80.6	71.5	79.4	68.4	73.3	71,2
		25	74.5	70.1	75.4	66.3	74.0	63.8
SFDR	**dBFS**	2	80.2	80.1	82.7	71.8	78,0	70,3
		5	90.1	75.9	85.1	72.8	71,5	67.9
		10	82.5	72.4	80.5	70.9	80.0	76.0
		25	75.7	77.9	77.1	73.9	75.0	66.4

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5.2 Radiation tests

5.2.1 *TID test*

The samples of repeater have withstood correctly the applied total dose up to 130 Krad with a small degradation of the ENOB parameter. All samples are tested according to the sequence described by radiation test plan. After each test relevant degradation, or main failure, has not been detected in ENOB parameter.

The ENOB shows a degradation at low bit rates (10-30 Mbps) in two samples (sample 7 & 10). The maximum degradation observe is 1.1 bits in this parameter. At higher bit rates (50-110 Mbps) the observed degradation is less than 0.5bits in ENOB.

Additionally, all ENOB characteristics measured during this TID test have shown a dip at 40Msps. This dip has been analyzed and this effect likely is caused by a measurement/calibration issue and is not related to the component itself

5.2.2 *SEE test*

The main obtained results during SEE test on ADC16 are:

- The ADC have not shown SEL events during the test. Three tested samples withstand up to 62.4 MeV cm2/s (Xe ion) at 25ºC and 85 ºC without any SEL event, therefore the devices are latch-up free.

- The ADC show sensibility at low LETs. The number the SEU/SEFI events are increased with the LET and temperature, but the devices show also sensibility from the smaller level applied according to test plan (10 MeV cm2/s Ar ion).

Annex 01 of the SEE report provides specific analysis of results according to DARE technology performance.

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T: 34-91-804 18 93, Fax: 34-91-804 18 93, E-Mail: info@altertechnology.com

The following table shows the results of the SEE test.

Sample	Ion	LET [MeV/(mg/cm^2)]	Flux [ion/s·cm^2]	Fluence [ion/cm^2]	Temp	SEU	SEFI	SEL
s9	Ar	10	1E+03	1E+06	25±3	10	0	0
s9	Cr	16	1E+03	1E+06	25±3	16	8	0
s9	Kr	32.4	1E+03	1E+06	25±3	52	8	0
s9	Xe	62.5	1E+03	1E+06	25±3	59	13	0
s9	Xe	62.5	1E+04	1E+07	85+5/-0	360	93	0
s3	Cr	16	1E+03	1E+06	25±3	15	4	0
s3	Kr	32.4	1E+03	1E+06	25±3	40	5	0
s3	Xe	62.5	1E+03	1E+06	25±3	83	13	0
s3	Xe	62.5	1E+04	1E+07	85+5/-0	365	124	0
s5	Ar	10	1E+03	1E+06	25±3	10	11	0
s5	Kr	32.4	1E+03	1E+06	25±3	40	23	0
s5	Xe	62.5	1E+03	1E+06	25±3	57	33	0
s5	Xe	62.5	1E+04	1E+07	85+5/-0	354	103	0

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5.3 Endurance tests

The results are summarized below, according to the of different types of samples:

1. New Samples (1 & 6):
   - After 1000h the new samples (sample 1 & 6) have withstood correctly the endurance test (1000h at 85ºC) without main degradation. The maximum degradation observe is 0.6 bits in this parameter. At higher bit rates (70-110 Mbps) the observed degradation is less than 0.2bits in ENOB.

2. Additional Endurance test on TID samples (4, 7 & 10):
   - Firstly, the TID test was performed and after these samples were aging in the endurance test.
   - After 1000h of endurance test the samples 4 and 10 have withstood correctly the endurance test (1000h at 85ºC) without main degradation. Their ENOB does not show degradation in all frequency range (10-110 Mbps).
   - The sample 7 failed after 1000h with a functional failure mode, but this sample was re-characterized during the failure analysis and it worked correctly (see 4.6 clause).

Additionally, a characterization was performed after this endurance test on the three available samples at four temperatures: -55/25/100/125ºC. This characterization included an ADC power consumption has been recorded.

SAMPLES	Temp: 25ºC	Temp: -55ºC	Temp: 100ºC	Temp: 125ºC
SAMPLE 4	OK	OK	OK	OK
SAMPLE 6	OK	OK	OK	OK
SAMPLE 10	OK	OK	OK	OK

Additionally, all ENOB characteristics measured during this endurance test have shown a drop at 40Mbps. This dip has been analyzed and this effect likely is caused by a measurement/calibration issue and is not related to the component itself

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6 Compliance Status

The following table provides current compliance status of the devices versus initial requirements as per applicable SOW

Parameter	Unit	Specified Value	Measured Value			Comments
		WP 1600 16bADC	Electrical Charact.	After TID	After Endurance Test	
Number of digitized bits	bits	17	**16**	**16**	**16**	Externally available bits
Range of allowable sampling rates	Msps	100 (÷1,2,4,8,16)	**from 1 to 110**	**from 1 to 110**	**from 1 to 110**	
Analog input voltage FullScale-Range (differential)	Vpp	2.0	**2.0**	**2.0**	**2.0**	0.5Vpk single-ended signals on a ~1V common mode.
Power supply	V	1.8-1.9 3.3±5%	**1.8-1.9** **3.3±5%**	**1.8-1.9** **3.3±5%**	**1.8-1.9** **3.3±5%**	Analogue and Digital Cores CMOS Digital I/O
Power consumption (Typical conditions)	mW	< 400	**~380mW @ 20Mhz** **~450mW @ 80Mhz**	**<385mW @ 20Mhz** **<455mW @ 80Mhz**	**<385mW @ 20Mhz** **<455mW @ 80Mhz**	Only ASIC Core is considered
DNL	LSB @16bits	n.a.	**[-0.6, +1]**	**[-0.6, +1]**	**[-0.6, +1]**	[-55ºC,125 ºC] , f_{in}≤2MHz
	LSB @14bits	n.a.	**±0.4**	**±0.4**	**±0.4**	[-55ºC,125 ºC] , f_{in}≤2MHz
|INL|	LSB @16bits	n.a.	**≤5**	**≤5**	**≤5**	[-55ºC,125 ºC] , f_{in}≤2MHz
	LSB @14bits	n.a.	**≤2**	**≤2**	**≤2**	[-55ºC,125 ºC] , f_{in}≤2MHz
THD	dB	n.a.	**~ -80**	**~ -80**	**~ -80**	f_{in}≤10MHz
SFDR	dBc	n.a.	**~ 83**	**~ 83**	**~ 83**	f_{in}≤10MHz
NPR	dB	n.a.	**Not measured**	**Not measured**	**Not measured**	
SNR	dB	n.a.	**~ 73**	n.a *	n.a *	f_{in}≤10MHz
ENOB	bits	n.a.	**~ 12** **~ 10.5**	**~ 12** **~ 10**	**~ 12** **~ 10.5**	f_{in}≤10MHz 10MHz<f_{in}≤100MHz
Operational temperature range	ºC	-55 to +125	**-55 to +125**	n.a *	n.a *	

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