Autocatalytic Silver for Space applications

Executive Summary Report

June 2019

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ESA Contract No. 4000122510/17/NL/LvH/gp “Autocatalytic Silver for Space Applications”, June 2019, version 1

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Abstract

This report is related to ESA Contract No. 4000122510/17/NL/LvH/gp “Autocatalytic Silver for Space Applications”.

Autocatalytic silver is an alternative to electroplating and immersion processes and it has the potential to improve both performance and reduce plating costs. The autocatalytic nature of the process means that plating is continued as long as the substrate is immersed in the plating bath, without applying a current to the substrate.

For space use, two important applications are, microwave components, (MWC), and surface finish for soldering of printed circuit boards (PCBs).

In this work, the ASIG process, (Autocatalytic Silver Immersion Gold, a final finish for PCB and the ESM 200 process, an autocatalytic silver process for microwave components, were evaluated with the aim to fulfil space demands.

The ASIG finish provided surfaces with good solderability even after having been exposed to two soldering processes. Solder joints formed to various types of components had good reliability.

The ESM 200 plated samples, with an undercoat of electroless nickel, were found to withstand a simulated space environment.

RF-measurements of a silver plated, WR 75, waveguide filter shows a performance as expected for similar electroplated filter.

1. Introduction

Autocatalytic silver is an alternative to electroplating and immersion processes and it has the potential to improve both performance and reduce plating costs. The autocatalytic nature of the process means that plating is continued as long as the substrate is immersed in the plating bath, without applying a current to the substrate.

For space use, two important applications are microwave components (MWC) and surface finish for PCBs.

The work has been carried out to demonstrate the technology´s feasibility, manufacturability, reliability and performance, with the aim to fulfil space demands for these applications.

ASIG (Autocatalytic Silver Immersion Gold) was developed primarily as an alternative surface finish for chip packaging substrates. For PCBs, ASIG has been developed as a replacement for nickel based surface finishes which are known to suffer from quality issues, such as brittle intermetallics or black pad failures. The ASIG process is today in commercial use by the South African company Trax Interconnect Ltd.

In this work, printed circuit boards were plated with ASIG, assembled and soldered. The boards were evaluated for quality of ASIG plating, quality for assembled boards, resistance against electrochemical migration and integrity of solder joints.

For microwave components application, the autocatalytic silver process ESM 200 was used.

The ESM 200 autocatalytic silver process, is a multi-purpose silver plating solution, designed to give a conformal coating of silver, with excellent electrical conductivity. The ESM 200 is especially suited for RF and microwave components with complex geometrical shapes such as filters, waveguides, connectors or solar cells with narrow conductive lines, to be silver plated. The silver deposits are pure and dense. ESM 200 can be applied onto different surfaces such as gold, copper, copper alloys and nickel. The ESM 200 process is a further development of the autocatalytic process, presented in [4] and [5].

Modified formulation has resulted in improved coverage, layer smoothness and deposition speed. The modified formulation gives also increased bath stability and allows a wider process window, i.e. plating at higher pH.

The ESM 200 autocatalytic silver plating process is an alternative to electroplating processes and it has the potential to improve both performance and reduce plating costs. The autocatalytic nature of the process means that plating is continued as long as the substrate is immersed in the plating bath, without applying a current to the substrate.

Being an autocatalytic silver plating process, the ESM 200 process differs from conventional chemical silver processes of immersion type. The key difference is that the autocatalytic process can plate to any desired thickness, while immersion processes plates to a few tenths of a micron.

In order to get the smallest losses and best RF transmission possible, it is a common practice to plate aluminium wave guides with silver. This is currently carried out by using electroplating and thus there is a need to put auxiliary anodes into the waveguides. With higher frequencies, the dimensions decrease and this makes it finally impossible to use auxiliary anodes inside the waveguide. The same goes for bended and twisted waveguides.

In this work, the ESM 200 process was evaluated, in order to offer a solution to plate complex geometries for microwave components and to achieve good appearance, coverage and adhesion, also for thicker layers, i.e. > 5 µm of silver, and thus meet both RF- and space environment requirements.

2. Experimental

2.1 ASIG Application

Lay-out of PCB

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Eighteen 2 mm thick, 4-layers PCBs with FR4 laminate and copper circuit were manufactured by Teltex AB. The lay-outs of the top and bottom sides of the test board are shown in Figure 1. It is a test board designed for evaluation of the surface insulation resistance (SIR). It has test patterns for measuring SIR between solder joints to various types of components and for comb patterns, both on free surfaces and beneath the PLCC, QFP and SOIC components. Layer two and three are ground (copper) layers. No solder mask was applied to the PCBs.

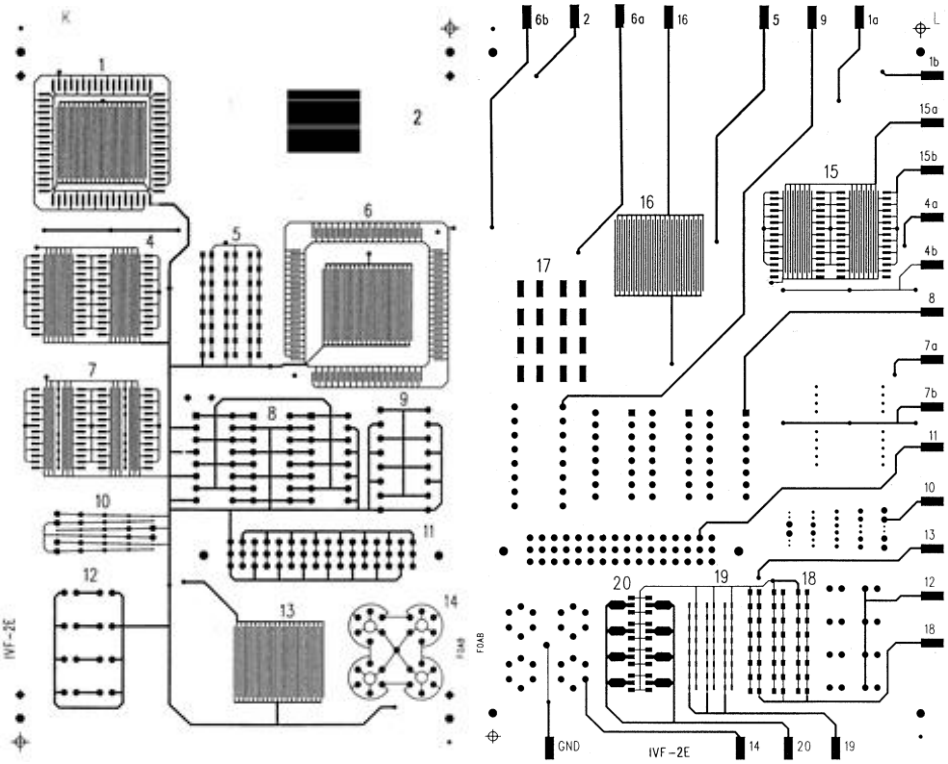

Figure 1 Lay-outs of the top and bottom sides of the SIR test board designed for mixed technology.

Application of ASIG

The PCBs were plated with ASIG at RISE IVF.

The following process was used for application of the ASIG coating:

1. Cleaner 5 min, 40°C, (Ronaclean PC 960)
2. Cold water rinse 2 min
3. Cold water rinse 2 min
4. Microetch 1 min, 27°C, (Circuposit Etch 3330)
5. Cold water rinse 1 min
6. Cold water rinse 1 min

7. Autocatalytic silver 8 min, 63°C, (ESM 100)
8. Cold water rinse 1 min
9. Cold water rinse 1 min
10. Immersion gold 5 min, 85°C, (Aurolectroless SMT)
11. Cold water rinse 1 min
12. Cold water rinse 1 min
13. Dry hot air

Quality controls of the ASIG finish

Visual inspection

The PCBs plated with ASIG were examined using optical microscopy with up to 40 times magnification.

Adhesion test

The adhesion of the ASIG finish was tested using a tape test per ECSS-Q-ST-70-10C, § 6.5.8 [1]. The tape test was performed on test pattern 2 on one ASIG plated PCB. The tape used was Scotch 508 with a width of 19 mm.

Thickness measurement

The samples were prepared using broad ion beam milling using a Gatan Ilion+ equipment, Model 693. This preparation method facilitates measurement of the thickness of very thin coatings (less than 50 nm) when analysed using scanning electron microscopy (SEM). The advantage of using ion beam milling for preparing the samples is that no smearing will occur of soft metallic layers facilitating correct determination of their thicknesses.

Assembly and soldering of PCBs

Twelve test boards were assembled and soldered at RUAG Space AB using their ordinary processes for SnPb soldering including cleaning. The test matrix for soldering of the boards and testing of the boards are given in *Table 1*. Half of the boards to be soldered passed two times through a reflow oven with no mounted components prior to soldering of components on the test boards. This was done in order to evaluate the impact of multiple soldering processes on the solderability. The remaining test boards to be soldered were soldered directly with no prior simulated soldering processes. In addition, three non-soldered test boards were used as reference boards.

Table 1 Test matrix for soldering and testing of the test boards.

PCB ID	2 x Reflow	SMT Assembly	PTH Assembly	Shear test	Pull test	Visual, X-ray	SIR test
38	-	X	-	X	X	-	-
39	-	X	-	X	X	-	-
40	-	X	-	-	-	-	-
41	-	X	X	-	-	-	X
42	-	X	X	-	-	-	X
43	-	X	X	-	-	-	X
44	X	X	-	X	X	-	-
45	X	X	-	X	X	-	-
46	X	X	-	-	-	-	-
47	X	X	X	-	-	X	X
48	X	X	X	-	-	X	X
49	X	X	X	-	-	X	X
51	-	-	-	-	-	X	X
52	-	-	-	-	-	X	X
53	-	-	-	-	-	X	X

One PLCC68 (pos. 1), two SO28 (pos. 4), twenty-four 0805 ceramic capacitors (pos. 5 and one QFP144 (pos. 6) were soldered to each of the twelve boards. In addition, three DIL16 (pos. 8) were soldered to three of the boards that were soldered directly and to three of the boards that first passed two simulated soldering processes. The surface mount components were reflow soldered and the DIL16 components were hand soldered.

For reflow soldering, solder paste NC-SMQ92J from Indium was used. Its composition is Sn63Pb37 and it has a ROL0 flux. After reflow soldering, the boards were cleaned using Vigon A201 as cleaning agent.

The DIL16 components were mounted on the boards using Dissopad as spacer. The components were then soldered using a Sn63Pb37 core solder wire with a ROL0 flux. Small amounts of an additional flux, Kester 186, was added during the hand soldering. This is a flux of the old RMA type.

After the hand soldering, the boards were cleaned with isopropanol using a brush. No rework was performed on any of the solder joints and no conformal coating was applied.

Quality controls of assembled PCBs

The quality controls performed were:

- Visual inspection
- X-ray inspection
- Cross-sections of solder joints

- Shear test of ceramic capacitors
- Pull test of leads to the QFP 144

Resistance against electrochemical migration

Performance of the test

The susceptibility to electrochemical migration (ECM) was evaluated by a prolonged surface insulation resistance (SIR) test with bias applied during the whole test, as recommended in IPC-TR-476A, “Electrochemical Migration: Electrically Induced Failures in Printed Wiring Assemblies”. The SIR measurements were basically performed per IPC-TM-650, Method 2.6.3.3, which is recommended for non-condensing environments in J-STD-001D. The temperature and humidity during the test were 85 °C and 85 % RH, respectively. A bias voltage of 5 V DC was applied during a test period of 500 hours.

The SIR was automatically measured every twenty minutes during the test using a test voltage of 5 V DC with the same polarity as the bias voltage. It was measured for the free comb pattern on Pos. 13, the comb pattern beneath the QFP144, between the solder lands to the QFP144, PLCC68, SO28 and DIL16 components, and between the solder lands to the 0805 ceramic capacitors. In addition, the test boards were visually inspected after the SIR test for any signs of corrosion or formation of electrochemical migration.

2.2 MWC Application

In order to optimize the overall process, plating trials were, at first, performed on a set of technology demonstrator samples. The objective was to achieve a robust silver plating process, with a capability to produce smooth, thick, (>5 µm) and even layers.

The test vehicles used for the technology demonstrator samples, were flat samples of aluminium 6063 T6 with a thickness of 1 mm.

10 samples, 25 x 100 mm, were plated with the optimized process for 6 µm electroless nickel + >5 µm autocatalytic silver and evaluated according to a designed test plan.

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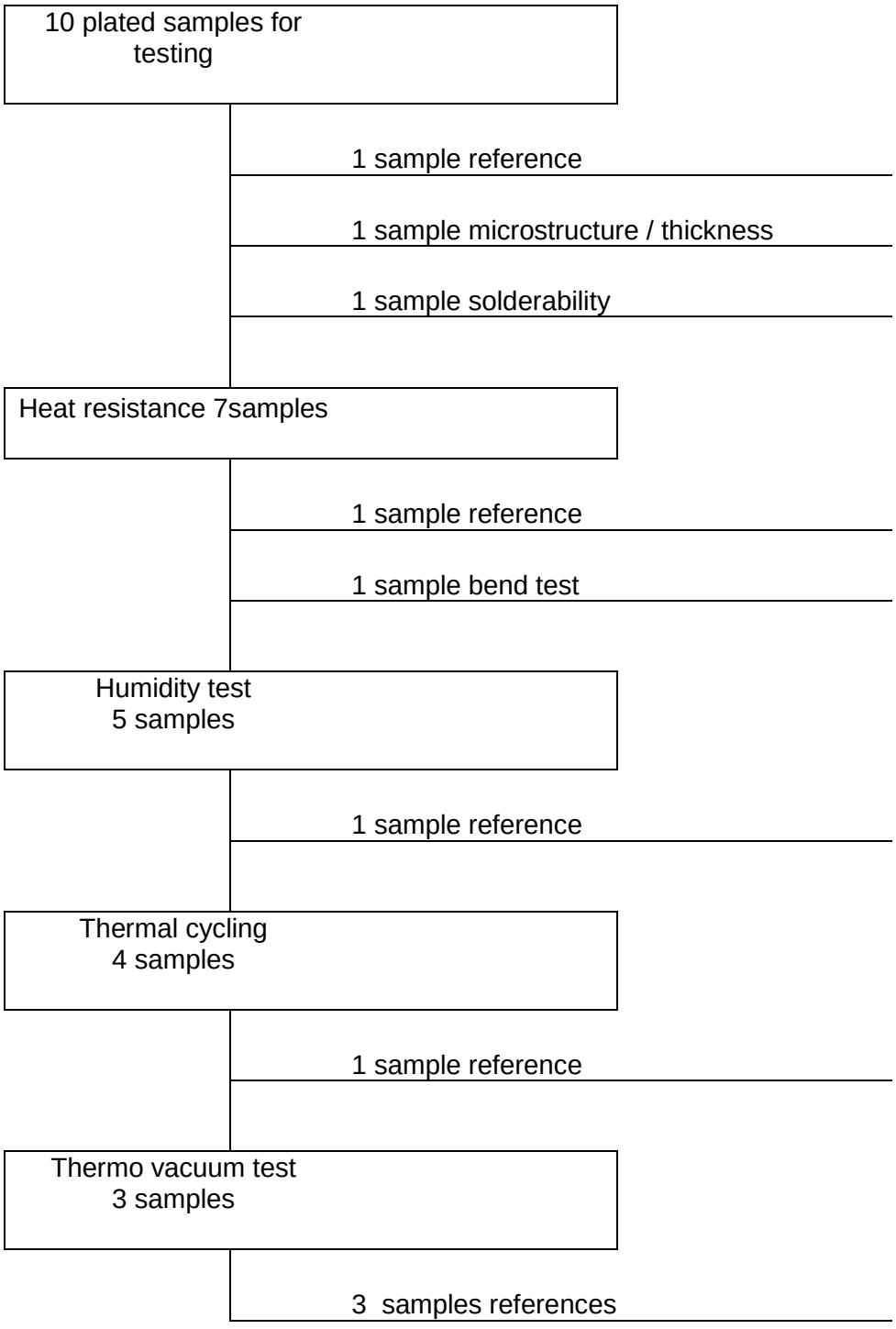


The requirements were as follows:

Thickness measurement:

Thickness of plated layers was measured by X-ray and/or by optical microscopy and/or SEM on cross section specimens.

Samples passed the test if nickel > 6µm and silver > 5 µm.

Microstructure:

Microstructure was examined by low vacuum SEM model JEOL JSM-6610LV and/or field emission SEM model JEDLJSM-7800F.

Samples passed the test if the surface shows complete coverage with silver and a homogeneous appearance of the surface roughness.

Solderability test:

Terminal solderability was evaluated through a solderability test by dipping a sample in a solder bath at 245 C for 5-10 s, according to ASTM B678-86(2011).

Samples passed there test if visual inspection shows a bright, smooth and uniform surface and if the surface is adherent when scraping with a sharp blade.

Heat resistance test:

Performance of the coating after 2 h in an oven at 190 °C.

Samples passed the test if visual inspection shows no weak non-adhering coating develop spots or blisters.

Bend test:

The ductility of the plated layers and adhesion between layers, after heat resistance, was tested according to ASTM E290-09. A sample was bent over an 8 mm mandrel.

Samples passed the test if visual inspection shows no signs for cracking of metal or peeling of the coating.

Humidity test:

Samples were placed in a controlled temperature and humidity chamber at a temperature of 50 °C and relative humidity of 95% for 48 h.

Samples passed the test if visual inspection shows no signs of patches or discoloration of the surface.

Thermal cycling test:

The capability of the coating to withstand the cyclic temperature variations occurring in space was tested by thermal cycling. 1000 cycles were performed between -65 °C +- 3 °C to +170 °C +-3 °C, with less than 1 min transfer time and 5 min dwell time in each zone after stabilization.

Samples passed the test if visual inspection shows no deterioration of the surface.

Thermo vacuum test:

The capability to withstand space environment was tested by the thermal vacuum test. Samples were sent to ESA for this test.

Samples passed the test if visual inspection shows no deterioration of the surface.

After the evaluation of the technology demonstrator samples had been performed, a set of test coupons were manufactured and evaluated. The test coupons were square tubes of aluminium AW-6060, with size 20 x 10 mm and a length of 100 mm.

Eight test coupons were silver plated and evaluated according to the test plan below.

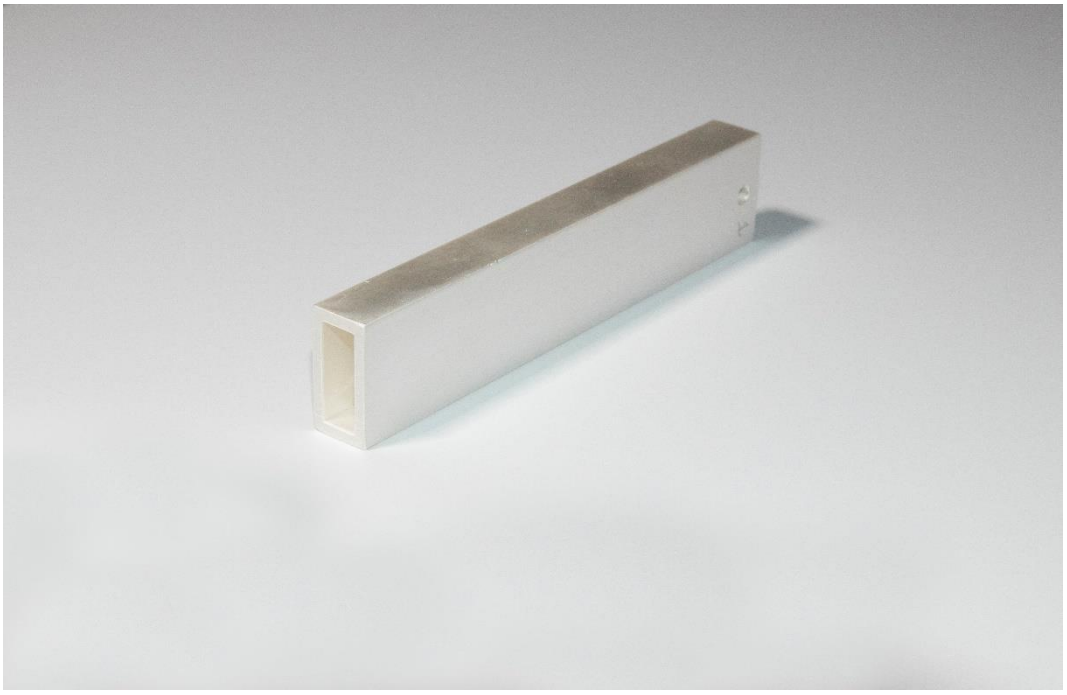
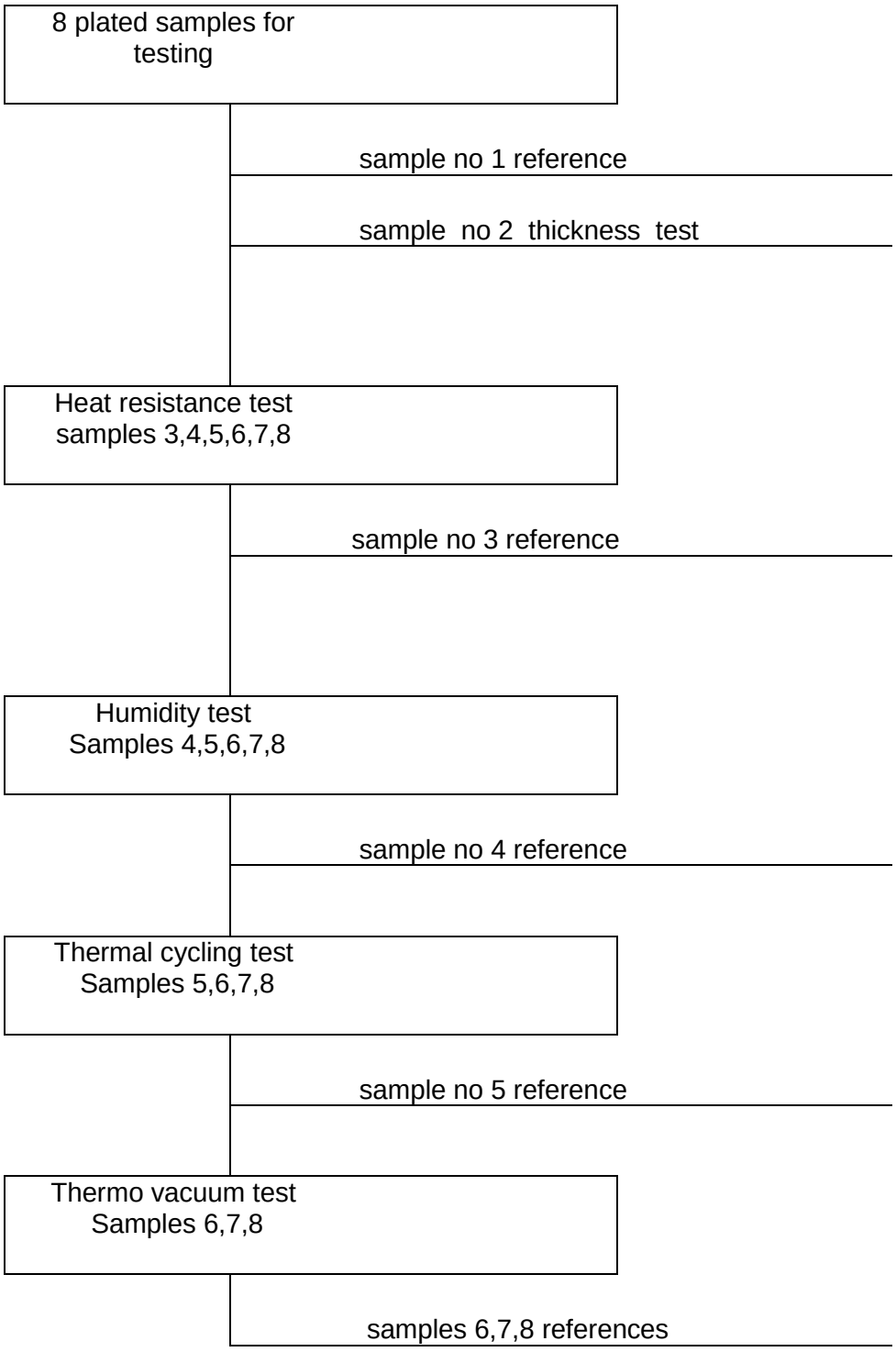


Figure 2 Silver plated test coupon.


8 plated samples for testing
sample no 1 reference
sample no 2 thickness test
Heat resistance test samples 3,4,5,6,7,8
sample no 3 reference
Humidity test Samples 4,5,6,7,8
sample no 4 reference
Thermal cycling test Samples 5,6,7,8
sample no 5 reference
Thermo vacuum test Samples 6,7,8
samples 6,7,8 references

After the evaluation of the test coupons was performed, two halves of an aluminium, WR 75, waveguide filter, recieved from ESA, were plated, assembled and evaluated for RF-performance.

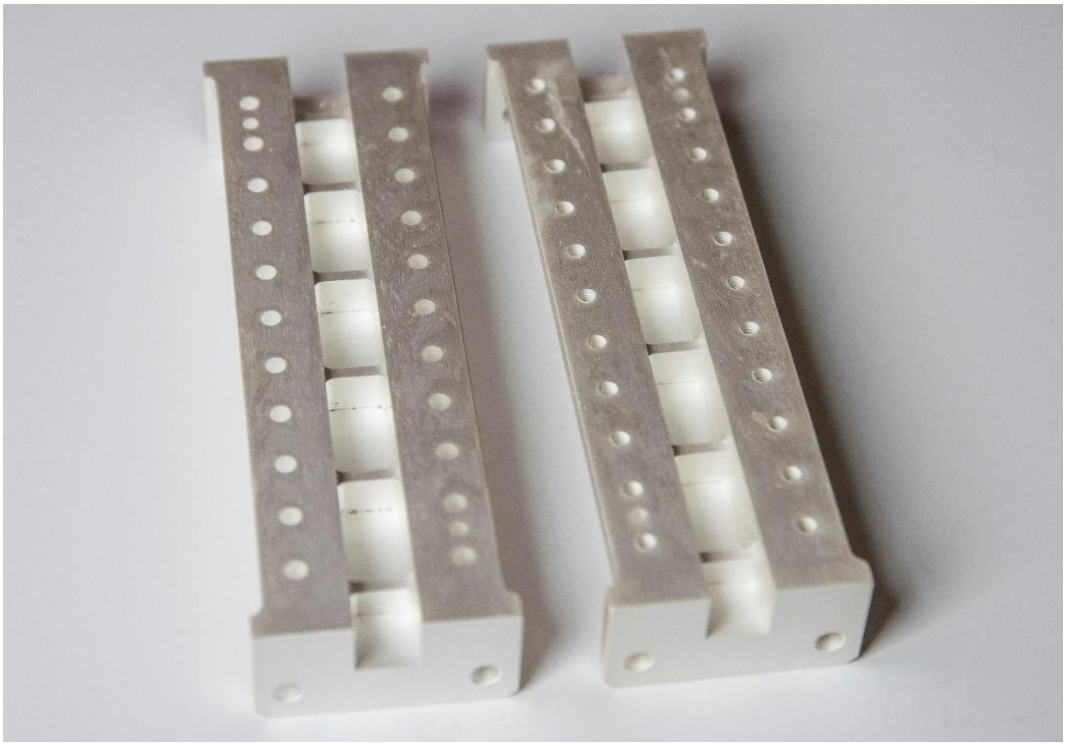


Figure 3 Silver plated, WR 75, waveguide filter.

3. Results and Discussion

3.1 ASIG Application

Visual inspection of ASIG plated PCBs

No anomalies were observed on the plated surfaces. They had a smooth and even surface with a light gold colour.

Adhesion of the ASIG finish

The ASIG plated test pattern passed the tape test as no coating adhered to the tape and the test surface showed no scaling.

Thickness of the ASIG finish

The thicknesses of the silver and gold layers in the ASIG plating were determined for one 5.0 mm wide and one 0.40 mm wide “conductor” in test pattern 2 and for PTHs with 1.00, 0.50 and 0.35 mm diameters, respectively.

ASIG thickness on conductors

Cross-sections of the ASIG plating on the conductors showed typically 150 to 300 nm with somewhat thinner thickness at the edges of the conductors and, perhaps, also somewhat thinner thickness on the wider conductor. Etching of the copper under the silver layer could be observed frequently. This created microvoids that in most cases were smaller than one micrometre. The formation of this type of microvoids is typical for an immersion plating process.

Since the gold layer is very thin, it is difficult to determine its thickness with high accuracy, but it is in the range of 10-20 nm.

ASIG thickness in printed through holes

Cross-sections of the PTHs, showed that the Ag plating was slightly thicker than on the conductors, typically 200 to 400 nm. Otherwise, the results were very similar to the plating on the conductors. The thickness of the ASIG coating was about the same in the PTHs as on the annular ring.

Visual inspection of assembled PCBs

All soldered boards were visually inspected after soldering. Only one defective solder joint was observed. This was a solder joint to a 0805 ceramic capacitor which had a defective plating at one of the terminations. All other solder joints had acceptable appearance. No difference in appearance of the solder joints could be observed between the boards that were soldered directly and the boards that were soldered after two simulated soldering processes.

X-ray inspection of assembled PCBs

The solder joints to the various types of components were examined using X-ray inspection on board 41 (soldered directly) and on board 47 (soldered after two simulated soldering processes). The results were almost identical for both boards.

In most solder joints, a large number of small voids can be observed. They are most abundant in the solder joints to the SO28 and QFP144 components.

Cross-sections of solder joints

Cross-sections were performed of solder joints to the QFP144 component and one DIL16 component on board 47. Voids of various sizes can be observed in all solder joints. They are a little more abundant at the surface of the solder lands on the PCB.

Shear test of ceramic capacitors

RUAG performed shear testing of ten 0805 ceramic capacitors on each of test boards 38, 39, 44 and 45. The testing was done using DAGE 4000 DS100. The results from the shear testing are presented in Table 2. The shear force was high for all tested components and was about the same for the boards that were

soldered directly as for the boards that were soldered after two simulated soldering processes.

Table 2 Results from shear testing of 0805 ceramic resistors.

PCB nr / Pos	38	39	44	45
1	6,29 kg	5,04 kg	7,95 kg	6,82 kg
2	6,90 kg	6,35 kg	7,38 kg	5,33 kg
3	6,10 kg	4,81 kg	7,10 kg	5,91 kg
4	6,35 kg	5,21 kg	5,81 kg	7,46 kg
5	6,24 kg	6,33 kg	6,17 kg	5,96 kg
6	5,20 kg	7,60 kg	7,26 kg	4,67 kg
7	6,94 kg	6,50 kg	5,12 kg	6,17 kg
8	5,11 kg	5,94 kg	6,10 kg	6,51 kg
9	5,28 kg	7,30 kg	6,40 kg	5,13 kg
10	6,13 kg	7,63 kg	6,74 kg	7,61 kg

Pull test of leads to the QFP144

RUAG performed pull testing of 10 leads to the QFP144 on each of test boards 38, 39, 44 and 45. The testing was done using DAGE 4000 WP1GK. The results from the pull testing are presented in **Error! Reference source not found.**. All fractures occurred between the solder pads and the PCB laminate, i.e. the results were the same for the boards that were soldered directly as for the boards that were soldered after two simulated soldering processes.

Table 3 Results from pull testing of leads to QFP144 (measured values in grams).

PCB nr / Pos	38	39	44	45
1	854,8	1 014,2 *	1 012,7 *	1 014,8 *
2	981,3	1 014,1 *	1 013,2 *	1 010,4 *
3	815,7	1 011,2 *	891,5	1 014,5 *
4	931,7	994,8	839,2	1 014,6 *
5	970,6	877,2	811,0	1 014,6 *
6	719,6	978,6	841,8	1 012,2 *
7	718,5	1 011,4 *	1 013,4 *	1 011,5 *
8	634,6	972,7	991,9	1 012,8 *
9	1 011,9 *	1 015,5 *	909,8	1 010,6 *
10	896,0	701,3	1 012,8 *	1 014,8 *
11	1 010,5 *	1 015,3 *	948,9	1 012,2 *
12	803,9	1 014,7 *	501,1	1 007,8 *
13	1 010,7 *	1 002,9 *	1 011,4 *	975,4
14	1 010,8 *	962,8	1 013,8 *	963,8
15	1 012,5 *	1 014,1 *	1 011,3 *	1 014,5 *
16	982,4	1 012,8 *	1 012,8 *	942,2

* Value surpassed the maximum pull force from the equipment. No fracture occurred.

Visual inspection after SIR testing

All test boards were visually inspected after the SIR test using an optical microscope with up to 40 times magnification.

Non-soldered reference boards

Many of the ASIG coated surfaces had a dark appearance on all reference boards, both biased and non-biased surfaces. For biased patterns, surfaces with negative potential were slightly more affected than surfaces with positive potential.

Between the conductors in the comb patterns (patterns 6a and 13) and between the solder lands for the QFP144 components, corrosion products and dendrites were observed between the conductors to varying extent.

Soldered boards

With some exceptions, the non-soldered, ASIG plated surfaces did not show any discolouration when the test boards were visually inspected after the SIR test.

Results from surface insulation resistance measurements

In IPC's standard IPC-9202 [2], it is required that all SIR test patterns shall show a minimum resistance of 100 Mohms when tested at 40°C and 90% RH. In addition, any patterns that exhibit dendrites that extend more than 20% of the conductor spacing shall be considered failures. The test temperature used in this investigation was 45°C higher, which can be expected to cause SIR values that are one to two decades lower compared to testing at 40°C. However, this will not be considered when discussing the results from the electrochemical migration test.

With only one exception, the only test patterns that did not pass the requirements in IPC-9202 were the comb patterns and the solder lands to the QFP144 on the non-soldered reference boards. They failed both the SIR requirement and dendrite requirement. Furthermore, discolouration of ASIG plated surfaces was observed.

The exception was the pattern with the DIL16 component for which a particle was located behind one of the leads. This particle was most likely the cause of the low SIR value. That is, the failure was not related to the ASIG finish. The discolouration around this component and the black corrosion products to some solder joints to an adjacent QFP144 were likely also caused by this trapped particle. The other test patterns on the assembled boards passed the requirements in IPC-9202 with good margin and much less discolouration.

A possible explanation for the better performance of the soldered boards may be that the non-soldered boards had process residues from the plating processes remaining on the boards, possibly trapped in the microvoids formed beneath the silver layer due to under-etching. Since the assembled boards went through cleaning processes after soldering, this may have removed the plating residues.

Integrity of solder joints

The solder joints formed to the various types of components were acceptable on all boards. No difference could be observed between the solder joints that were formed on the boards that were soldered directly and those that were formed on the boards that had passed through two simulated soldering processes prior to the soldering. That is, eventual residues trapped in the microvoids did not degrade the solderability when going through soldering processes.

Voids in solder joints are normal and does not usually affect the reliability of the solder joint. However, if numerous small voids are present at the interface

between the solder and the solder pad, they may degrade the reliability. Numerous small microvoids at this interface, often called “champagne voids”, have been reported for many types of surfaces finishes but seems to predominantly form with immersion silver finishes [3]. Likely, they are, at least to some extent, caused by voids formed under the silver finish due to under-etching during the plating process.

In this investigation most voids were observed in the solder joints to the SO and QFP components. The pull test of the leads to an QFP component indicate that the level of voids in the solder joints did not degrade the strength of the solder joints.

3.2 MWC Application

An initial set of technology demonstrator samples were plated with approx. 10 µm Ni + approx.9 µm Ag.

Although the manufactured and plated technology demonstrator samples, were found to be without defects and covered with an even and smooth silver layer, they surprisingly did not pass the heat resistance test. The problem was the adhesion between nickel and aluminium.

As the nickel layer acts as a corrosion barrier between silver and aluminium, it´s very important that the layer is dense enough. It is also well known that a heat treatment of electroless nickel plated aluminium, can improve adhesion.

The problem was solved by plating a new set of samples, with 18 µm nickel and by introducing an intermediate heat baking, (h at 190 °C) after a short time, (15 min.), in the silver bath. After the baking the silver plating was restarted and plating continued to > 5µm Ag.

All technology demonstrator samples passed the tests.

A further optimisation of the plating process was performed for the test coupons.

In order to avoid chemical depletion inside the tube, a slow oscillating vertical movement of the tube, was applied, both in nickel and in silver baths.

The amplitude of the movement was approx. 20 mm and the speed was 50 rpm.

A further increase of the thickness of the nickel layer, to approx. 30 µm, allowed to exclude the intermediate heat baking and thus the silver plating could be performed in one sequence.

All test coupons passed the tests.

Two halves of an aluminium, WR 75, waveguide filter, were plated with 30 µm electroless nickel + 5 µm autocatalytic silver.

The plating was performed as follows:

1. Cleaning, (Ronaclean PC 960, LeaRonal) 3 min, 50° C

2. Rinse, 2 min

3. NaOH/ NaCl, 1 min, 50 °C
4. Rinse, 2 min
5. NH4HF2 / HNO3, 30 s
6. Rinse, 2 min
7. H2SO4, 1 min
8. Rinse, 2 min
9. HNO3, 1 min
10. Rinse, 2 min
11. Zincate, (Duraprep 520 Zincate, Dow), 1 min
12. Rinse, 1 min,
13. HNO3, 1 min
14. Rinse, 1 min
15. Zincate, (Duraprep 520 Zincate, Dow) 15 s
16. Rinse, 1 min
17. Electroless Ni,(Ronamax SR, Dow), 3 h, 87 °C, pH 5.0
18. Rinse 1 min, 60 C
19. Rinse 0.5 min
20. Activation, (NIAG-Activator), 3 min, rt, pH 6.3
21. Autocatalytic Ag, (ESM 200), 4 h, 63 °C, pH @ 63 °C 10.6-10.7
22. Rinse, 2 min
23. Drying, hot air

After plating, the filter was assembled and RF measurements were performed at:

Microwave Electronics Laboratory,Microtechnology and Nanoscience-MC2,

Chalmers University of Technology.

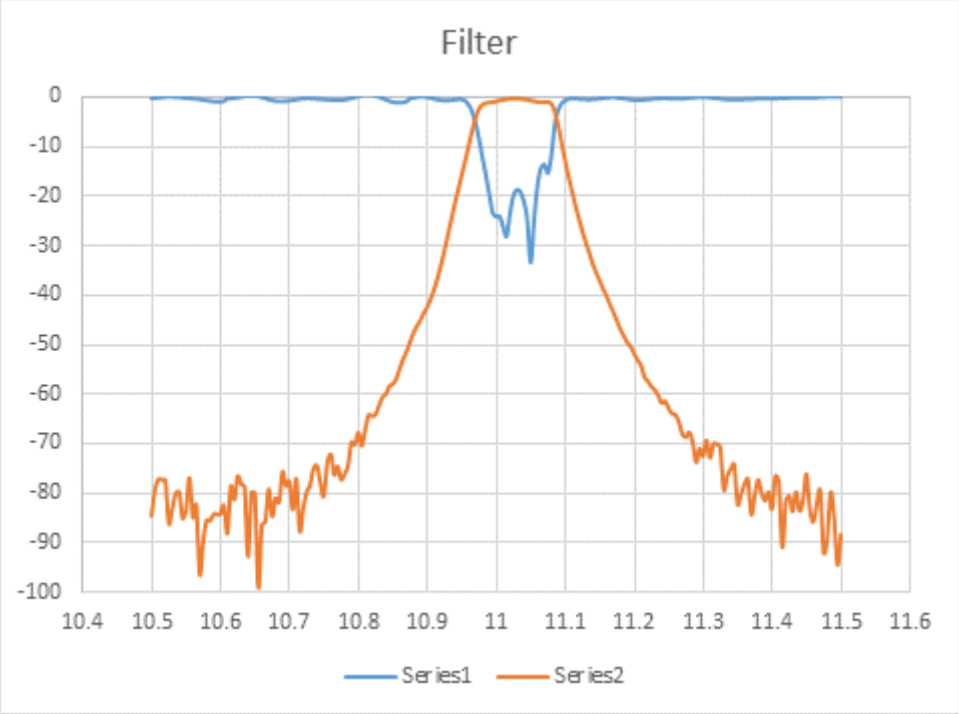
Adapters were connected to the filter and the performance was evaluated by using a network analyser.

The figures below show the measured, WR 75, filter performance, where:

Series 1 is the return loss (S11)

Series 2 is the insertion loss (S2)

X-axis in GHz unit and Y-axis in dB unit.


Filter
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
10.4
10.5
10.6
10.7
10.8
10.9
11
11.1
11.2
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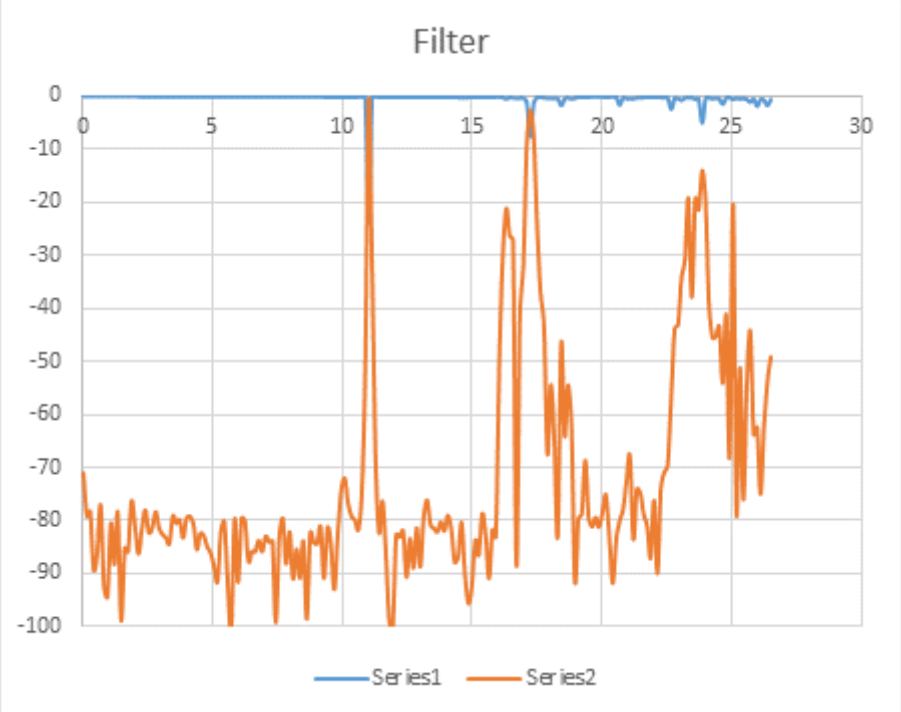
11.6
Series1
Series2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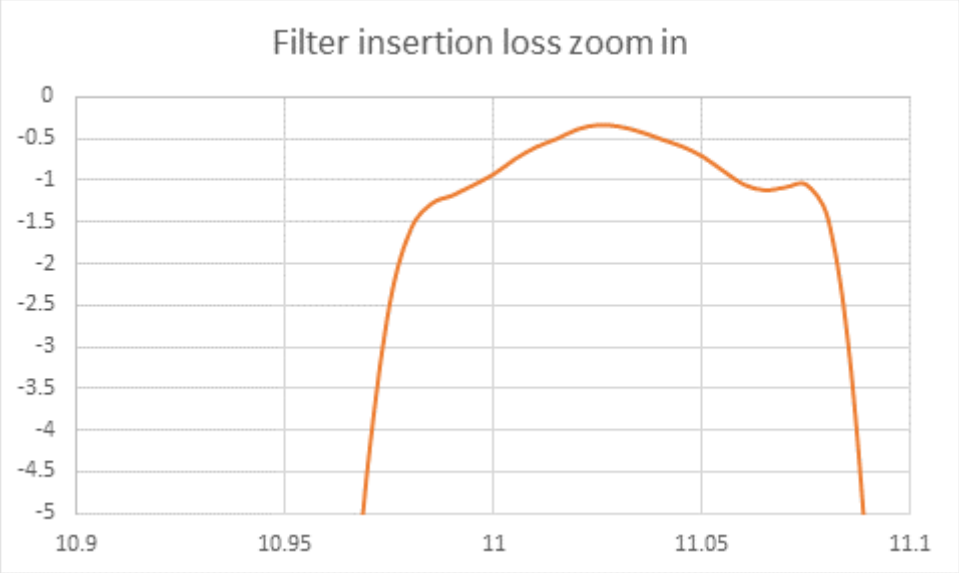

4. Conclusions

4.1 ASIG Application

The ASIG finish provided surfaces with good solderability even after having been exposed to two soldering processes. Solder joints formed to various types of components had good reliability.

Issues were observed regarding resistance against electrochemical migration for non-soldered PCBs. This was not observed for soldered assemblies. Likely, the susceptibility for electrochemical migration of the non-soldered PCBs were due to inadequate rinsing after the plating with the ASIG finish. An improved rinsing process would probably eliminate this issue.

Lesson learnt from the work with ASIG application is that the rinsing after plating, has to be thoroughly in order to avoid problems with resistance against electrochemical migration.

4.2 MWC Application

The autocatalytic silver plated samples passed the heat resistance test, the humidity test and the thermal cycling test and a well working plating process is now verified.

RF-measurements of an autocatalytic silver plated, WR 75, waveguide filter shows a performance as expected for a similar electroplated filter.

The evaluation shows that, the autocatalytic silver plating process, ESM 200, meets both RF- and space environment requirements.

Lessons learnt from the work with MWC application are, that the thickness of the nickel barrier has to be optimized in order to keep good adhesion between aluminium and nickel after the silver plating process and that movement of the goods is important to avoid chemical depletion /gas traps.

References

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