EXECUTIVE SUMMARY REPORT
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Executive Summary Report

Contract No. 4000131921/20/NL/BJ/rk

”Preparation of enabling space technologies and building blocks”

“Prototyping and initial evaluation of a monolithic, rad-hard, high-power POL converter”

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Table of Contents

List of Figures

Reference Documents

[1] SPACE IC: Preliminary Datasheet SPPL14080RH, 8 A, 40 V Synchronous Rectified Step-Down Converter, V2401, June 2024, https://space-ic.com/files/space/pdf/SPPL14080RH_preliminary_datasheet.pdf

[2] SPACE IC: Datasheet SPPL12420RH, 2 A Synchronous Rectified Step-Down Converter, V2401, February 2024, https://space-ic.com/files/space/pdf/SPPL12420RH.pdf

[3] ECSS Secretariat: “Space Engineering - Technology readiness level (TRL) guidelines”, ECSS-E-HB-11A, 01-Mar-2017

[4] ESCC Generic Specification No. 9000: Integrated Circuits, Monolithic, Hermetically Sealed, Issue 11, February 2021

[5] ESCC Generic Specification No. 2269000: “Evaluation Test Programme for Integrated Circuits: Monolithic and Multichip Microcircuits, wire-bonded, hermetically sealed”, Issue 7, November 2018

1 Introduction

This documentation is the summary of the project:

Contract No. 4000131921/20/NL/BJ/rk

"Preparation of enabling space technologies and building blocks"
"Prototyping and initial evaluation of a monolithic, rad-hard, high-power POL converter"

The power conditioning and distribution in newer space systems will be realized in a modern modular point-of-load architecture. Here, the secondary power conditioning unit provides only a few intermediate voltage busses with significantly reduced accuracy for nearly all electronic power consumers in the payload or OBC. A simplified bus system with just a few rails distributes the intermediate voltage to the payload modules.

The supply voltages needed inside a module are generated from the intermediate power rails at exactly the right levels directly at the electronic component to be supplied – the point of load (POL). This has to be done by compact and highly efficient DC/DC converters which can be flexibly configured to deliver a wide range of output voltage values down to <1 V from a standard intermediate voltage.

Monolithic POL converter ICs are highly integrated and versatile components including all necessary electronic functions to build a compact and highly efficient DC/DC converter. They can be used for point-of-load power conversion in on-board computers, payloads and other electronics with or without modular architecture in any space mission, e.g. Juice, Euclid, Plato, Athena, Copernicus, Galileo Next Generation etc.

The SPPL14080RH can be flexibly used in various application scenarios, which are shown in Figure 1.

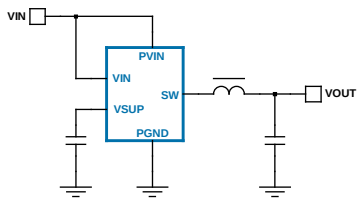
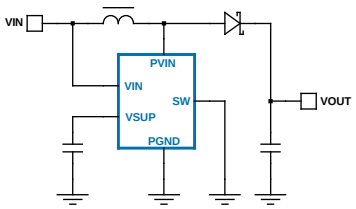
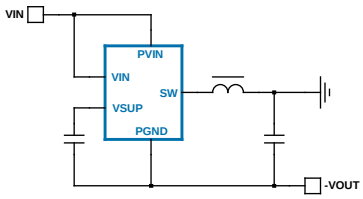
Buck Mode	Boost Mode	Buck-Boost-Mode
		
e.g. V_{IN} = 12V V_{OUT} = 1.8V	e.g. V_{IN} = 5V V_{OUT} = 12V	e.g. V_{IN} = 5V V_{OUT} = -5V

Figure 1: Various Applications

Also, for load current values beyond 8 A two or more components can be synchronously operated in load-sharing mode without additional external control electronic.

Starting point of this activity was the market assessment (including technical feedback from power management specialists from ESA, DLR and many European companies), the component specification, the chip architectural design, the feasibility assessment and design of critical building

blocks and the conception of the hermetic power package. With that the SPPL14080RH component was considered to be TRL 3 level.

That was the base for the subsequent design completion, prototyping and initial electrical and radiation evaluation. At the end of these follow-up processes the SPPL14080RH became available to the European space industry as TRL 4 engineering models.

The main objective of this activity was to obtain validated prototypes of a fully designed SPPL14080RH component in ceramic power package by:

- performing detailed design and layout until GDS delivery (tape-out)
- manufacturing prototypes (package manufacturing, die manufacturing and assembly)
- validating the design by construction analysis, electrically measuring the prototypes on bench and application test boards and evaluating the TID and SEE radiation performance

The device was developed and manufactured in Atmel ATMX150RHA technology, which has ESCC capability approval. The manufacturing approach is comparable to the current SPPL12420RH component from SPACE IC, which is already ESCC-certified. Also the Flatpack-32 chip package was developed and manufactured similar to the Flatpack-16 chip packaging of the current SPPL12420RH component from SPACE IC.

The project started in September 2020 and has been finished in June 2024.

2 Overview of the activity

The activity was split into three project phases. The first phase (WP1) was the detailed design of the IC and the design of the final ceramic flatpack package. The content of the second phase of the activity (WP2) was the preparation of the test setup for validation and characterization of the IC. In parallel, the dies and the packages were manufactured followed by the component assembly of the first engineering models.

In the third phase (WP3) the initial evaluation of the ICs including TID and SEE radiation testing were executed. Finally, all test results were used to update all required specifications for a subsequent design optimization to improve the performance of the IC.

Figure 2 shows the logical execution of the activity.

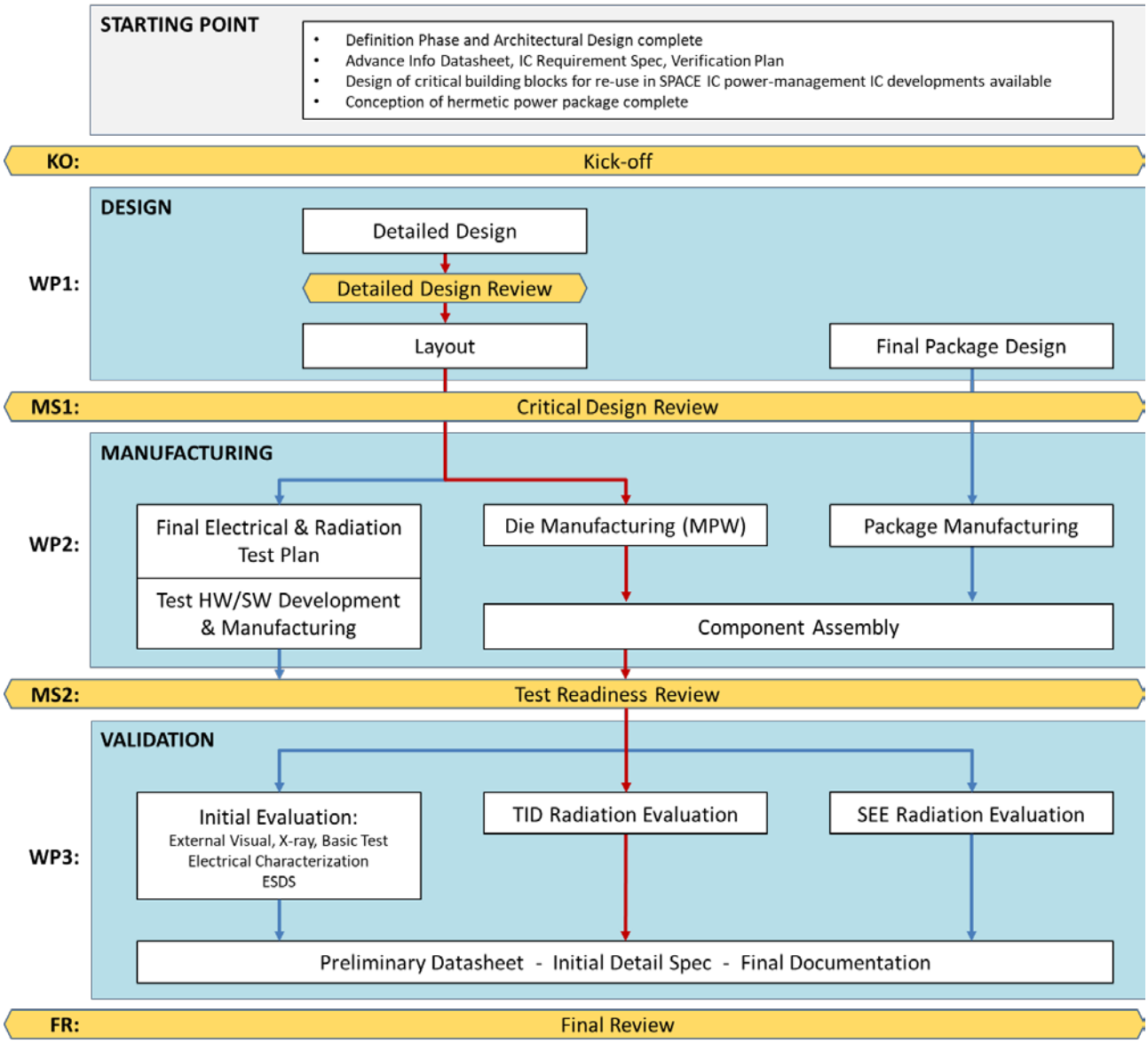


Figure 2: Flow chart of the activity

3 Work performed and main results

In the following chapters, the different work packages according to Figure 2 are summarized.

3.1 Design Phase (WP1)

Based on the market assessment, the component specification, the chip architectural design and design of critical building blocks the chip design, chip layout and development of the hermetic ceramic package were executed. The work package was finished by the critical design review to check all data relevant for manufacturing of the IC and the package.

- *Detailed Design and Detailed Design Review:*
  In this phase the different IC design blocks were specified. After schematic entry the blocks were verified by simulations over process, mismatch, temperature and supply conditions. Furthermore measures were implemented to reach the required radiation hardness. At the end of this process the verifications were reviewed together with ESA in the Detailed Design Review.

- *Layout and Critical Design Review:*
  After the design review the modules were layouted. All modules were checked in layout reviews and by executing the standard checks, e.g. design rule checks (DRC) and layout-versus-schematic checks (LVS). Finally all results were checked with ESA in the critical design review before the GDSII file was sent to the semiconductor foundry for manufacturing. Figure 3 shows the layout of the full chip.

- *Final Package Design:*
  In parallel to the chip design the design and layout of the 32 pin hermetic ceramic flatpack package were executed in close cooperation with the package manufacturer. For reaching a high device efficiency the serial resistance of the package has to be as small as possible. Furthermore the current distribution inside the package and the thermal behavior are important, so a customized package is required which fits to the designed integrated circuit.

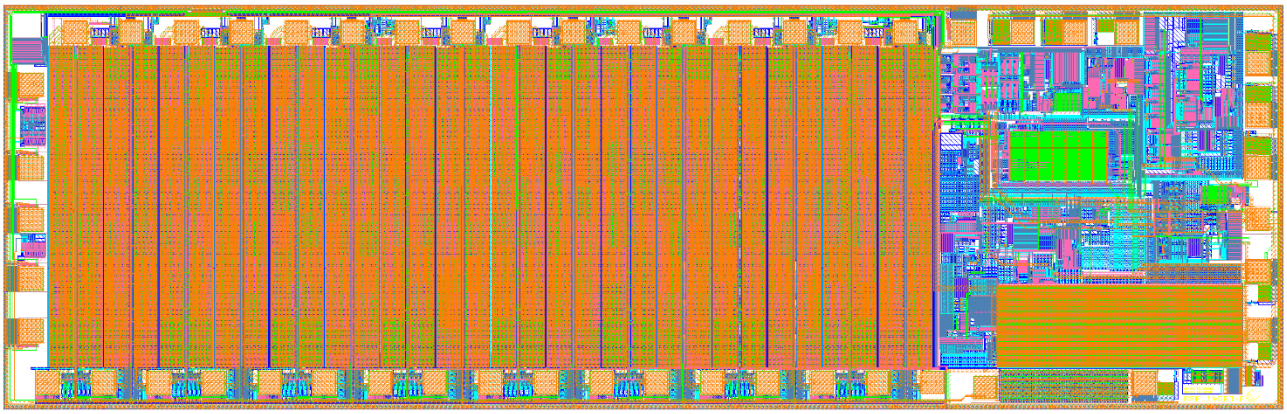


Figure 3: IC Layout

3.2 Manufacturing and Test Development (WP2)

In the subsequent Manufacturing Phase the prototype dies were manufactured in the semiconductor foundry. Simultaneously the customized hermetic ceramic packages were manufactured at SPACE ICs main supplier for hermetic ceramic packages.

The manufacturing was executed by strategic suppliers that share SPACE ICs commitment to deliver space-grade quality products. These suppliers have long-term experience in the space market and have the relevant capabilities. They are part of the SPACE IC manufacturing organization and work under supply chain management and overall quality assurance of SPACE IC.

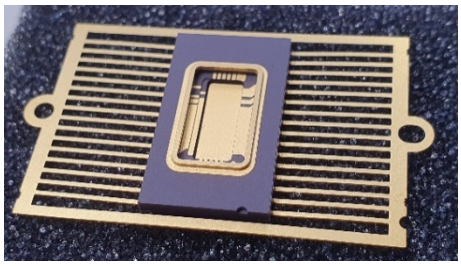


Figure 4: Hermetic ceramic flatpack package for SPPL14080RH

With the availability of the dies and the package the assembly was executed to get prototypes for first bench tests. The dies were assembled in both the final ceramic 32 pin flatpack package for the application tests and in PCB-based DIL packages for first bench validation tests.

Simultaneously to the manufacturing test plans for electrical characterization on bench over temperature and supply, for application and radiation testing were generated. For the IC validation breadboards were developed and manufactured to ensure that all the required testing can be performed as expected. These boards were designed by SPACE IC and manufactured by a PCB supplier.

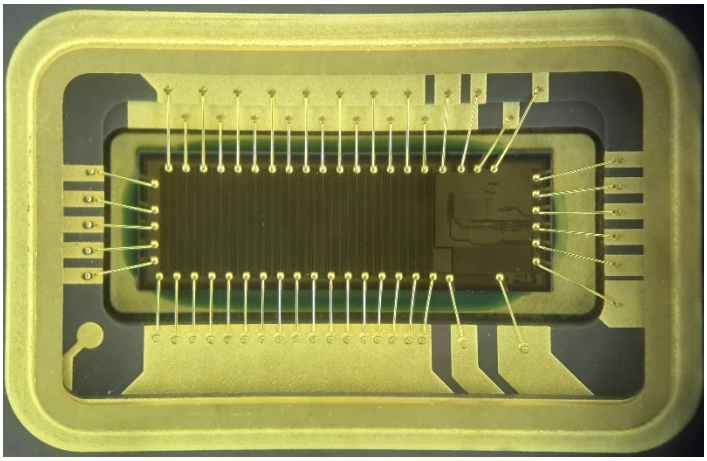


Figure 5: Assembled SPPL14080RH die in ceramic flatpack package

All bench measurement devices and setups can be controlled by LabVIEW test programs to ensure the efficient execution of the measurements including the required repeatability. The LabVIEW test programs were developed by SPACE IC.

The Manufacturing Phase ended with the Test Readiness Review.

3.3 Validation (WP3)

In this work package the validation of the first prototypes was executed. The electrical verification of the ICs was performed in the SPACE IC measurement lab. The lab fulfils all requirements regarding ESD protection. The available key measurement equipment consists of oscilloscope, different sourcemeters and supplies, electronic load, current probe and digital multimeter. For the characterization depending on the device temperature a thermostream was used.

1. Electrical Characterization
   According to the electrical test plans and test setups, which were developed in work package WP2 of this activity, the first bench tests were done to evaluate the general device functionality. Afterwards during the characterization the device was analysed on performance level depending on different supply and temperature conditions.
   Furthermore the device was tested in different application test setups to verify the correct behaviour of the device in applications. For these tests in particular, the prototypes in the ceramic flatpack package were used to check the functionality and performance in the target environment. Figure 6 shows the different setups for characterization and application tests.

2. ESDS tests
   For the ESDS tests first prototypes of the SPPL14080RH in ceramic flatpack package were used. An ESD robustness of 4 kV was the test target. The component passed the 5 kV ESDS tests without any deviation. First deviations were observed between 5 kV and 6 kV, so the component shows sufficient margin in ESD robustness.

3. Radiation Evaluation (TID and SEE)
   Also a first radiation evaluation was part of this activity to check the TID and SEE radiation hardness. The aim of the TID test campaign was to evaluate the radiation hardness level of the SPPL14080RH in unbiased and different biased conditions up to and beyond 150 krad(Si) to achieve a TID class of 100 krad according to ESCC 22900 and to evaluate the worst-case bias conditions. The objective of the SEE test was to investigate the sensitivity of the POL Converter IC SPPL14080RH to the destructive events up to an effective LET of 60 MeV·cm2/mg and optionally 75 MeV·cm2/mg regardless the incidence angle and the tilt direction. Voltage thresholds have been evaluated and SETs captured at different conditions.

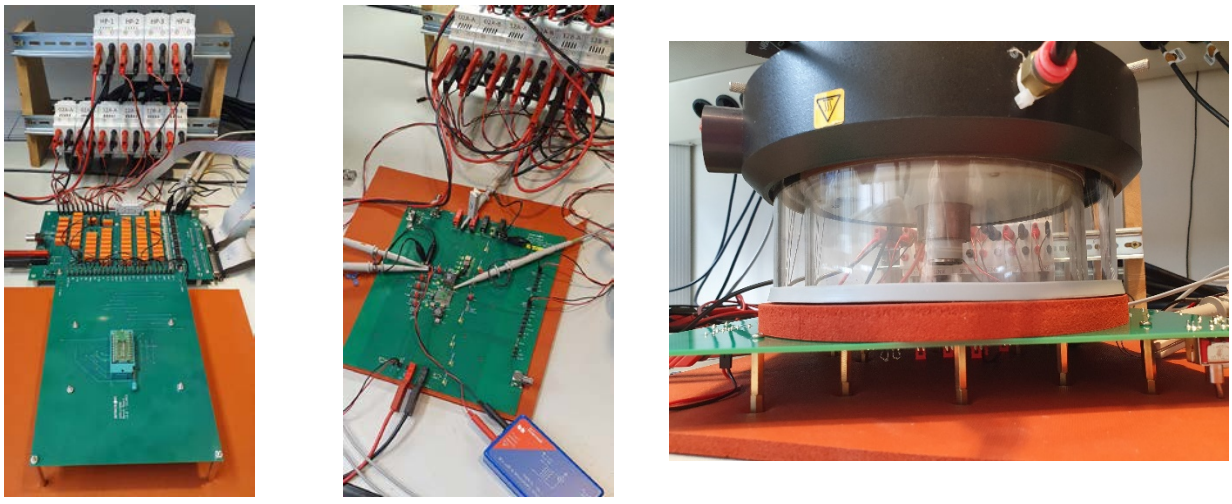


Figure 6: Test setup for Characterization, Application and Temperature Tests

4 Summary and Outlook

After the finalization of this activity the SPPL14080RH became available to the European space industry as TRL 4 engineering models.

The detailed validation and characterization of the component during bench and application testing as part of this activity demonstrated a good functionality and performance of the device. The radiation tests also showed good results.

This activity led to the achievement of Technology Readiness Level TRL 4 through the successful completion of the following project goals:

- performing detailed design and layout until GDS delivery (tape-out)
- manufacturing prototypes (package manufacturing, die manufacturing and assembly)
- availability of engineering models assembled in a ceramic power package
- electrically measuring the prototypes on bench and application test boards and evaluating the TID and SEE radiation performance

Nevertheless, some items for design optimization were found during the tests, so the design of the IC will be improved. This is quite common with complex analog components like this one, as the simulation models cannot represent reality to 100%. It was also necessary to re-select the main supplier for the assembly at an advanced stage, so that the construction analysis and the pre-cap inspection were shifted into the follow-up project with ESA Contact No. 4000143365/23/NL.

Regardless of the changes to the design and assembly, engineering models are now available to space customers for evaluation in a variety of customer applications.

Considering the achievements of this activity and the planned design optimization, the suitability of the device for the evaluation and qualification according to ESCC specifications can be achieved with sufficient confidence.

After successful passing the component evaluation and qualification, the SPPL14080RH will become available to the European space industry as Class 1 flight models screened according to ESCC9000.