NIRCA
Prototype ASIC Development
for
Large Format NIR/SWIR Detector Array

4000107615/12/NL/EL/fk

Final Presentation
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Content

Introduction

IDEAS

More than 100 different designs of integrated circuits for high energy, nuclear and astrophysics research.

We own all IP used in our circuits

Main market segments

- Space
- Science (Nuclear/High Energy Physics)
- Environmental monitoring
- Medical and biomedical

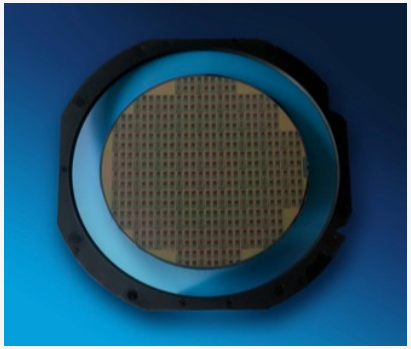
Number of Employees: 20

Technical team

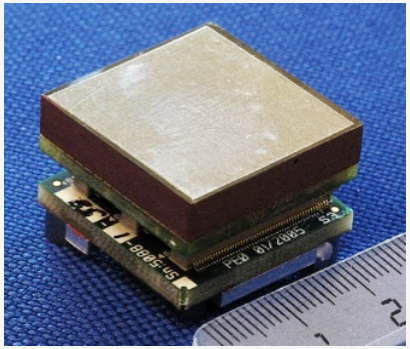
- ASIC design: 7 team members
- System design & test: 7 team members

Products

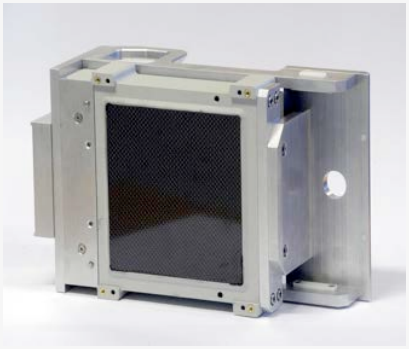
Solutions for radiation detection and imaging



Readout ICs and ASICs



Radiation Detector Modules



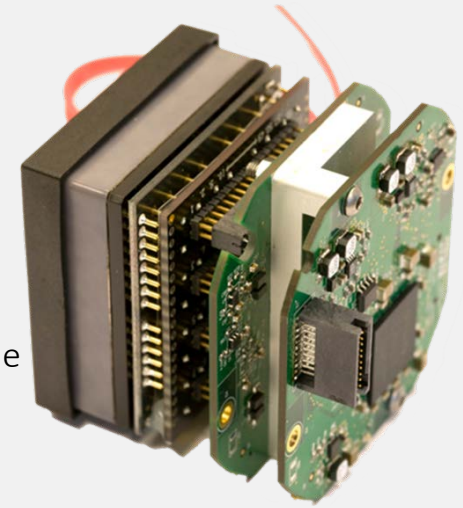
Gamma Cameras

OEM Modules

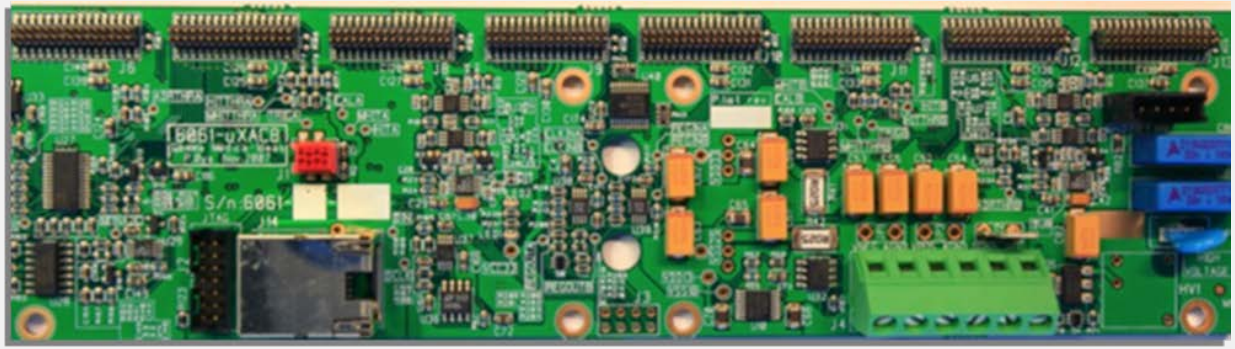
(OEM = Original Equipment Manufacturer)

We develop customized solutions for use with our ASICs, including embedded processors and systems.

Self contained R/O for the H8500C multi-anode photomultiplier tube

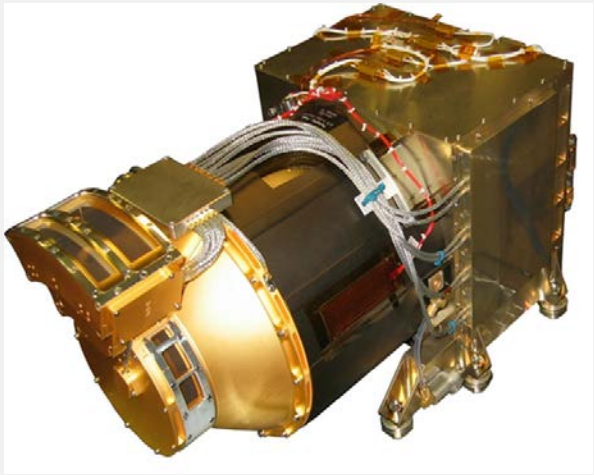


Data acquisition card used in a gamma camera for medical diagnostics. Reads 12280 CZT pixels for gamma ray spectroscopic imaging in a camera for medical use.



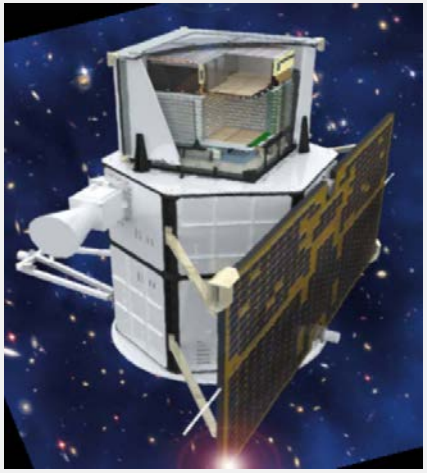
Introduction

Application Example, Space ASIC Development



The PLAsma and SupraThermal Ion Composition (PLASTIC)
experiment on the STEREO mission.

Customer: NASA
IDEAS delivered ASIC for read out of detectors of the spectrometer. Launched 2006



SuperAGILE an X-ray monitor of AGILE

Customer: Italian Space Agency (ASI)
devoted to observations for astrophysics in the
gamma ray energy range 30 MeV-50 GeV.

Application Example, Space

ASIC Development, NASA, AMS2 on ISS

The Alpha Magnetic Spectrometer on the International Space Station

Launched on the last NASA Endeavour Space Shuttle mission to the ISS in 2011.

IDEAS delivered about 2000 ASICs for the readout of the silicon charged particle tracker. In total several 10000 channels of preamplifiers.

The experiment is visible above the truss on ISS.

In orbit operation since summer 2011

Introduction

Integrated Detector Electronics AS

Space missions

Mission	Operator	Launch	Instrument utilizing IDEAS ASICs
SWIFT	NASA	2004	BAT gamma-ray telescope and spectrometer
CREAM	NASA	2004-2010	Several balloon flights
AMS/AMS02	NASA	1997 / 2011	Charged particle tracker
PAMELA	INFN	2006	Charged particle tracker
STEREO	NASA	2006	PLASTIC, Particle and ion Spectrometer
Super AGILE	INAF-IASF INFN	2007	Gamma ray spectrometer
Chandrayaan-1	ISRO	2008	HEX, High Energy gamma and x ray spectrometer
FOXSI	NASA	2014	X ray telescope/spectrometer
ASIM	DNSC	2016	MXGS, Miniature X- and Gamma-Ray Sensor, an X and gamma ray spectrometer
CALET	JAXA	2015	CALorimetric Electron Telescope
ASTRO-H	JAXA	2016	SDG Soft Gamma Ray Imager HXI Hard X-ray Imager
BepiColombo	ESA/JAXA	2016	MPPE instrument on MMO, BERM radiation monitor ELENA instrument
EDRS-C	ESA	2016	NGRM, Next Generation Radiation Monitor, electron and proton spectrometer. This instrument is also under consideration for MetOp-C, EuroStar and Euclid.
DAMPE	CAS	2016	DArk Matter Particle Explorer. High energy calorimeter and tracker.
JUICE	ESA	2022	Rad-Hard Electron Monitor for JUICE. Electron and proton spectrometer.
Polar	CAS	na	Gamma ray spectrometer using multi-anode photomul-tipliers.

Introduction

NIRCA

Project purpose and objective

Integrated Detector Electronics AS (IDEAS) has in Contract No. 4000107615/12/NL/EL/fk,

“Prototype ASIC Development for Large Format NIR/SWIR Detector Array”,

developed an Application Specific Integrated Circuit (ASIC) for data acquisition and control of Mercury cadmium telluride focal plane arrays.

This development was part of a series of developments that aims to culminate in the availability of a flight quality 2k×2k large-format NIR detector hybrid with a single chip controller.

The ASIC is fabricated in AMS 0.35 µm CMOS process.

NIRCA overview

NIRCA overview

Programmable Sequencer

- Custom instruction set.
- 8192 instructions (ECC-RAM).
- 8 nested loops.
- 8× Digital inputs.
- 32× Digital waveforms and 8x control outputs.
- 256x32b wave vector table (ECC-RAM).

Interfaces

- SPI programming interface.
- SPI direct bridge to remote unit.
- 2×200 Mbps upstream LVDS (8b/10b).
- IRQ for exception, sequencer messages.

Analogue Acquisition

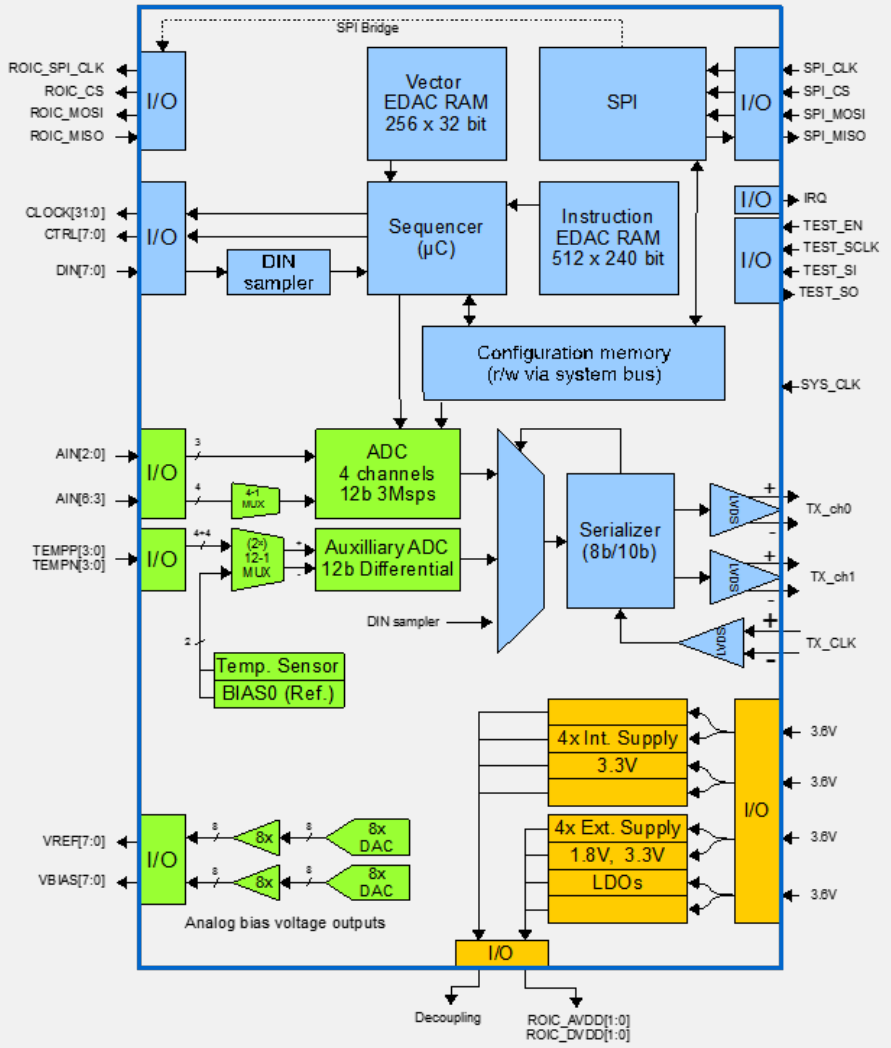
- 4× 12-bit, 2 Msps SAR ADCs.
- Programmable gain.
- 3× direct single-ended analogue inputs.
- 4× muxed single-ended analogue inputs.
- Simultaneous ADC sampling.

Analogue monitoring

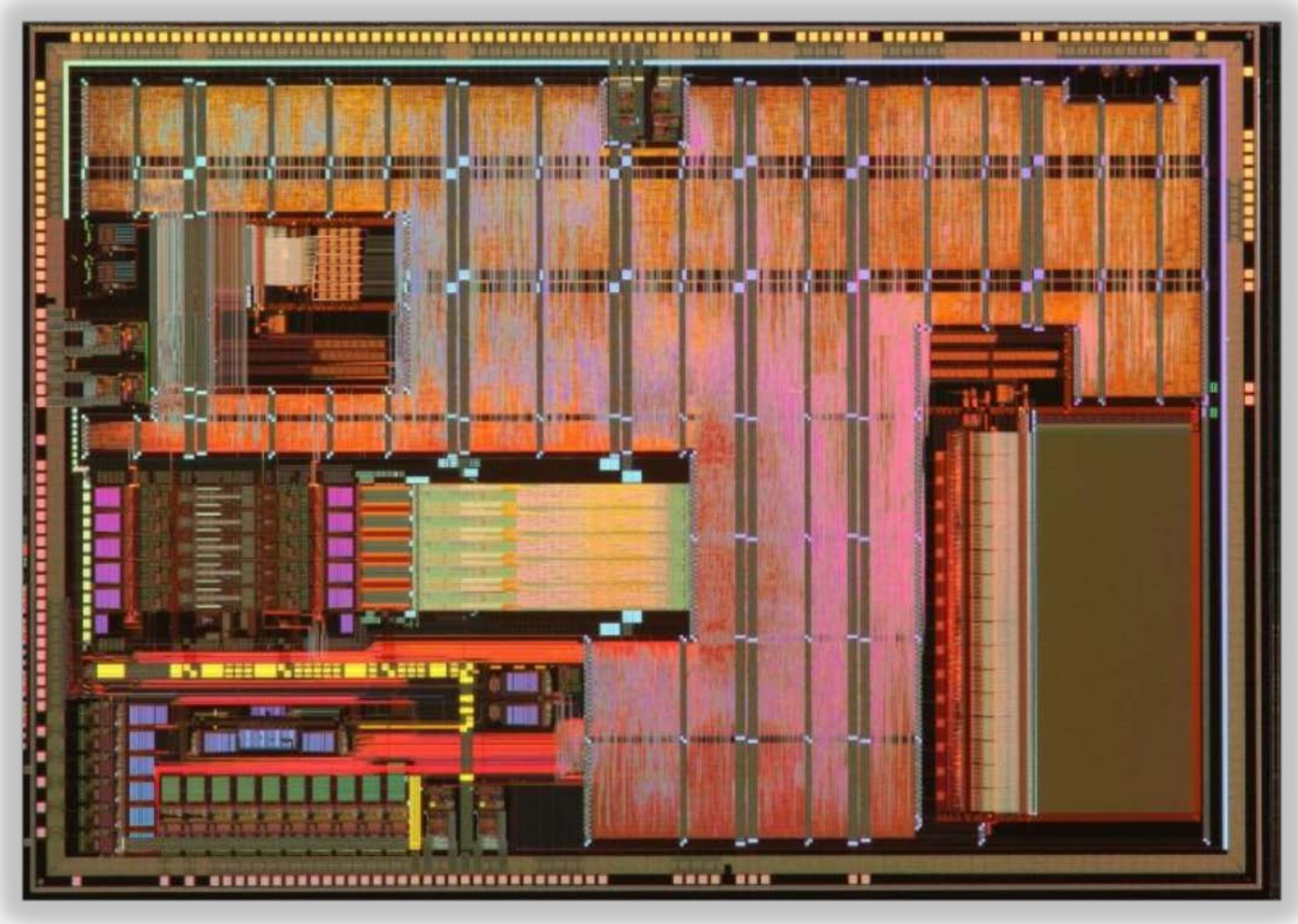
- 1× 12-bit, 2 Msps SAR ADC.
- Programmable gain.
- 4x differential or
- 8x single-ended inputs (muxed).
- Internal temperature sensor.
- Ext. resistance measurement capability.

Bias and supply generation

- 16× ext. voltage output (16× 10-bit DACs).
- 2× 1.8V LDO regulators for ext. use.
- 2× 3.3V LDO regulators for ext. use.
- Internal temperature stable V & I reference.



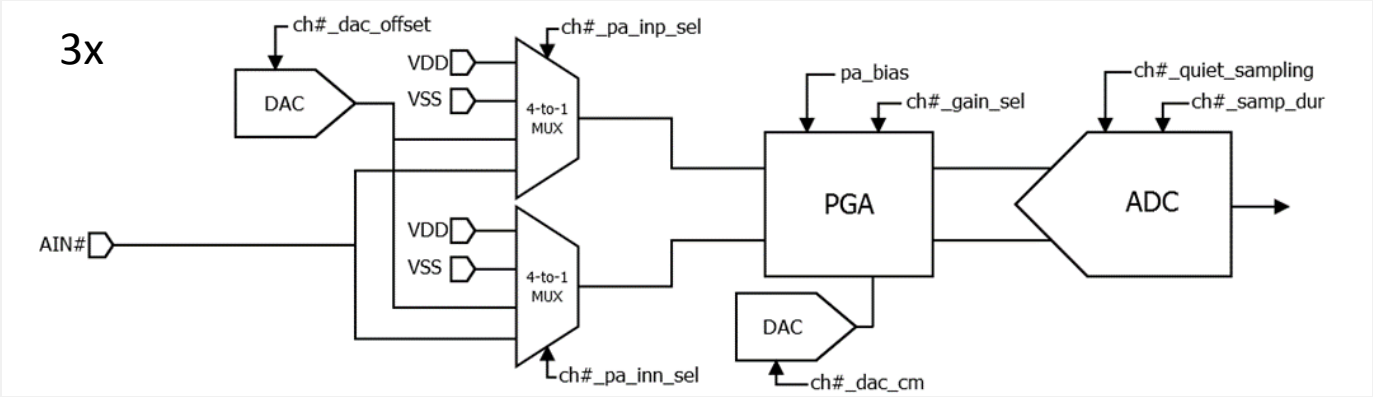
NIRCA overview



NIRCA overview

Analogue inputs (image data)

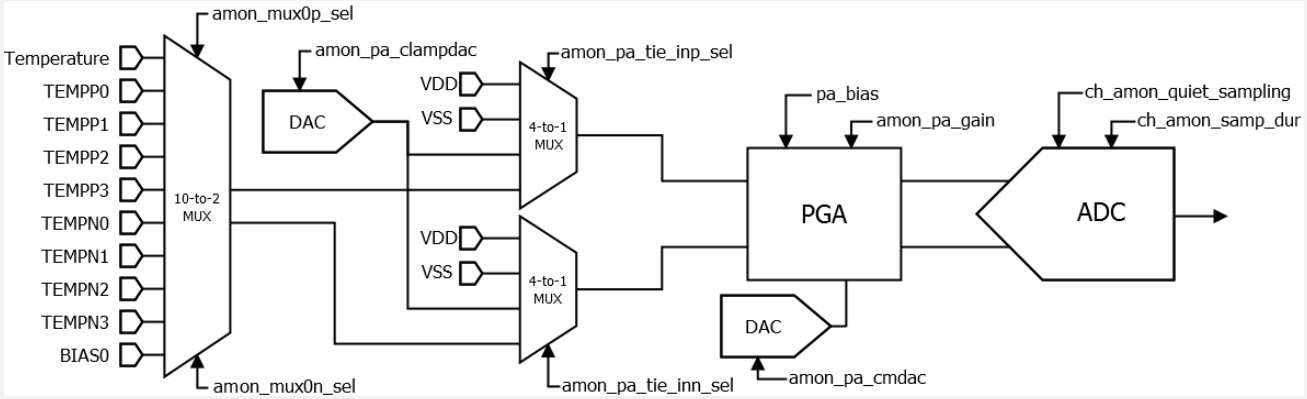
- 3 channels with single-ended inputs
- 1 channel with 3 muxed single-ended inputs
- Reference to VDD, VSS or programmable value from a 10 bit DAC (0.65 V – 1.65 V)
- References and signals are interchangeable
- Programmable gain: 1x, 2x, 4x, 8x, 16x



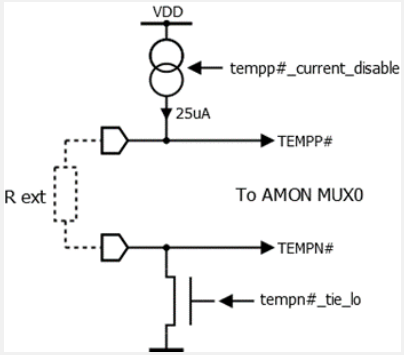
NIRCA overview

Analogue inputs, auxiliary channel (monitor signals)

- 4 muxed differential inputs: Any combinations of TEMPP[3:0], TEMPN[3:0]
- Internal monitor signals: Temperature, BIAS0
- Reference to VDD, GND or programmable value from a 10 bit DAC (0.65 V – 1.65 V)
- References and signals are interchangeable
- Programmable gains: 1x, 2x, 4x, 8x, 16x



Each TEMPP[3:0] can source 25 µA current
Each TEMPN[3:0] can sink the return current
- while sensing the voltage



NIRCA overview

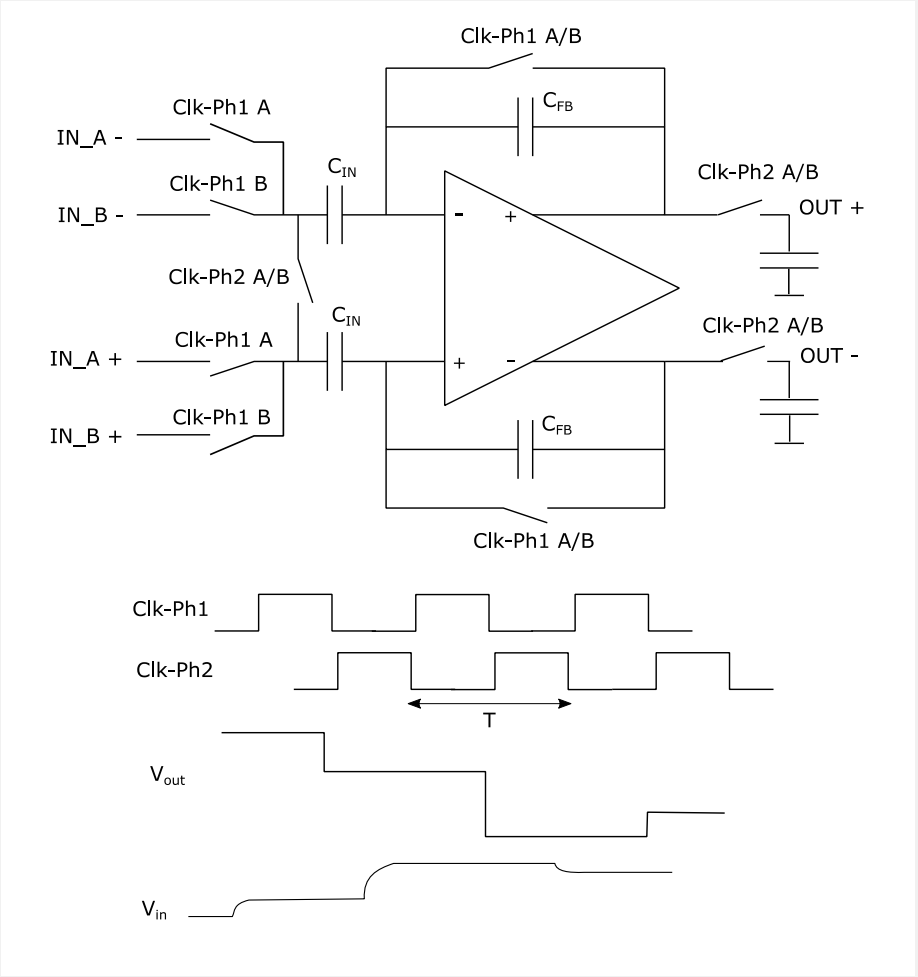
Analogue inputs

Switch Capacitor preamplifier

- Voltage gain = C_{FB}/C_{IN}

  $\Delta V_{out}(t_n) = - C_{FB}/C_{IN}[\Delta V_{in}(t_n - T/2)]$

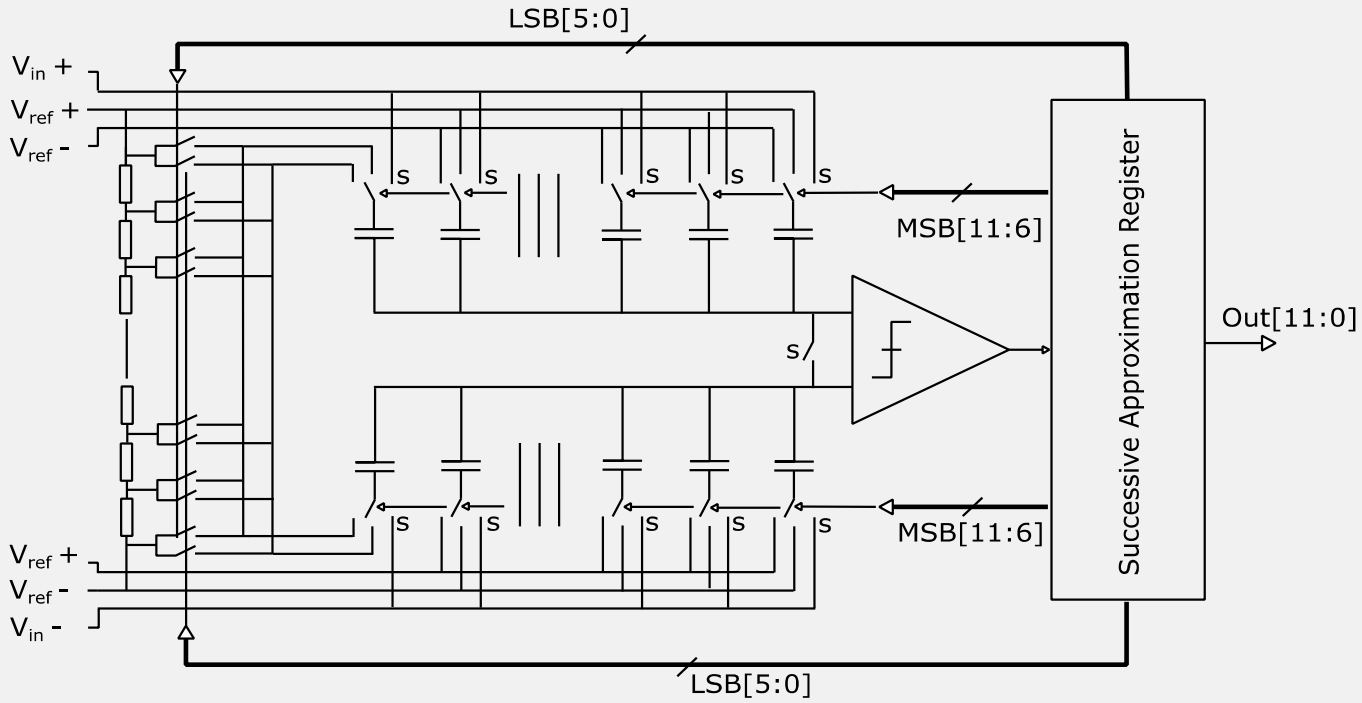
- Multiplexing do not add serial resistance.



NIRCA overview

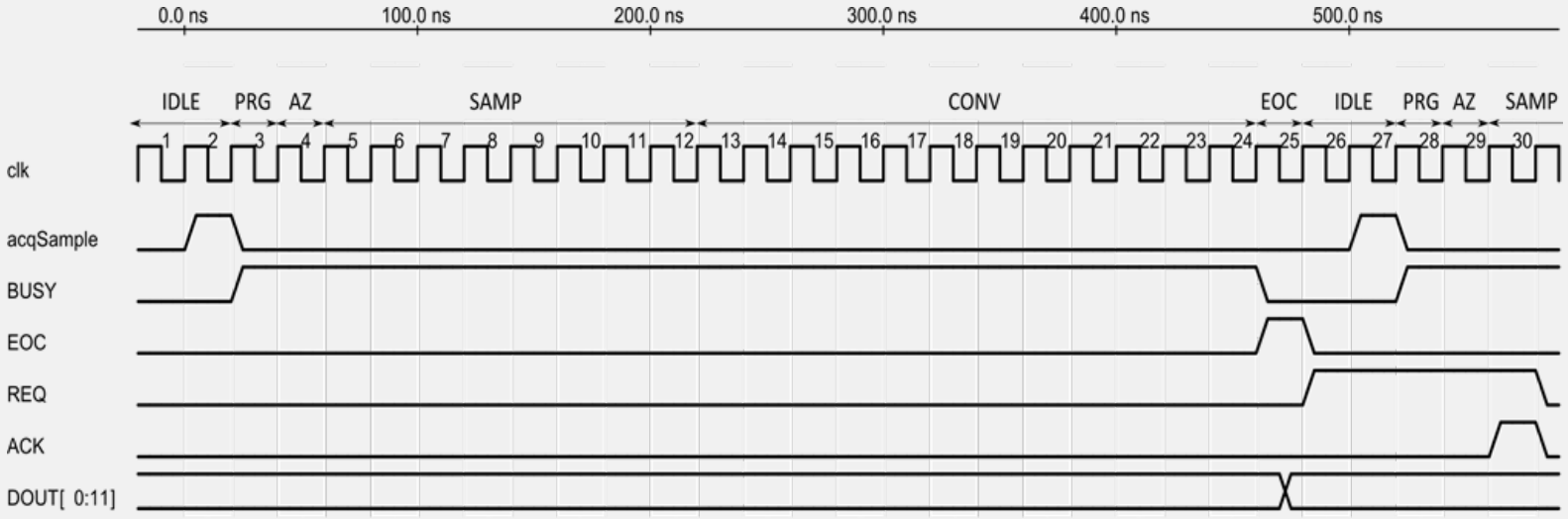
Analogue to digital converter

- Resolution: 12 bit
- Type: Successive approximation register (SAR)
- Feedback DAC is a weighted capacitor charge redistribution (MSBs)
  in combination with
  thermometer coded resistor string (LSBs)



Analogue to Digital Converter

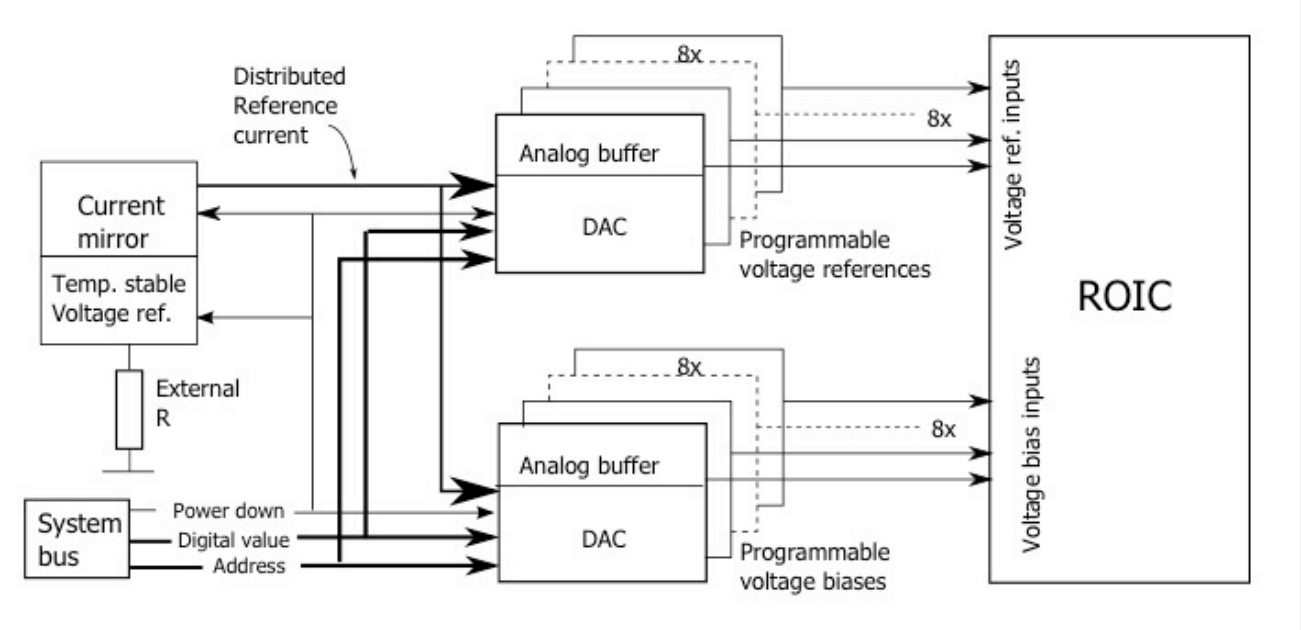
IDLE	User contr.	The ADC is inactive
PRG	1 tclk	Removal of charge of all internal capacitors in the signal paths
AZ	1 tclk	Auto zero offset cancellation is performed. VCM is established
SAMP	1-8 tclk	Sampling of the input signals is performed
CONV	12 tclk	Bit decisions and converging up on the correct digital value
EOC	1 tclk	Indication of when the digital output is valid



Voltage references and biases

- 8 Voltage references
- 8 now noise voltage biases

Programmable output voltage by individual 10 bit DACs.



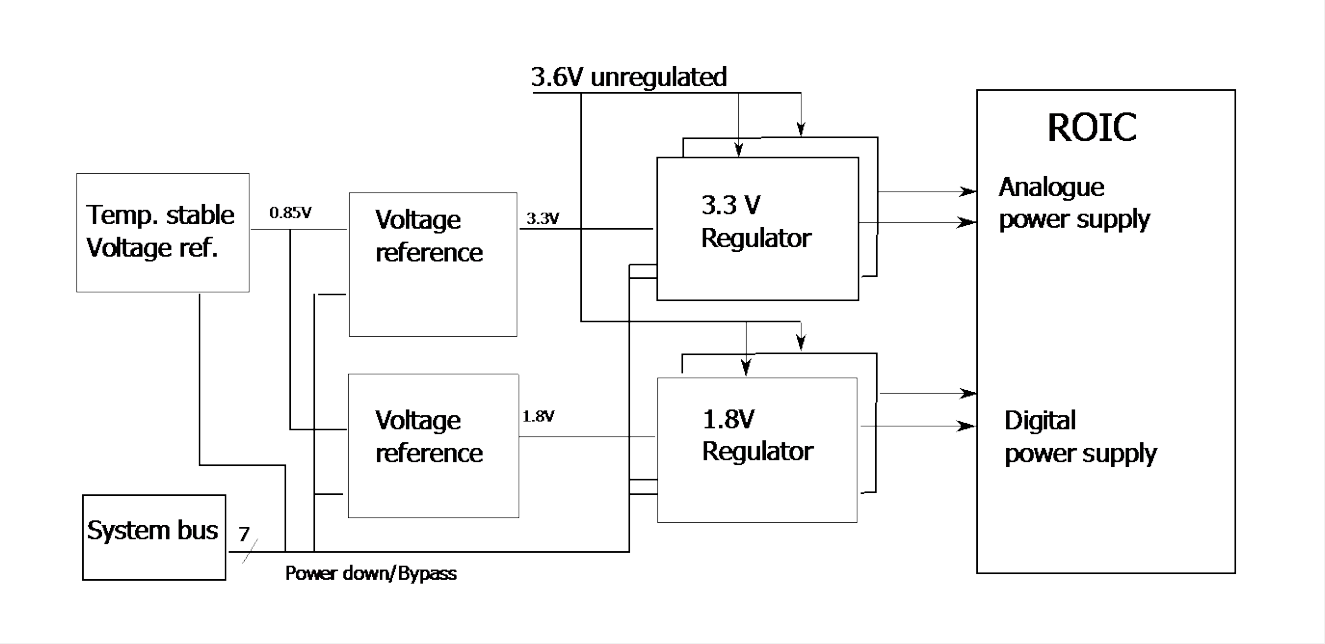
NIRCA overview

Power supply for ROIC

- Two 3.3 V low dropout (LDO) regulators
- Two 1.8 V regulators

Input: Unregulated voltage from 3.4 V to 3.6 V

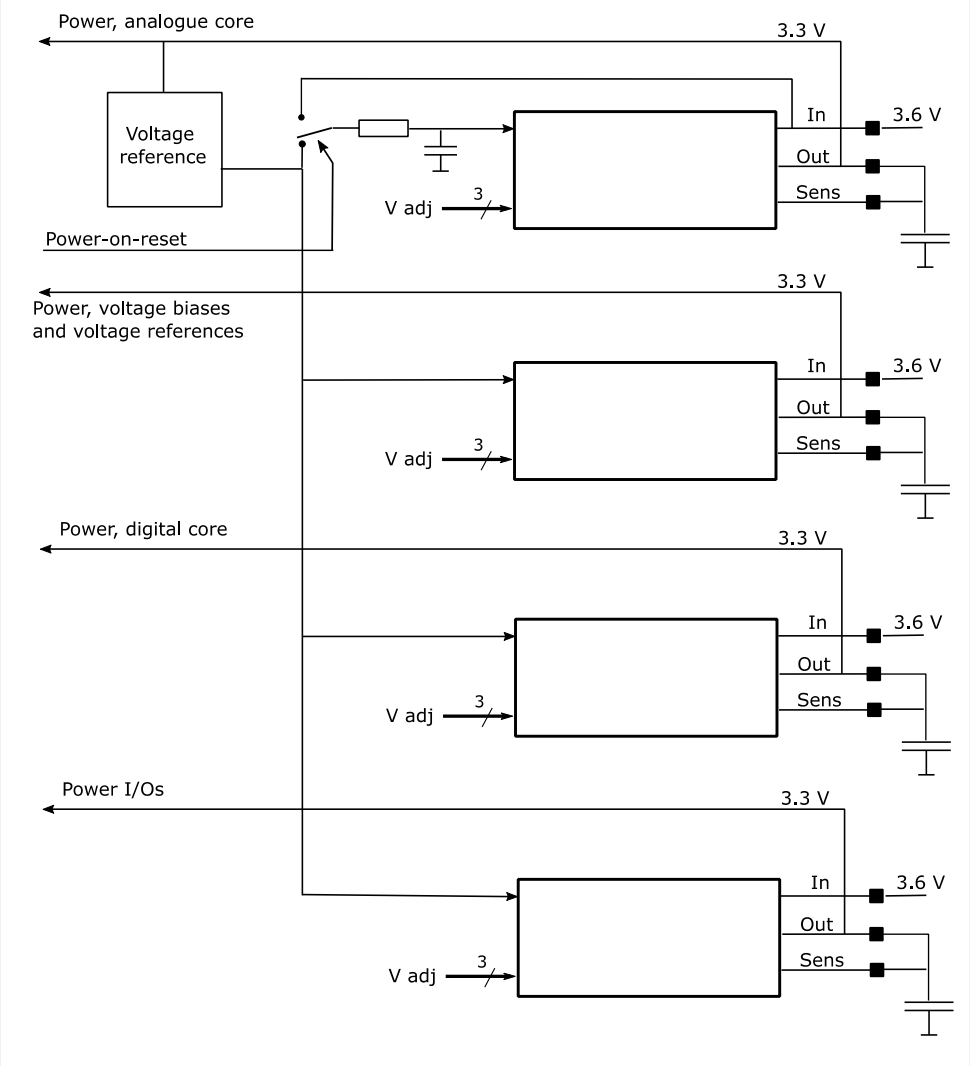
Output: Low ripple and low noise 3.3V and 1.8V



NIRCA overview

Internal power regulators

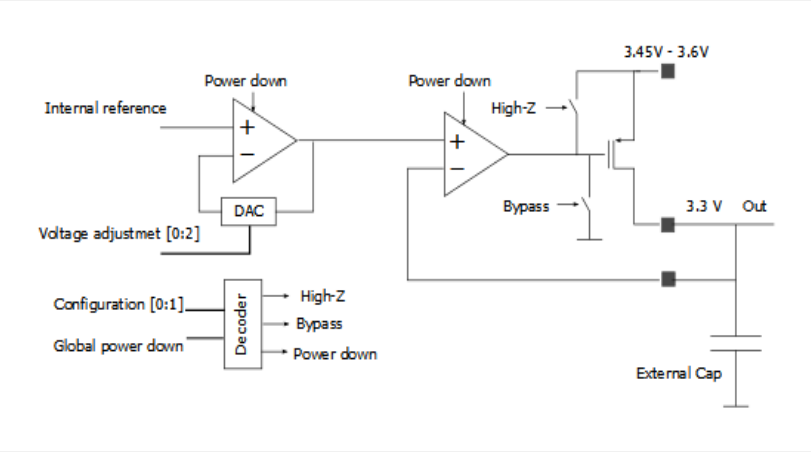
- Four low dropout (LDO) regulators
- Input: Unregulated voltage from 3.4 V to 3.6 V
- Output: 3.3 V, Low ripple and low noise
- Internal power to onchip voltage reference



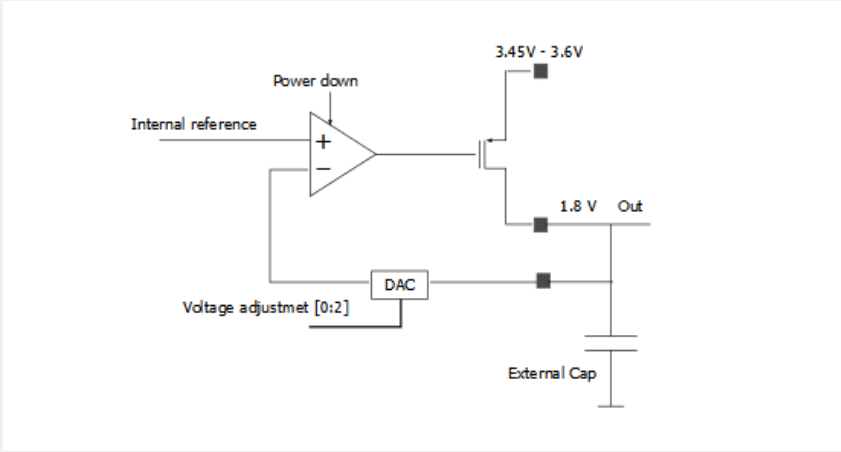
Voltage regulators

- Programmable output range: 3.0 V – 3.4 V
- Inactive states
  - High-Z: Output transistor is turned off. High output impedance. Regulator is powered down
  - Bypass: Output transistor is fully on without regulation. Low resistive path from input to output.

3.3 V LDO

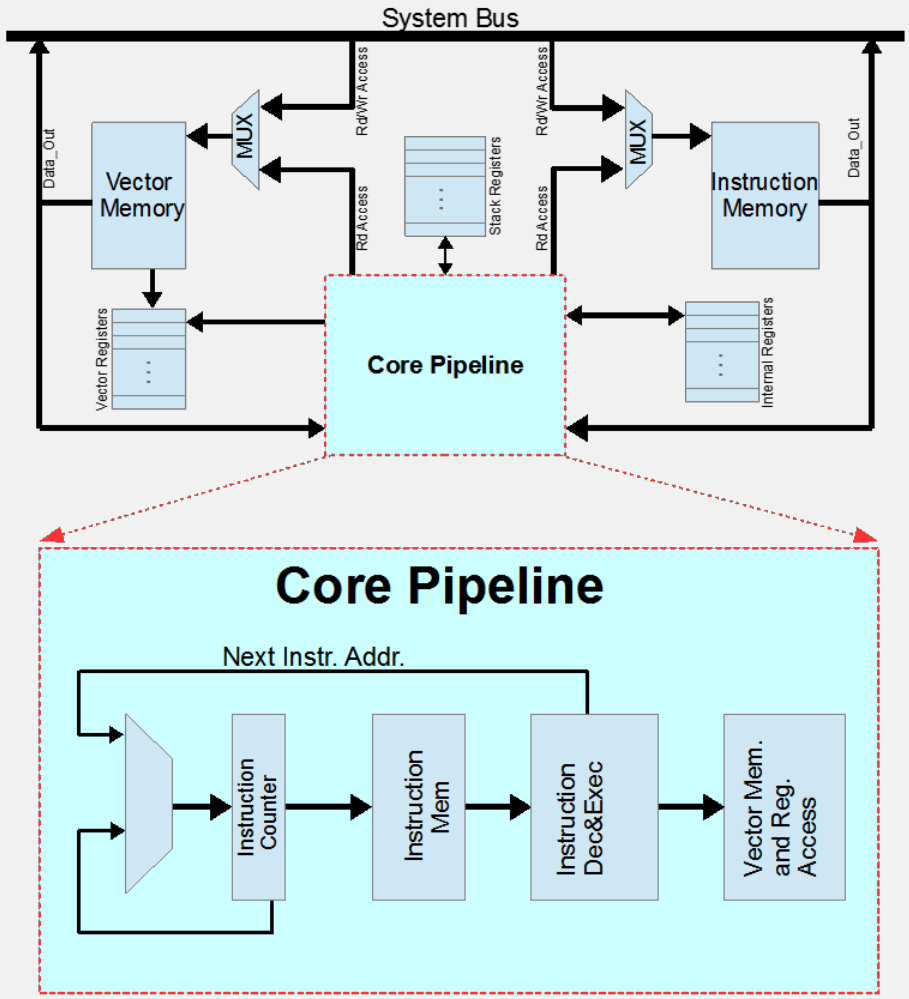


1.8 v regulator



NIRCA overview

Sequencer architecture



NIRCA overview

Sequencer instructions

Short	Bit-fields				Comment
	Code	Parameters/Values			
LDC	000	[11:0] = Loop Counter Value			Load Loop Counter (LC)
n.u.	001x				Reserved, Current effect is NOOP
CALL	0100	PCYCLE	[9:0] = ADDR		Store IP&LC on stack + Jump.
JUMP	0101	n.u.	[9:0] = ADDR		Jump to address
JUMPC	0110	n.u.	[9:0] = ADDR		Conditional jump to address
POP	0111	n.u.	n.u.		Restore IP&LC from stack
LOOP	1000	n.u.	[9:0] = ADDR		Loop to ADDR, or continue if LC==0
LOOPP	1001	n.u.	[9:0] = ADDR		Loop to ADDR, or return (restore IP&LC from stack) when LC==0
LDV	1010	SYNC	[9:8] byte-sel	[7:0] value	Load Vector Register with value.
LDREG	1011	[10:8] REG#		[7:0] value	Load internal register with value, see Table 24.
MOVV	1100	SYNC	[7:0] = INDEX		Move 32-bit vector from Vector RAM to Vector Register. INDEX is row-index in Vector RAM.
MOVD	1101	n.u.	[7:0] = Data		Bus Write. Moves Data to BAR:AR (Base-Address, Address)
NOOPC	1110	SYNC	[7:0] = Counter		Do NOOP (Counter+1) times. Using Sync means that the NOOPC counter runs on the SYNC-counter frequency.
NOOP	1111	n.u.	n.u.		No operation. Single cycle.

NIRCA overview

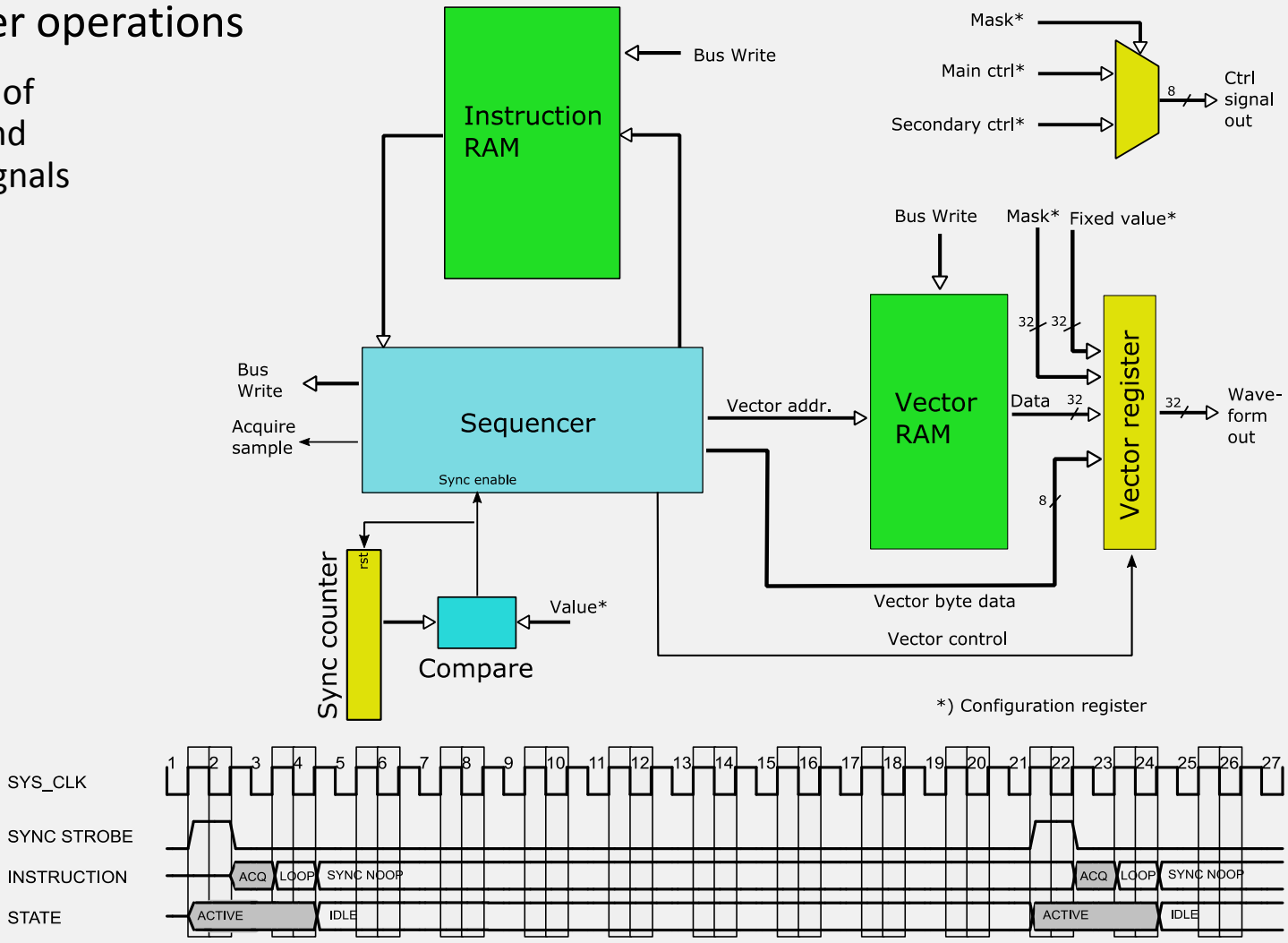
Registers

REG#	Name	Width	Comment
0	BAR	4:0	Upper byte of address for MOVD command.
1	AR	7:0	Lower byte of address for MOVD command.
2	CR	7:0	8 bit compare register for JUMPC command.
3	ACQR	7:0	Analogue and digital acquire sample commands. Accessible on system bus at address 0x0016.
4	ASELR	1:0	ADC3 source selection. Accessible on system bus at address 0x0017.
5	Reserved	5:0	Reserved. Not used. Not connected. Writable from sequencer, may be used for debug. Accessible on system bus at address 0x0018.
6	USERIRQ	5:0	Set User IRQ flags (Flag IRQ message to external system)
7	SP	2:0	Stack pointer (set/reset of stack pointer as clean-up)
	LC	11:0	Loop counter value.

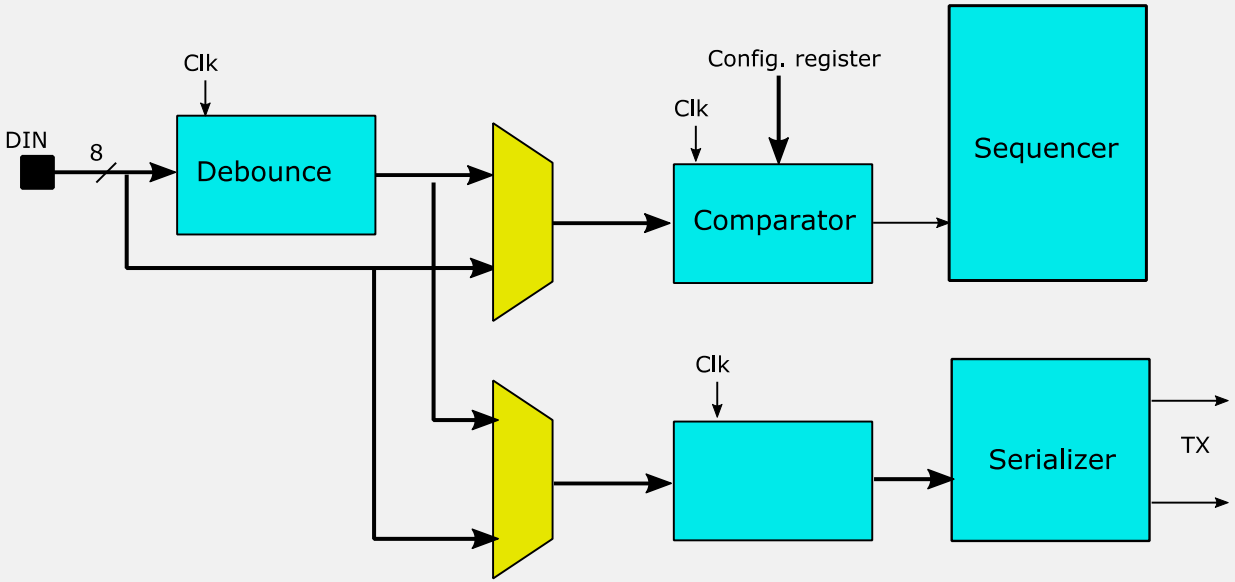
Nirca overview

Sequencer operations

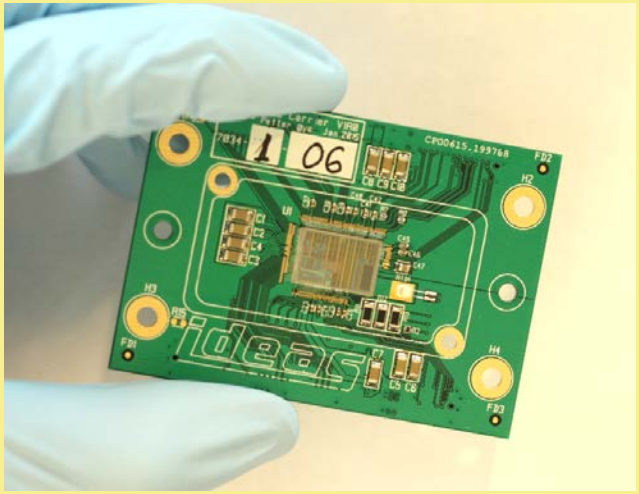
Generation of
32 clocks and
8 control signals



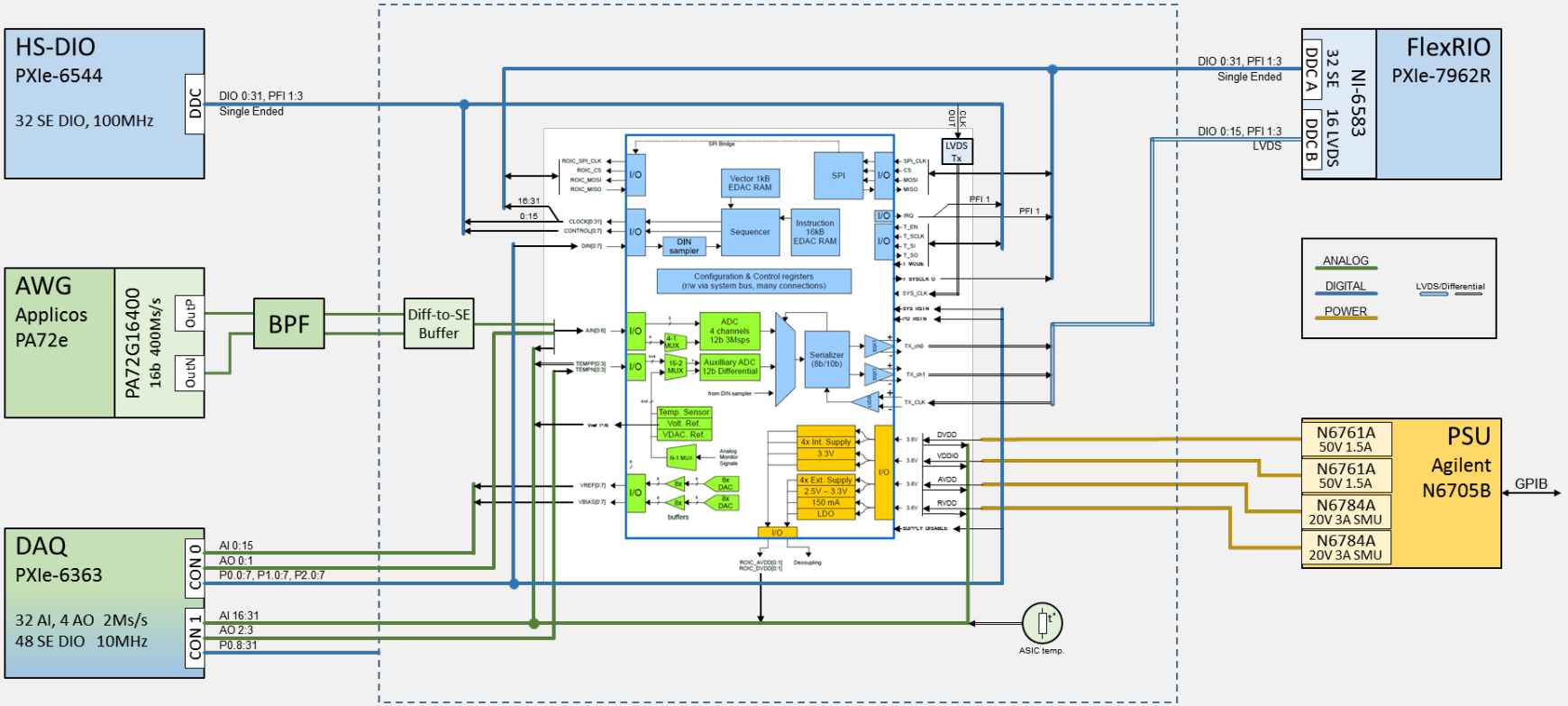
Digital sampler



NIRCA validation



NIRCA validation

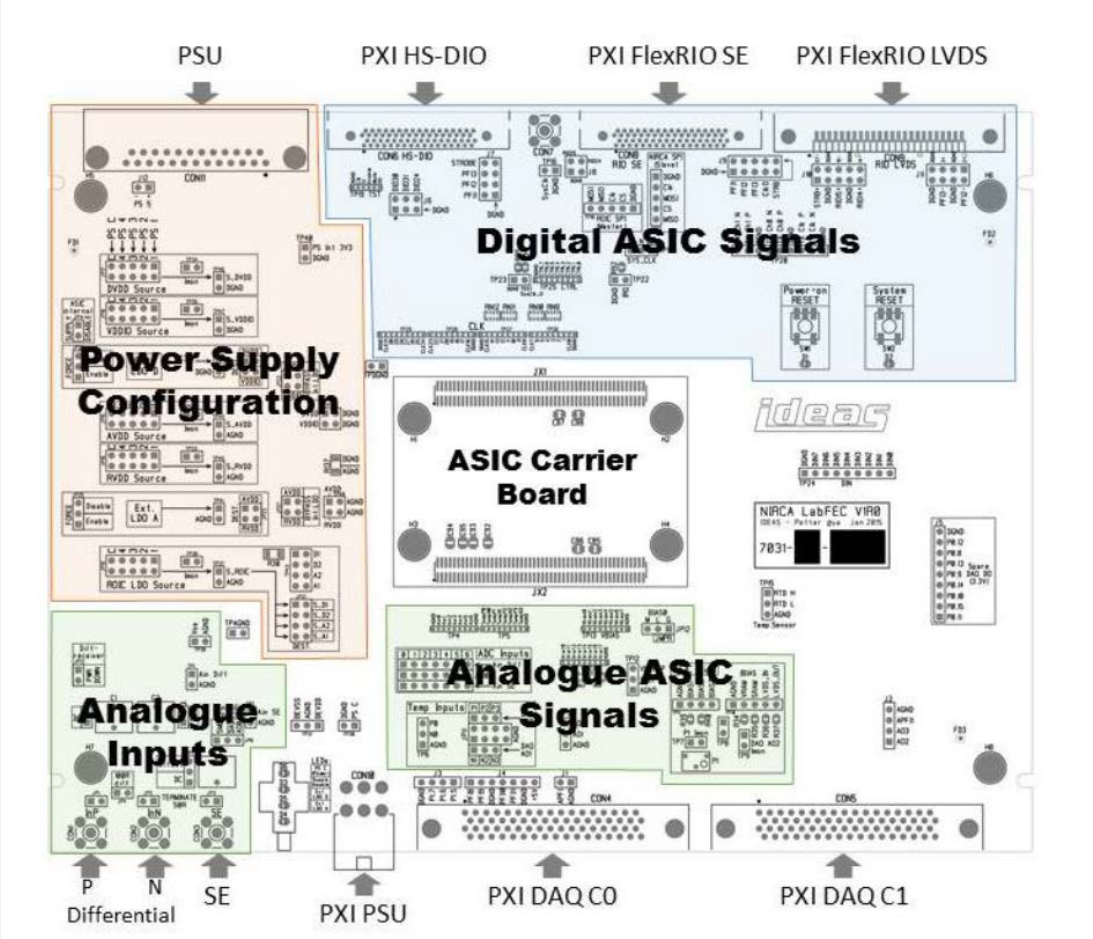


NIRCA validation

Two test-cards

- Interconnection to instruments and signal conditioning (LAB-FEC)
- Interface NIRCA (ACB)

Connectors to a ROIC on the ACB enable testing of the entire IR detection chain.



NIRCA validation

Channel gain and full input scale

- ADC histogram at the output
- Presicion DMM at the input

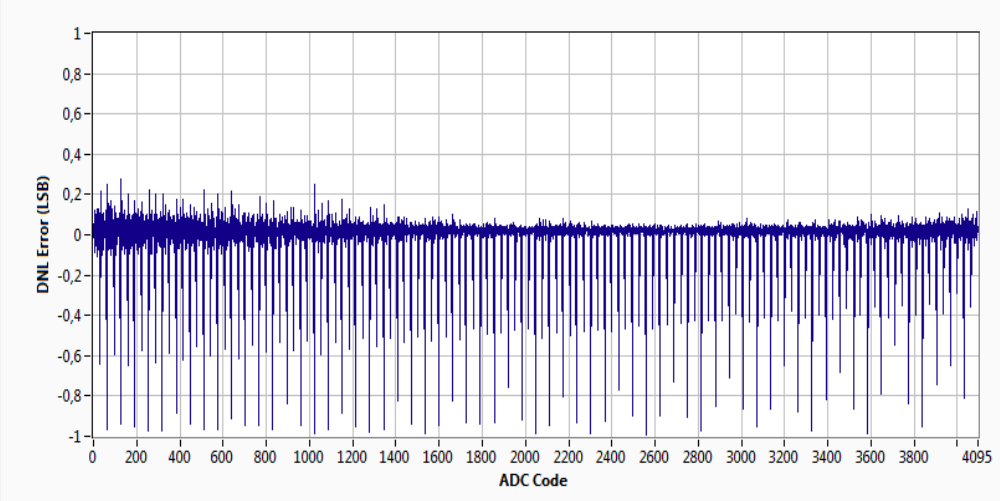
Gain Setting	Measured Gain @ 110 K	Measured Gain @ 300 K	Gain Drift (ppm/K)
1	0,942	0,952	60
2	1,639	1,655	50
4	2,822	2,841	35
8	4,495	4,525	35
16	6,615	6,651	29

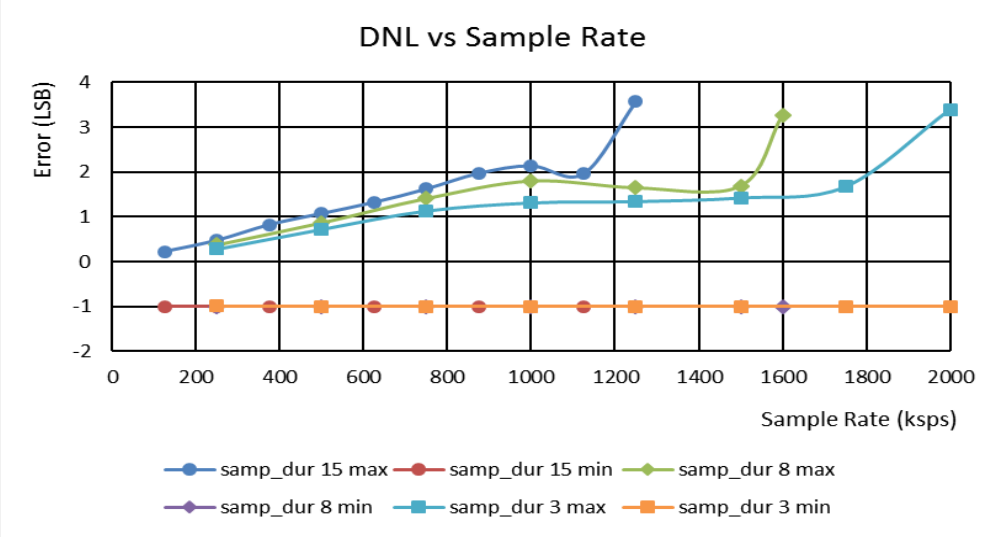
NIRCA validation

Preamp and ADC

Upper plot:
DNL vs. ADC code
at low sample rate

Lower plot:
Max DNL vs sample rate.
Parameter is the duration of the ADC sampling phase.
("max" and "min" refer to positive and negative errors)





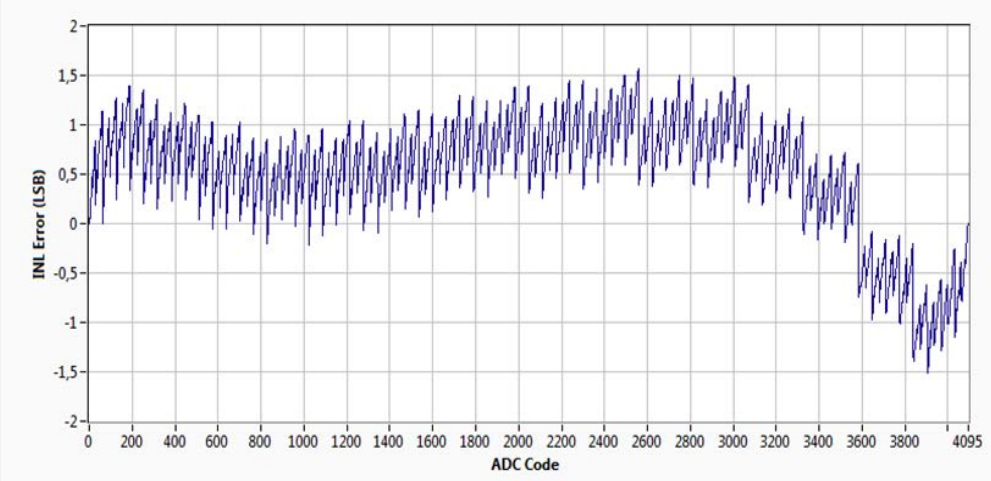
NIRCA validation

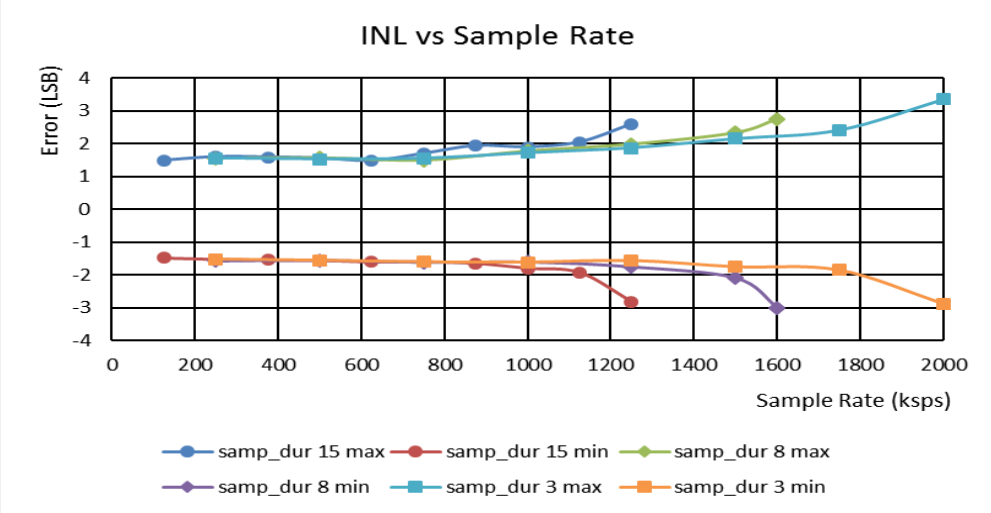
Preamp and ADC

Upper plot:
INL vs. ADC code at low sampling rate.

Lower plot:
Max INL vs sample rate.
Parameter is the duration of the ADC sampling phase.

3.5 LSB is < 0.1 % of full scale





NIRCA validation

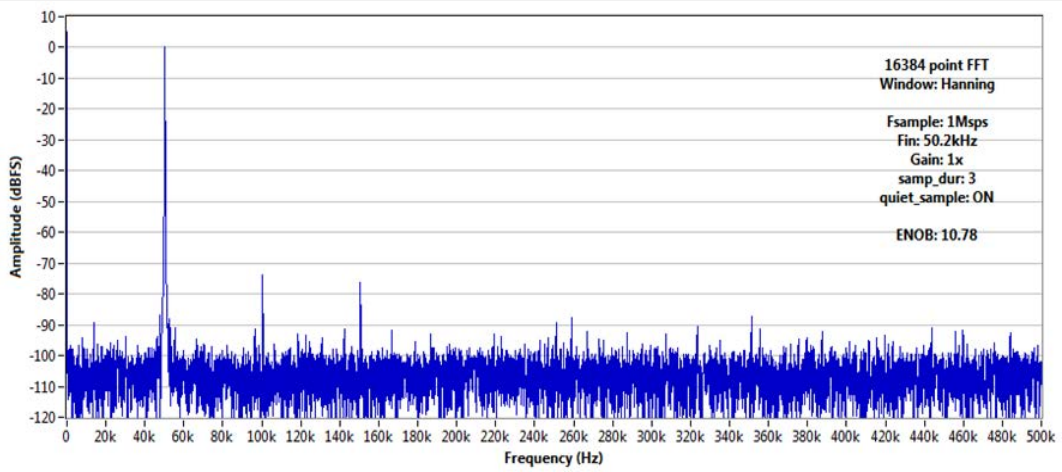
Preamp and ADC

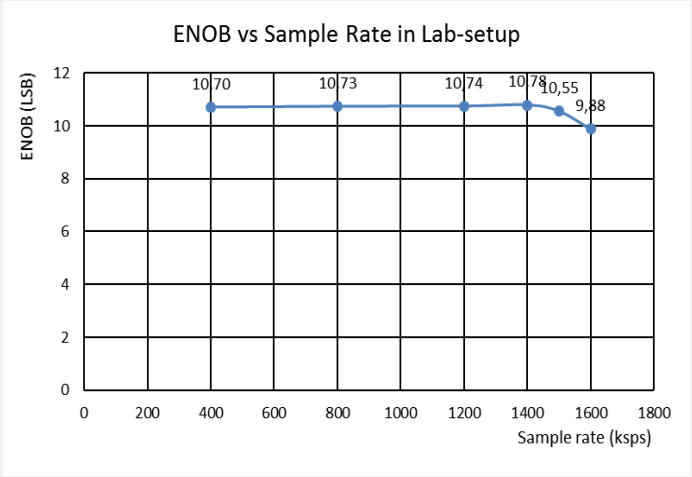
Frequency response

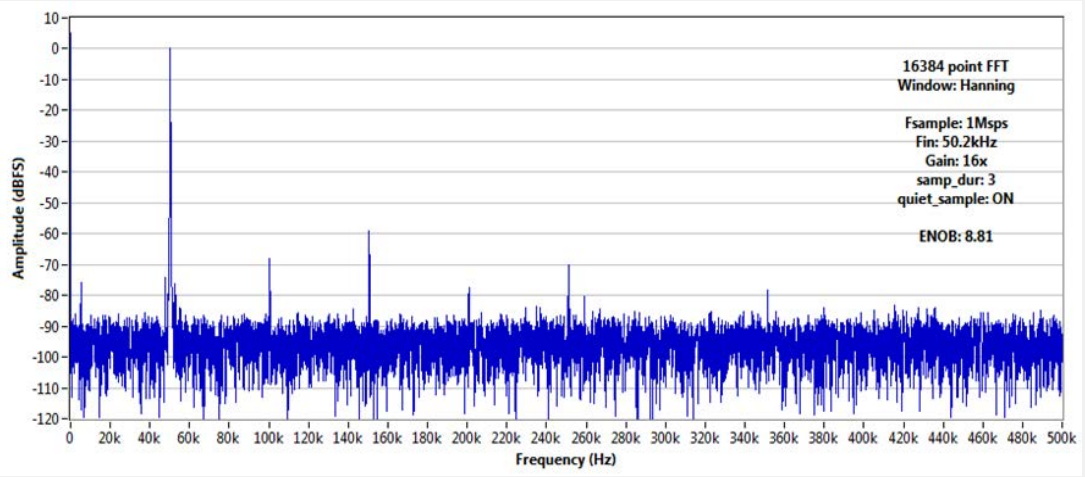
Gain 1 (top right

Gain 16 (bottom right)

ENOB vs sample rate (below)





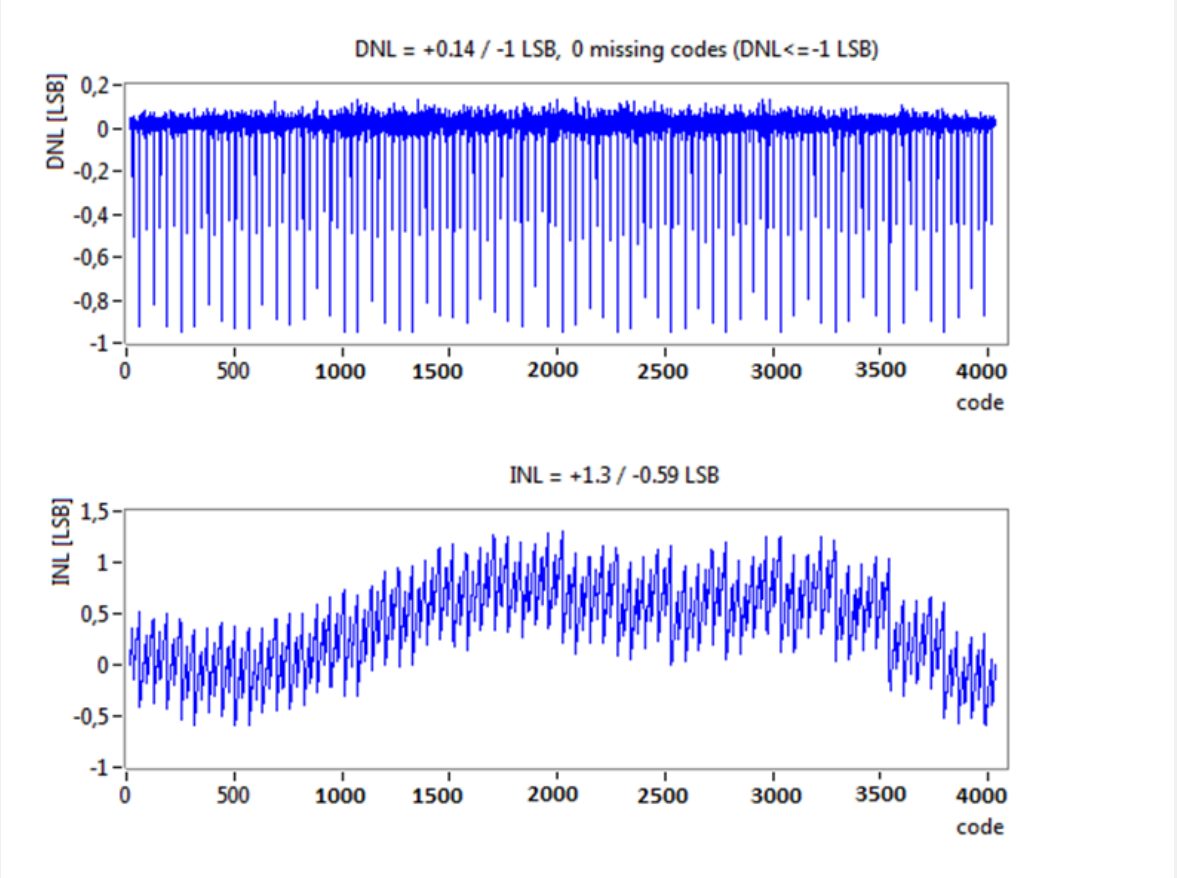


NIRCA validation

ADC results form test vehicle

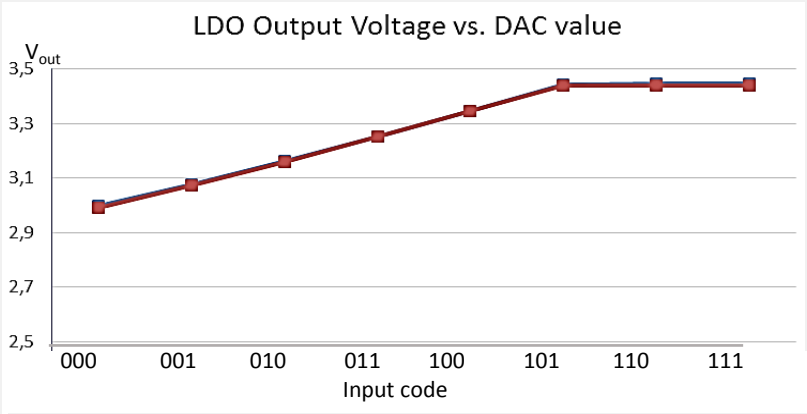
Sample rate: 642 ksps

INL and DNL starts to increase above 1 Msps

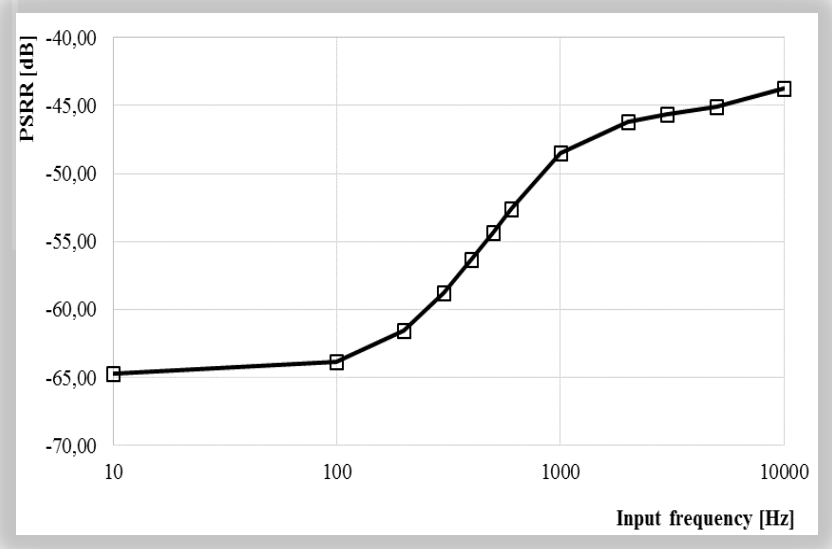


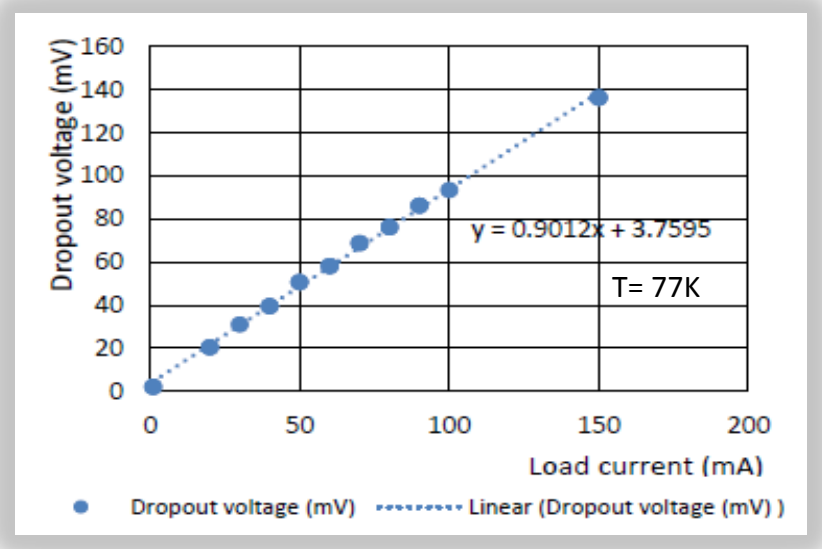
NIRCA validation

3.3 V LDO



Parameter	Value	Unit	Comments
V_{out}	3.0 - 3.45	V	Adjustable
$I_{outmax1}$	> 150	mA	Maximum current drain
R_o @ 300 K R_o @ 77 K	0.14 0.9	Ω	Output resistance
PSRR 0 – 10kHz	> 43	dB	Power supply rippel rejection
V_n	< 100	μV_{rms}	Output noise, [AD03]
$\Delta V_{out}/\Delta I_{out}$	<3	%	Load regulation From I_{out}=15 mA to I_{out}=150 mA,



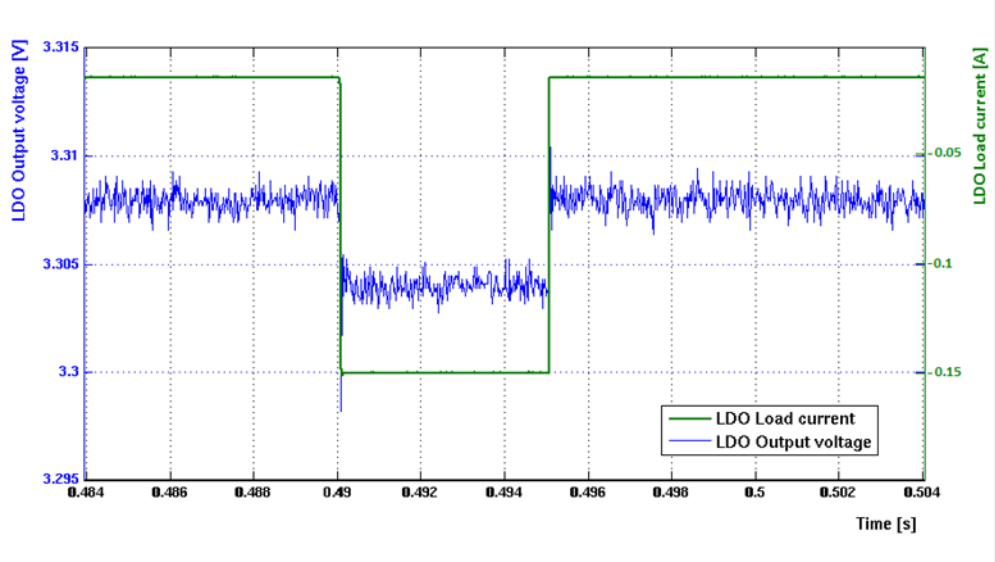


NIRCA validation

The 3.3 V LDO transient response shows a small overshoot, but no ringing.

Green trace: Load current 150 mA step

Blue trace: Resulting 4 mV drop at the LDO output.

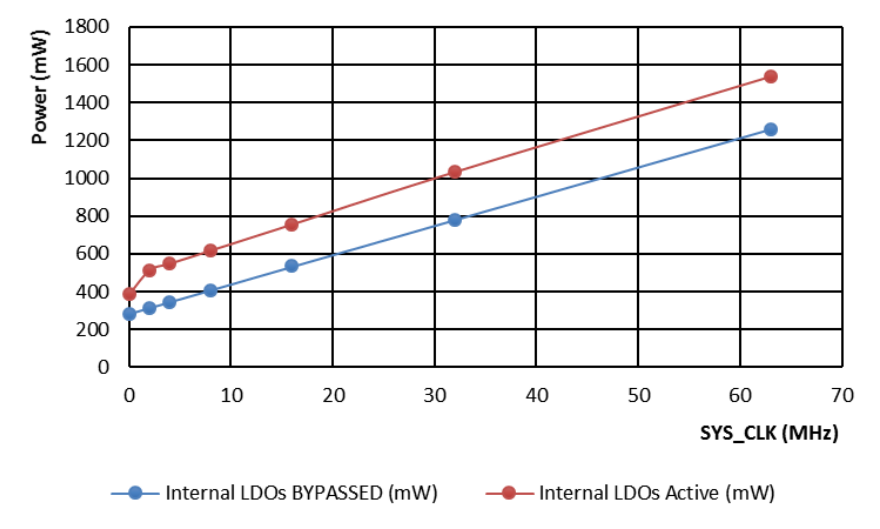


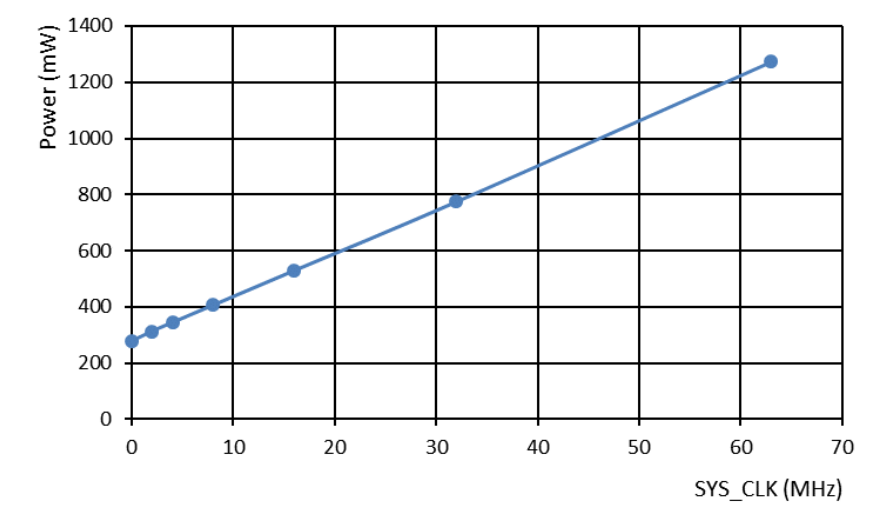
NIRCA Validation

Power dissipation vs. System clock

Top: 30 °C to 35 °C

Bottom: 92 K to 100 K

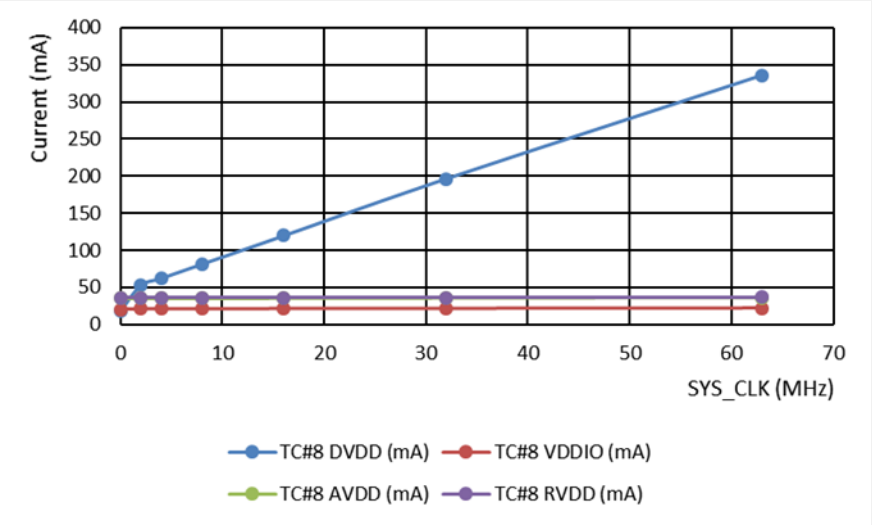


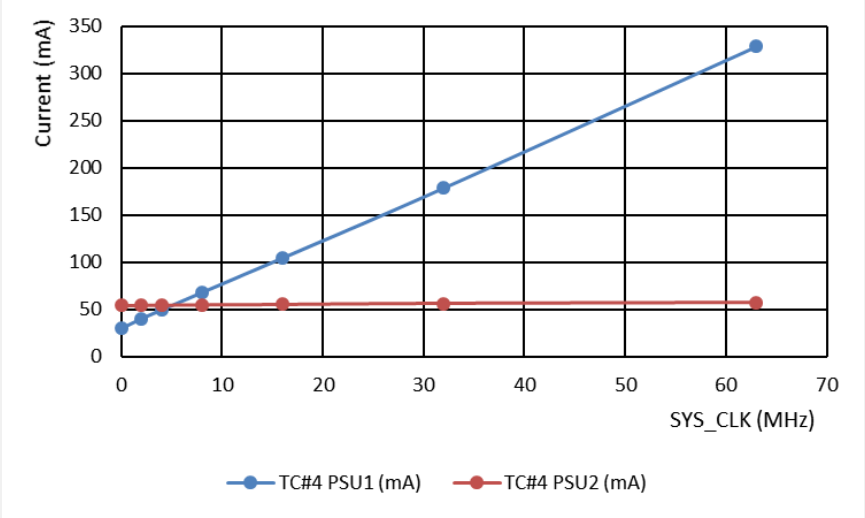


Current drain per power domain

Top: 30 C to 35 C

Bottom: 92 K to 100 K





NIRCA validation

Instruction SRAM tests

Algorithm	# R/W	SYS_CLK	DVDD	VDDIO	Value, Lab	Value, Cryo (Room)	Value, Cryo (77°K)
Random	10000	40 MHz	3.4 V	3.4 V	*N/A*	PASS	*N/A*
Random	10000	40 MHz	3.35 V	3.35 V	*N/A*	FAIL	*N/A*
Random	10000	40 MHz	3.35 V	3.3V	PASS	*N/A*	*N/A*
Random	10000	40 MHz	3.3 V	3.3 V	FAIL	FAIL	FAIL
Random	10000	40 MHz	3.25 V	3.25 V	*N/A*	*N/A*	PASS

300 K

DVDD [V]	10	15	20	25	30	35	40	45	50	55	60	65	70
3,6	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,55	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,5	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,45	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,4	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,35	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,3	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,25	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,2	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,15	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,1	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3,05	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
3	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL
2,95													
2,9													
2,85													
2,8													
2,75													
2,7													

SYS_CLK

77 K

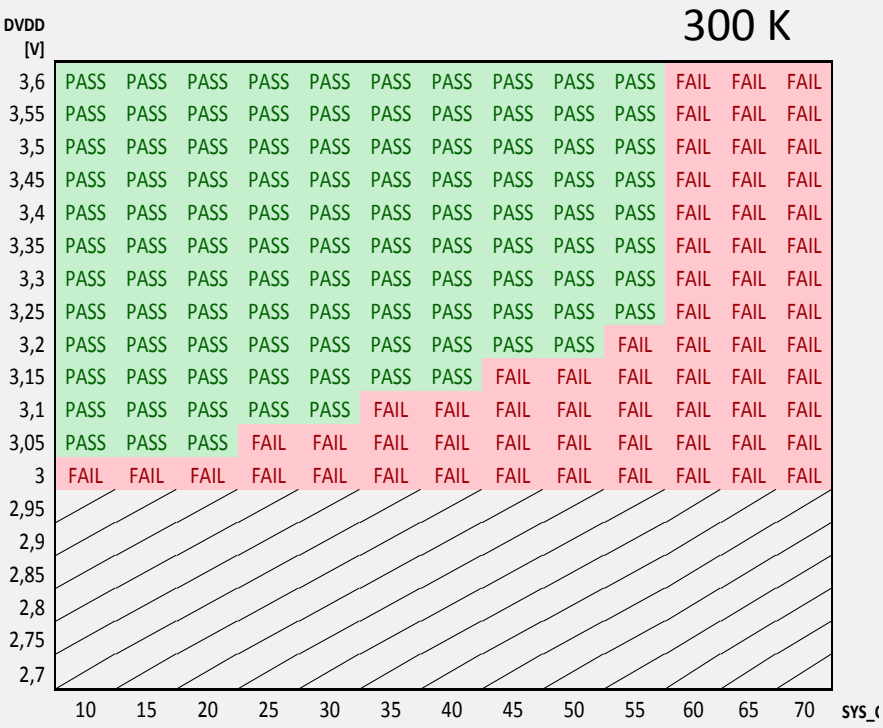
DVDD [V]	10	15	20	25	30	35	40	45	50	55	60	65	70
3,6													
3,55													
3,5													
3,45													
3,4													
3,35	PASS	PASS	PASS	PASS	FAIL	FAIL	FAIL	PASS	FAIL	FAIL	FAIL		
3,3	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL		
3,25	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL		
3,2	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL		
3,15	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL		
3,1	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL		
3,05	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	FAIL		
3	FAIL	FAIL	FAIL	FAIL	PASS	PASS	FAIL	FAIL	FAIL	FAIL	FAIL		
2,95	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL		
2,9	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL		
2,85	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL		
2,8	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL		
2,75	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL		
2,7	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL	FAIL		

SYS_ [MH

NIRCA validation

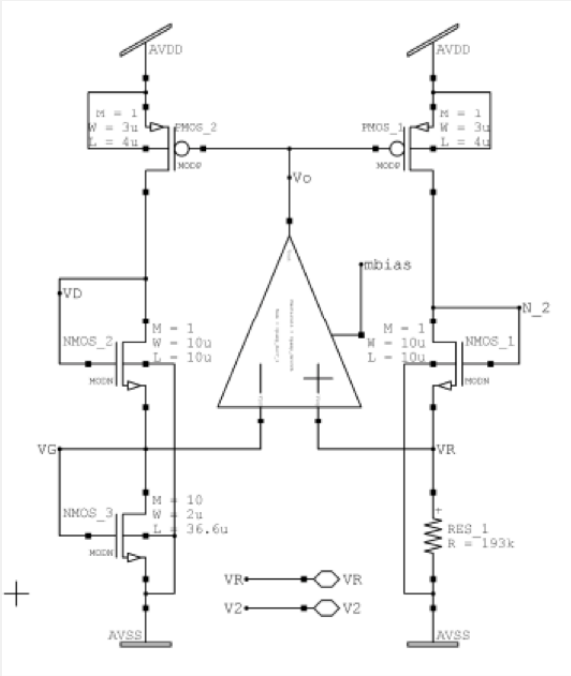
Vector SRAM tests

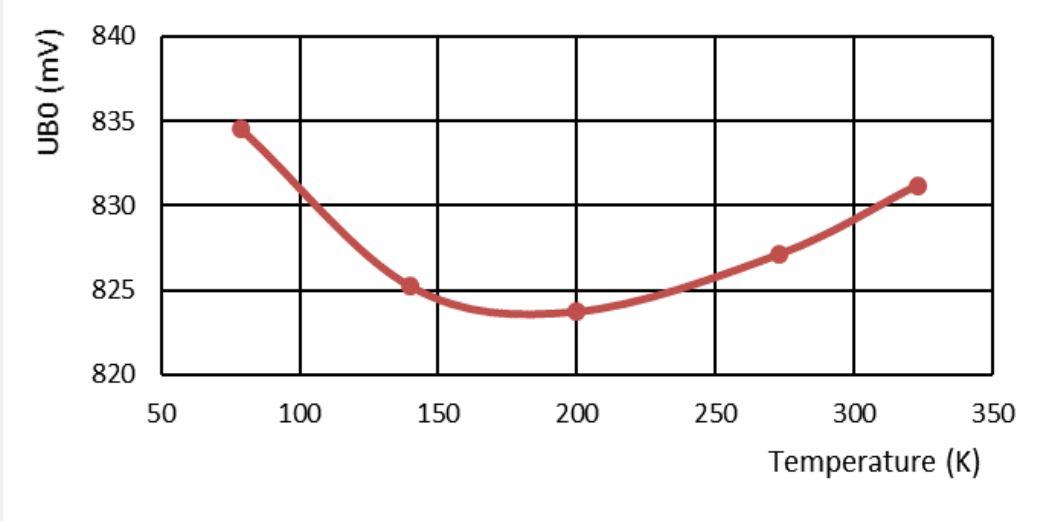
Algorithm	# R/W	SYS_CLK	DVDD	VDDIO	Value, LAB	Value, CRYO (Room)	Value, CRYO (77°K)
Random	10000	40 MHz	3.3 V	3.3 V	PASS	PASS	FAIL
Random	10000	40 MHz	3.25 V	3.25 V	*N/A*	*N/A*	PASS



NIRCA validation

Internal reference voltage vs temperature for R_{REF} 18kΩ

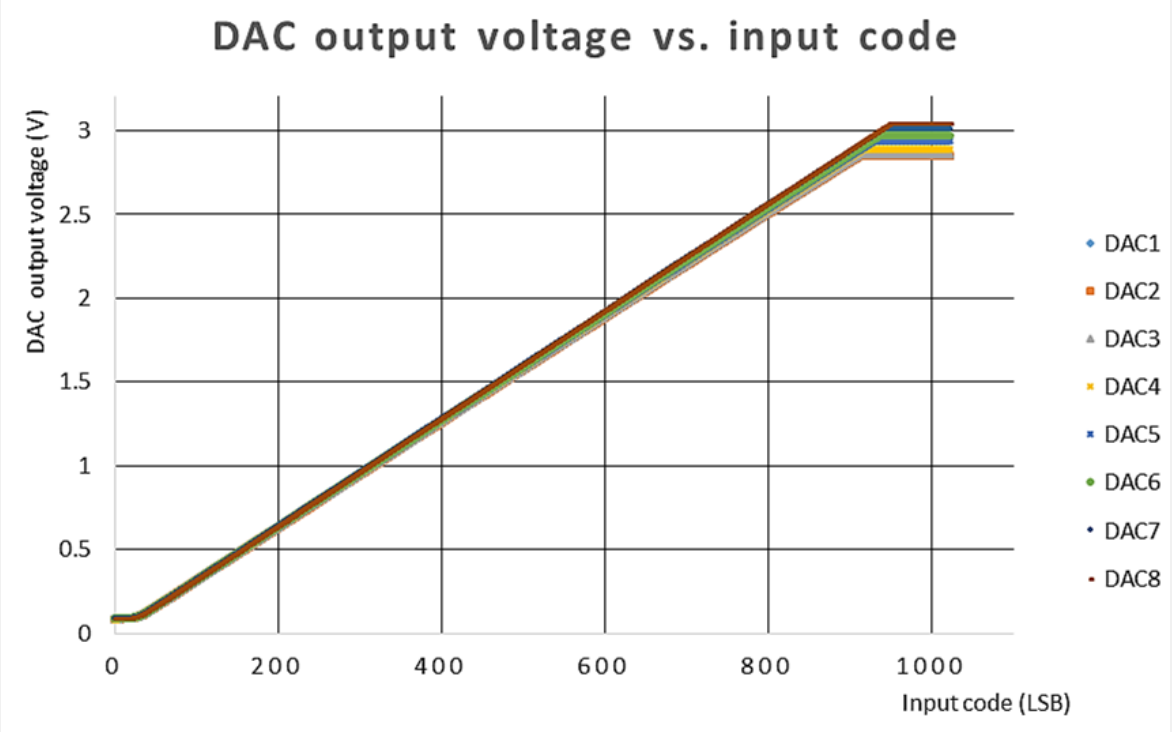




NIRCA validation

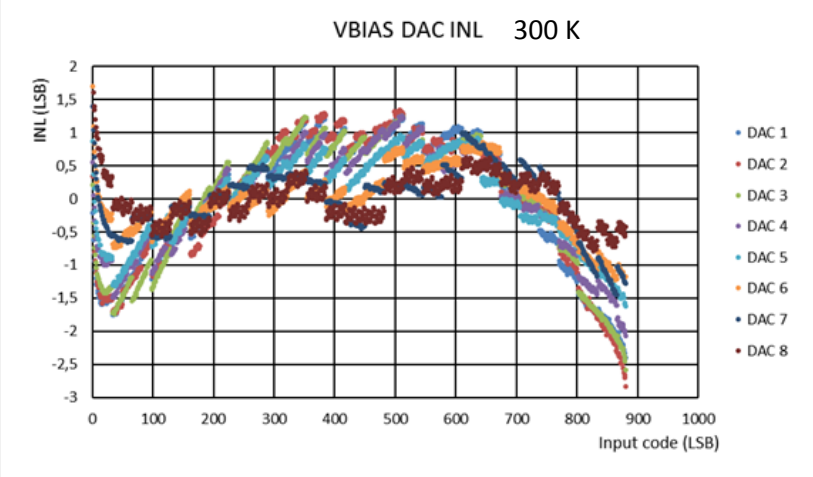
Bias voltages

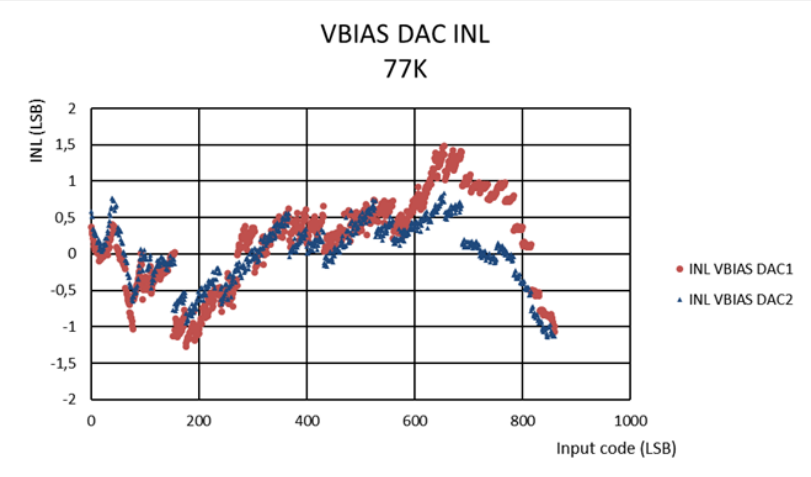
Comments
Range less than 3 V / 1024

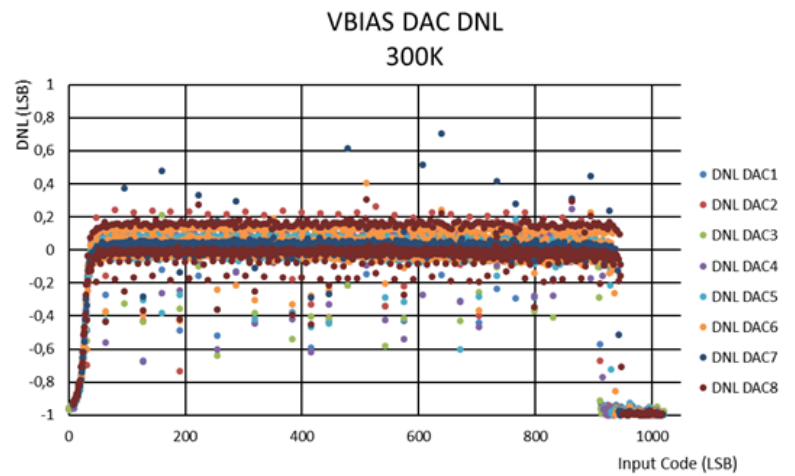


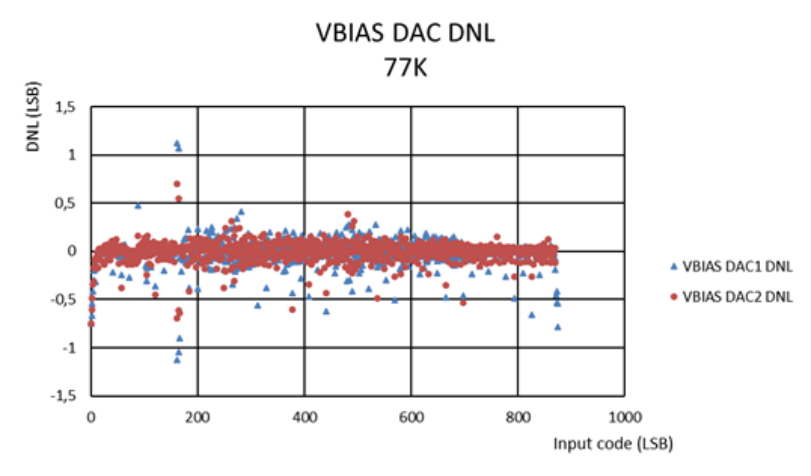
NIRCA validation

Bias Voltages





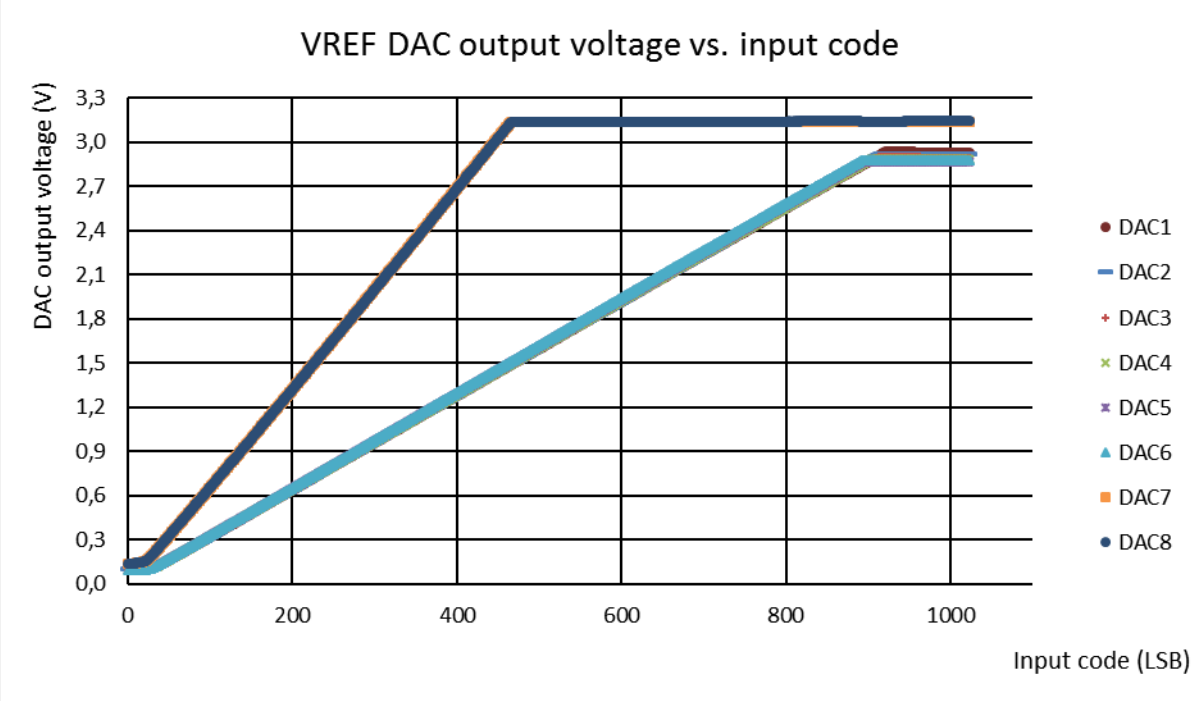




NIRCA validation

Reference voltages

DAC 7 and 8 have about 2x gain

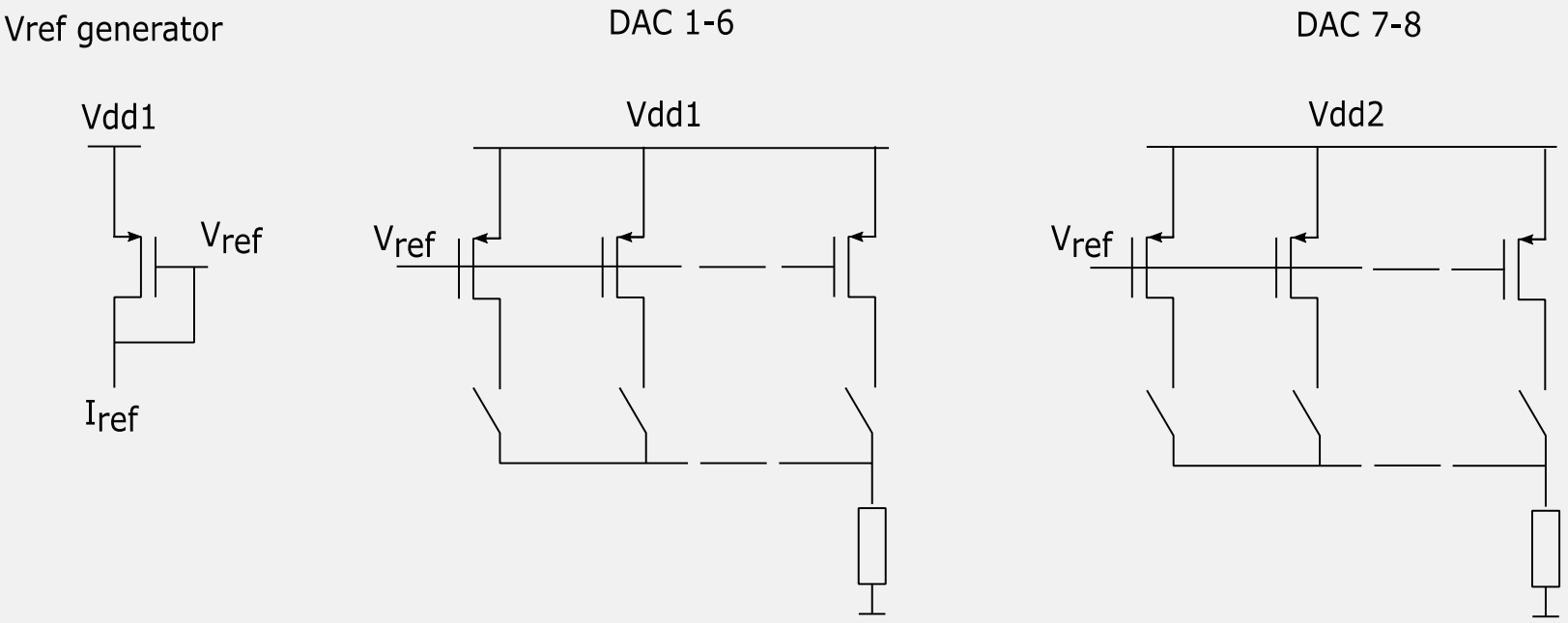


NIRCA validation

Missing power routing to 6 out of 8 reference modules (DAC and buffer), and the Vref generator creates IR drop for these.

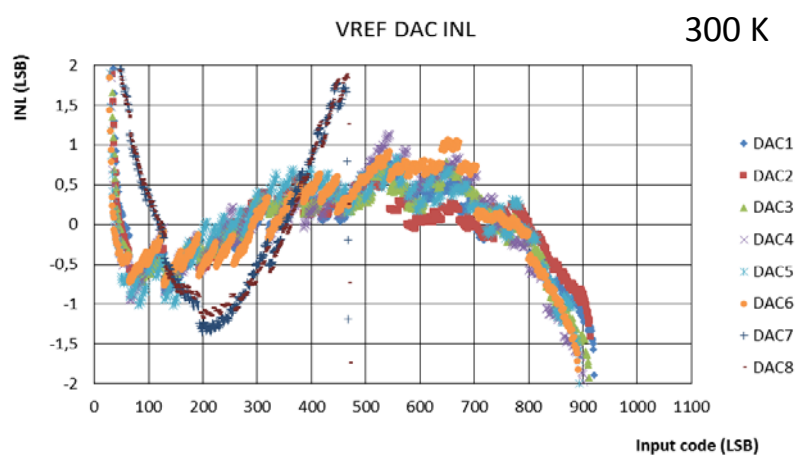
2 of the modules get higher VDD than the Vref generator and higher current which reach max output with a low input code.

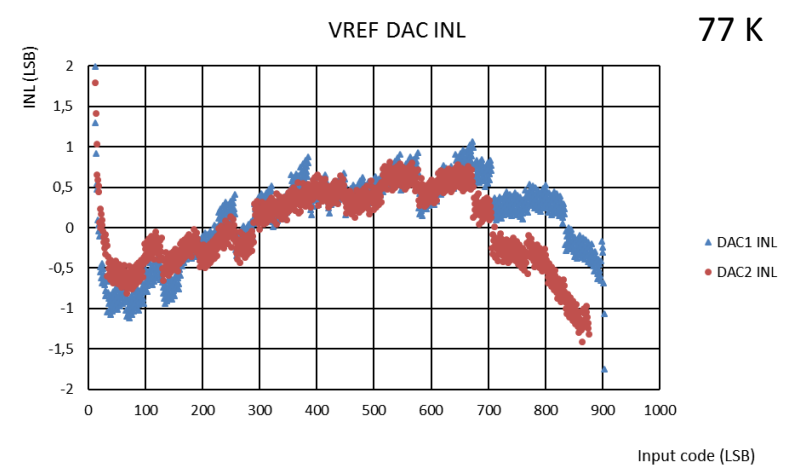
The 6 get VDD via guard ring - the missing power was therefore not detected by LVS.

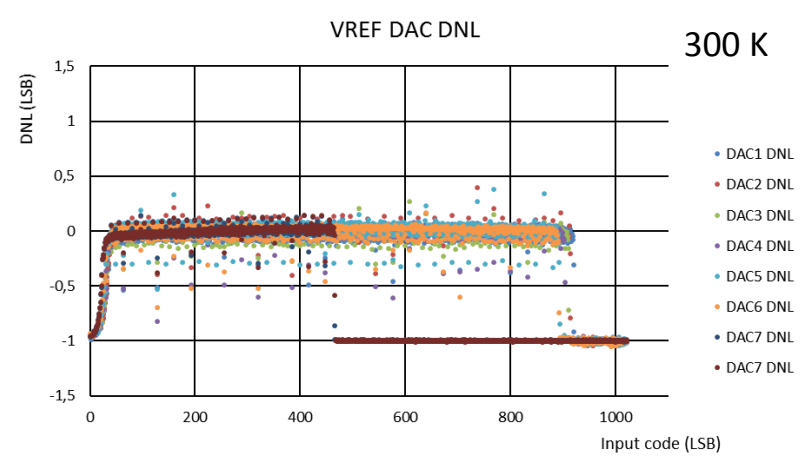


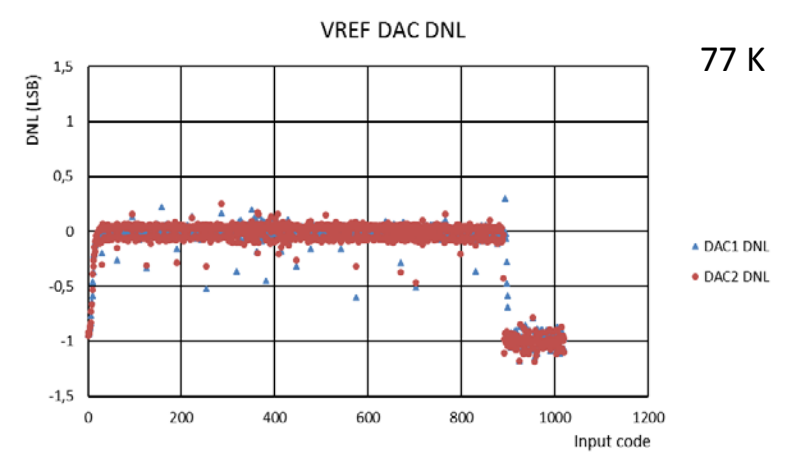
NIRCA validation

Refrence votages
INL and DNL at 300 K and 77 K









NIRCA validation

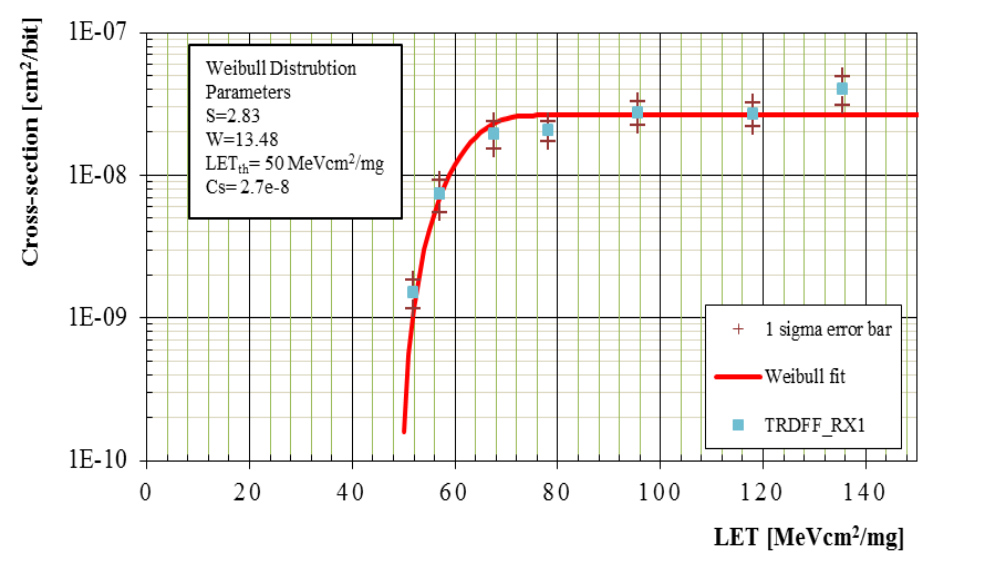
Radiation tests

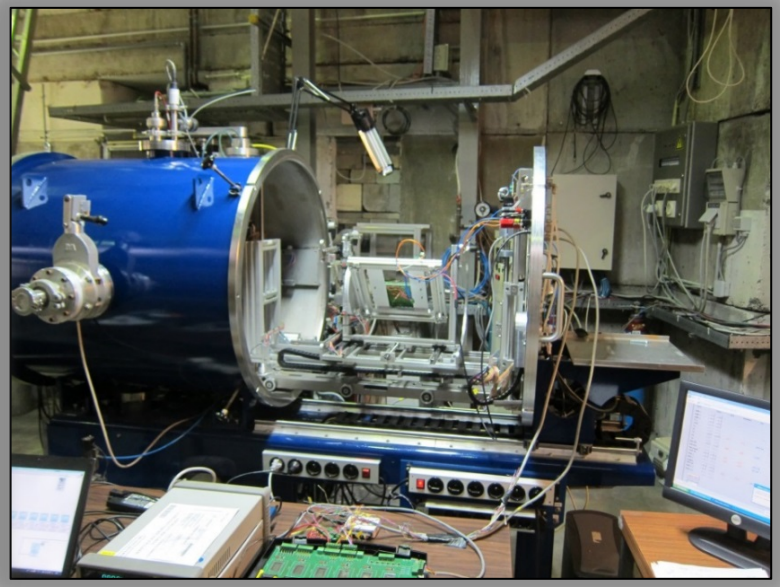
Triple modular redundancy (TMR) data Flip-Flops (DFF) on test vehicle 200 bit shift registers.

Radiation tolerance
SEL LET_{th} > 135 $MeVcm^2/mg$
SEU LET_{th} 50 $MeVcm^2/mg$

Operating temperature
-196°C to +50°C

HIF beam at Universitè Catholique de Louvain





NIRCA validation

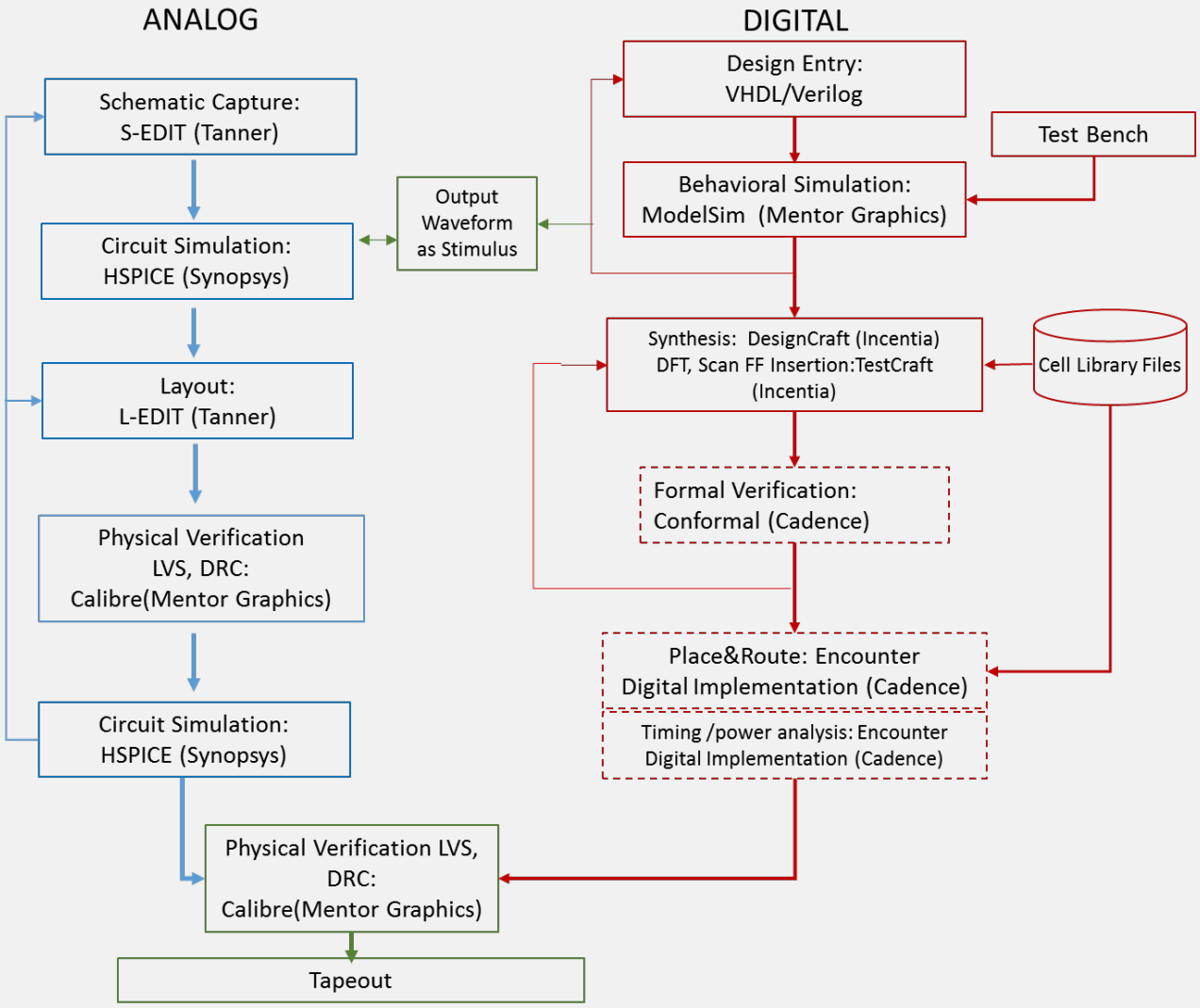
Non-compliances

- 2 of the 8 Bias voltage has limited code range
  - Missing power routing, “powered” via latch-up guard rings.
- Channel gain lower than expected
  - Parasitic capacitance and low loop gain in preamplifier.
- ADC DNL 1 bit
  - Caused by a parasitic capacitance connected to the 7^{th} bit.
- 1.8 V regulator outputs rises to input voltage (3.6 V) in reset state
  - Missing clamp on output transistor gate.
- Internal regulator cannot power the digital core running at clock rates above 25MHz
  - New rate specs was not followed by updated regulator specs.
- Low digital power tolerances
  - Tight voltage adjustments compensates for small time margins during RAM read.

Design flow

Design flow

ASIC design flow
Used for NIRCA



Design flow

Analogue Design

- Tanner EDA S-Edit v16.2 for schematic design : Good
- Synopsys Hspice for simulation: Good
- Tanner EDA L-Edit v16.2 for manual layout: Good
- Tanner HiPer DRC LVS v16.2 for verification: OK, but too slow for full chip verification.
- Tanner HiPer PX v 16.2 for parasitic extraction: Did not work with AMS 0.35

Modelling

- NanGate Library Characterizer for standard cell characterization: Good

Digital simulation

- Mentor ModelSim DE 10.1 d for functional verification: Good

Synthesis

- Incentia DesignCraft for synthesis including DFT: OK, but likely not with the best result.
  T wo critical bugs, quick response fixed these bugs.

Place & route, and verification

- Tanner EDA Place and Route: Not Good, but could be used on small modules. Caused delay.

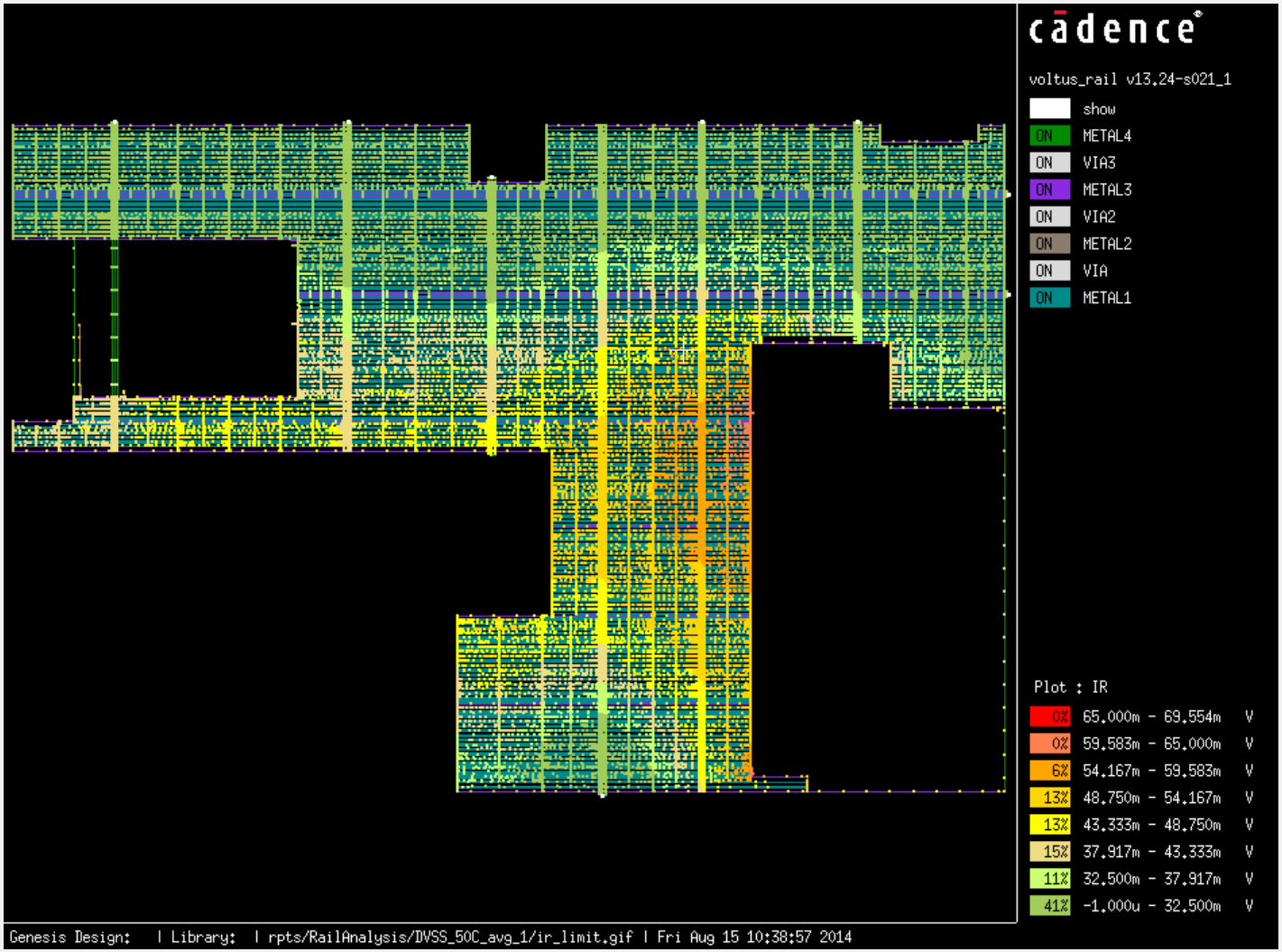
We sub-contracted the P&R and post-layout verification of the digital core.
The subcontractor used Cadence Encounter EDI for P&R, and Conformal for Equivalence checking.

- Mentor Calibre DRC, LVS: Very efficient and easy to use.

PCB Design

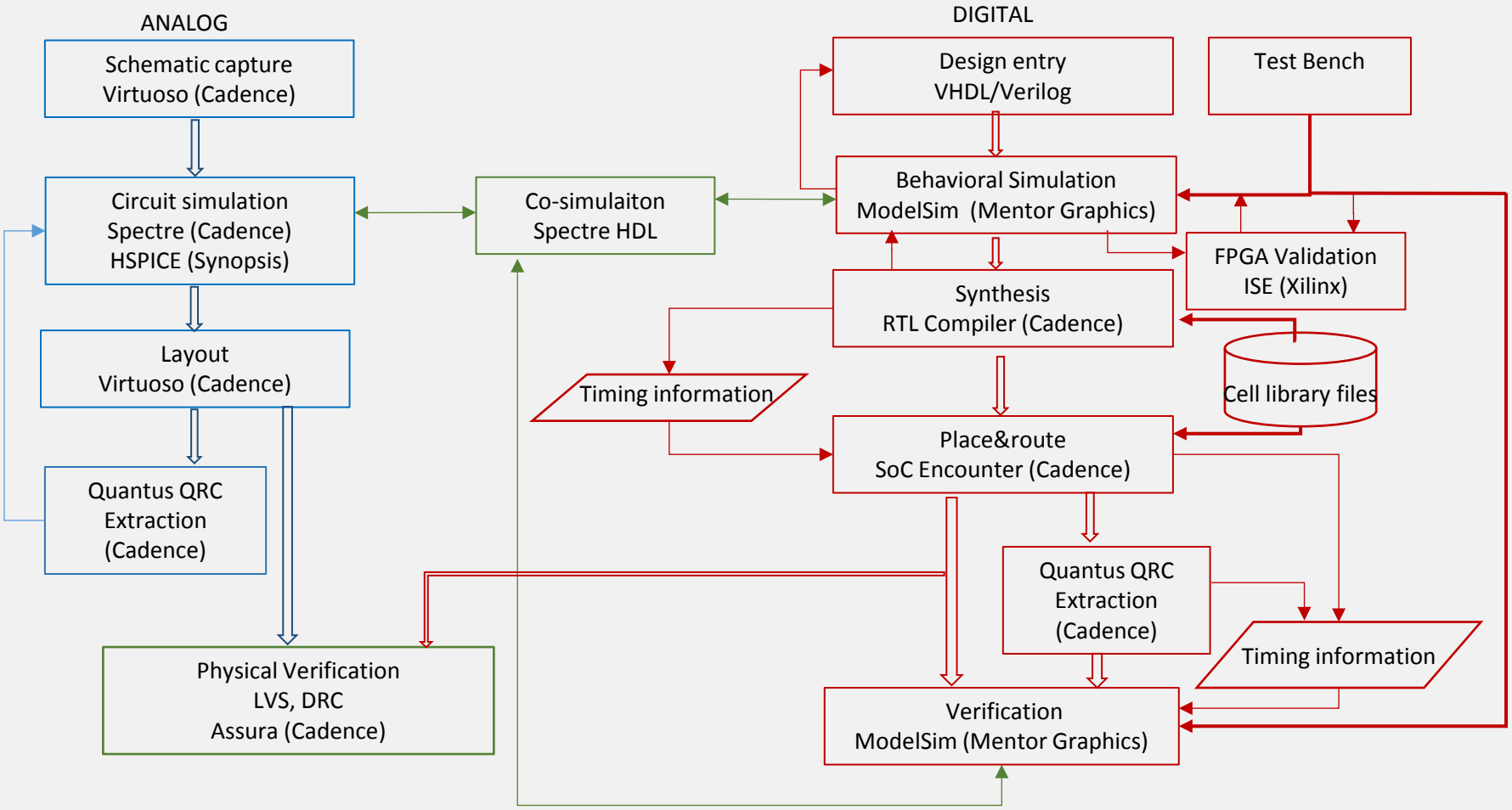
- Zuken Cadstar EDA for board level design: Good

Design flow


cadence
voltus_rail v13.24-s021_1
show
ON METAL4
ON VIA3
ON METAL3
ON VIA2
ON METAL2
ON VIA
ON METAL1
Plot : IR
0% 65.000m - 69.554m V
0% 59.583m - 65.000m V
6% 54.167m - 59.583m V
13% 48.750m - 54.167m V
13% 43.333m - 48.750m V
15% 37.917m - 43.333m V
11% 32.500m - 37.917m V
41% -1.000u - 32.500m V
Genesis Design: | Library: | rpts/RailAnalysis/DVSS_50C_avg_1/ir_limit.gif | Fri Aug 15 10:38:57 2014

Design Flow

New ASIC design flow



Technology

ASIC manufacturer:
Austria Microsystems (**AMS**), AG located at Tobelbader Strasse 30 , A-8141 Unterpremstaetten, Austria

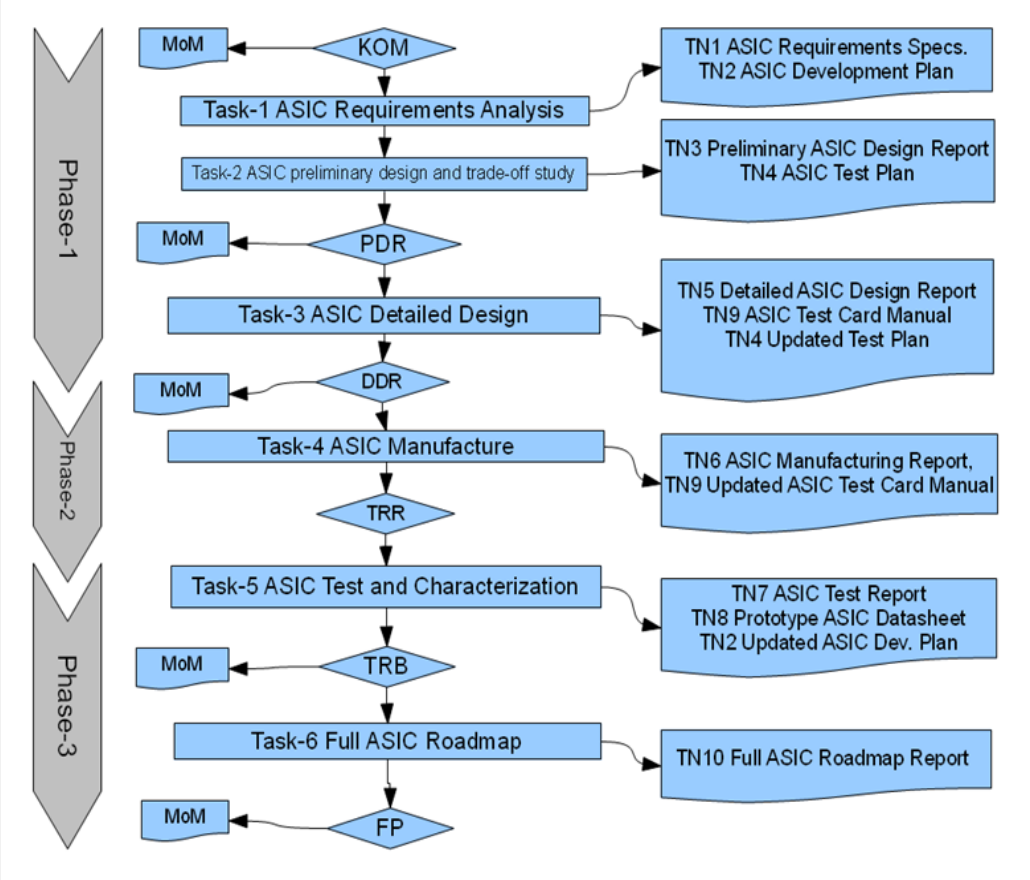
Process:
C35 B4O1 **0.35µm** process at Austria Microsystems, AG.

- Our experienced very good support with regard to design documents.
- Flexibility regarding process options.
- The lead time is guaranteed to 8 week,
  we received the chips after 7 weeks.

Project progress

Project progress

Milestones



Project progress

Milestone	Planned	Achieved
Kick off	01.03.2013	01.03.2013
Preliminary design review (PDR)	29.09.2013	27.09.2013
Detailed design review (DDR)	20.01.2014	25.03.2014
Test readiness review (TRR)	16.06.2014	16.04.2015
Tape out review (TOR)		16.06.2014
Test review board (TRB)	01.09.2014	07.10.2015
Final presentation (FP)	01.11.2014	04.12.2015 (Planned)

Full ASIC roadmap

Phase 3

Full ASIC roadmap

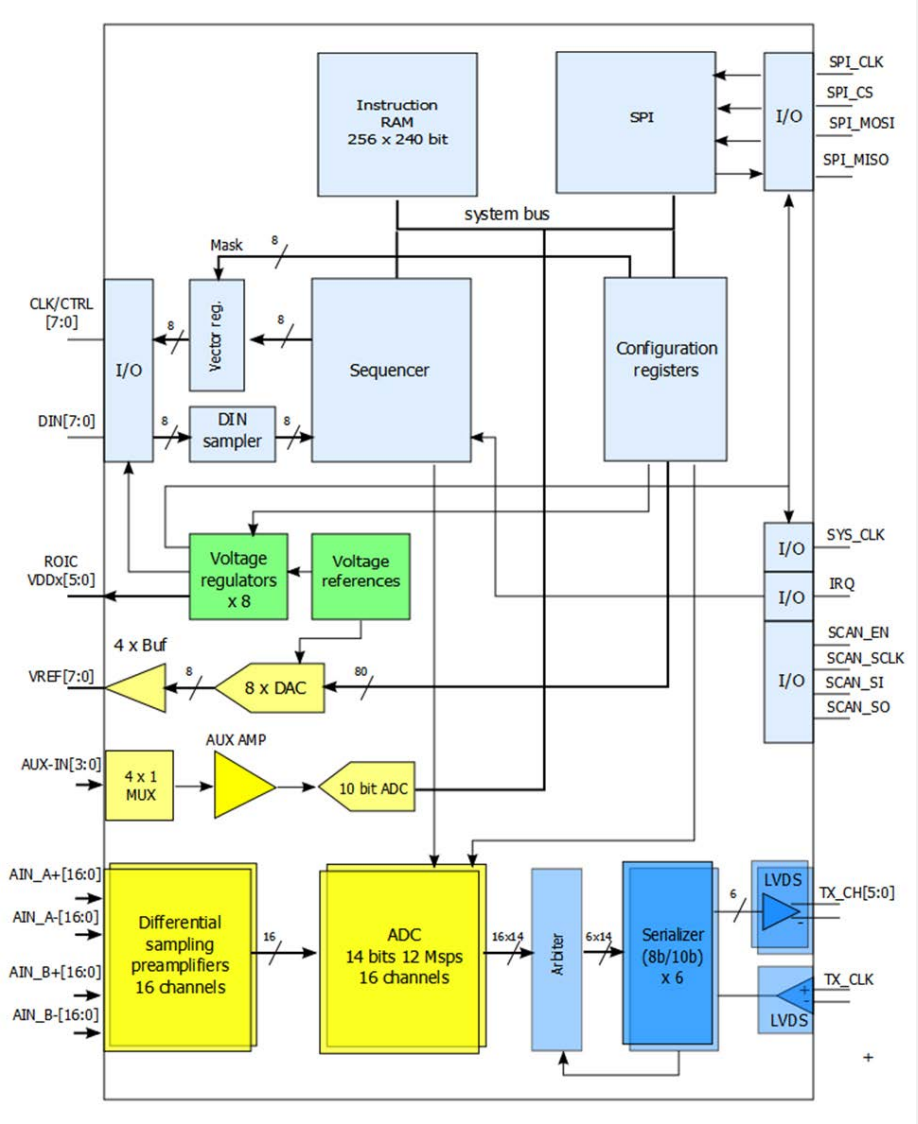
	Sofradir NGP	Sofradir Jupiter MW	Selex ME930 ROIC	CEA LETI CL103 ROIC	ESA AO8295 NIR/SWIR
Number of pixels	1024*1024	1280*1024	2056*2048	648*520	2048*2048
Nominal readout rate	30Hz	120 Hz	30FPS?	2.5 Hz	40FPS
Number of video channels	4/8 Pseudo-diff.	4/8	16/32	8	32
Required sampling speed	8Msps	20Msps	8Msps/4Msps		6Msps
Datarate (bit/s) per output	1.10E+08	5.51E+08	1.11E+08		7.34E+07
Datarate (bit/s) total	4.40E+08	2.20E+09	1.77E+09		2.35E+09
Num. of required control signals	5	?	4+SPI	13	
Number of digital output signals (from ROIC to ASIC)	3	?	4	?	
Number of references/biases required (to ROIC)	5	?	1	15+6	<24
Digital signal voltage	VIL: 0V VIH: 2.75V	?	VIL: 0V VIH: 3.3V VOL:0.4V VOH: 2.65V	VIL: 0V VIH: 1.8V	
Supply voltages	VSS: 0V VDD[1-3]: 2.75V VREF: 1V VAB: 2.75V	?	VDD[1-4]: 3.3V	AVDD: 3.3V VDD_IO: 3.8V DVDD: 1.8V	

A question mark indicate that the information is not available to IDEAS.

Full ASIC roadmap

Proposed architecture

- Samplings rate: 12 Msps
- 16 channels:
  16 differential inputs
  at full rate
- 2:1 input mux:
  32 differential inputs
  at ½ rate
- ADC resolution: 14 bits
- Analogue reference
  outputs: 8
- Power outputs: 6
- Digital inputs: 8
- Digital control signals and
  clocks: 8
- 6 high speed data channels
- SPI control interface



Full ASIC roadmap

High speed data channels to be considered.

NIRCA-V2 requires 2.4 Gbps in total
(2k x 2k, 30 fps, 16 acquisition channels, 8 Msps)

Propose 6 TX channels at 400 Msps

For further discussions

- 8b/10b encoding
- SpaceWire
- SpaceFibre

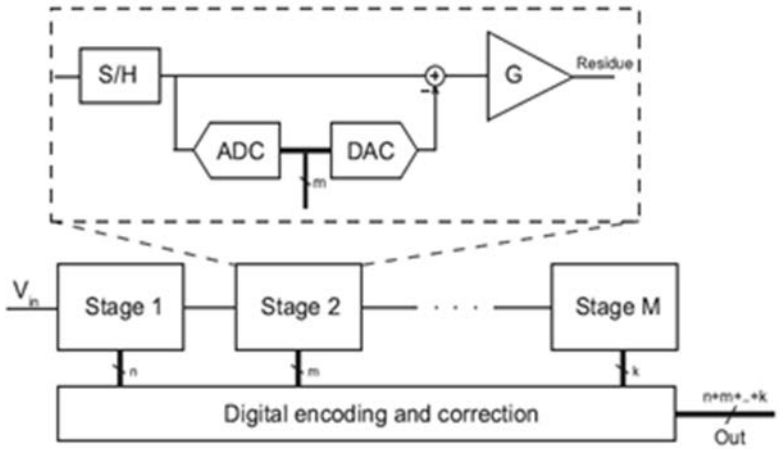
SPI interface

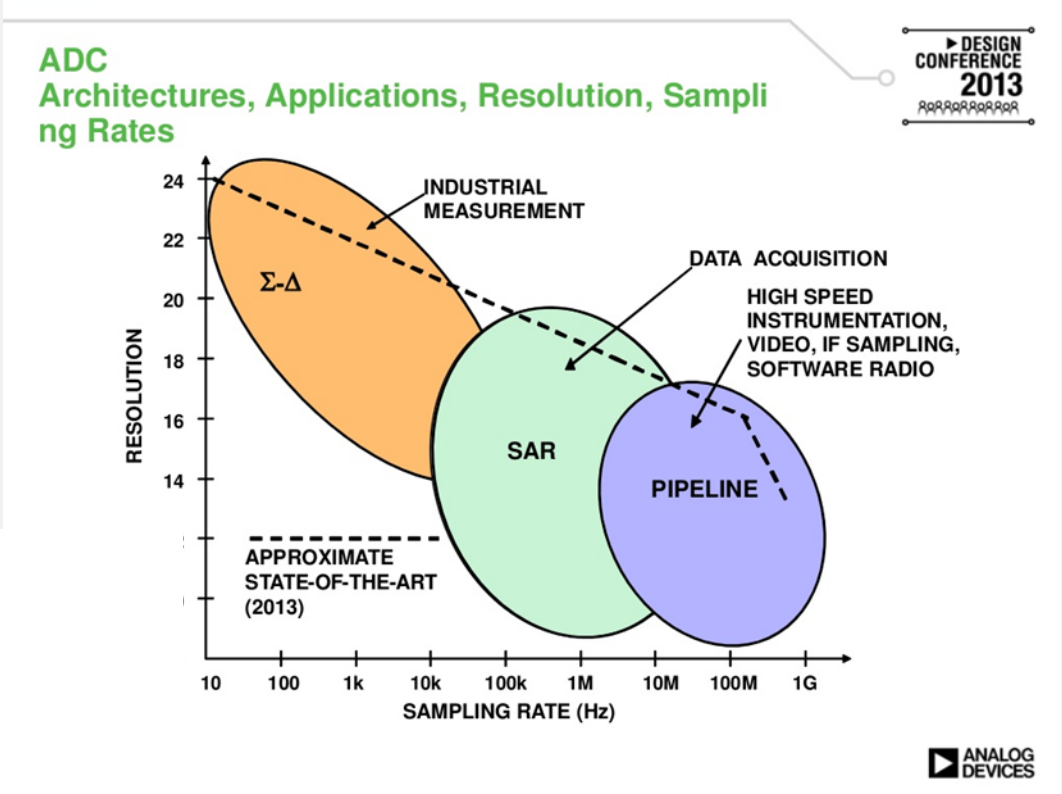
SPI is not required if SpaceWire of SpaceFibre is selected (2-way)

Might want to implement an SPI bridge to ROIC.

Full ASIC roadmap

Pipe line ADC principle





Full ASIC roadmap

Other input to specifications

Band gap reference

Well defined temperature voltage reference.

Absolute temperature .

Internal PLL ?

TX-clock provided by the ASIC requires a PLL (upscaling system clock). Radiation tolerance is maybe relaxed due to the communication system EDAC algorithms.

Control signal and fine tuning ?

Delay line made from a chain of inverters can provide fine tuning of the clock phases during readout of i.e. CCDs.

Thank you for your attention

BACK-UP

Voltage references and Biases