Contract 4200022947/10/NL/CP Near Infrared Large Format Sensor Array

Final Presentation Meeting

European Space Agency

3 November 2010

QinetiQ

© Copyright QinetiQ Limited 2010

Agenda

Introductions

Progress on Actions

Contractual Matters

Review of Technical Progress

- WP1 Detector Requirements Analysis
- WP2 Test Plan Development
- WP3 MCT Material Demonstration
- WP4 Thinning Development

Review of Deliverables

Review of Project Plan

Risks

Any Other Business

Summarise Actions and Decisions

Approval and Sign-off of Minutes

© Copyright QinetiQ Limited 2010

Update on Emerging Technologies Future

QinetiQ is still exploring opportunities for some or all of the capabilities of the Emerging Technologies Group to continue in some other form

Bids have been received formally and are being reviewed

The consultation period is due to complete on 18 November

It is probable that work on this and other projects can continue until then subject to facilities remaining in place and operational

QinetiQ

© Copyright QinetiQ Limited 2010

Actions from Review Meeting – 22 September 2010

No	Action	Action on	Target Date	Status
3.1	Contact ESA Contracts Officer to notify change of PM.	QinetiQ (JB)	30/09/10	Complete
3.2	Contact ESTEC about the advance payment	QinetiQ (JB)	30/09/10	Complete

QinetiQ

© Copyright QinetiQ Limited 2010

Review of Technical Progress

WP1 – Detector Requirements Analysis

WP2 – Test Plan Development

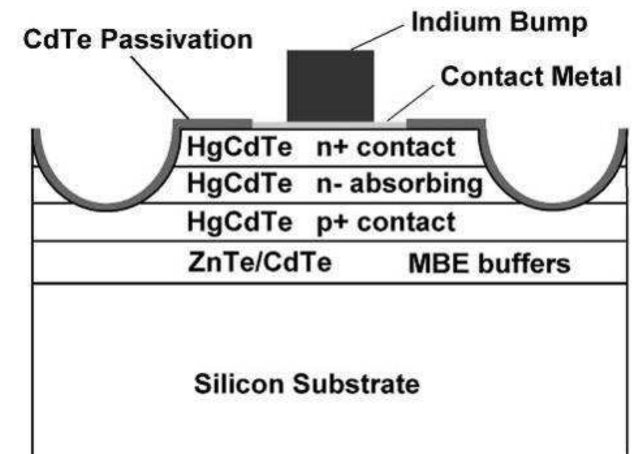
WP3 – MCT Material Demonstration

WP4 – Thinning Development

© Copyright QinetiQ Limited 2010

Technical Progress - Introduction

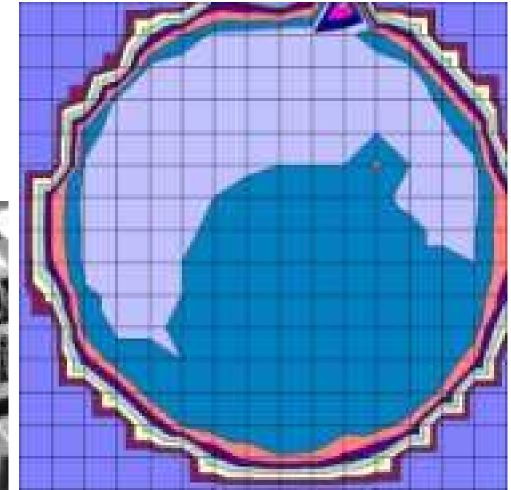
- Based on QinetiQ's hybrid technology
  - Design and fabrication of reticle-stitched ROICs
  - MBE growth of buffer layers onto silicon
  - MOVPE growth of MCT doped layers
  - Mesa pixel formation
  - Flip-chip bonding
  - Phase 1 & 2 low temperature testing at QinetiQ
- Phase 2 testing performed at RAL
  - Experience of testing NIR Detectors



QinetiQ
© Copyright QinetiQ Limited 2010

WP1

Detector Requirements Analysis



QinetiQ

© Copyright QinetiQ Limited 2010

WP1 – Introduction to Requirements Analysis

Aims of work package

- Record requirements in Detector Requirements Specification Document (TN1)
  - Inputs from Statement of Work and Kick-off Meeting

- Generate Detector Development Plan – 2 Part Document
  - Based on review of requirements relative to current status
  - Generate preliminary detector design elements
  - Part 1 – development required to meet goals of phase 1 of programme
  - Part 2 – development required to meet goals of phase 2 of programme

QinetiQ

© Copyright QinetiQ Limited 2010

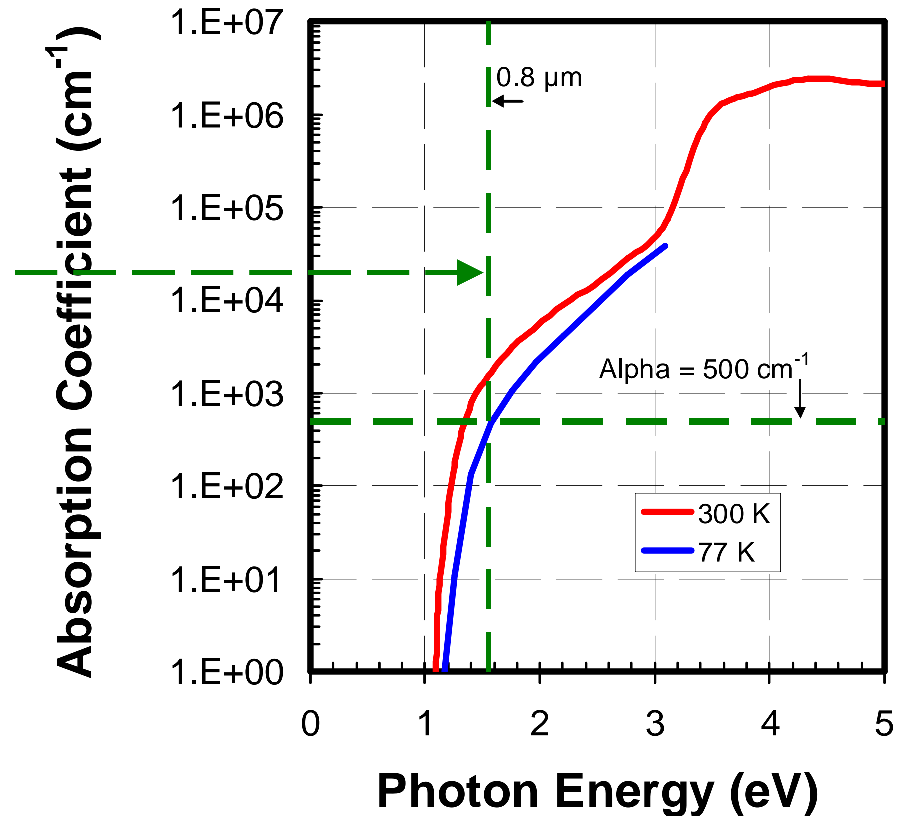
WP1 - Initial Design Elements 1

Effect of silicon substrate absorption

- Standard QinetiQ process involves growth on a silicon substrate
- Absorption coefficient > 500 cm^{-1} at cut-on wavelength of 0.8 μm.

Need to remove all / most of silicon substrate

- 4 μm thickness will transmit around 67% incident radiation



Sze, S. M., *Physics of Semiconductor Devices,* John Wiley and Sons, N.Y., 1981.

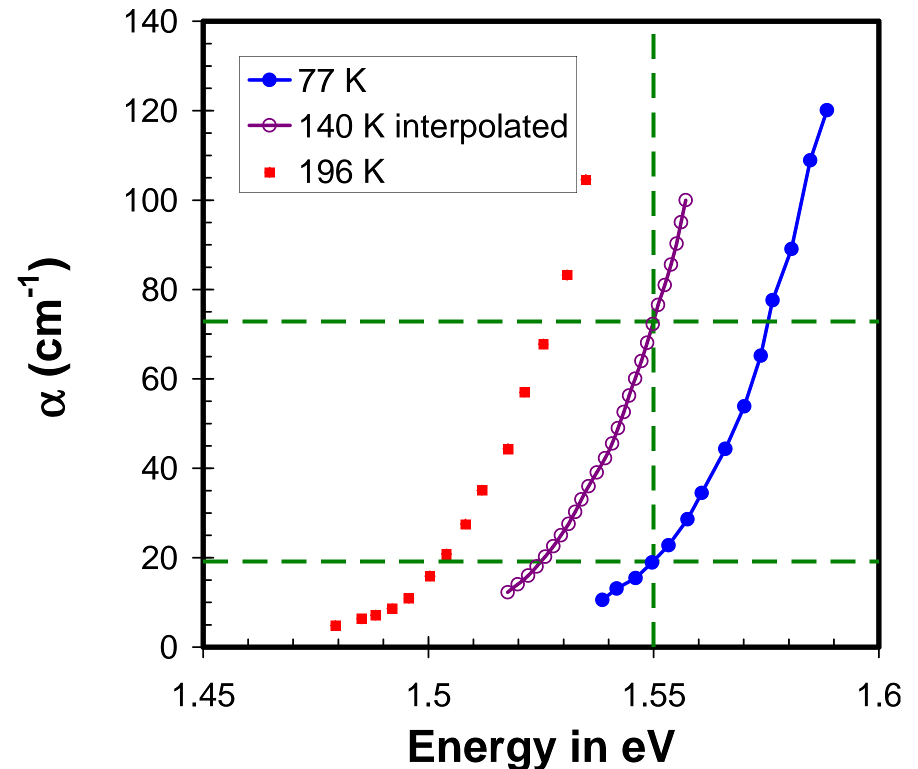
QinetiQ

© Copyright QinetiQ Limited 2010

WP1 - Initial Design Elements 2

Effect of Cadmium Telluride Absorption

- Absorption coefficient appears to be less than 100 cm^{-1} over range of temperatures
- Suitable for window layer in structure
  - Ideally this should be conducting
- Buffer layers of a few μm should not be a problem



W.C Dash and R. Newman, "Intrinsic Optical Absorption in Single-Crystal Germanium and Silicon at 77 K and 300 K", Phys. Rev. 99(4), 1151-1155, 1955.

QinetiQ

© Copyright QinetiQ Limited 2010

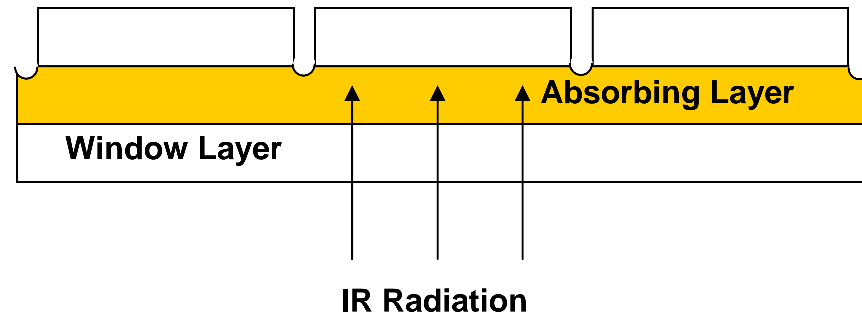
WP1 - Pixel Design

Layer structures (see next slides)

- Standard design for n-on-p structure
- Alternative design using grades

Pixel layout

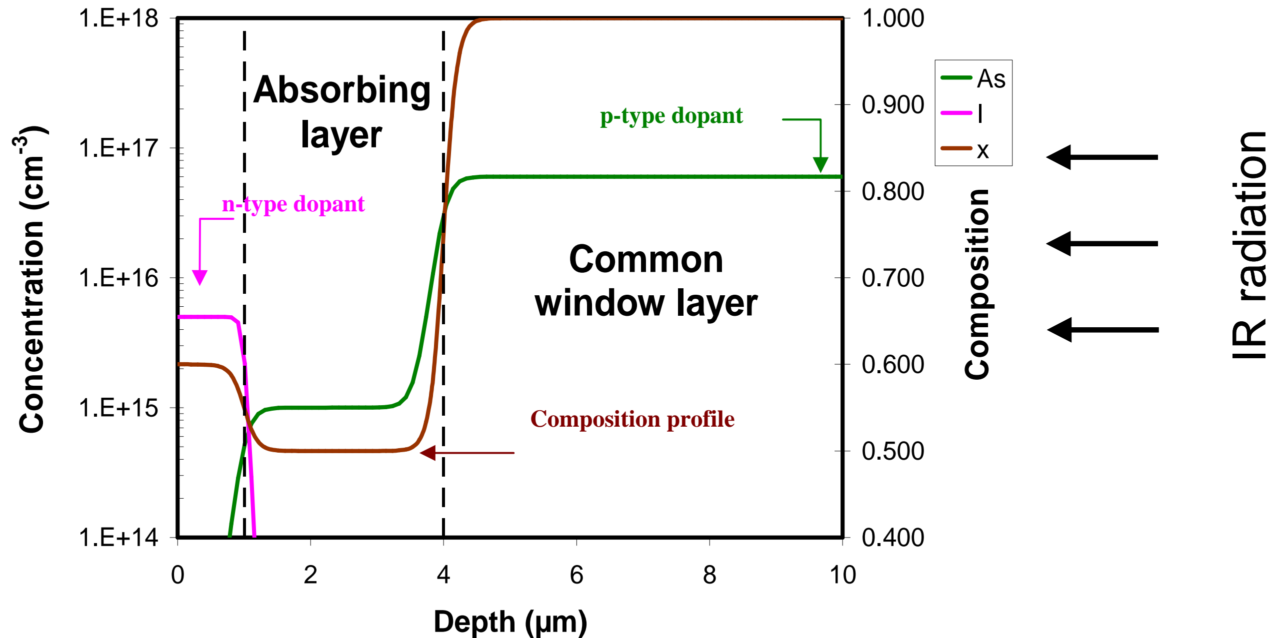
- Mesa structure
- Minimum etch depth
  - Maintains high fill-factor



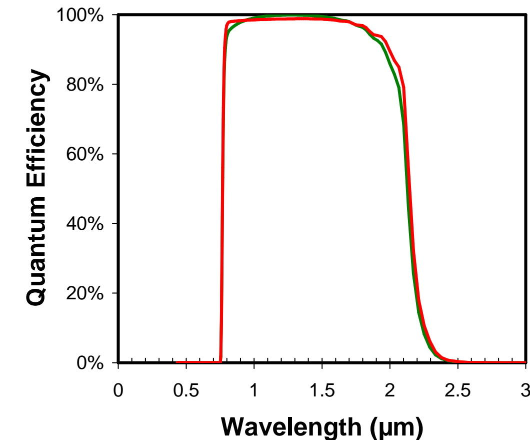
QinetiQ

© Copyright QinetiQ Limited 2010

WP1 - Ungraded n-on-p Device



IR radiation

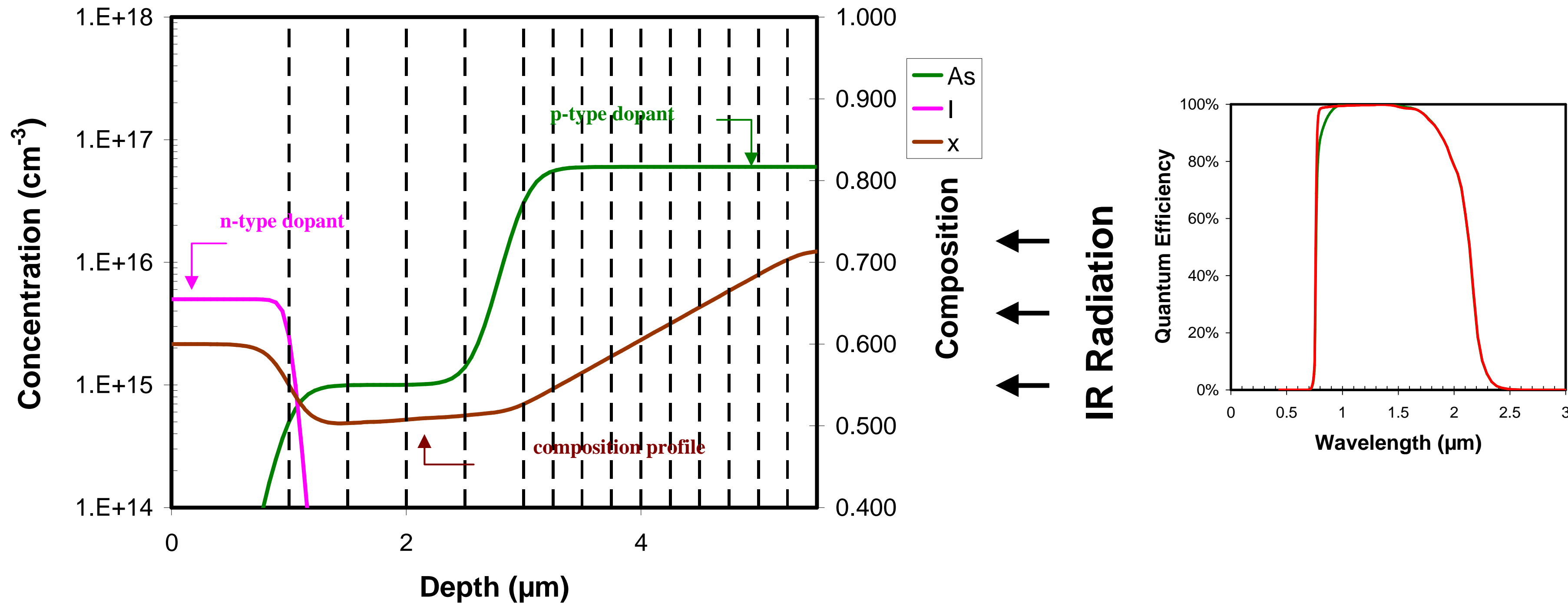


Requirements

- Ideally conducting x=1: p-type layer for common
- Shallow mesa etch to maintain quantum efficiency

QinetiQ
© Copyright QinetiQ Limited 2010

WP1 - Graded n-on-p Device



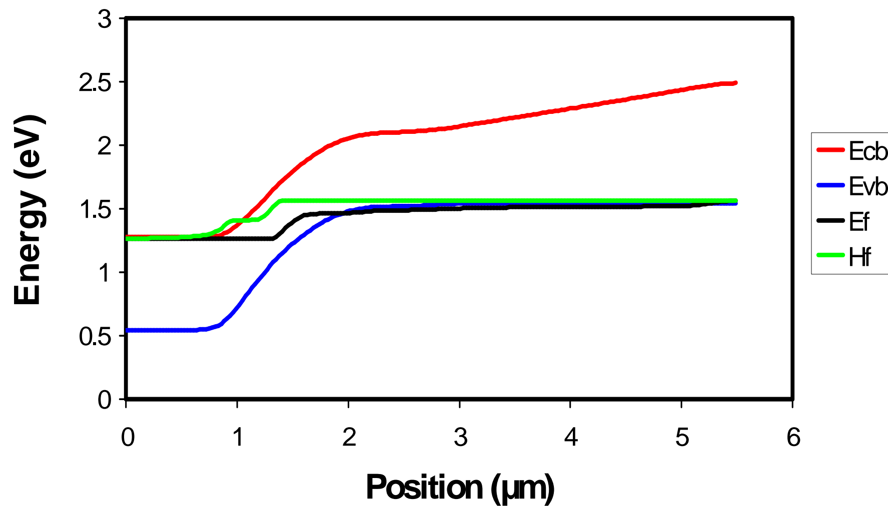
Main advantage: lower composition material is needed, easier doping

Main disadvantages: greater complexity: longer diffusion distance

QinetiQ

© Copyright QinetiQ Limited 2010

WP1 - Field-assisted diffusion



$$l_{diff} = \sqrt{\frac{kT}{q}\frac{w}{\xi_{eff}}}$$

$$\xi_{eff} = \frac{\partial E_{cb}}{\partial x}$$

Carriers can diffuse sideways during the time taken to reach the junction

- Maximum lateral diffusion estimated from bands
- Effective fields
  - Window region: 1400 Vcm^{-1}
  - Absorption region: 160 Vcm^{-1}
- Lateral diffusion
  - Window region: 0.4 μm
  - Absorption region: 1.1 μm

May be useful to include small grade in standard structure

- Growth of graded structures is discussed in growth section

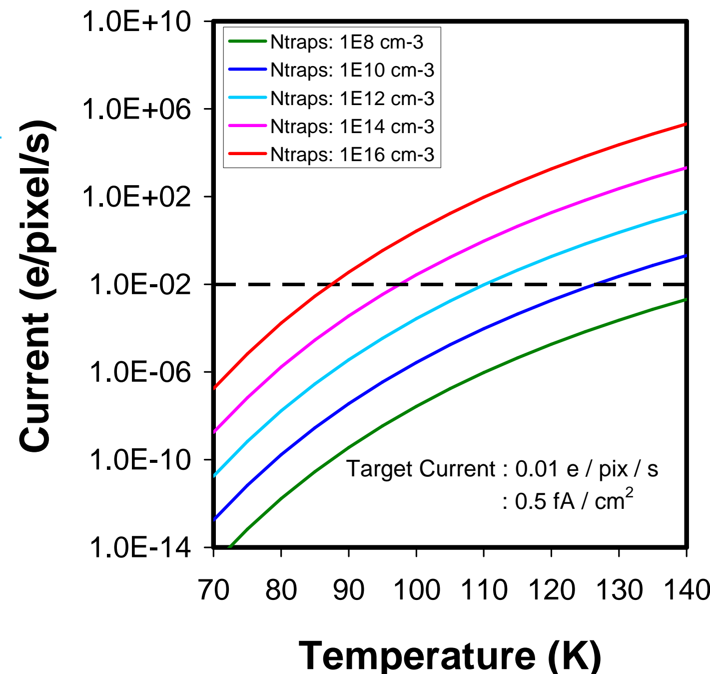
QinetiQ

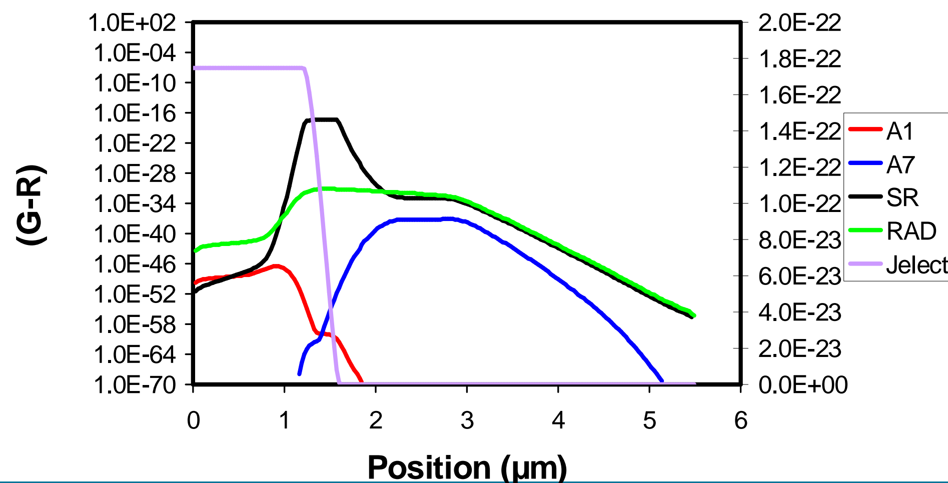
© Copyright QinetiQ Limited 2010

WP1 - Dark Current

Linear model suggests most of the current will be generated in the depletion region

- Current depends on trap density and properties
- Dark currents will be measured and compared with model and used to monitor progress towards target current

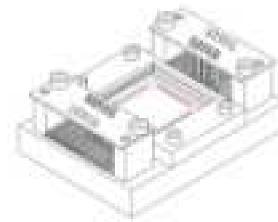


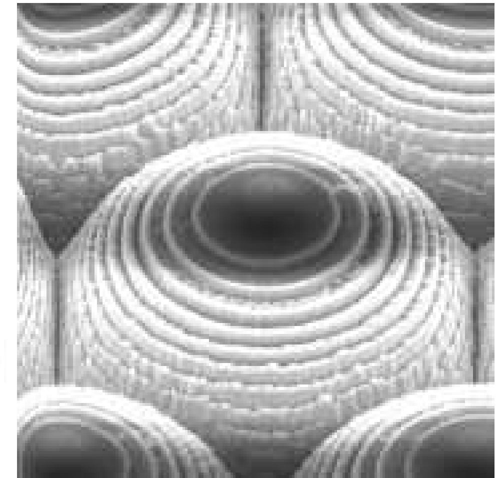


© Copyright QinetiQ Limited 2010

WP2

Test Plan Preparation





QinetiQ

© Copyright QinetiQ Limited 2010

WP2 – Test Plan Preparation

Aims of work package

- Record test plan in MCT Demonstration Test Plan Document (TN3)
  - Inputs from Statement of Work, Kick-off Meeting and review meeting

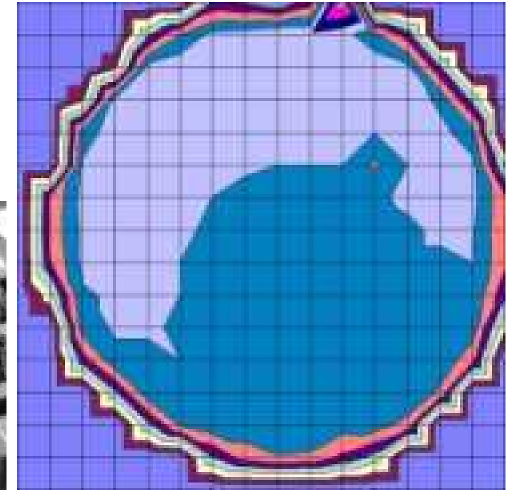
QinetiQ

© Copyright QinetiQ Limited 2010

WP3

MCT Material Demonstration

- Material Growth
  - MBE Buffer Growth
  - MOVPE MCT Growth
- Detector Fabrication
- AR Coating
- Testing

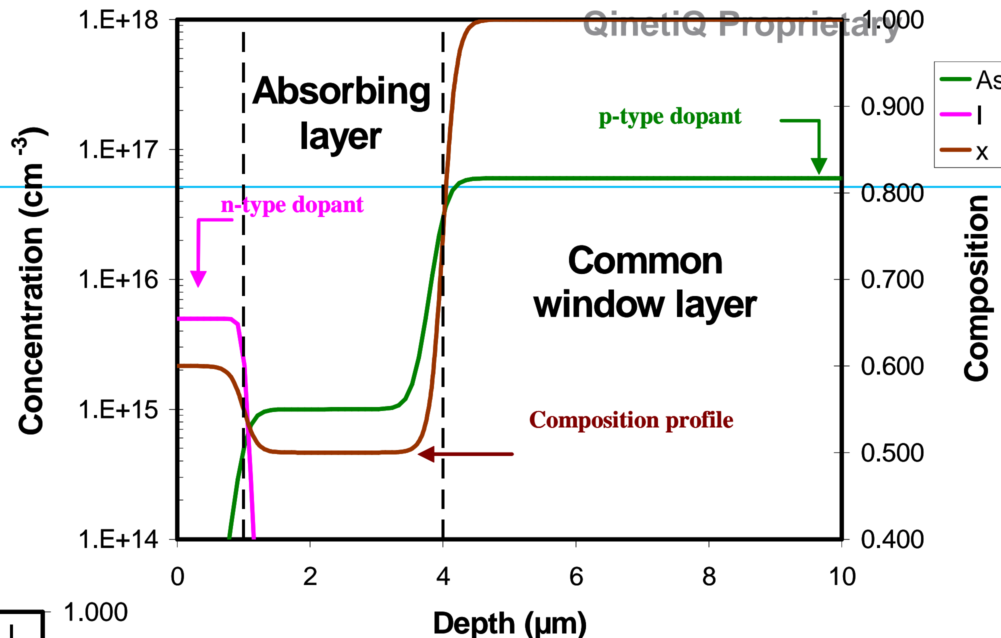


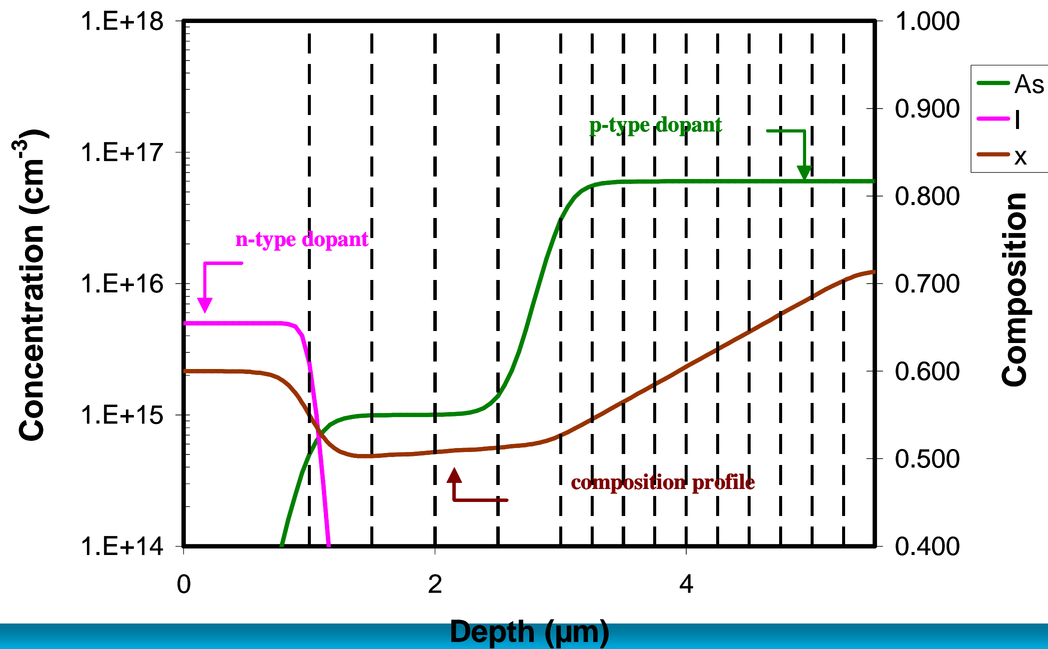
QinetiQ

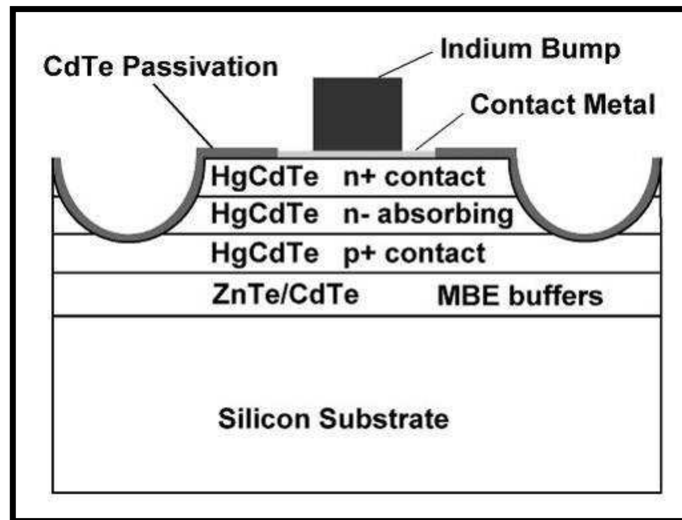
© Copyright QinetiQ Limited 2010

WP3 - Material Growth

- From modelling have 2 options for materials structure
- Single x layers only
- Incorporating x grade



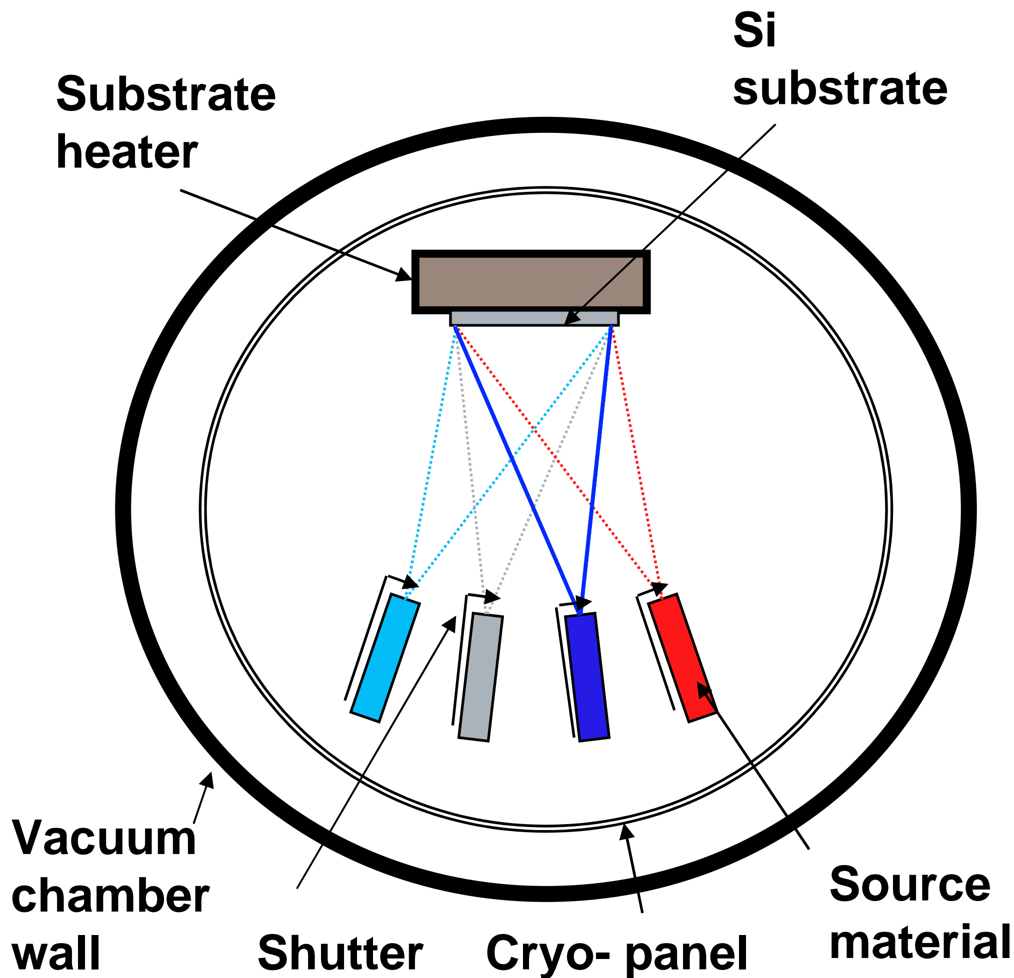




QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – 3" Buffer Growth MBE process



- Growth of buffer layer between Si and MCT
- Ultra high vacuum process
- Source materials evaporated from heated crucibles contained in cells
- CdTe, ZnTe, Zn, Cd, Te used as source materials
- Shutters turn beams on and off

© Copyright QinetiQ Limited 2010

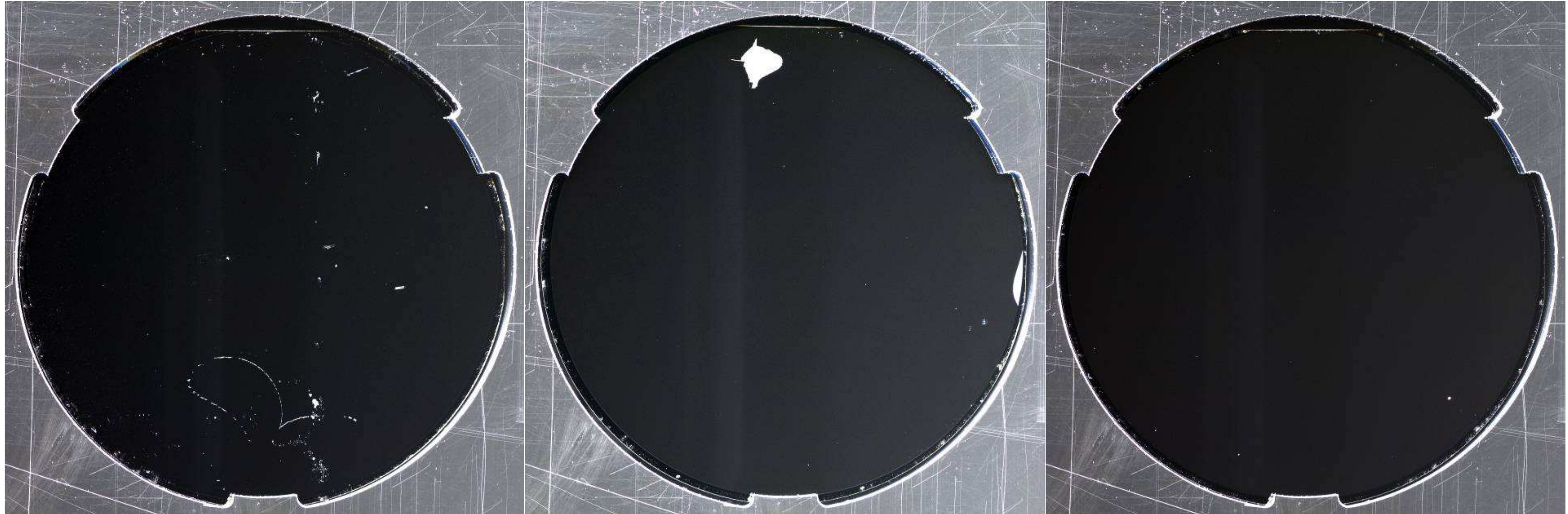
WP3 - Buffer Growth Tasks

- Write a specification and order buried oxide (BOX) releasable Si substrates
  - Complete
- Grow a stock of standard II-VI buffers on standard Si
  - Complete
- Grow standard buffer layer on BOX Si substrates
  - Complete
  - Start with method for growth on standard Si and modify as necessary to achieve good growth
    - Complete, no modification necessary
  - Build up a stock of buffers on BOX substrates suitable for CMT growth
    - Complete
- Grow II-VI buffers on GaAs as risk mitigation should Si removal be difficult
  - In progress

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – Buffer Growth on BOX Si substrates



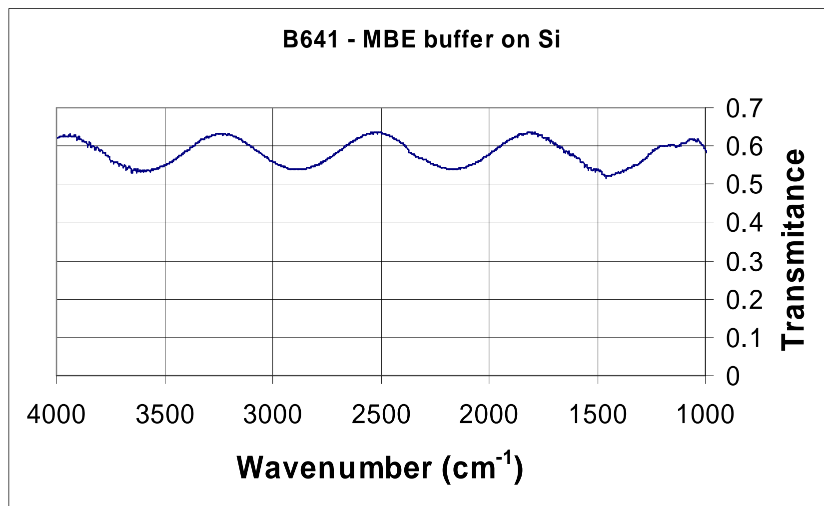
- Quality of Si substrates readily revelled by growth of buffer layer *
- BOX substrates were variable in quality
  - Best are excellent (right) (~70% are of this standard)
  - Worst one (left) was awful
  - Several had been thinned too much (centre) in some areas but were otherwise OK

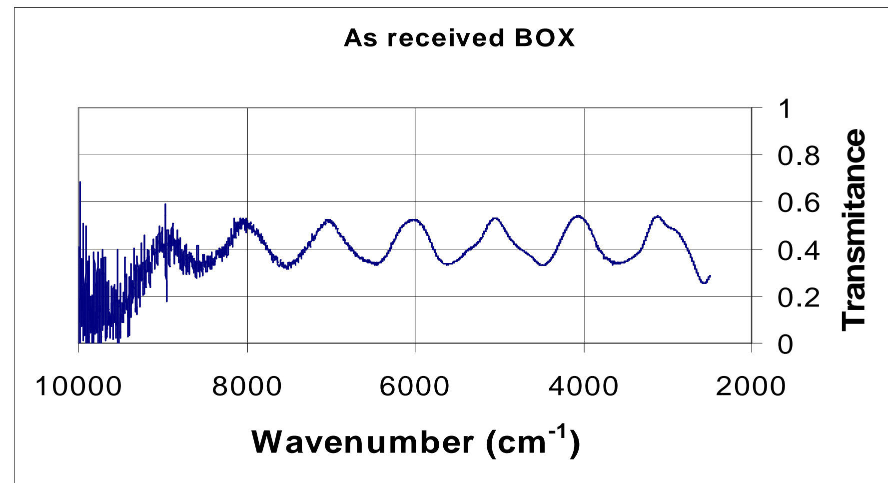
* Hails, J.E., Keir, A.M., Graham, A., Williams, G.M., Giess, J. (2007) *Journal of Electronic Materials*, 36, 864

QinetiQ

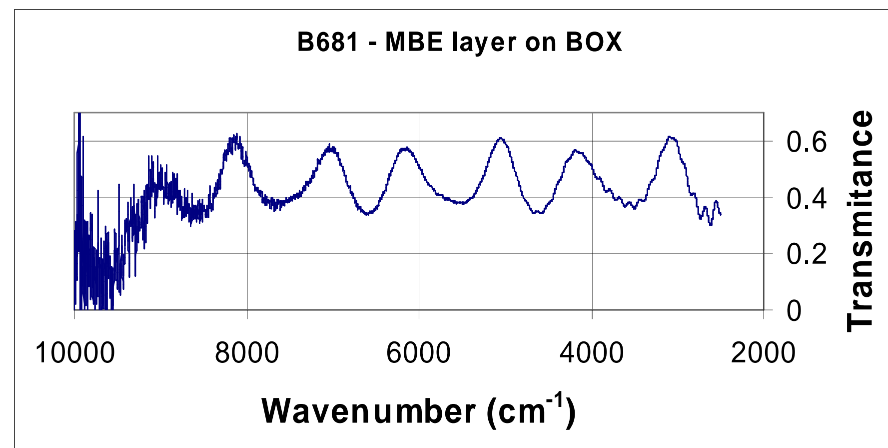
© Copyright QinetiQ Limited 2010

WP3 – Transmission of Buffer Layer on BOX Substrate



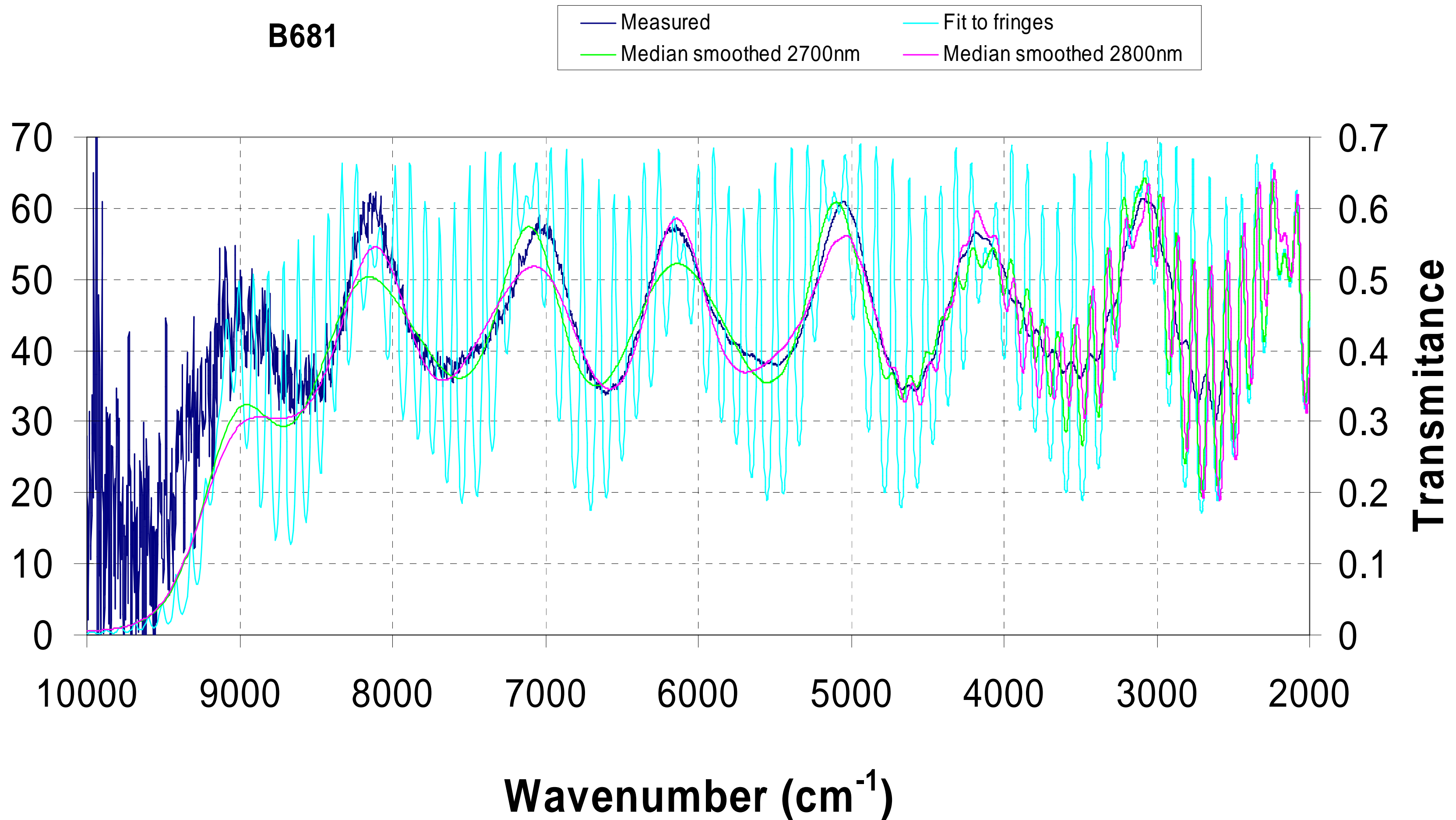


- Layers on Si show regular fringes
- BOX substrate and buffer on BOX show uneven fringing
- Modelling allows fit of MBE on BOX…
  - fringe spacing to Si thickness of ~11040nm
  - beats to a SiO_2 thickness of 3400nm
  - buffer layer to 2.7 – 2.8 um



© Copyright QinetiQ Limited 2010

WP3 - Modelled Transmission of Buffer on BOX Si Substrate



QinetiQ

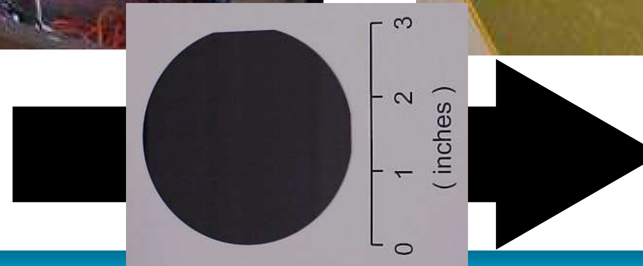
© Copyright QinetiQ Limited 2010

WP3 - 3” MOVPE MCT Growth

II-VI buffer on Si

VG V80H MBE Reactor
(QinetiQ upgraded)

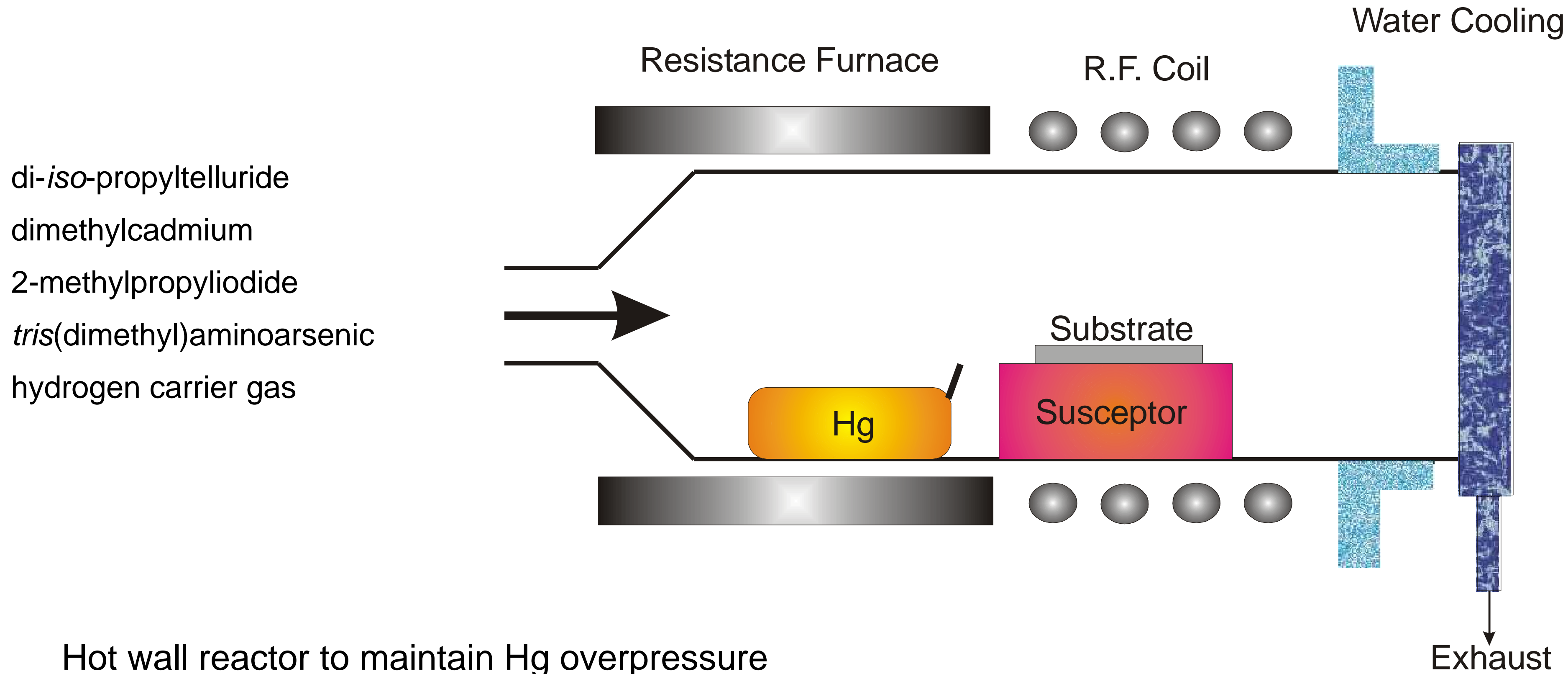
MCT growth on II-VI buffered Si



MR Semicon MOVPE Machine
(QinetiQ Reactor and upgrades)

© Copyright QinetiQ Limited 2010

WP3 - MOVPE MCT Growth



Hot wall reactor to maintain Hg overpressure

Growth temperature ~ 370 ℃

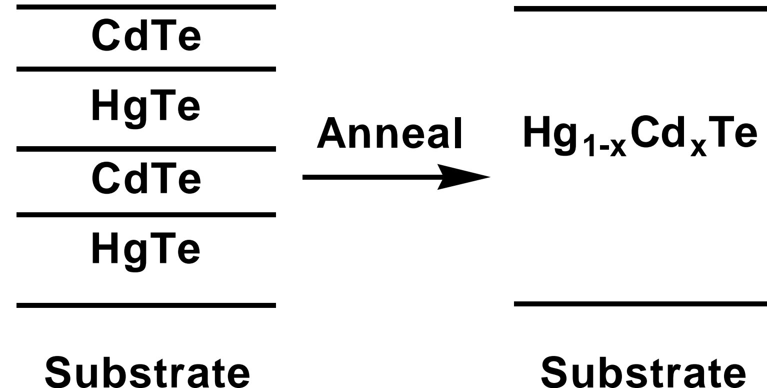
Hg boat temperature ~ 165 ℃

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 - MOVPE MCT Interdiffused Multilayer Process (IMP)

- Grow thin HgTe and CdTe layers
- Layers interdiffuse during and at end of growth
- Total number of layer pairs controls total thickness
- Composition controlled by relative thickness of HgTe and CdTe
- QinetiQ patented process



Ref: J. Tunnicliffe, S.J.C. Irvine, O.D. Dosser and J.B. Mullin, *J. Cryst. Growth* 66, 245, (1984).

QinetiQ

© Copyright QinetiQ Limited 2010

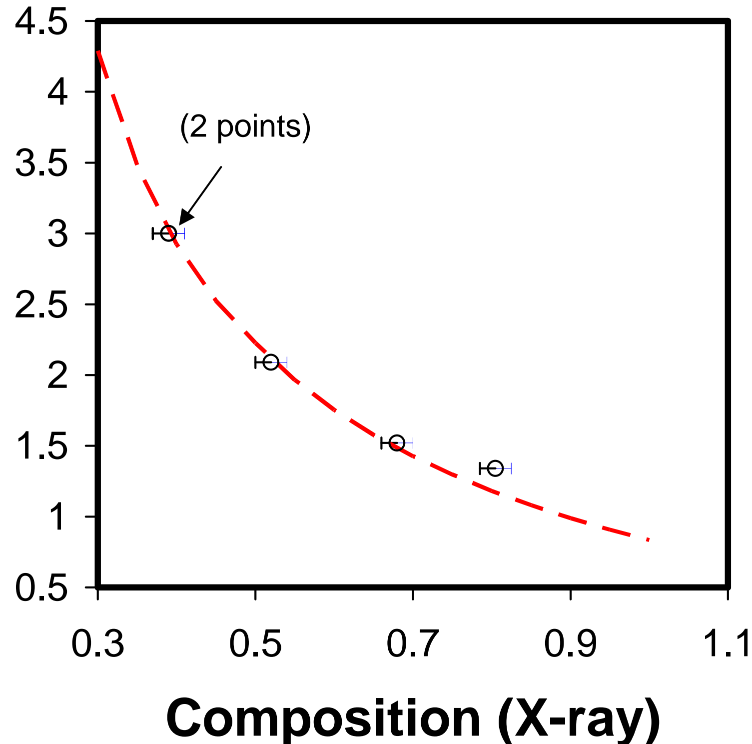
WP3 - MCT Growth Tasks

- Grow individual layers of proposed device structure for 0.8 - 2 μm operation separately onto standard buffered Si substrates
  - Demonstrated that the composition is correct for the individual layers
  - Dopant activation assessed by comparing SIMS and electrical results
  - Growth conditions have been modified to improve activation at the correct composition for all individual layers
- Grow MCT device structure to the requirements of the device design on standard buffered Si substrates
  - Assessed using SIMS and FTIR spectroscopy for doping profiles, composition and uniformity
  - Modified growth process to achieve good control of the growth of the device structure
- Grow the CMT device structure on buffered BOX substrates, including wafer assessment and modification of process as necessary
- Supply standard and BOX wafers for fabrication
  - Complete

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – MCT Growth Composition



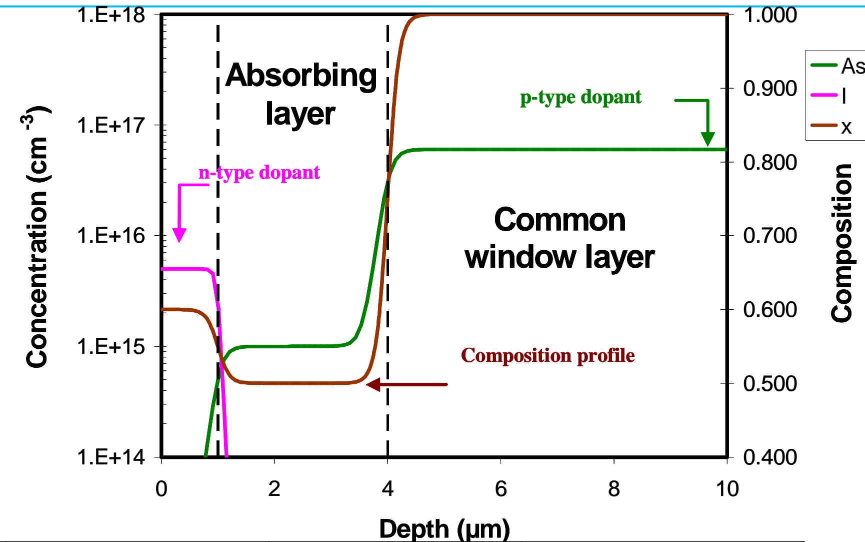
- X-ray measurements based on average lattice parameter of the layer.
- x-value calculated from x-ray assuming Vegard's law and end-point lattice parameters
  - HgTe: a0 = 6.4615Å , CdTe: a0 = 6.4810Å.
- Samples with x from 0.39 to 0.68 agree with Chu equation to better than error in x (+/- 0.02)
- Significant difference for the highest x sample
- The second highest x sample looks slightly shifted.
- Critical cut-off part of the structure is quite close to the Chu curve.

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – MCT Growth Doping Activation – p-type (Arsenic)

- Dopant activation is approximately 50% in the absorbing layer
- Not possible to make good electrical contacts to the layers with higher x



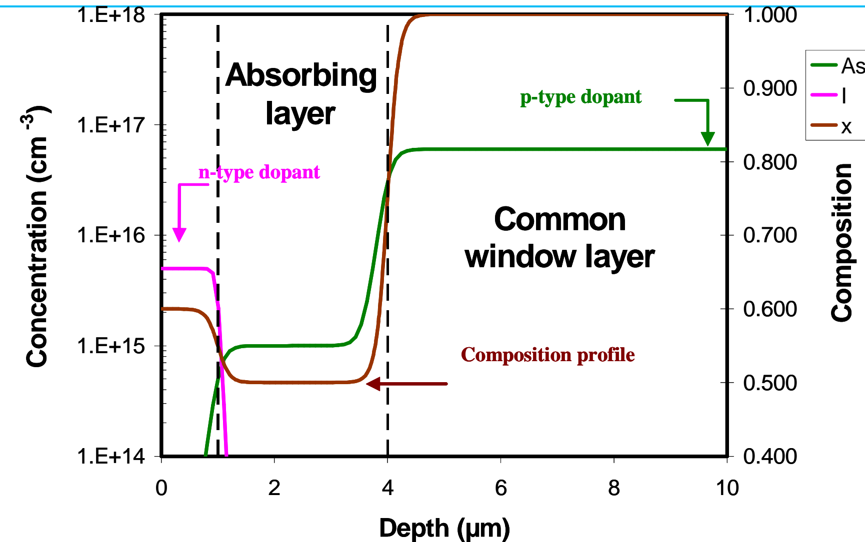
Sample	M504(B573)	M533(B622)	M536(B624)	M548(B677)	M550(B673)
x	0.220	0.654	0.748	0.850	1.000 (CdTe)
Hall carrier conc (cm^{-3})	$6x10^{16}$	$2x10^{16}$	$3x10^{16}$		
SIMS conc (cm^{-3})	$1x10^{16}$ to $4x10^{16}$	$3x10^{16}$ to $8x10^{16}$	$6x10^{16}$	~ $2x10^{18}$	
Activation	>100%	25 - 67%	*54%*		
		Approx x of absorbing layer		*contacting difficulties*	*Awaiting results*

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – MCT Growth Doping Activation – n-type (Iodine)

- Dopant activation is approximately 100% in the contact layer

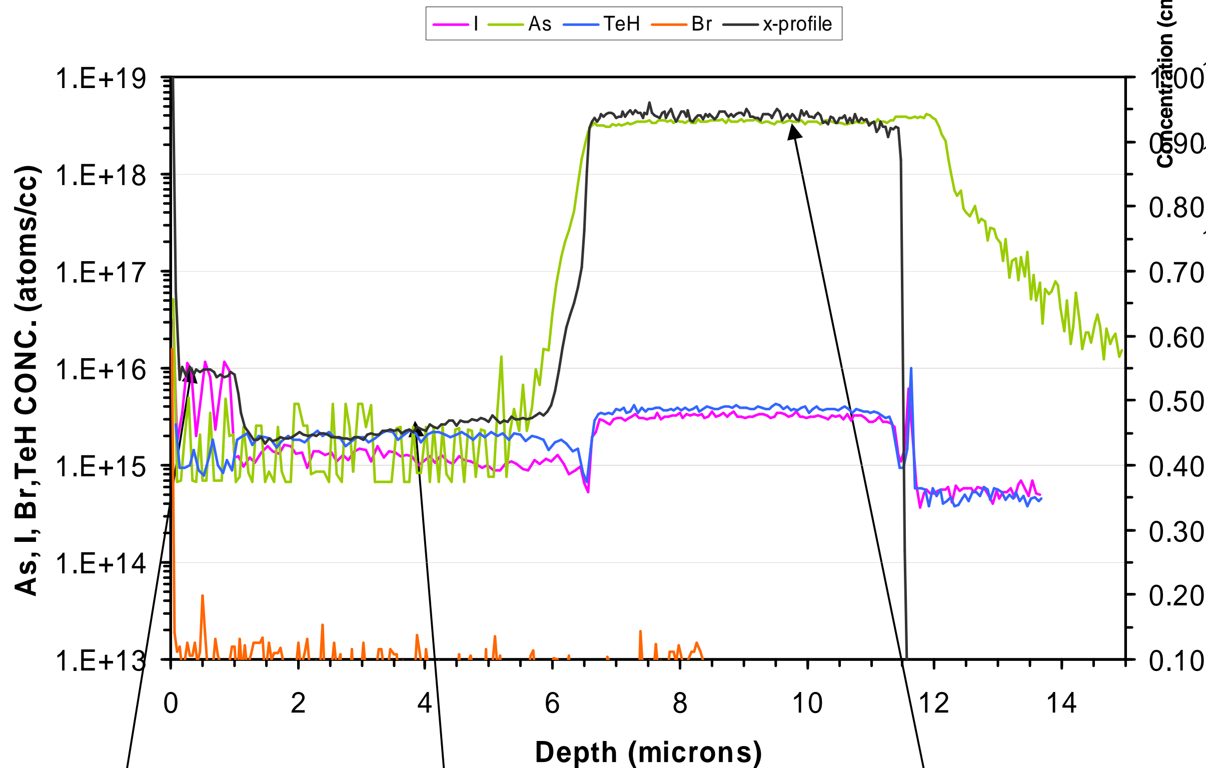


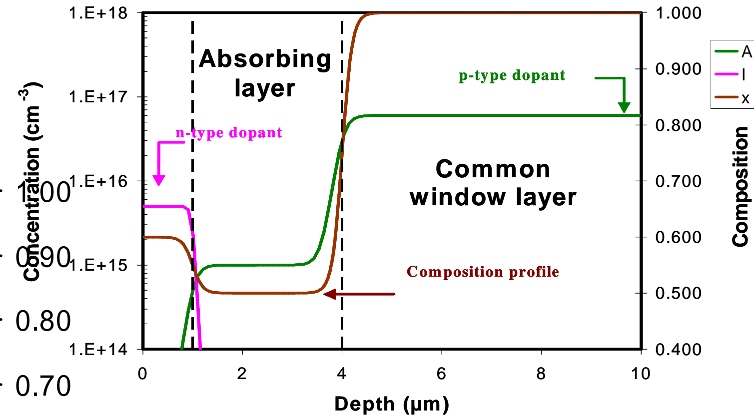
Sample	M505(B588)	M519(B605)	M520(B607)	M525(B611)
x	0.310	0.450	0.400	0.530
Hall carrier conc (cm^{-3})	9.7×10^{15}	4.0×10^{16}	5.8×10^{16}	7.5×10^{15}
SIMS conc (cm^{-3})	1.1×10^{16}	4.5×10^{16}	6.8×10^{16}	7.5×10^{15}
Activation	88%	89%	85%	100%
				Approx x of contact layer

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – MCT Growth of Ungraded Structure





X too low

X too low and unintentional grade

[As] too high

- Corrections made for subsequent wafers

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – MCT Growth of Individual Graded Layer

SIMS profile of M522(B609)

I, As, TeH, Br, x-profile

As, I, Br,TeH CONC. (atoms/cc)

1.E+18
1.E+17
1.E+16
1.E+15
1.E+14
1.E+13

x-profile

0.80
0.75
0.70
0.65
0.60
0.55
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10

0 2 4 6 8 10 12 14 16 18 20

Depth (microns)

As doping

Calibration x

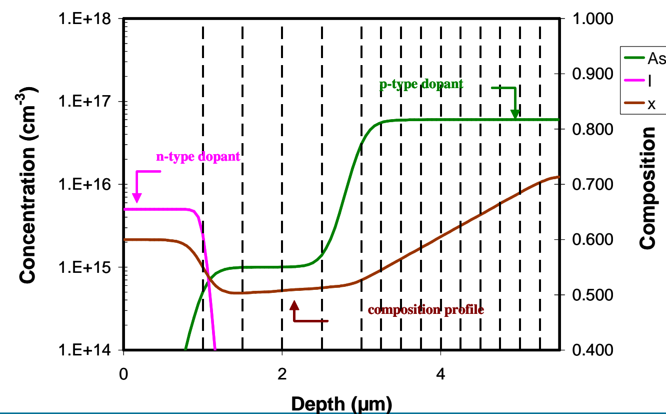
"Normal" grade

Final composition

"Grown" grade

Initial composition

- Designed structure may require use of composition grades with constant doping level
- Demonstrated MOVPE system can be used to deliberately grade alloy composition



QinetiQ
© Copyright QinetiQ Limited 2010

WP3 - MCT Growth of Graded Structure

SIMS profile of M538(B614)

X too high

I, As, TeH, Br, x-profile

As, I, Br,TeH CONC. (atoms/cc)

1.E+18, 1.E+17, 1.E+16, 1.E+15, 1.E+14, 1.E+13

x-profile

1.00, 0.90, 0.80, 0.70, 0.60, 0.50, 0.40, 0.30, 0.20, 0.10

0, 2, 4, 6, 8, 10

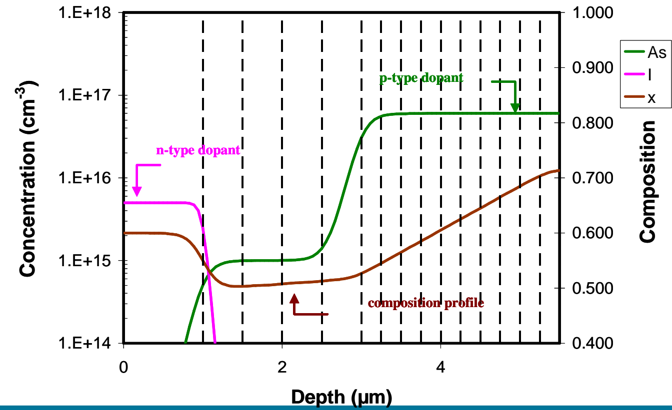
Depth (microns)

Backgrounds - As - 5E14
I - 7E14
Br - 1E12

[I] bit high

Dips in x at interfaces

- First attempt at growth of graded device structure



© Copyright QinetiQ Limited 2010

WP3 - MCT Growth of Graded Structure

SIMS profile of G868-M551-M546-B640

I — As — TeH — Br — x-profile

As, I, Br,TeH CONC. (atoms/cc)

1.E+18
1.E+17
1.E+16
1.E+15
1.E+14

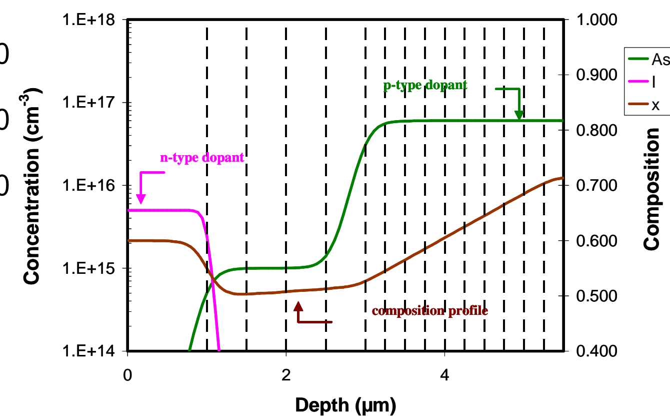
0 2 4 6 8 10

Depth (microns)

x-profile

1.00
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10

- Second attempt at growth of graded device structure after device fabrication
- As doping OK
- I doping OK
- x grade OK
- Removed dips in x at interfaces

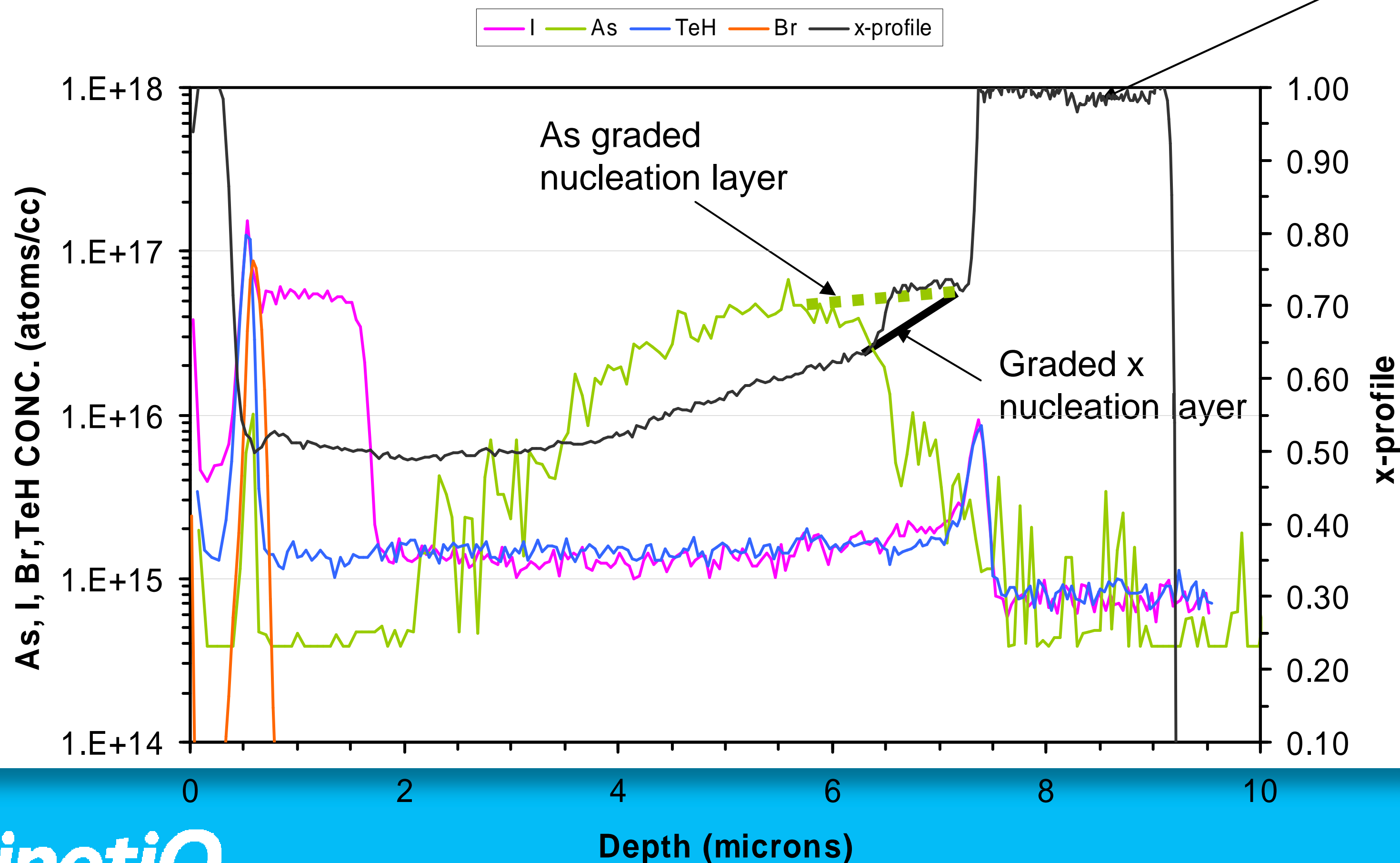


QinetiQ

© Copyright QinetiQ Limited 2010

WP3 - MCT Growth of Graded Structure

- Device results indicate junction involving 0.74 material (corresponds to nucleation layer)
- Grown with graded x nucleation layer (undoped & As doped)



QinetiQ

© Copyright QinetiQ Limited 2010

WP3 - MCT Growth Wafer Summary

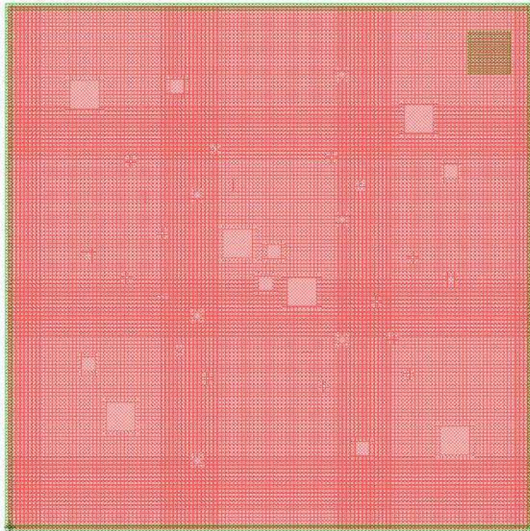
	Graded structure	Ungraded structure
Standard Si	M538 (SIMS) M546 (fabrication development) M556	M549 (SIMS) M554 (lowest x = 0.6) M557
BOX Si substrates	M547 M564 and M565 (graded undoped nucleation layer) M566 (graded As doped nucleation layer)	M555 (lowest x = 0.6) M558 M563

QinetiQ

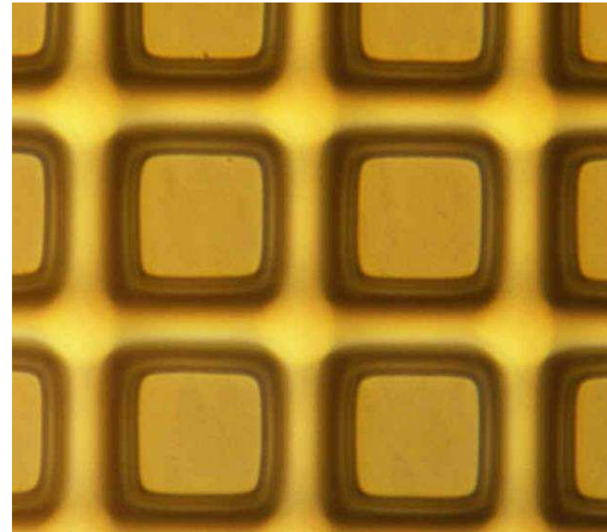
© Copyright QinetiQ Limited 2010

WP3 - Detector Fabrication Tasks

- Photomask design - Complete
  - Includes 128 "leadout" arrays with 18μm to 400μm device sizes
  - Includes a 1280x1280 18μm pitch array
- Mesa etch depth defined in modelling (2μm) calibration – Complete
- Wafer run to test and amend process flow - Complete



"leadout" part of the photomask design



Mesa etch depth calibration

© Copyright QinetiQ Limited 2010

WP3 – Detector Fabrication Wafer Summary

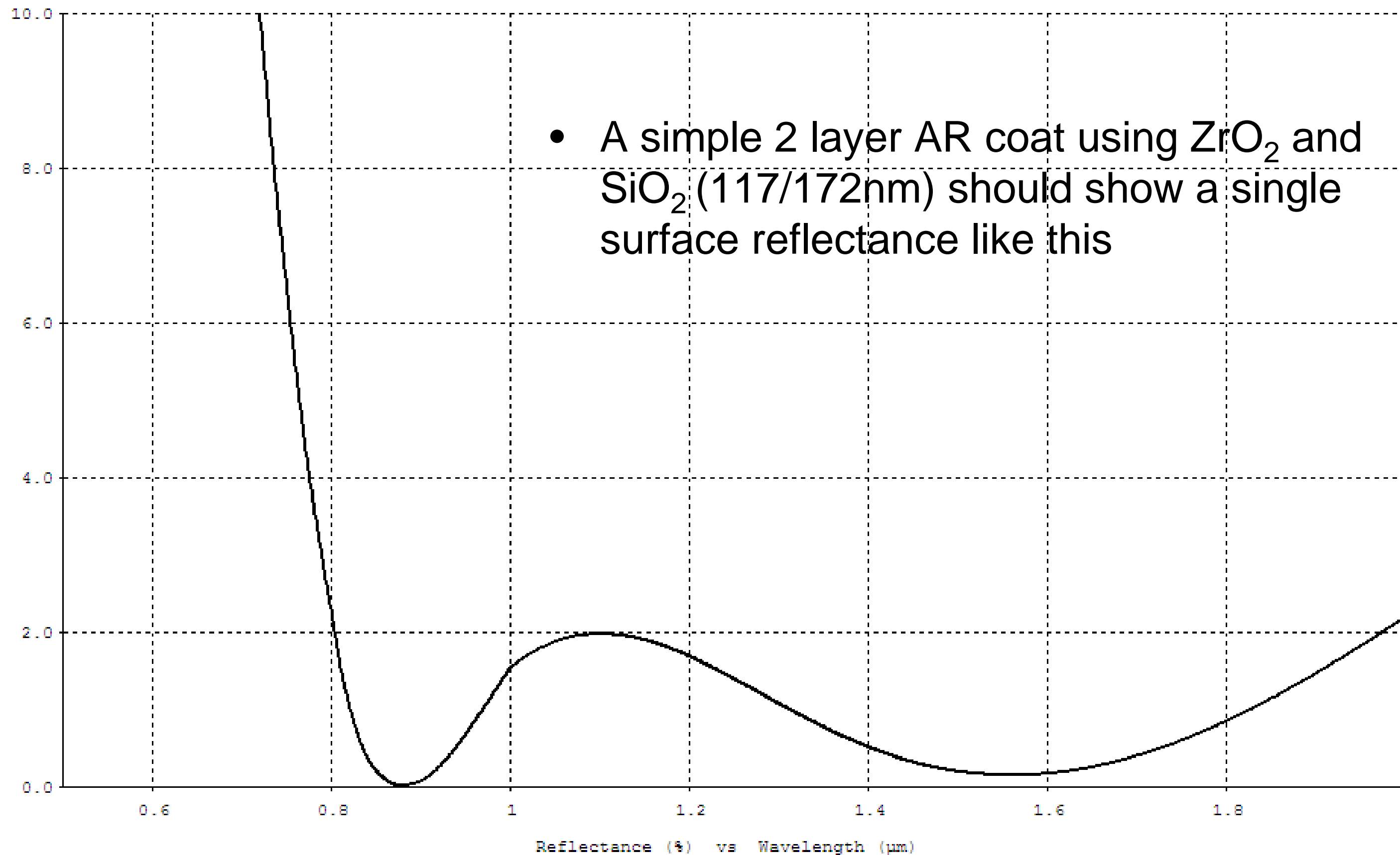
	Graded structure	Ungraded structure
Standard Si	M556 – In Progress (due 8th Nov)	M554 - Complete M557
BOX Si substrates	M547 – Complete and Testing M564 M565 M566	M555 – In Progress (due 8th Nov) M558 M563

2x wafers to be chosen to fabricated without passivation (start 8th Nov)

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 - Anti-Reflection Coating



- A simple 2 layer AR coat using ZrO_2 and SiO_2 (117/172nm) should show a single surface reflectance like this

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 - Anti-Reflection Coating

- QinetiQ AR coating facility has now been closed down
- External company identified
  - Their modelling data looks good
  - Test samples sent
  - Expect test deposition w/e 12th November 2010
  - Evaluate test samples
- Plan for 2x hybrid sample runs

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – Testing

Parameter	Value
Operating Temperature	80K to 140K
Cut-on Wavelength	< 0.8μm
Cut-off Wavelength	> 2.1μm
Dark Current	0.5 fA/cm^2
Quantum Efficiency	≥80%

This test plan has been designed to demonstrate that the MCT material meets the Phase 1 requirement specification

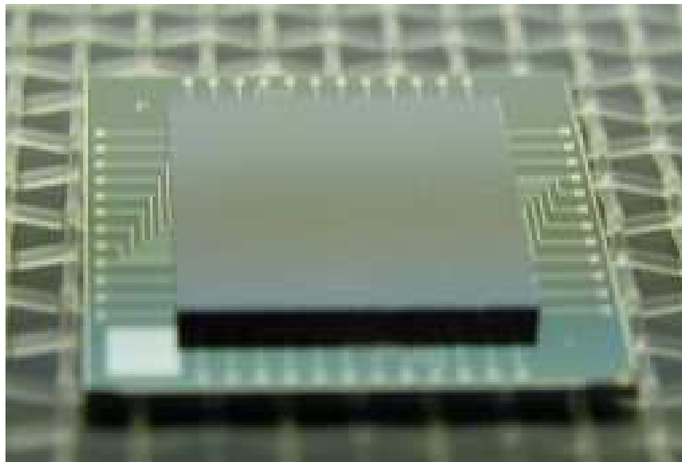
QinetiQ

© Copyright QinetiQ Limited 2010

WP3 - Phase 1 MCT Detector Test Set Up

MCT detector performance will be evaluated using leadout hybrid arrays

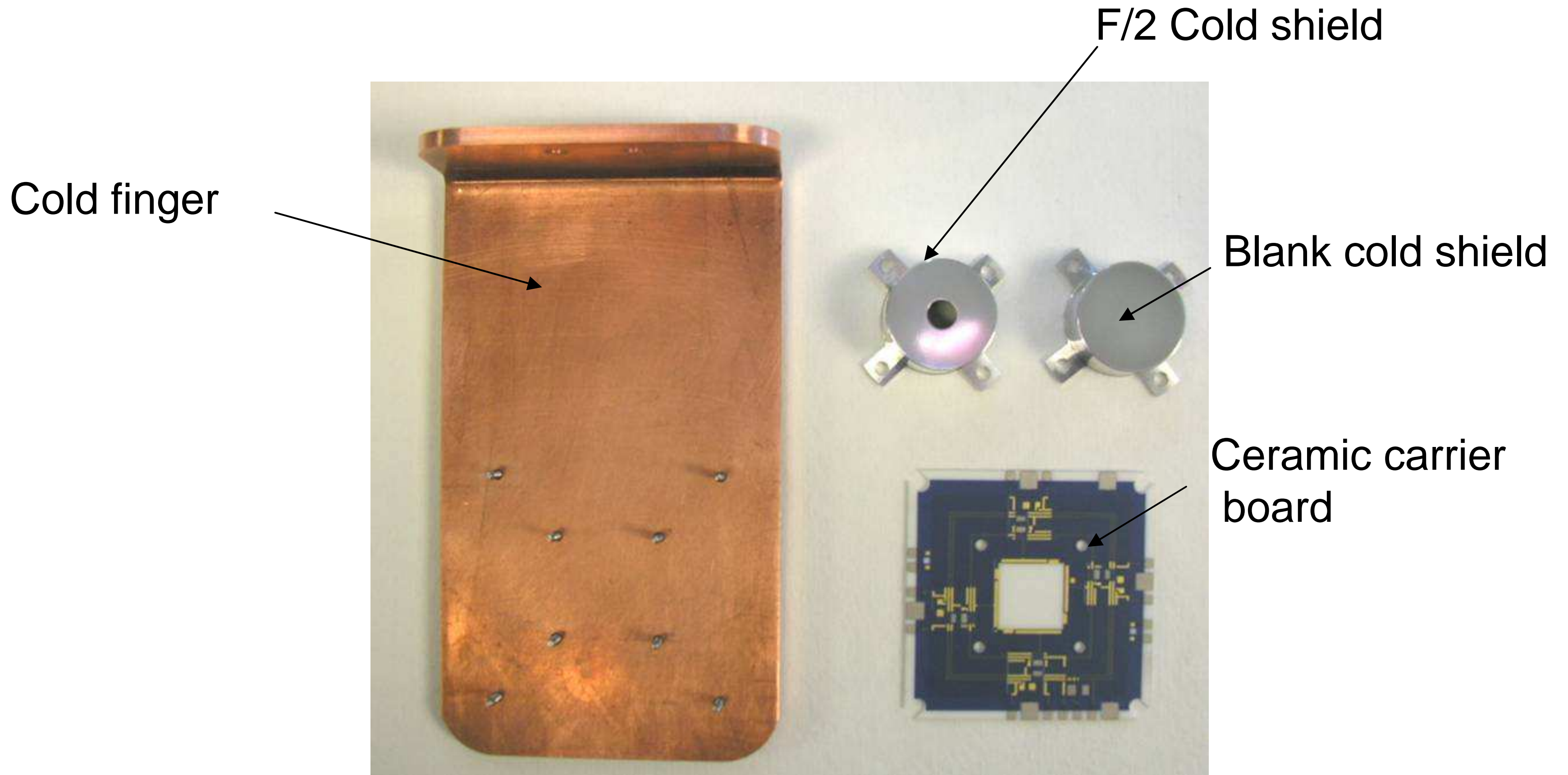
- MCT detector test chip is bump bond hybridised to a silicon leadout substrate
  - Test chips have a range of detector sizes
- Hybrids are glued to a ceramic carrier and fitted into a liquid nitrogen cryostat
- Individual detectors characterised over the required temperature range of 80K to 140K



Detector size (μm x μm)	Capacitance (fF at 0.5V)
18	32
30	89
50	247
100	988
200	3951
400	15802

© Copyright QinetiQ Limited 2010

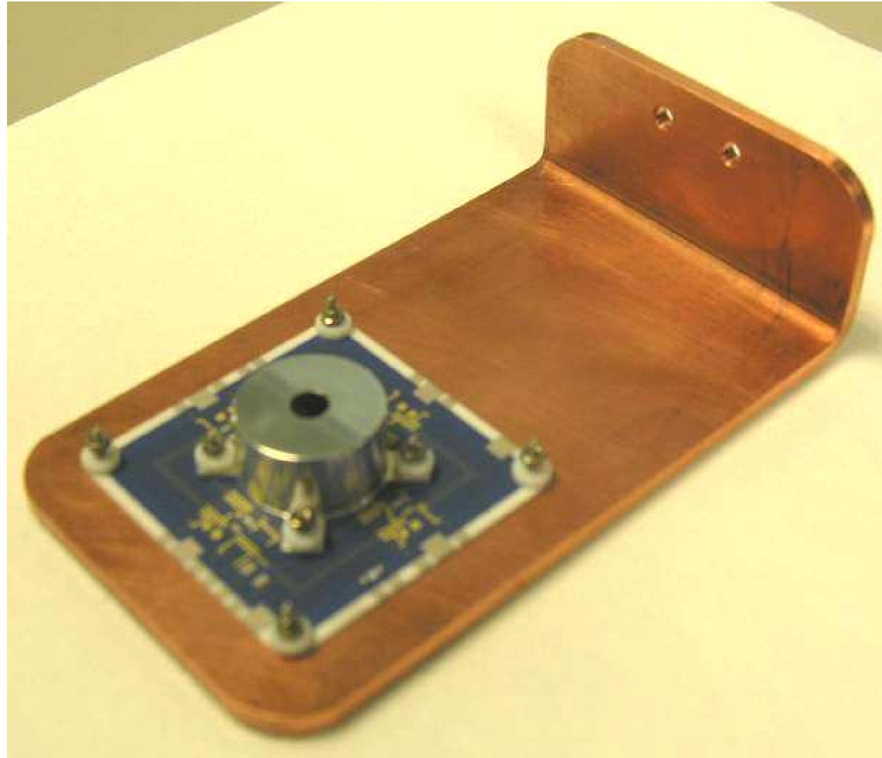
WP3 - Cold Finger Components



QinetiQ

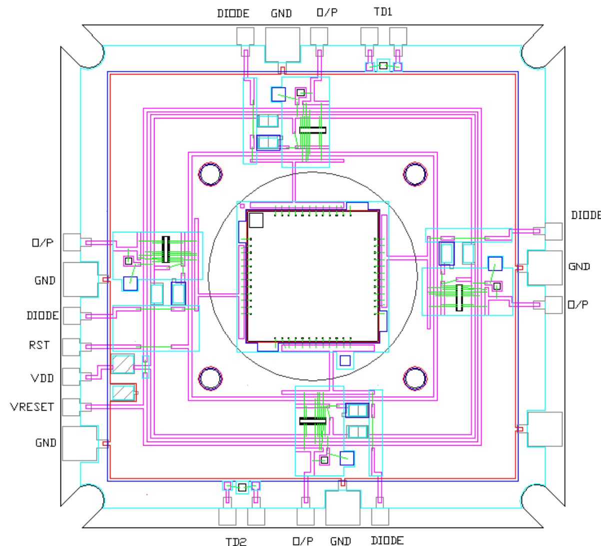
© Copyright QinetiQ Limited 2010

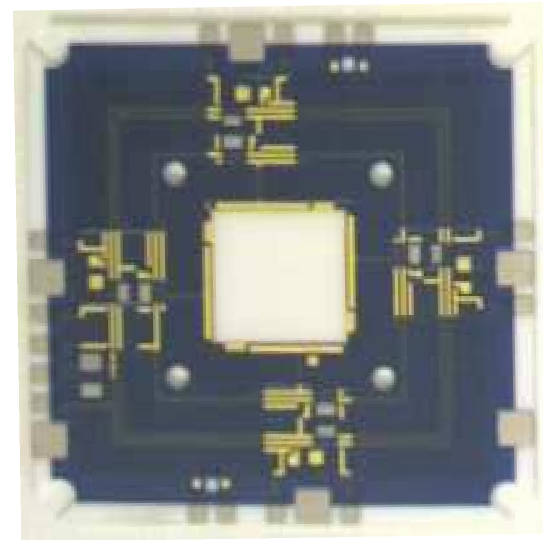
WP3 - Cold Finger Assembly



© Copyright QinetiQ Limited 2010

WP3 - Ceramic Carrier



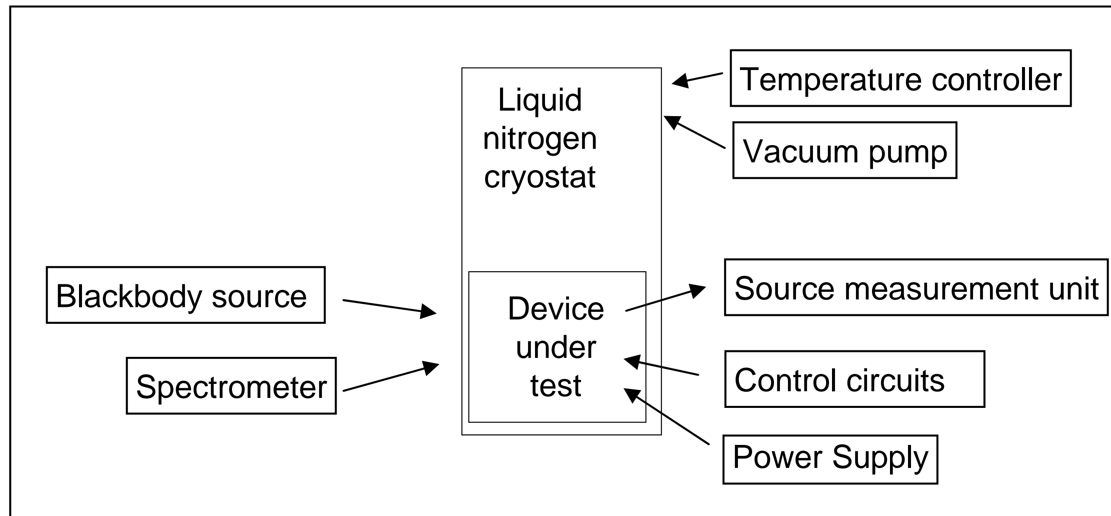


Wire bond configurable ceramic carrier

- Direct connection to detectors for radiometric measurements
- MOSFET buffer circuits for dark current measurement
- Up to four MCT detectors can be characterised at a time
- Thermal drift measurement using dummy channel with 15pF ceramic capacitor

© Copyright QinetiQ Limited 2010

WP3 - Test Equipment Setup



Sample mounted in low noise liquid nitrogen cryostat with sapphire window

QinetiQ

© Copyright QinetiQ Limited 2010

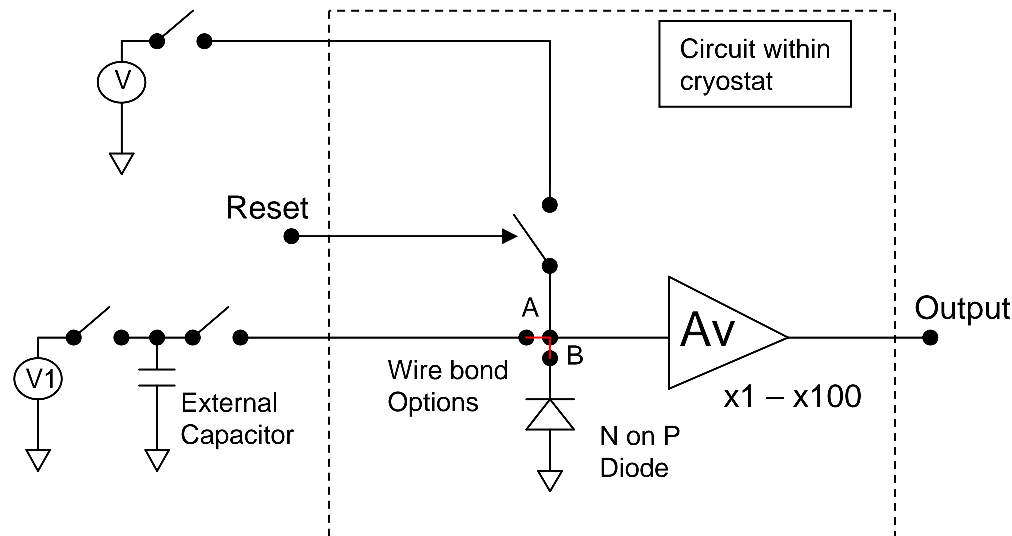
WP3 - Radiometric Characterisation

- Detector wavelength response will be characterised using a Fourier Transform Infra Red (FTIR) spectrometer
- Absolute response will be measured using a calibrated black-body source
- Measured values will be used to generate quantum efficiency data as a function of wavelength
- Data will be used to measure cut-on and cut-off wavelength at 50% QE max

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 - Dark Current



Test circuit has the same configuration as a SFD pixel circuit

Built using chip MOSFETS assembled on a ceramic carrier with metal / wire bond interconnects

Reconfigurable by changing bond out so that different measurement techniques can be assessed

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – Test Summary

Test arrays are characterised over a temperature range of 80K to 140K using a liquid nitrogen cryostat

Measurement include

- Cut-on and cut-off wavelengths (50% QE max)
- Quantum efficiency
- Dark current

Ceramic is initially configured for radiometric measurements

- Radiometric measurements will be carried out using a calibrated Perkin Elmer spectrometer and calibrated blackbody sources

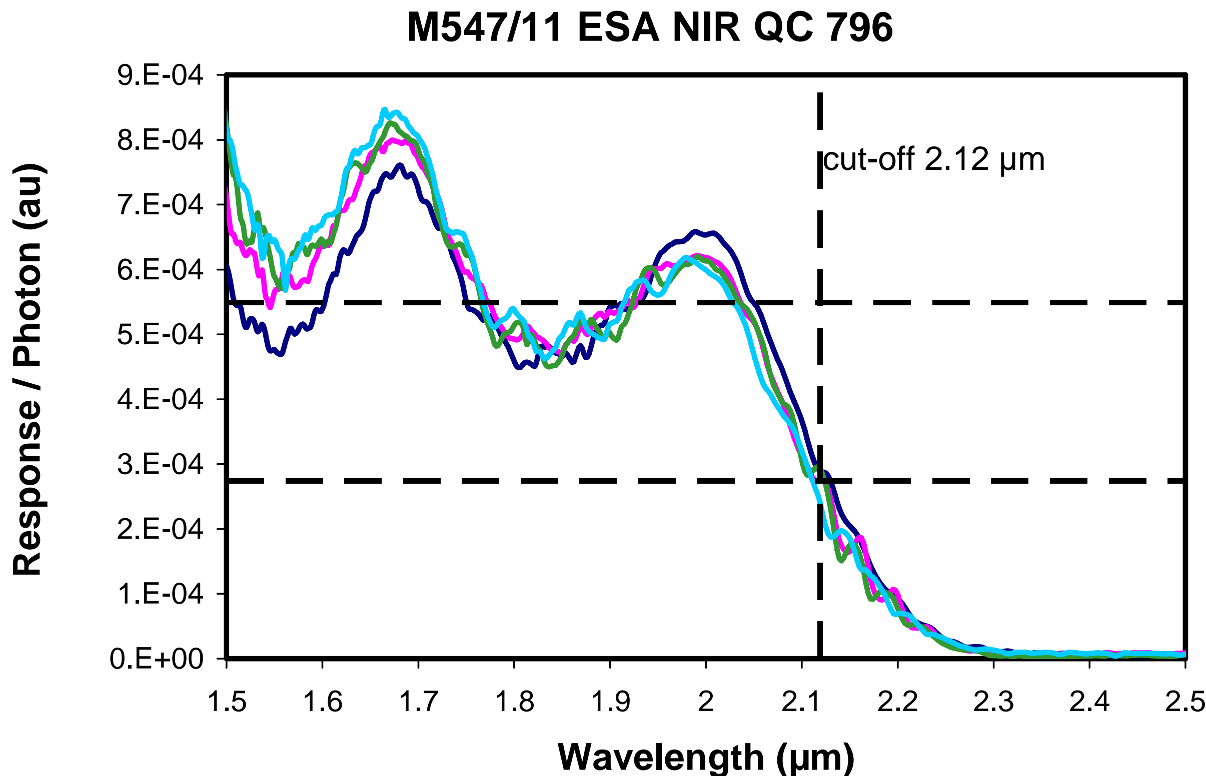
Ceramic is then reconfigured for dark current measurements

- Calibrated source-measurement units (SMU) together with on cold finger MOSFET circuits will be used to measure dark current

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – Testing first Hybrid QC796 from wafer M547



Initial results showed that cut-off was approximately correct.

Colours correspond to different elements

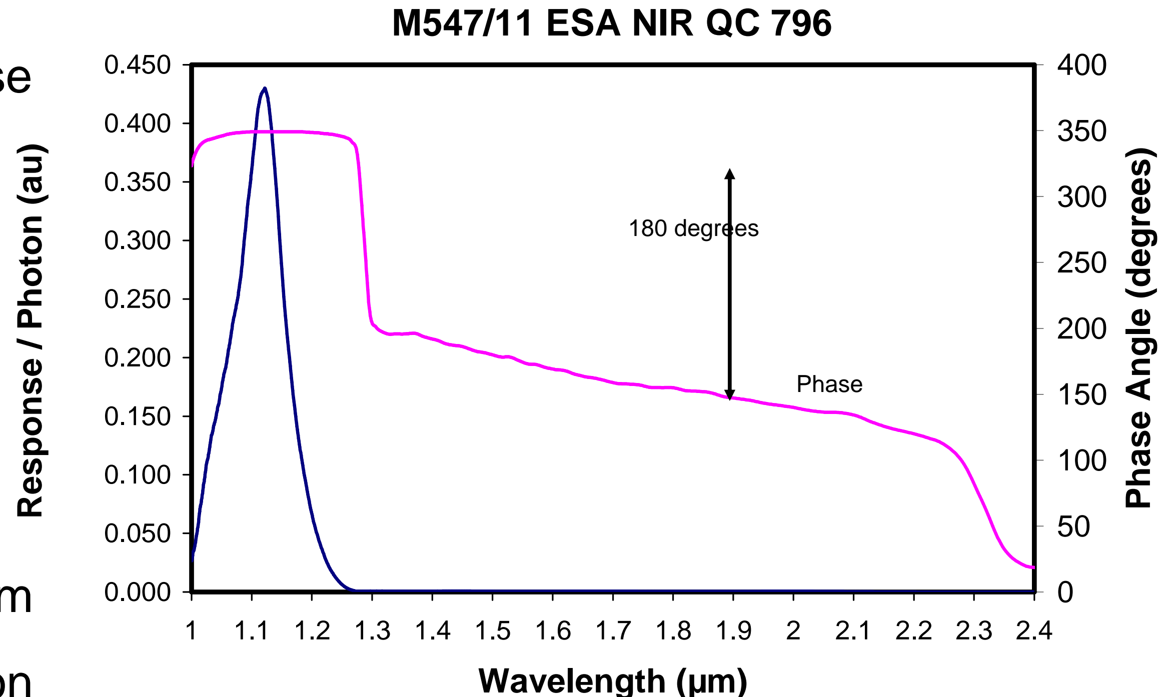
QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – Testing first Hybrid QC796 from wafer M547

Measurements to 1.0 μm

- Massively increased response in SW region
- Signal in SW region is opposite polarity from signal near cut-off
- Signal changes sign at 1.3 μm
  - Corresponds to composition x~ 0.74

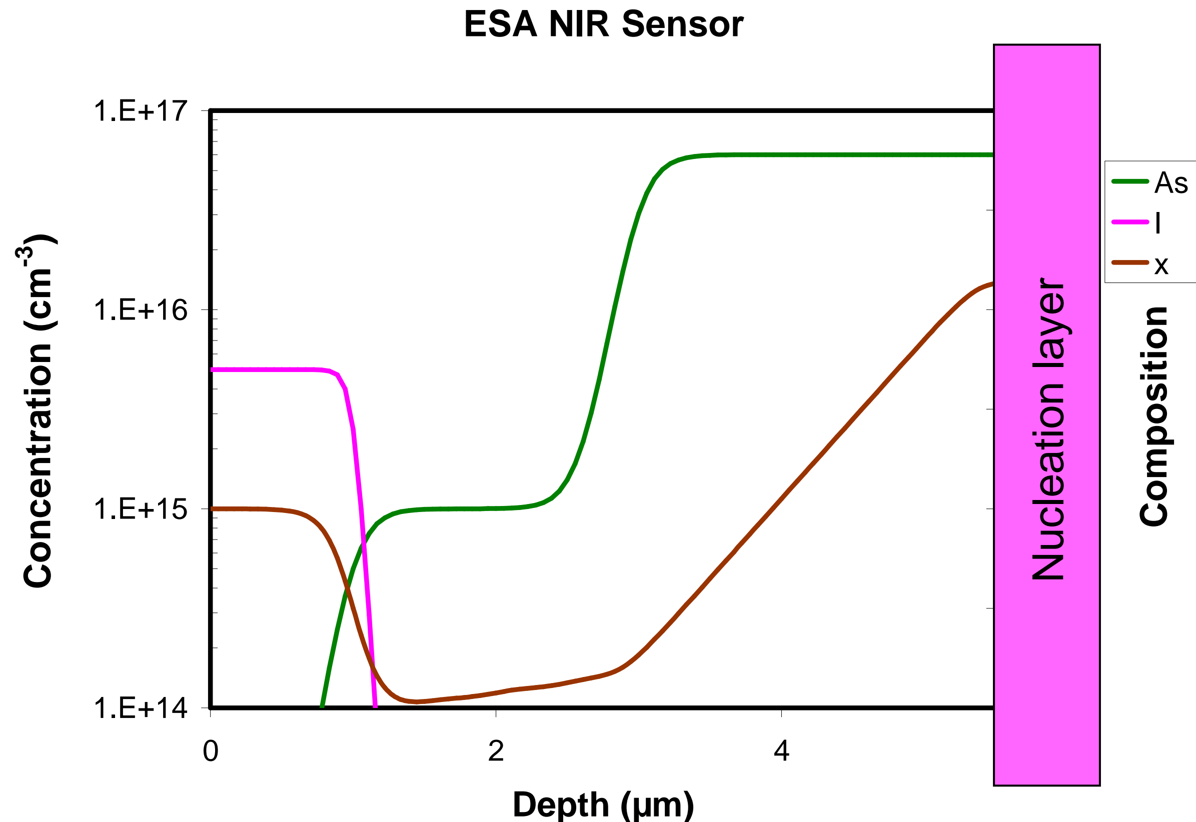


© Copyright QinetiQ Limited 2010

WP3 – Testing first Hybrid QC796 from wafer M547

Location of Inverse Signal

- Composition in design is mainly < 0.71
- The growth is started with a nucleation layer of higher x material which is nominally undoped
  - However, this could be n-type giving a npn transistor-like structure



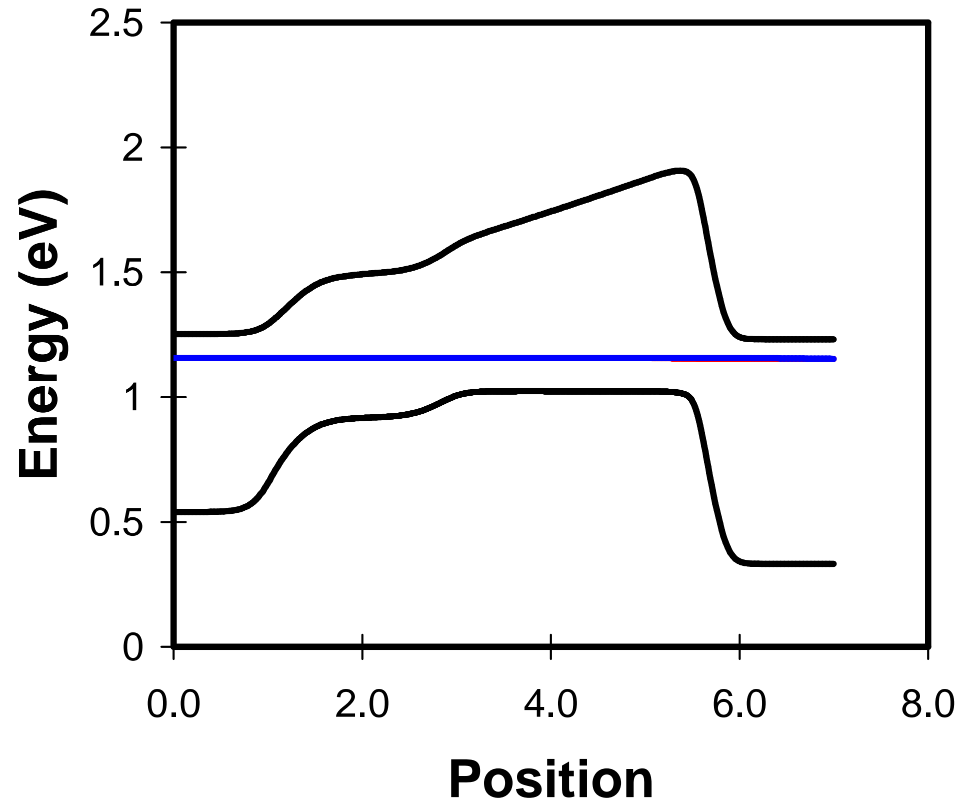
QinetiQ
© Copyright QinetiQ Limited 2010

WP3 – Testing first Hybrid QC796 from wafer M547

Suspected Cause of Negative Signal

n-type nucleation layer accidentally forms part of structure

- Photons with wavelength shorter than 1.3µm will get absorbed in this layer.
- Photo-generated holes will diffuse into common layer from full area of device – very large area detector.



Possible solutions

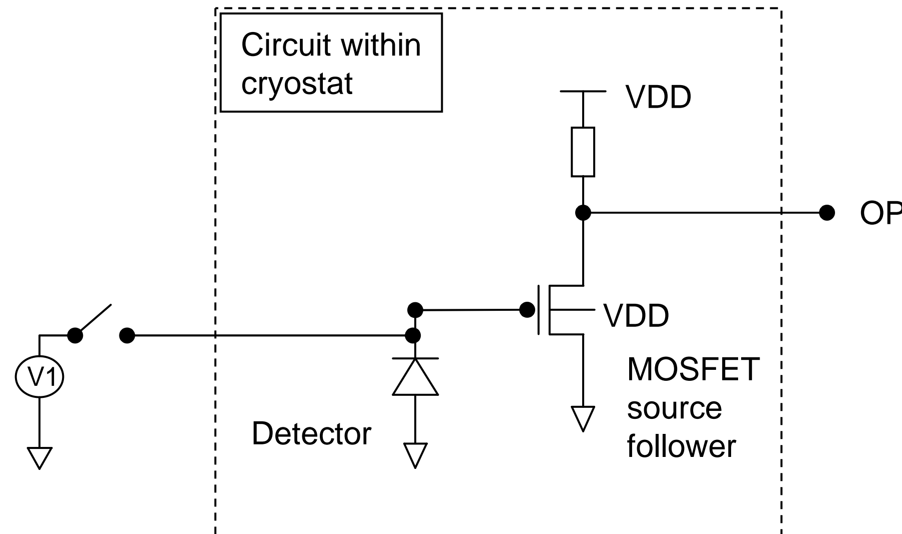
- Add p-doping to nucleation layer
- Etch off nucleation layer + passivate

QinetiQ

© Copyright QinetiQ Limited 2010

WP3 – Testing first Hybrid QC796 from wafer M547

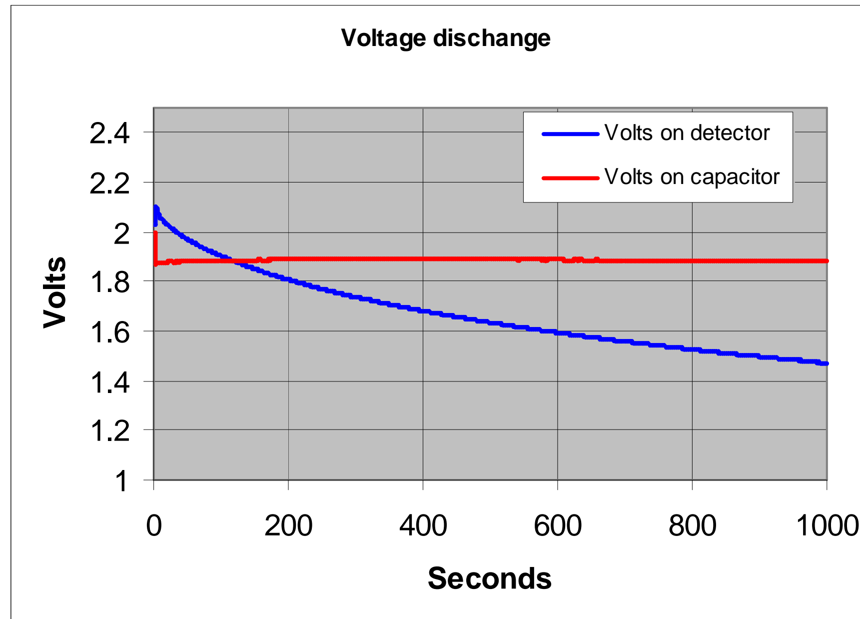
Initial circuit configuration for dark current measurements



- External voltage source used to charge detector
- Voltage discharge monitored using MOSFET source follower
- Identical channel with capacitor instead of detector is used for reference

© Copyright QinetiQ Limited 2010

WP3 – Testing first Hybrid QC796 from wafer M547



- Detector and capacitor channel are charged up to ~2V and allowed to discharge
- Plot shows voltage on detector and reference capacitor
- Detector/capacitor voltage derived from output voltage and MOSFET source follower transfer characteristics

QinetiQ
© Copyright QinetiQ Limited 2010

WP3 - Conclusions on First Device QC796

Spectral results

- Main junction is approximately at the correct wavelength
- However, SW results are being confused by the presence of an unintentional second junction in the structure
- Plan to repeat with p-doping in nucleation layer

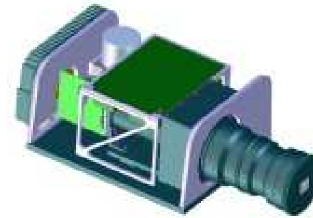
Dark current results

- Still being assessed – but may be leaky due to shorting from passivation
- Layer without passivation is in progress to test this

© Copyright QinetiQ Limited 2010

WP4

Thinning Development



© Copyright QinetiQ Limited 2010

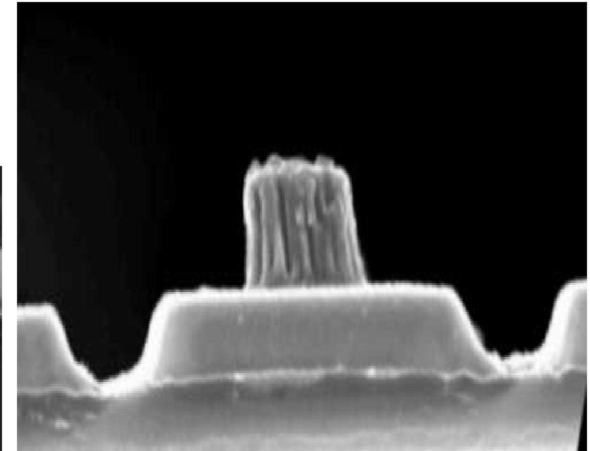
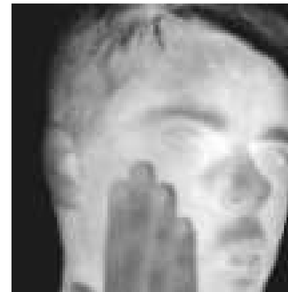
WP4 - Thinning Development Tasks

- Decide on the best etch chemistry - Complete
  - Initial etchant was TMAH
    - Confirmed that the buffer layers were not etched
    - The room temperature etch rate was too slow
  - KOH identified as a better etchant
    - Demonstrated a reasonable etch rate
- Establish a “leadout” protection process - Complete
  - A glue/wax combination has been developed to protect the hybrid
  - Further development would be required for larger detectors
- Confirm whether BOX substrates are required - Complete
  - Buffer layers are readily etched
  - Buried oxide layer confirmed as an etch stop
- Thin final hybrids – In Progress

QinetiQ

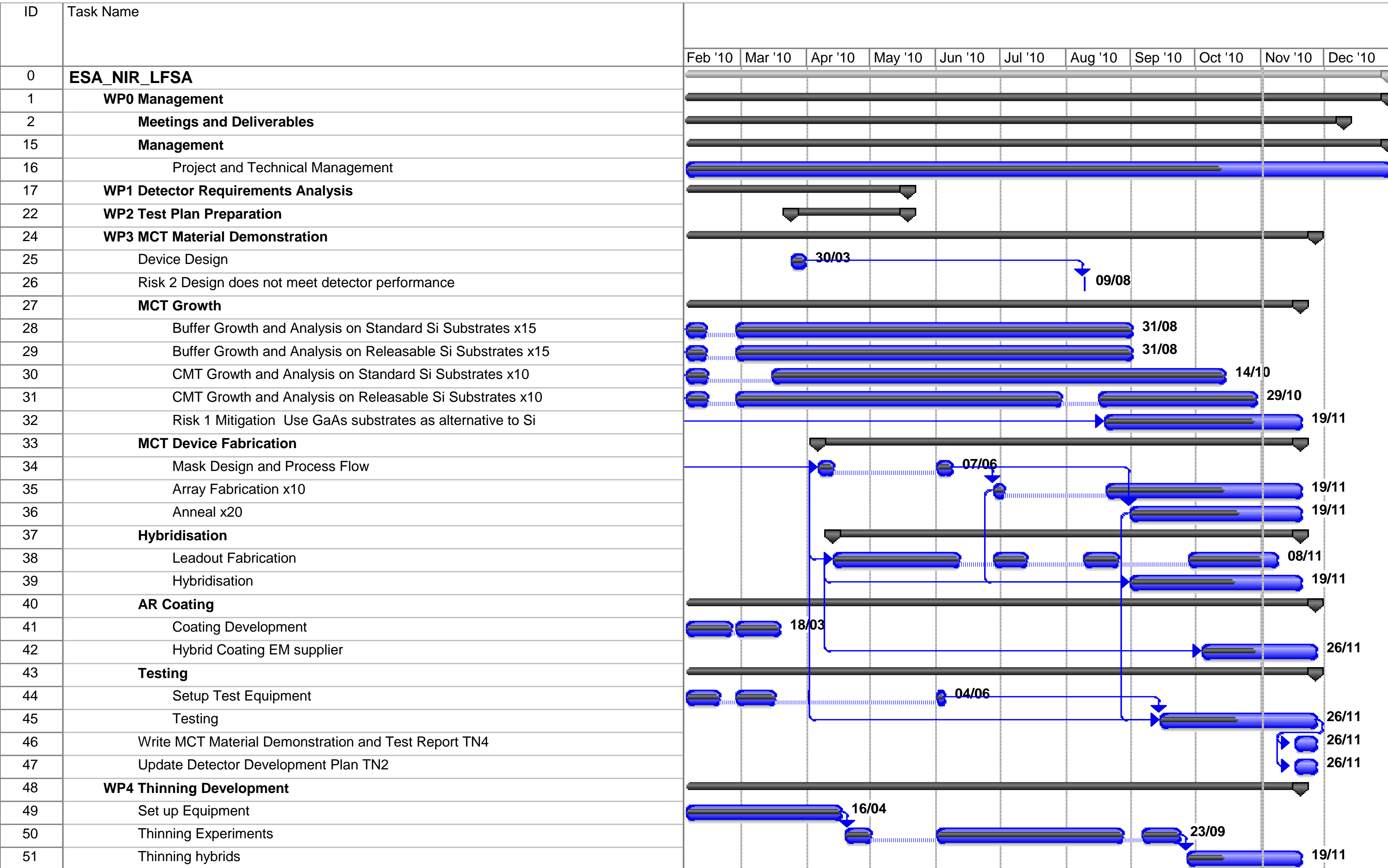
© Copyright QinetiQ Limited 2010

Review of Project Plan

© Copyright QinetiQ Limited 2010

Revised Gantt Chart



Phase 1 Deliverables

Documents

Identifier	Document Title	Delivery Date	
TN1	Detector Requirements Specification	REV-2 weeks	Complete
TN2	Detector Development Plan	REV-2 weeks	Complete, to be updated
TN3	MCT Material Demonstration Test Plan	REV-2 weeks	Complete
TN4	MCT Material Demonstration Design and Test Report	FP1-2 weeks	Still to write
SR1	Phase 1 Summary Report & Abstract & Technical Data Package	FP1-2 weeks	Still to write
PR1-PR8	Progress Reports	Monthly	Complete

Hardware

Item identifier	Description	Delivery Date	Quantity	
HW1	MCT Material Demonstration Test Structures	FP1	1 off	To be delivered

© Copyright QinetiQ Limited 2010

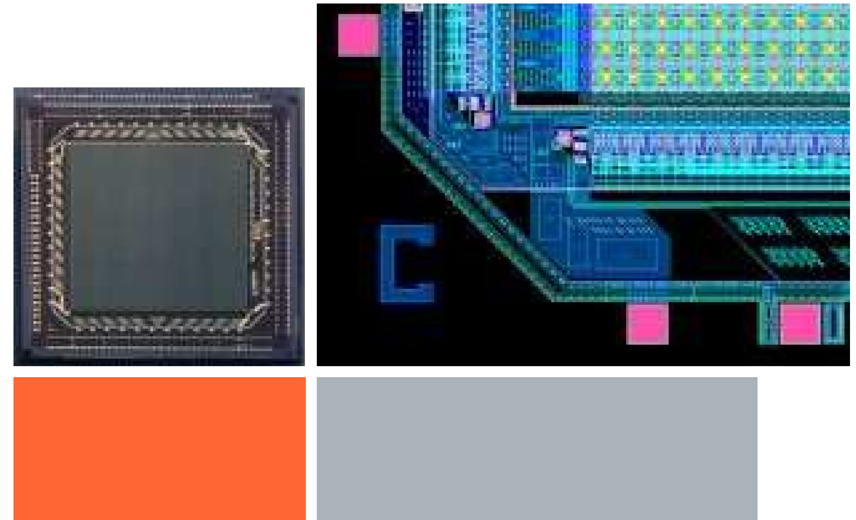
Payment Plan

Milestone	Description	Date	Payment in EUROs	%age
MS1.1	Kick-off Meeting	T0	€104,673	35
MS1.2	Project Review	T0 + 4 months	€164,486	55
MS1.3	Completion	T0 + 10 months	€29,907	10

QinetiQ

© Copyright QinetiQ Limited 2010

Update of Risks



© Copyright QinetiQ Limited 2010

Revised Risk Table

Risk	Mitigation
MCT dark current requirement cannot be achieved.	Use previous QinetiQ NIR data in the device modelling. Feed experimental results back into the model.
Degradation of MCT material quality when growing on substrates with buried oxides.	Initially use standard silicon substrates to verify MCT quality. Use buried oxide substrates manufactured from the QinetiQ standard silicon starting materials.
The substrate thinning process degrades the MCT.	Use QinetiQ standard protection process. Grow on GaAs substrates
Insufficient uniformity of MCT material quality over the FPA size when using the buried oxide substrates.	Use buried oxide substrates manufactured from the QinetiQ standard silicon starting materials.
Scaling the detector size down from the bulk material value to 18 µm degrades the dark current.	Modify the passivation process to improve any surface leakage effects.
Scaling the silicon substrate thinning process to the size of the FPA.	Modifications to the glue protection and multiple etch phases are anticipated to achieve the uniformity. Use alternative silicon etching options e.g. XeF_2.
A ROIC design or manufacturing failure.	Extensive modelling and verification. Hold part-finished batches at the foundry to allow problems to be identified and corrected. Consider reticle stitching throughout the design process.

QinetiQ

© Copyright QinetiQ Limited 2010

QinetiQ

www.QinetiQ.com

© Copyright QinetiQ Limited 2010