ESA AO/1-10269/20/NL/FE,

Preliminary space evaluation of a 0.15-0.1um GaN MMIC foundry process

Executive Summary Report

UMS/R/16-05-2024/BL/047

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List of Acronyms

Cf	Feeback Capacitance of the transistor extracted from S parameter measurement
DC	Direct Current
DEC	Dynamic Evaluation Circuit
DHD	High Density Dielectric for MIM capacitor
DUT	Device Under Test
GaN	Gallium Nitride
GHP	Gate Head Protection
HTOL	High Temperature Operating Life
HTRB	High Temperature Reverse Bias
LNA	Low Noise Amplifier
MIM	Metal Isolator Metal (Capacitor)
MMIC	Microwave Monolithic Integrated Circuit
PCM	Process Control Monitoring
PDK	Process design kit
RF	Radio Frequency
RFLT	RF life test
RIC	Representative Integrated Circuit
SEB	Single Event Burnout
SEE	Single Event Effect
SSPA	Solid State Power Amplifier
TCV	Technological Characterisation Vehicle
THB	Temperature Humidity Bias
TLM	Transmission Line module
WLR	Wafer Level Reliability

1 SCOPE OF THE DOCUMENT

The Executive Summaries Report summaries the activities and the finding achieved during the contract.

2 PROJECT SCOPE

The project aimed to develop and freeze a GaN semiconductor technology for millimeter wave frequency applications for space use. Gallium Nitride (GaN) semiconductor technology is foreseen due to its intrinsic physical properties (high breakdown field, high thermal conductivity, high carier density) to be used for high frequency power amplifier. It represents the next generation in replacement of the Gallium Arsenide (GaAs) due to its higher power density and high voltage operation, and Travelling Waves Tubes Amplifier due to its compactness.

A literature survey performed at the opening of the project highlight the move of space communication toward higher frequency: satellite feeder link, user link, intersatelite communication. This need is accelerated by the new MEO and LEO constallations deployement. Then, it is observed that communication in C and Ka frequency band are moving toward the Q and V band. Available GaN technologies with a space certification today to cover only up to the lowest part of the Q frequency band. A need appear for High power, efficiency and linearity GaN technology for Q and V frequency band space applications: UMS through this project freezed the GH10-10 0.1µm gate length GaN technology and demonstrated its suitability for space applications through a extensive reliability test campaign.

3 UMS GH10-10 DEVELOPMENT IN THE PROJECT

A market and technology survey was performed during the project, aiming to define technology specifications for the technology to be developed to meet application requirements. The table below include a comparison of on-wafer measurements to project target specifications as defined at the beginning of the project.

Technology	**Unit**	GH10-10		
Parameters			Required	Targeted
Power Density @ 45 GHz Optimum PAE	W/mm	2.0	1.8	2.2
Power Density @ 45 GHz Optimum Pout	W/mm	2.2	2	2.4
PAE @ 45GHz Optimum PAE	%	47	40	45
Associated power gain @ 45GHz Optimum PAE	dB	8	8	10
Small signal gain (MAG) @ 45GHz	dB	12.1	10	12
IDS+ - PCM	A/mm	1.55	>1.2	>1.4
Igl Gate leakage Vds=20V VG=-7V	µA/mm	300	<600	<500
Gm max Vds=+7V - PCM	mS/mm	540	>400	>450
Recovery time	µs		<100	<75
Fmax	GHz	207	>150	>165
Ft	GHz	52	>70	>80
MTF (Median Time to Failure)@ 200°C	Year		20	20-220°C

Figure 1: Key electrical parameters representing the performance of GH10-10, in comparison to the project target specification.

During the process development of the GH10-10 technology, different epitaxy suppliers and process variants have been evaluated to define the final epi and process (gate passivation) for the freeze of the GH10-10 technology in 2021.

The so called baseline 1 exhibit a low output power survived up to drain voltages of around 50V under high electric field stress conditions. Process adjustments to target higher output power resulted in rather early degradation in reverse bias stress tests. Wafers with output power above 3W/mm showed already Schottky degradation for drain voltages of around 15V.

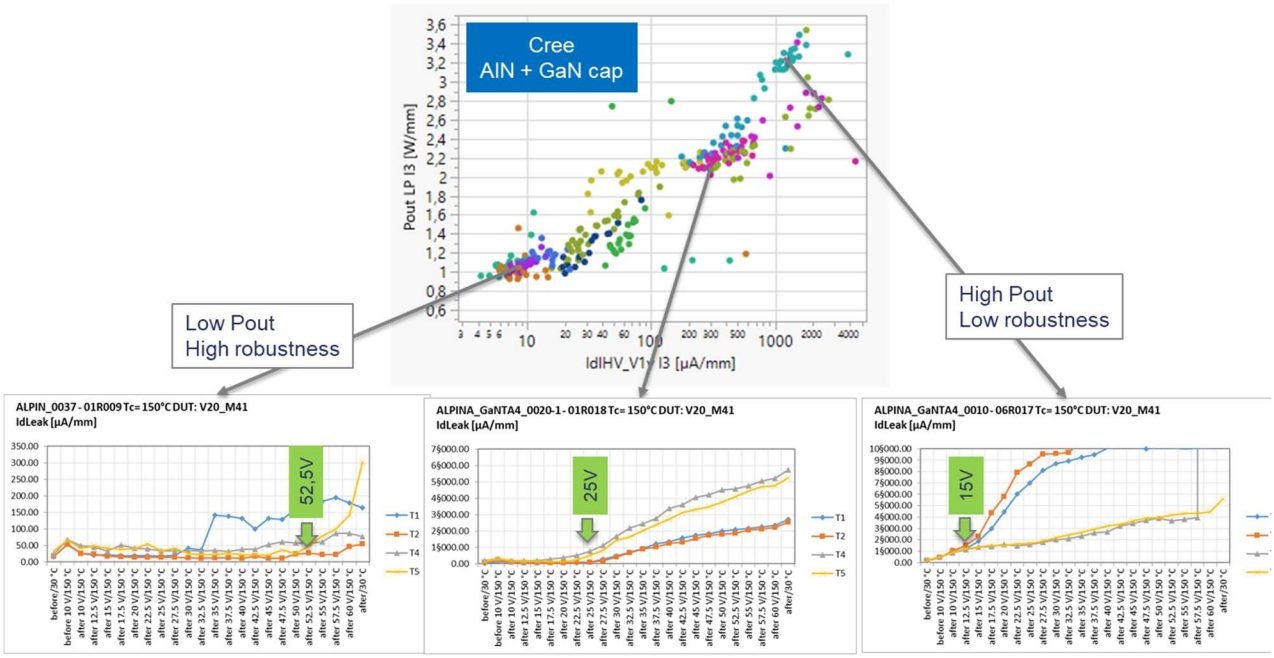

Figure 2: top: trade-off between performance (output power) and leakage current. Bottom: leakage current and degradation voltage (Vdeg) during step stress test at high temperature for devices with low, medium and high performance.

The original process freeze end 2021 had thus been decided to postpone by two years to try to understand the root cause for the HTRB degradation of baseline 1 and to optimize the process with major process changes.

The main root cause for the Schottky degradation was identified to be due to the very high electric field peak next to the gate foot at the interface to the epitaxy. Thus the focus on process optimization was put on electric field engineering with small field plates.To reach this a new gate approach had to be evaluated and implemented. Two process iterations were needed to define the final process and the GH10-10 technology could be frozen end 2023 based on HTOL and HTRB reliability results within the ESA program. With the new gate process the Schottky stability could be improved significantly with no degradation up to 60V.

4 PRE-SPACE EVALUATION TEST PLAN

Two wafers from two different lots were used for this reliability evaluation.

Lot id	wafer	lot nickname	Mask set	Idleak_HV µA/mm	Pout W/mm @9GHz	Ids++ A/mm	DIBL V/V	Vt (V)
I3 Specification limit V1DC				Na	[1.5 ;4.5]	[0.9 ;1.7]	0.03	[-4;-1]
V1Y (multi finger)				[1000 ; 0]	Na	Na	na	
E031523	6R	EVEREST_0002	EVEREST	18.4	2.74	1.56	0.017	-2.88
E284123	5R	EVEREST_0006	EVEREST	95.5	2.76	1.57	0.018	-2.9

Table 1. Wafer table manufactured for GH10-10 technology evaluation

4.1 Reliability Test plan

The reliability space assessment test plan executed during the project is describe in the table below. Two packaged test vehicles were used to execute the plan: The DEC_GH10_D00A based on Individual Source Via transitor topology as ground configuration and the DEC_GH10_D10A based on Air bridge source interconnection. These two transistor source interconnection topologies would be available in the GH10-10 technologie.

Test Id	Reliability batch	Lot-wafer	Type of test	Devices	Qty	Conditions	Outcome	Status
STO1		EVEREST_0006-3R	Storage	PCM / On wafer	1	T = 250°C	Life time extrapolation (Ea)	
STO2		EVEREST_0006-4R	Storage	PCM / On wafer	1	T = 325°C		
GH10_ISV_HTRB1	U300823	EVEREST_0002-6R	HTRB	GH10_D00A (ISV)	10+1ref	Vds = 30V Vgs = -7V Tc = 175°C	2000hr	2000hrs no failure
GH10_ISV_HTOL1	U300723	EVEREST_0002-6R	HTOL	GH10_D00A (ISV)	10+1ref	Vds = 15V Ids = 200mA/mm Tj = 280°C Tc = 170°C	Life time extrapolation Ea determination 70% failure	Stoppped at 4000hrs
GH10_EV6_HTOL1	U450123	EVEREST_0006-5R	HTOL	GH10_D00A (ISV)	10+2ref	Vds = 15V Ids = 200mA/mm Tj = 280°C Tc = 170°C		3000hrs Test in progress
GH10B8_D00_HTOL2	U411323	EVEREST_0002-6R	HTOL	GH10_D00A (ISV)	10+1ref	Vds = 15V Ids = 200mA/mm Tj = 310°C Tc = 180°C		Stoppped at 4000hrs
GH10_EV6_HTOL2	U450223	EVEREST_0006-5R	HTOL	GH10_D00A (ISV)	10+2ref	Vds = 15V Ids = 200mA/mm Tj = 310°C Tc = 180°C		3000hrs
GH10_TZ2_HTOL1	U301023	EVEREST_0002-6R	HTOL	GH10_D10A (TZ)	10+1ref	Vds = 15V Ids = 200mA/mm Tj = 280°C Tc = 165°C		Stopped at 1000hrs 8p/10p extrinsic failures
GH10_TZ2_HTOL2	U301123	EVEREST_0002-6R	HTOL	GH10_D10A (TZ)	10+1ref	Vds = 15V Ids = 200mA/mm Tj = 280°C Tc = 165°C		Stopped at 96hrs Not exploitable 9p/10p extrinsic failures
GH10B8_D10_RFLT	U411123	EVEREST_0002-6R	RFLT	GH10_D10A	4+1ref	Vds = 15V Ids = 150mA/mm Frequency = 9.5GHz Pin such as PAEmax + 1dB Tj = 200°C Tc = 100°C	2000hr	>3000hrs

GH10B8_D10_RFST	U411223	EVEREST_0002-6R	RFSST	GH10_D10A	4+1ref	Vds={15; 17.5; 18; 18.5; 19; 19.5 ; 20; 21; 22}/power cycles Ids = 150mA/mm Frequency = 9.5GHz Pin steps such as PAEmax PAEmax + 1dB PAEmax + 2dB PAEmax + 3dB Tcase = 75°C	Stopped at the third failure	Third failure not reached
GH10-TZ -THB	U040424	EVEREST_0002-6R	THB	GH10_D10A Open lid	5+1ref	Vds = 15V Vgs = -7V Tc= 85°C RH = 85%	1000hr	846hrs - stopped
GH10-ISV -THB	U512223	EVEREST_0002-6R	THB	GH10_D00A Open lid	5+1ref			
GH10-ISV-RAD	U512123	EVEREST_0002-6R + EVEREST_0006-5R	SEE	GH10_D00A Open lid	6	Semi On state: Ids = 200mA/mm, Vds = 15V +2.5V Pinch off : Vgs = -7V, Vds= 15V +2.5V	SEB determination	Completed
GH10-TZ-RAD	U040324	EVEREST_0002-6R + EVEREST_0006-5R	SEE	GH10_D10A Open lid	6	Semi On state: Ids = 200mA/mm, Vds = 15V +2.5V Pinch off : Vgs = -7V, Vds= 15V +2.5V		completed
SEE-Capa_Std		EVEREST_0002-6R	SEE	P18A	3(x20)	Vcapacitor [150-200V]	SEDR determination	
SEE-Capa-DHD		EVEREST_0002-6R	SEE	P18B	3 (x20)	V capacitor [50-85V]	SEDR determination	

Table 2: Reliability test plan executed during the project

5 TEST RESULTS

5.1 Storage

To assess the behaviour of components under temperature, storage in nitrogen ambient was performed at wafer level at 250°C and 325°C. No failure is reported after 1000hrs of test

5.2 End of life assessment

A High Temperature Operating Life test is performed to accelerate the failure mechanism. Two HTOL tests will be performed to extract an activation energy and an extrapolated life time. Test conditions are reported in the table below.

For each HTOL test, 10 DECs were submitted to the aging tests with at least one reference devices Interim measurement are performed to observe the degradation of the devices. The tests will be ended after 70% of failure.

The primary failure mode of wear out mechanism observed during the various HTOL tests is a decrease of the saturated power and a decrease of the Ids plus parameters. The evolution of this two parameters are correlated and seem to reflect the same degradation mechanism. Meanwhile, two degradation kinetics are observed on POUT2 and IDS+ and seem to be related to the position of the transistor in the maskset. The life time was extrapolated based on SRET2 life test results and SRET1 results separaretly.

For SRET2 devices , an activation energy of 1eV is extracted based on IDS+. A very low activation energy of 0.6eV is achieved based on POUT2. The large spread and the low statistics of the results lead to low confidence in the results. On the different HTOL test, the failure criteria is not reach on SRET1 devices allowing a time to failure extraction.

In order to estimate the end of life of SRET1 devices, the elapse time of the three life test and the T50% extrcated on one life test is reported in the Arrhenius graph below.

An extrapolated life is plotted based on activation energy of 1eV found for SRET2. It is used because the same degradation kinetic is observed. The tests need to be extended to consolidate this reliability figure.

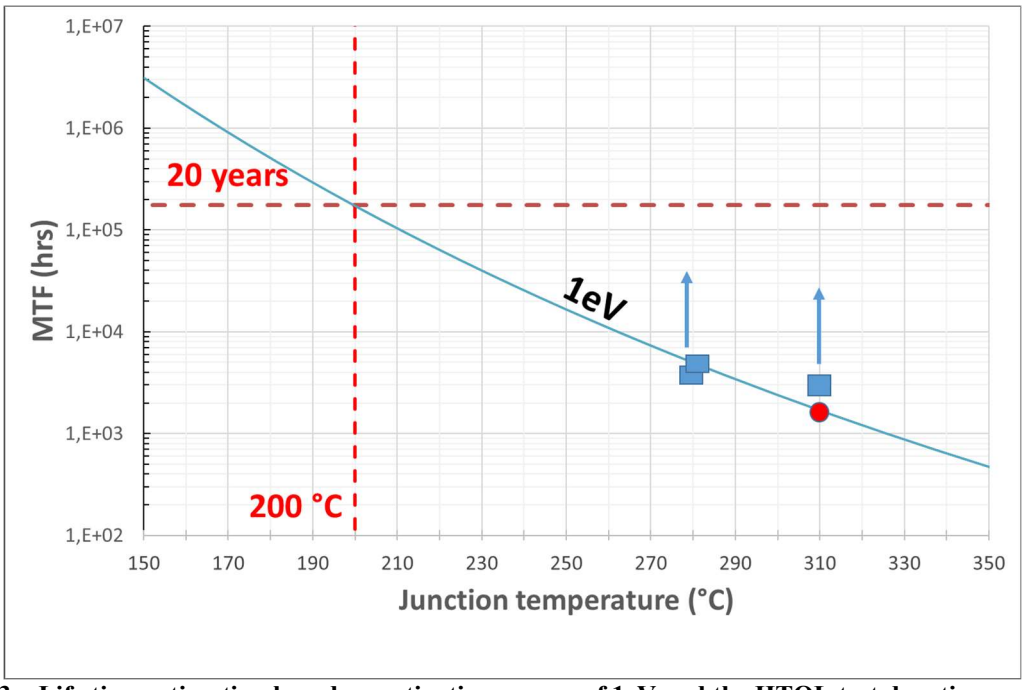

Figure 3 – Life time estimation based on activation energy of 1eV and the HTOL test duration on SRET1

5.3 Gate robustness assessment

A High Temperature Reverse Bias test is performed to check the robustness of the Schottky contact. No failure was observed during after 2000hr of test, demonstrating robustness of the Schottky gate contact.

5.4 High RF power compression stability

RF Life Test is performed to observe device behaviour under high RF power compression.

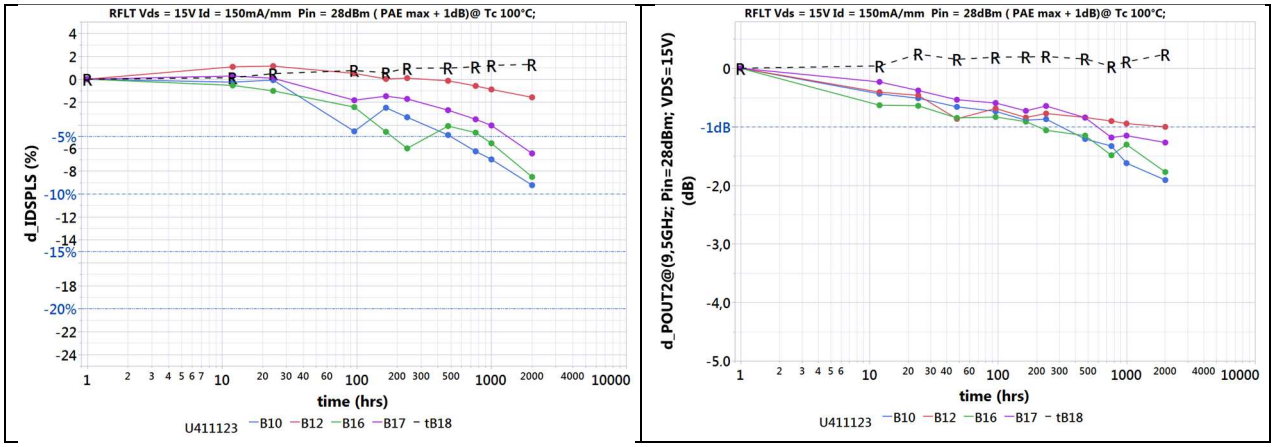

Figure 4 – Electrical parameters evolution during the RF life test on EVEREST_0002-6R (U411123)

The output power continuously decreases without sign of saturation and the failure crietria of -1dB is reached for 3 parts before 1000hrs of test. The same trend is also observed on the output power monitored during the RFLT. The saturated output power seems to degrade faster than the IDS+ at 1000hrs : whereas the Pout2 drift is beyond 1dB, the drift ot IDS+ is around -5%. The same root cause could explain the degradation observed in RFLT and observed on SRET2 devices in HTOL

5.5 Limit of operation assessment

RF Step Stress Test is performed to assess the limit of operation of the technology under high electric field and high compression.
Test start at operating condition. Then every 24 hours in mimum, the input power is stepped up

After the step at Vds=19.5V and Pin=28dBm, the IGLHV after each step stress. The maximum ating is established at Vds = 19V / PAEmax +1dBm

5.7 humidity sensitivity assessment

Thermal Humidity Bias life test is executed to observe the humidity sensitivity of the technology. Devices are bias under pinch off condition (no thermal dissiation), package opened air cavity and the conditions are defined as 85% of Relative Humidity and a case temperature of 85°C as described in JEDEC standard (JESD22-A101). The humidity sensisivity of the technology was evaluated on both ISV and TZ.

Whereas, the leakage current increase stongly after 50hrs of THB test for TZ transistor then increase continuously to reach the failure criteria of 1mA/mm. ISV transistors are less sensitive to humidity than TZ transistors.

5.8 Radiation hardness assessment

Radiation hardness of the GH10 will be assessed under heavy ion. The test was focus on two devices of the technology: the transistor and the capacitor.

The radiation test was focussed to validate the Single Event Burn-out (SEB) limit under a Xenon ion (highest LET) up to a fluency of 10^7 atom/cm².
Single Event Effect (SEE) limit was validated on three devices (DEC and MIM capacitor).
The SEE was validated on two TZ transistors and one ISV transistor for these two biasing conditions at Vds=40V.

The SEE was validated for semi-on state biasing condition of Vds=20V on two TZ transistors and one ISV transistor.

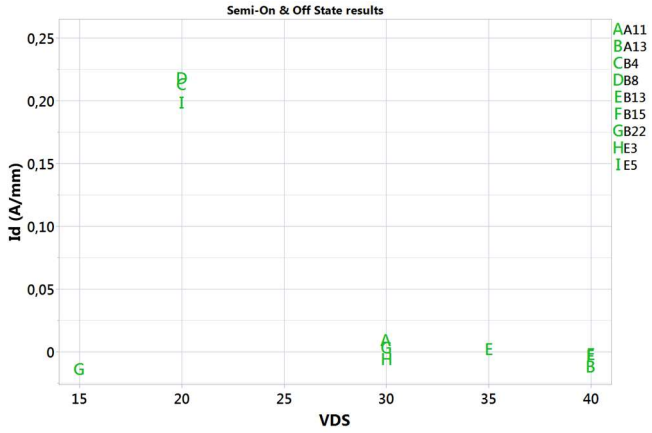

Figure 5 – Summary of SEE tests on transistor

Single Event Dielectric Rupture (SEDR) of DLD (Dielectric Low Density) MIM and DHD (Dielectric High Density) capacitor was determined by applying different voltage on the different capacitors in the package during one radiation shot. Then, the voltages will be step up to surround the SEDR value. The first failure occurs at 30V for DHD capacitor and 57.5V for DLD capacitor.
The SEE limit is set at :

- 27,5V for DHD
- 55V for DLD

5.9 Preliminary Safe Opertaing Area

Based on these results a preliminary Safe Opertaing Area can be defined :

Transistor for Power Amplifiers					
Parameter	**Symbol**	**Conditons**	**Unit**	**ROR**	**AMR**
Drain-Source Biasing Voltage	Vds	Idq = 150mA/mm	V	15	19
RF compression such as Pin equal to:		Linear point at 10dB back off from Pout such as Ig > 0	dB	5	7
Gate-Source Voltage (DC+RF)	Vgs	Under ROR dc biasing conditions	V	-8	
Drain-Gate Voltage (DC+RF)	Vdg		V	32	
Gate Current	Ig	Forward	mA/finger	2	
Peak Junction Temperature	Tj	Under ROR dc biasing conditions	°C	200	

Table 3. Preliminary recommended and absolute maximum rating for Hot-FET topology

MIM capacitor type	Parameter	Unit	ROR	AMR	Space rating
DLD non over via	Voltage (DC+RF)	V	80	130	55
DLD over via	Voltage (DC+RF)	V	80	130	55
DHD non over via	Voltage (DC+RF)	V	50	70	27,5
DHD over via	Voltage (DC+RF)	V	50	70	27,5

Table 4. Preliminary recommended and absolute maximum rating for MIM capacitor

6 CONCLUSIONS

Along the project, the 0.1µm UMS GH10-10 GaN technologies has been freezed to cover millimetrewave applications. Based of the market and technology survey, the achieved RF performences are in line with the state of the art with a power density of 2.2W/mm and 45% of PAE at 45GHz.

The major difficulties in the development of such technology is to achieved both the RF performances and the reliability together. Indeed, a clear correlation of the output power density and PAE with the Schottky degradation under high electric field has been observed. The Schottky degradation consist of an increase of the parasitc parallel leakage path to the Schottky contact. During the development, the gate process module has been optimized to smooth the electric field while achieving RF perfromences. On freezed wafer on an extensive reliability test demonstrated a safe operating area comptatible with 20years life time at a channel temperature of 200°C. Heavy ion test campaign on transistor and low&high density MIM capacitor allows to determine a SEE Radhard domain for the technology compatible to space operation.

This project supported the developpement and the freeze of the UMS GH10-10 technology. It has been demonstrated that the technology is compatible to space applications and is now in qualification phase at UMS.

As perspective, UMS entrering in a commercial qualification phase of the technology and the next step would be a space evaluation for an ESA EPPL entry.