SLA-SiPM Final Presentation

ESA Contract No. 4000111544/14/NL/SC

10/December/2015

Program Overview

Program Details

- SLA-SiPM (Scalable Large Area SiPM)
- ESA Contract No. 4000111544/14/NL/SC
- Kickoff: June 2014
- Planned Completion Date: December 2015
- Milestones
  - Progress (MS 1): Upon successful completion of Task 1 and successful TSV Development Review and acceptance of all related deliverables
  - Progress (MS 2): Upon successful completion of Task 2 and successful Qualification Review and acceptance of all related deliverables
  - Final Settlement (MS 3): Upon the Agency's acceptance of all deliverable items due under the Contract and the Contractor's fulfilment of all other contractual obligations including submission of the Contract Closure Documentation

Goals

- Develop a through silicon via (TSV) large area SiPM package
  - High fill factor in package
  - High fill factor in array
  - High photon detection efficiency (PDE)
  - Magnetic resonance imaging (MRI) compatible
- Produce a large area SiPM product
  - Product driven by market requirements
  - Perform qualification and reliability testing
- Produce an array from the large area SiPM
  - Perform qualification and reliability testing
- Validate product with external customers

Task Overview

- Task 1 - TSV Development
  - Development of the Through Silicon Via (TSV) Process
- Task 2 - TSV Qualification & Reliability
  - Qualification and reliability assessment of a large area SiPM manufactured in a TSV process
- Task 3 - Array Development
  - Production of a large area array based on large area SiPM
- Task 4 - Program Management
  - All program management
  - TN1, TN2, TN3, TN4, Final Presentation (this document)

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History of SiPM Development with ESA

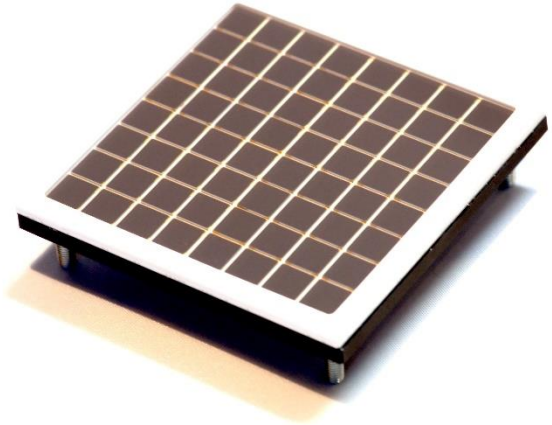
Products

SPM Matrix Product
M-Series (NonP)

B-Series Product
(PonN)

ESA Programs

DESSA1 & DESSA2



ESSA & TQSPM

J-Series 6 mm

SLA-SiPM

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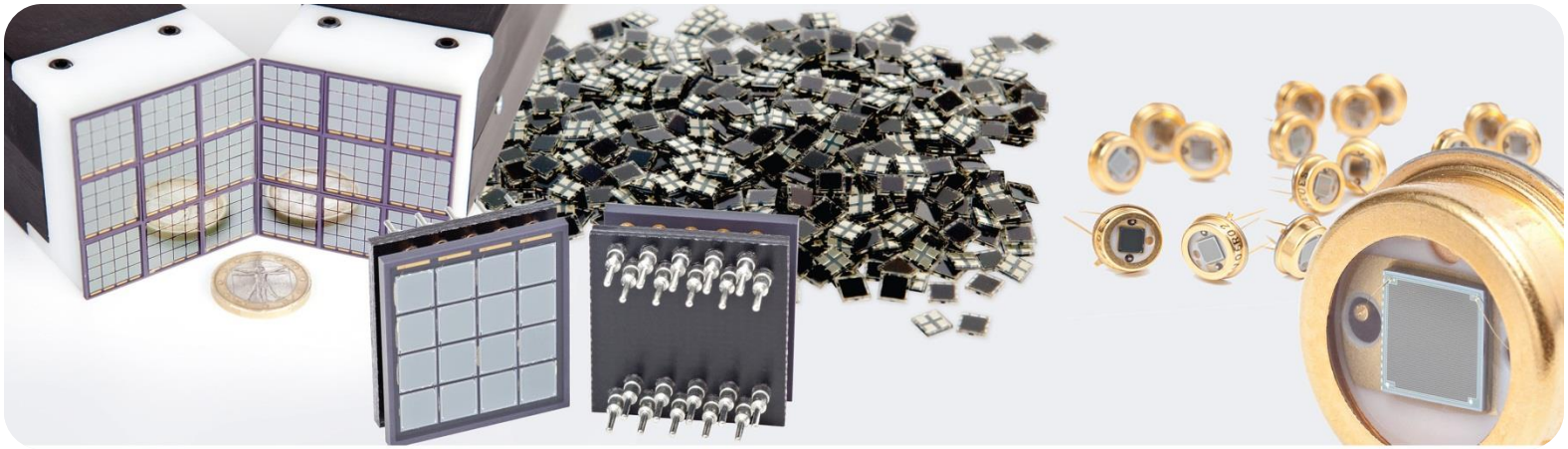
Background

SensL Quick Facts

Business	Low Light Sensors
Markets	Medical Imaging Radiation Detection (H&T) Automotive 3D Ranging and Sensing High Energy Physics
Model	Fabless Semiconductor

- Established 2004
- ISO9001:2008 Certified



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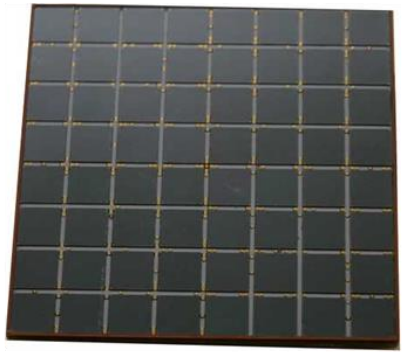
SensL Advantages

Photomultiplier
Vacuum Tube

SensL Advantages:

Performance
Uniformity
Large Area
Form Factor
Low Cost



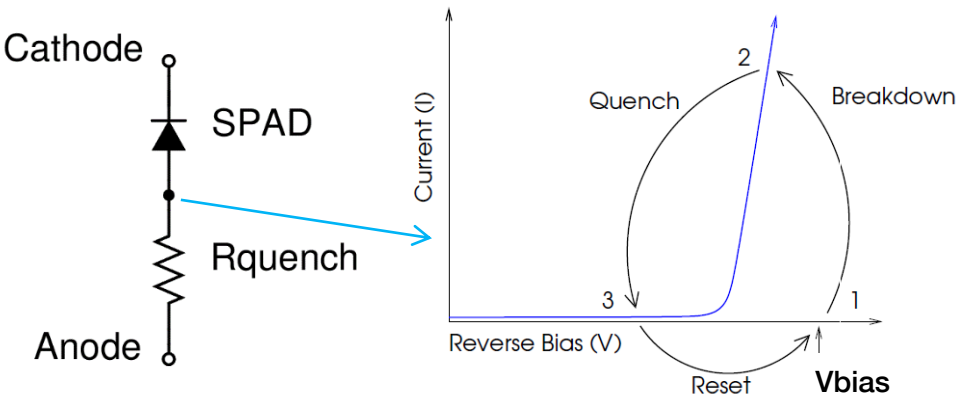
SensL
Silicon Photomultiplier

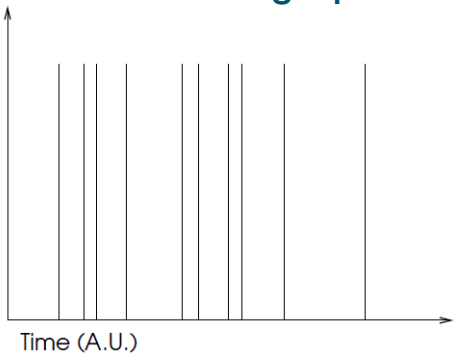
Overview of SPAD and SiPM Sensors

SPAD

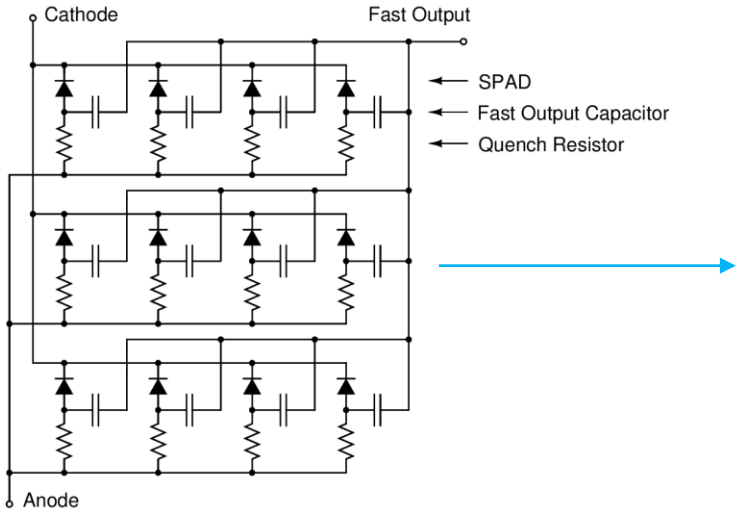
SiPM

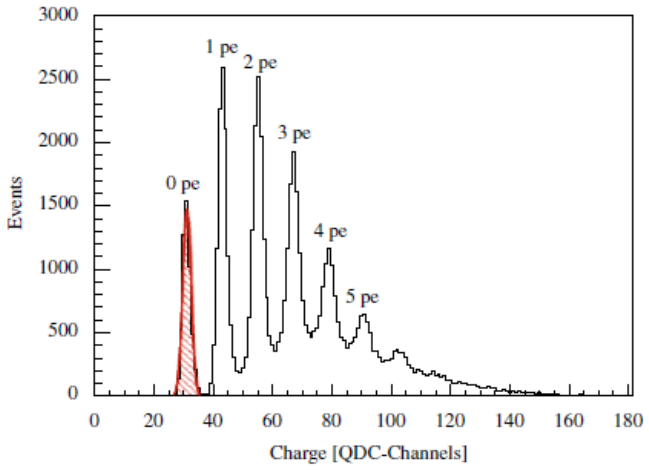
Time or count single photons





Time or count multiple photons





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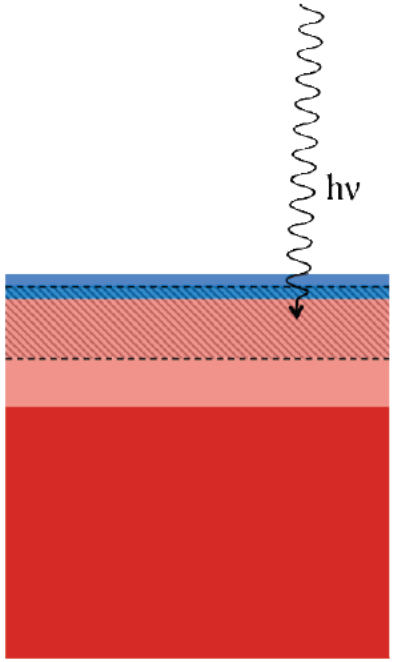
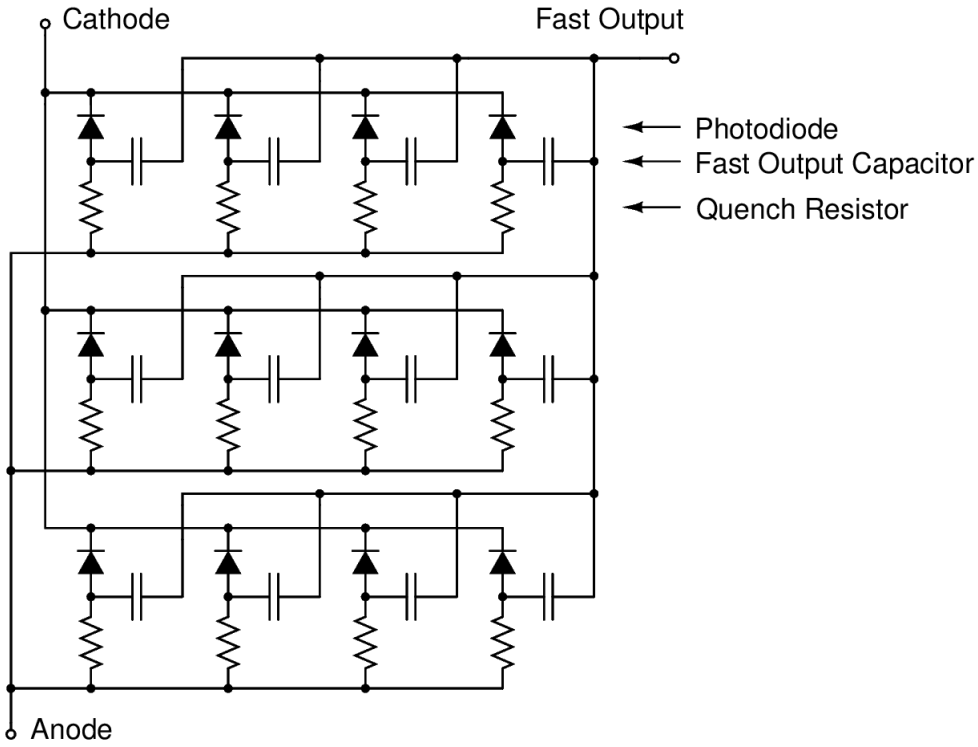
SiPM Technology
B-Series, C-Series & J-Series



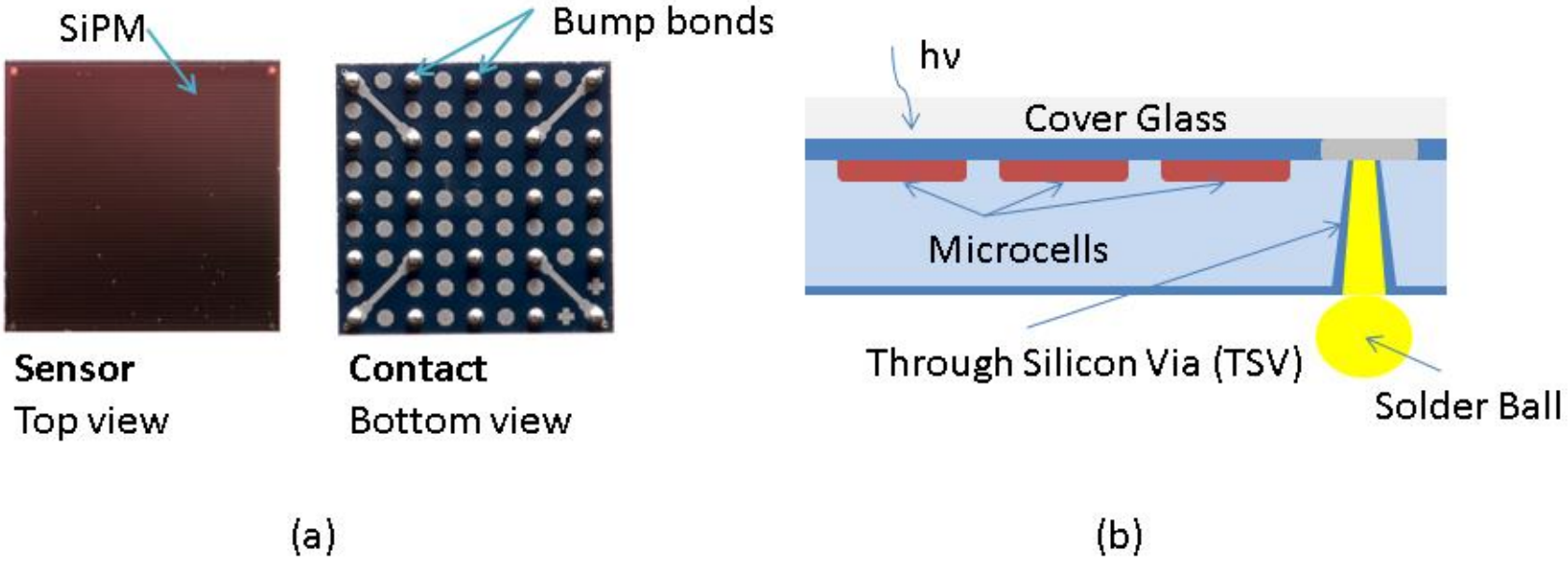


P on N technology provides the highest levels of Blue and UV photon sensitivity

Compatible with Fast Output (3-terminal) & Standard Output (2-terminal)

Through Silicon Via (TSV) Overview

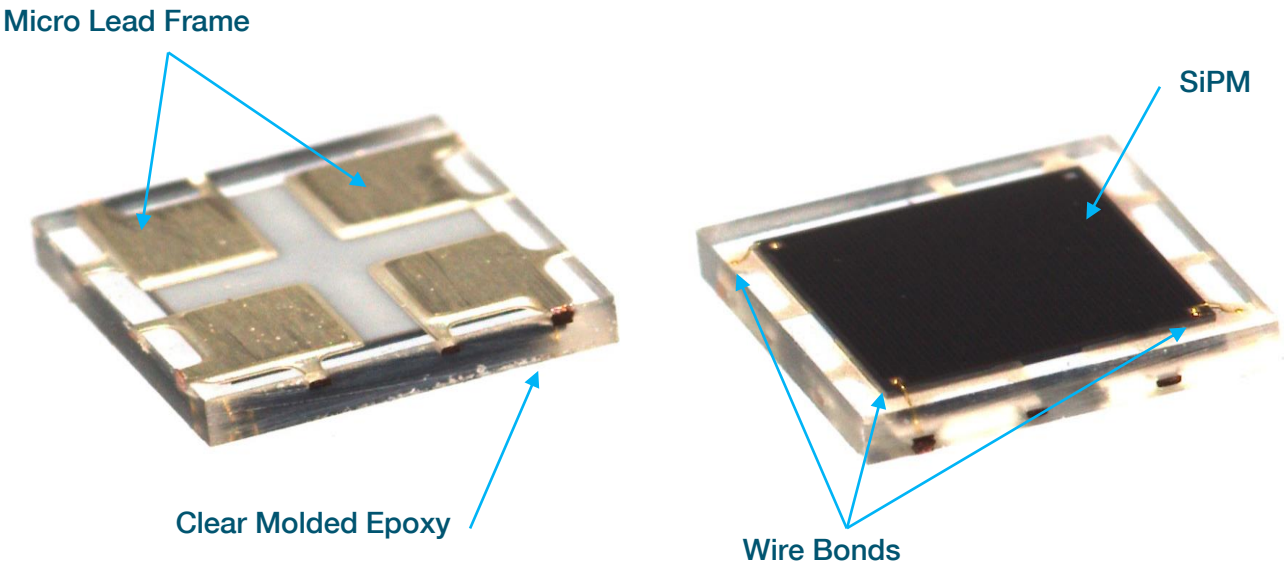
SensL's Through Silicon Via (TSV)



Advantages of the SensL TSV package

- No ferrous metals and No wire bonds
- SensL's TSV process is a true wafer scale package
  - SiPM can be placed directly on PCB by customers with minimal deadspace

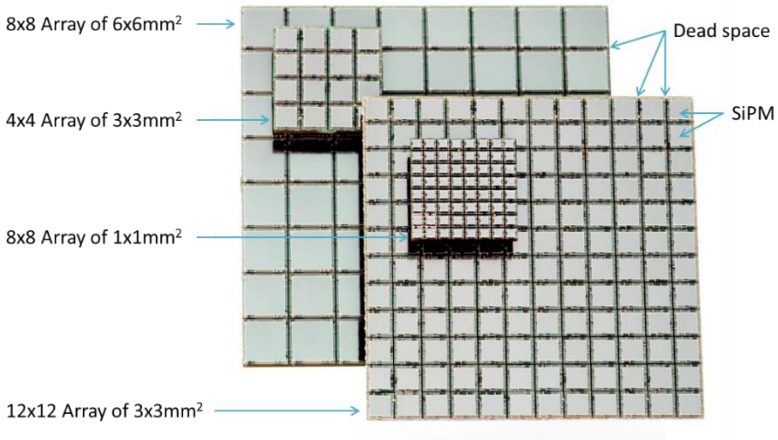
Why TSV?



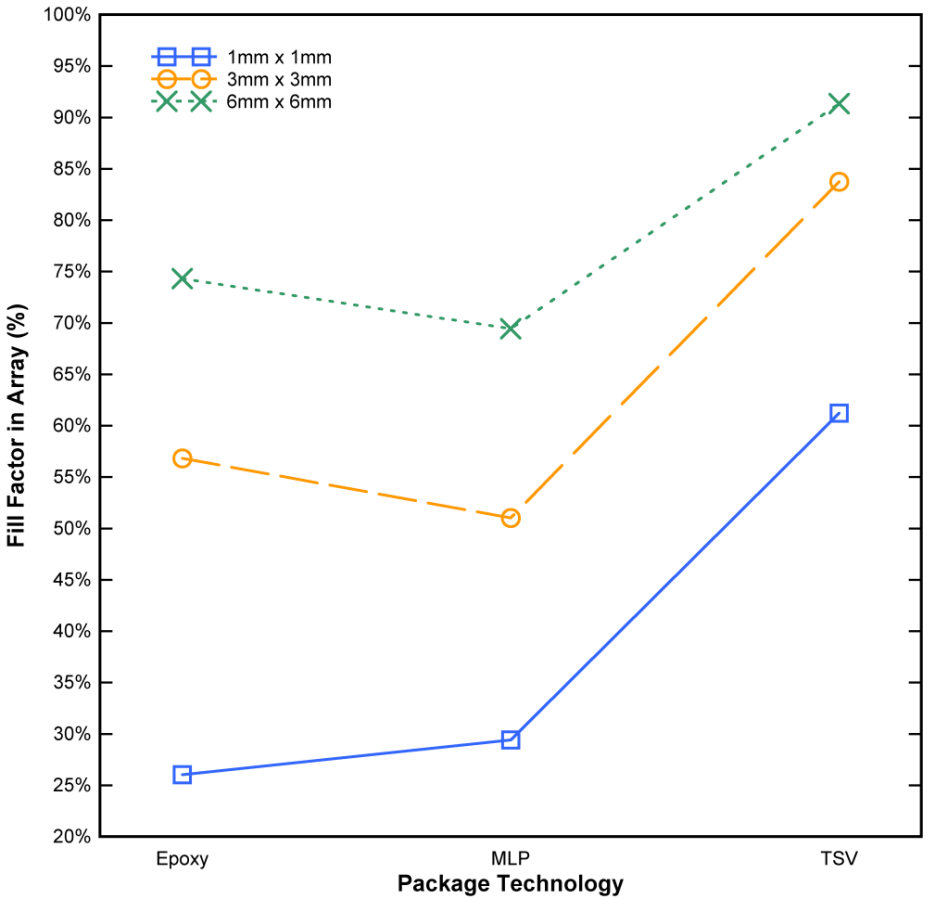
Die Size	Package Size	Active Area Fill Factor
1mm x 1mm	1.5mm x 1.8mm	37%
3mm x 3mm	4mm x 4mm	56%
6mm x 6mm	7mm x 7mm	73%

TSV High Fill Factor

Clear MLP SMT Arrays



TSV Array Fill Factor Comparison



TSV Arrays provide >90% fill factor for 6mm x 6mm SiPM

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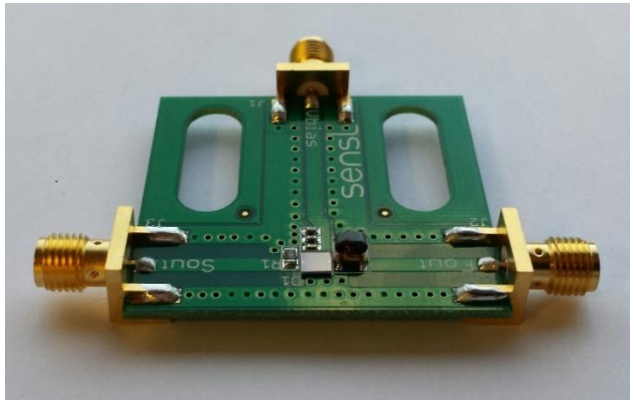
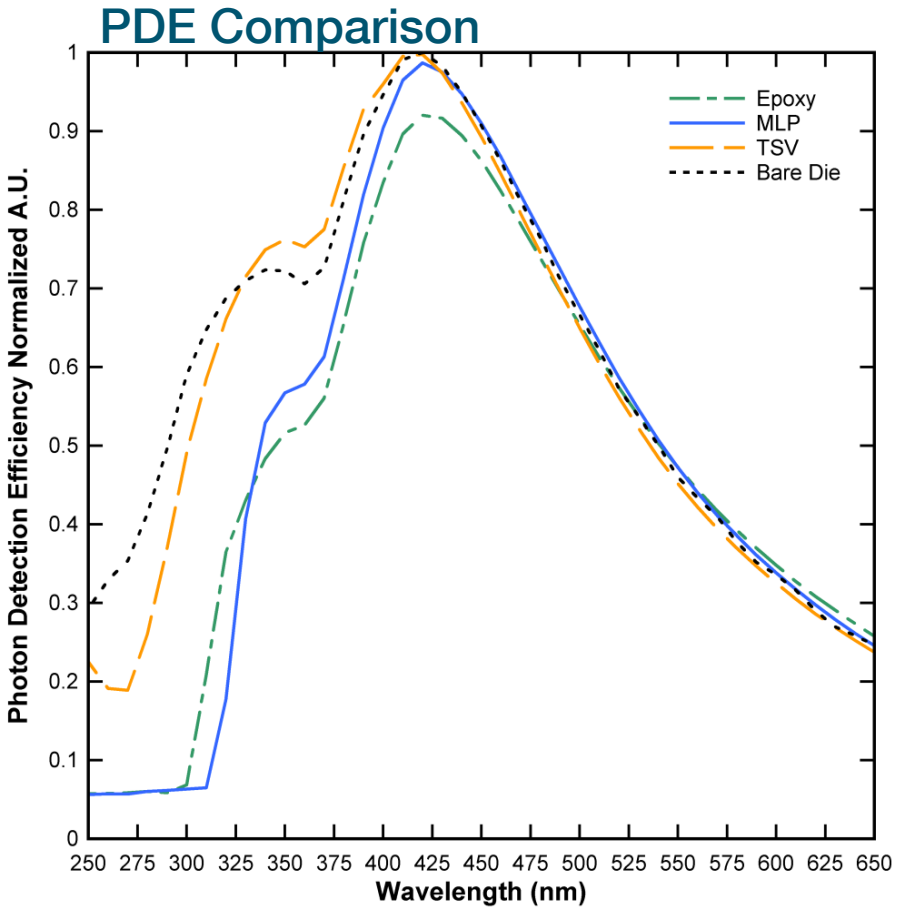
Photon Detection Efficiency (PDE)



TSV Test Board – SMA Output

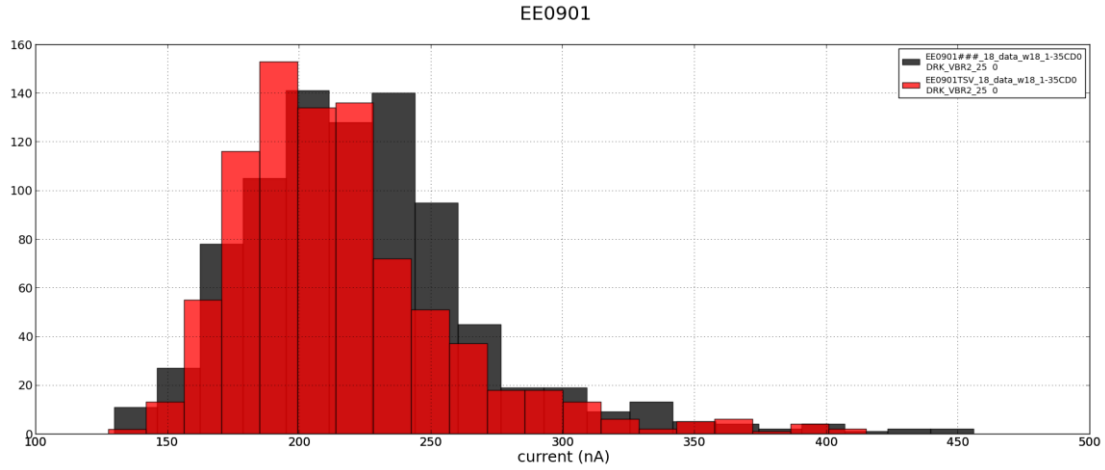


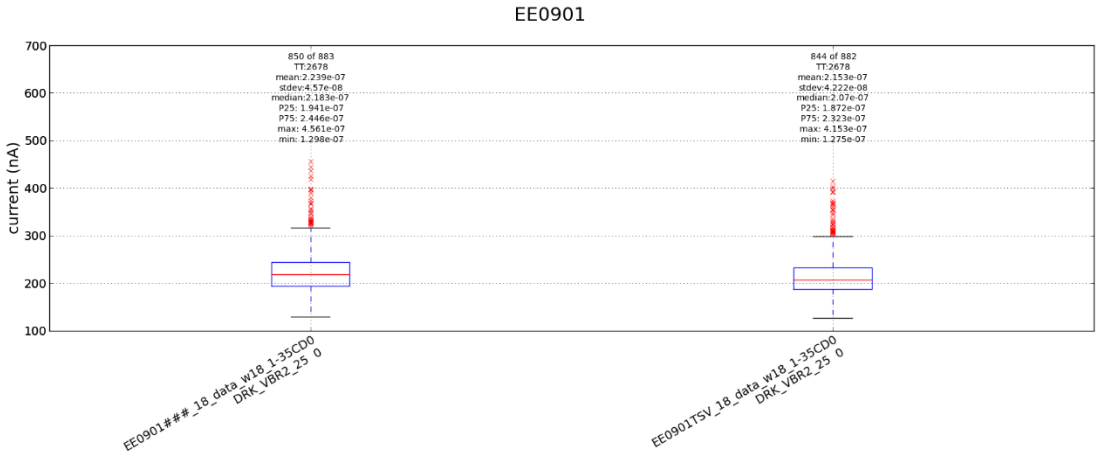
TSV glass has higher transmission compared to clear MLP

TN1 Activities

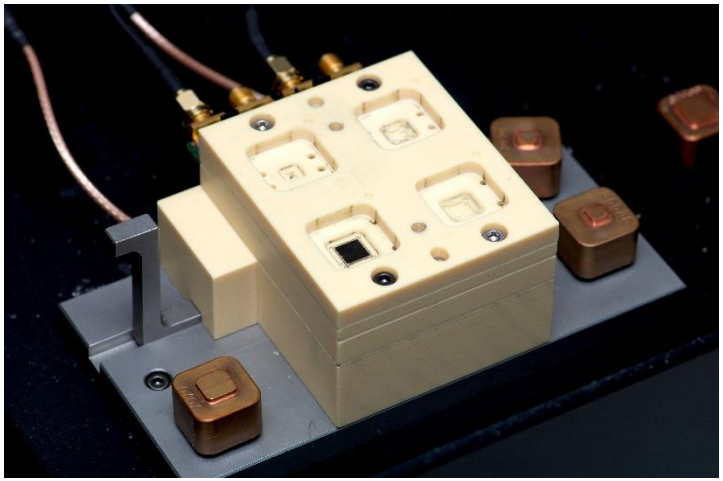
TSV Development

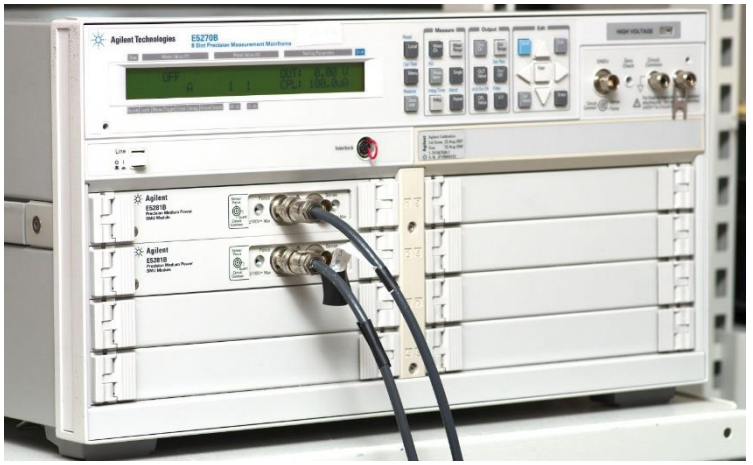
Initial Wafer Level Results

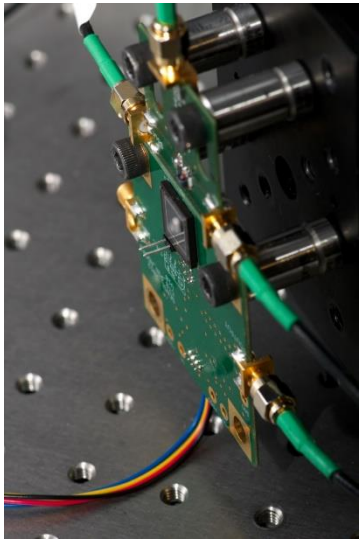




Laboratory Test Capability Development

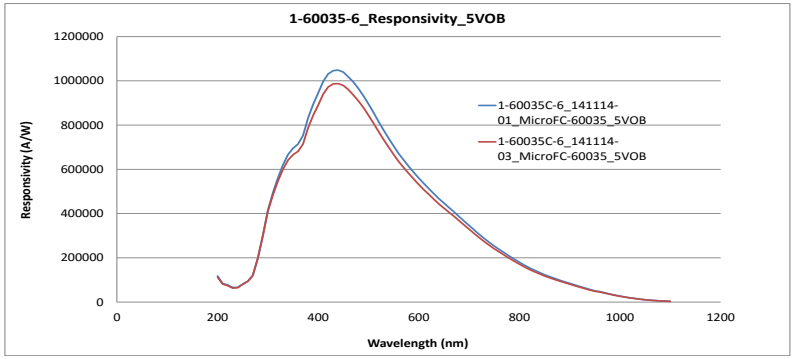




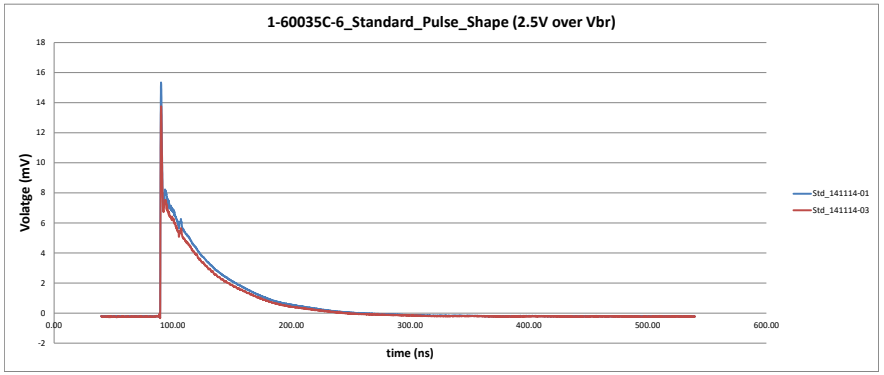


Die level and on PCB test infrastructure developed at SensL

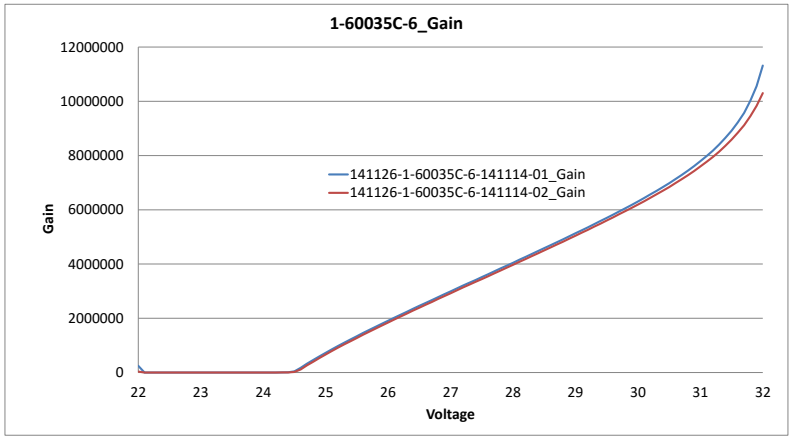
Initial Laboratory Test Results



Optical Responsivity



Pulse Shape

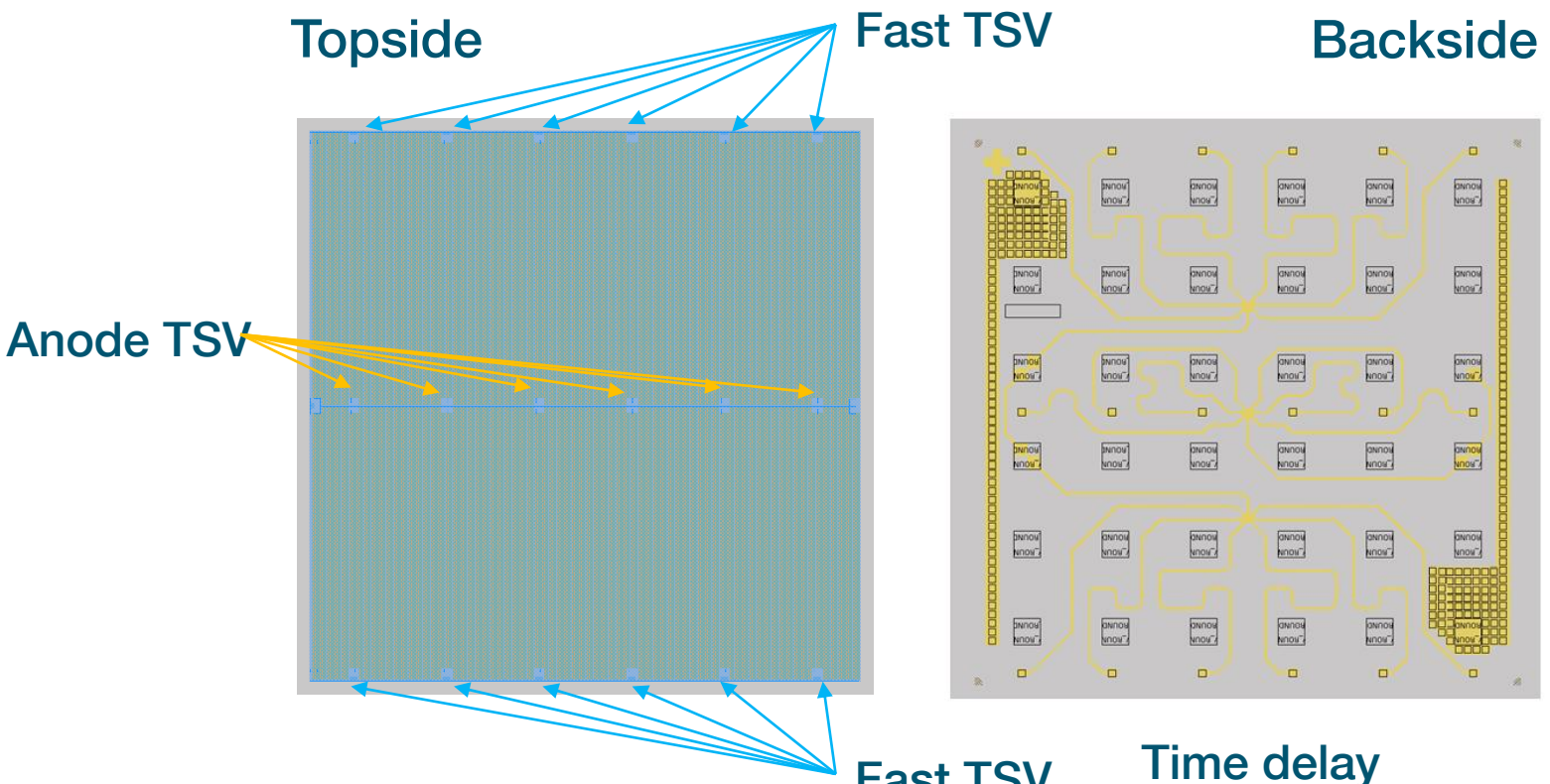


Gain

TN2 Activities

TSV Qualification & Reliability

Production Maskset

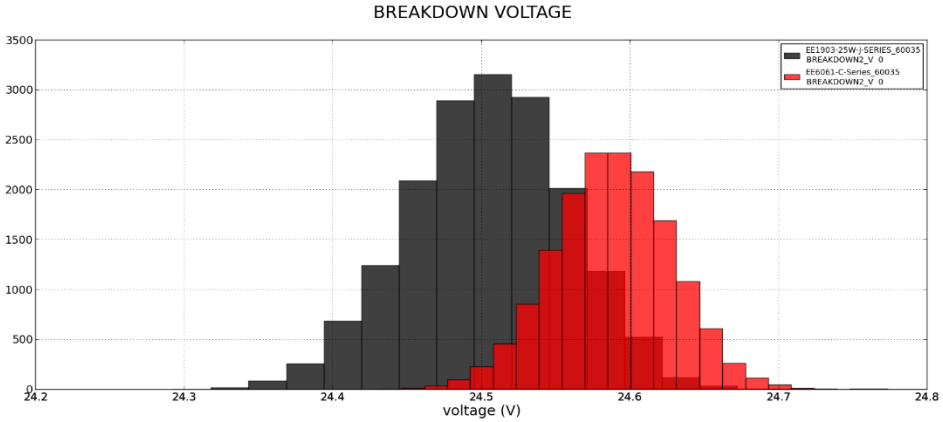


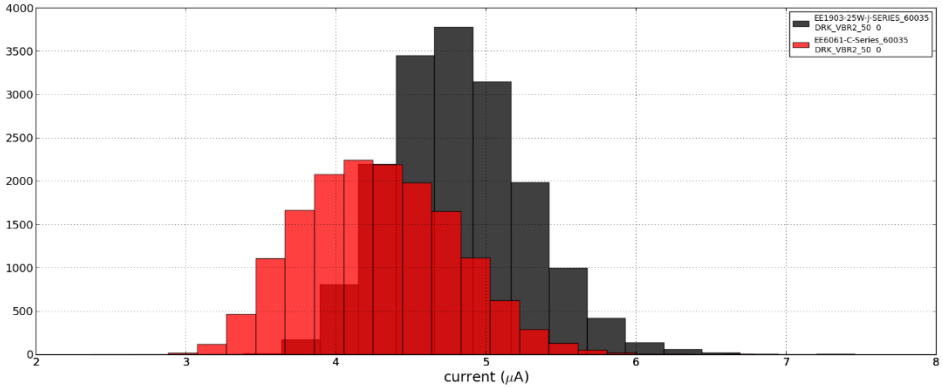
Multiple TSV high speed signal paths on top side

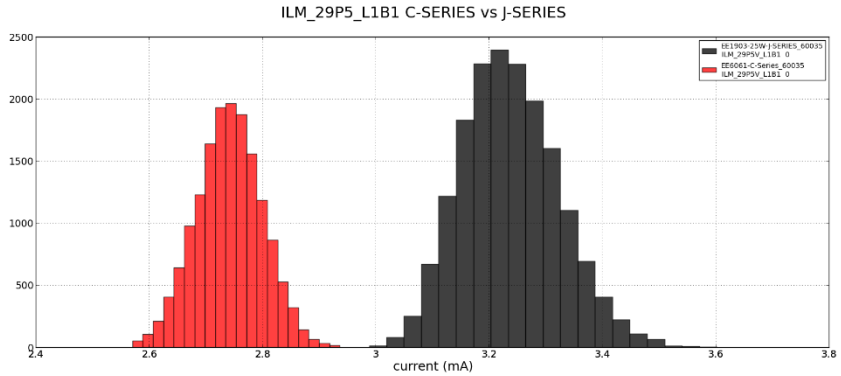
Time delay minimization using low impedance copper tracks on back side

Fabricated Sensors

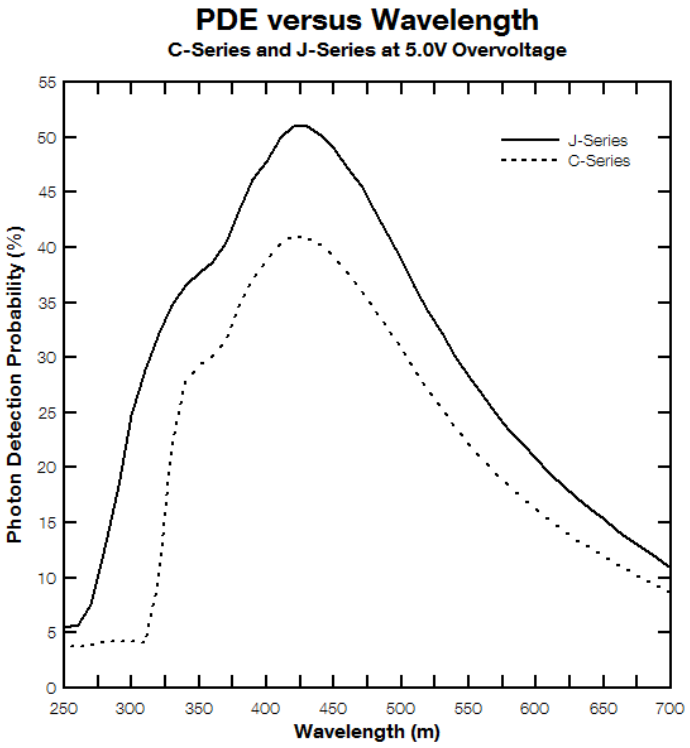
Wafer Level Results

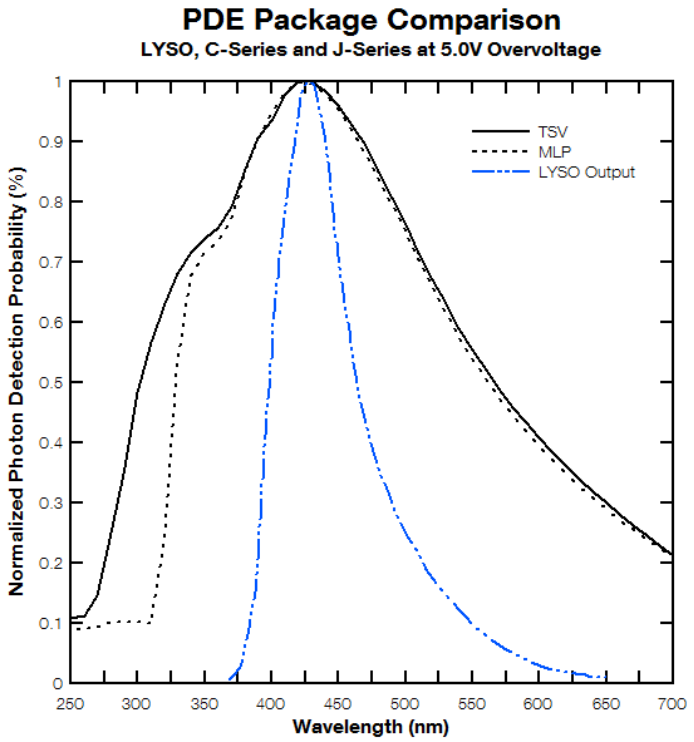






Photon Detection Efficiency (PDE)



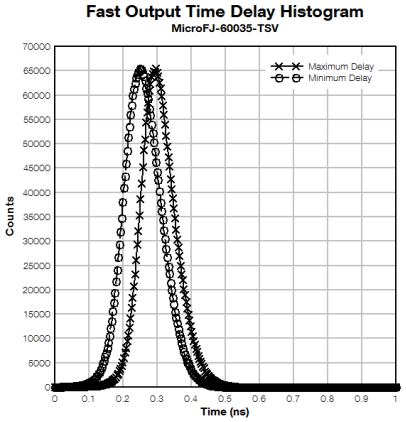


Time Delay Measurements

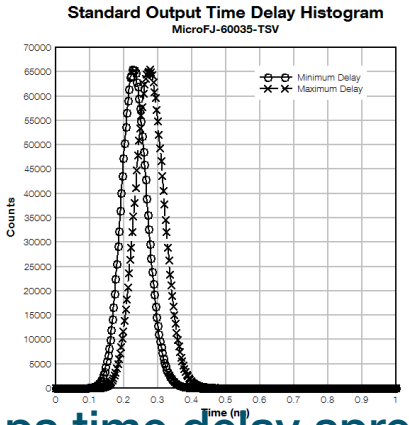
Fast Output

Standard Output

J-Series

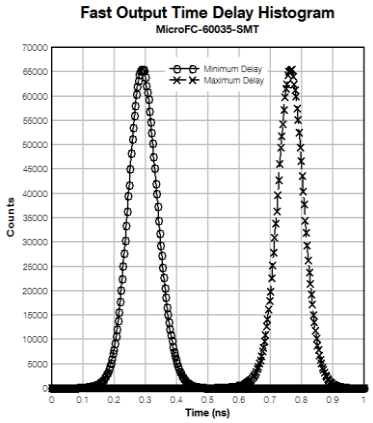


46 ps time delay spread

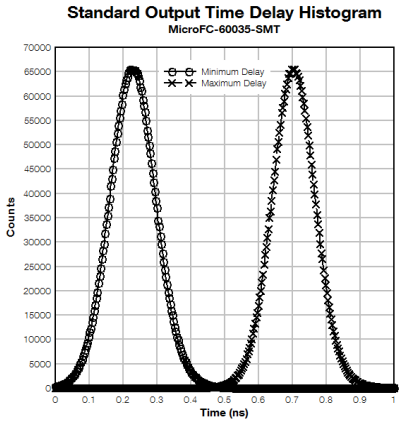


52 ps time delay spread

C-Series



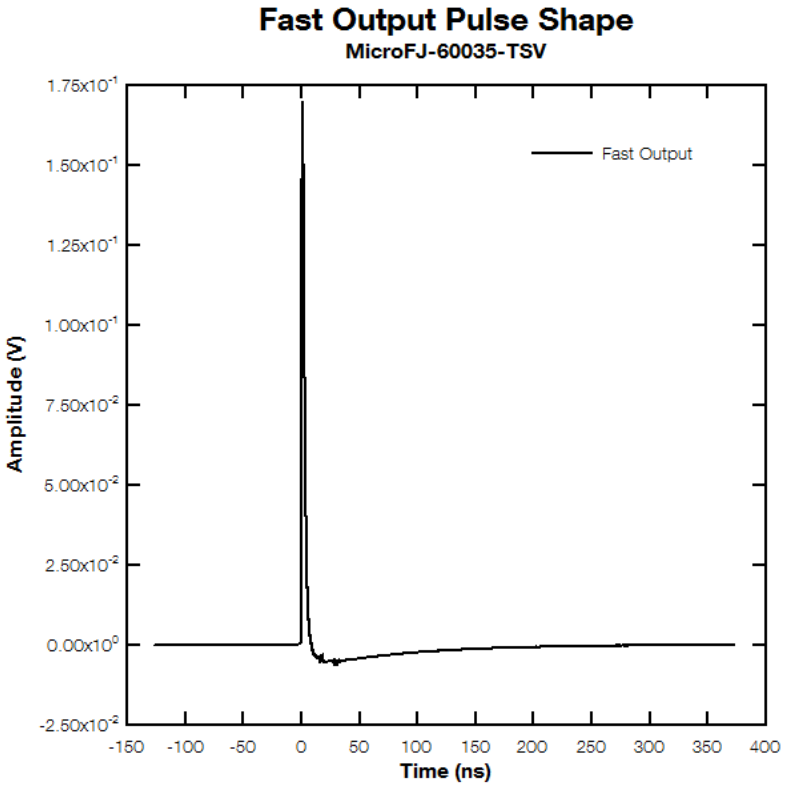
476 ps time delay spread

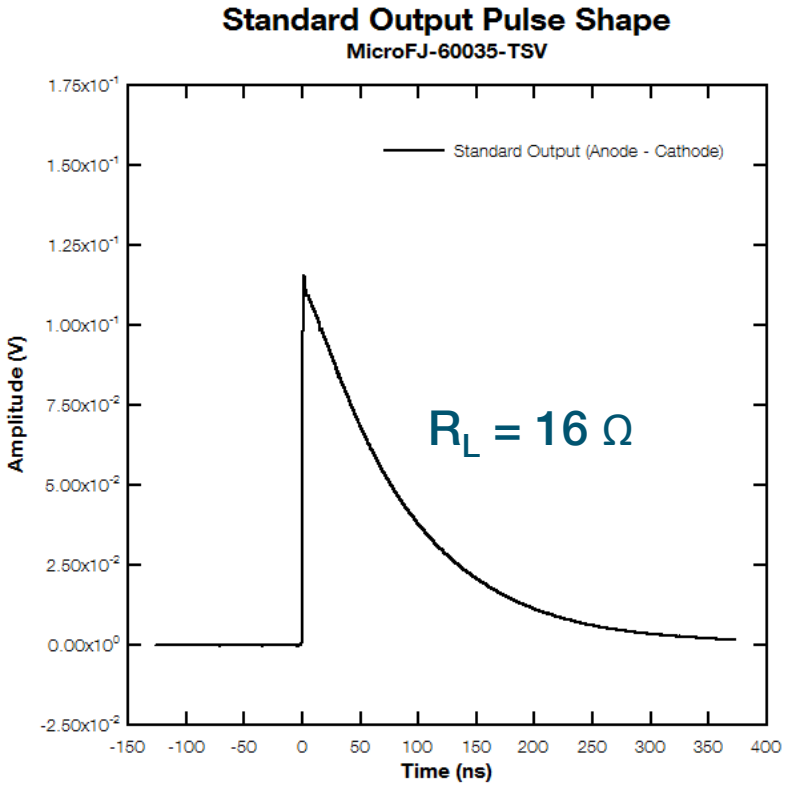


485 ps time delay spread

Pulse Shapes

Demonstrating Recovery Time Reduction





Fast Terminal Performance

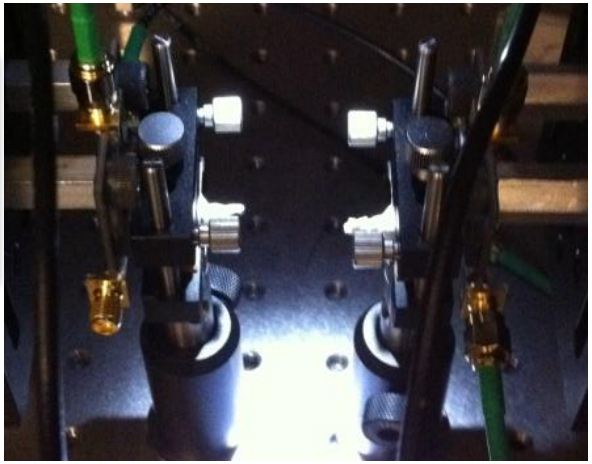
- Rise time 635 ps
- FWHM: 2.74 ns

Standard Terminal Performance:

- Rise time 706 ps
- Recovery Tau (1/e): 49 ns
- 1 Ω External R_L

Coincidence Resolving Time (CRT)
Measurement Setup

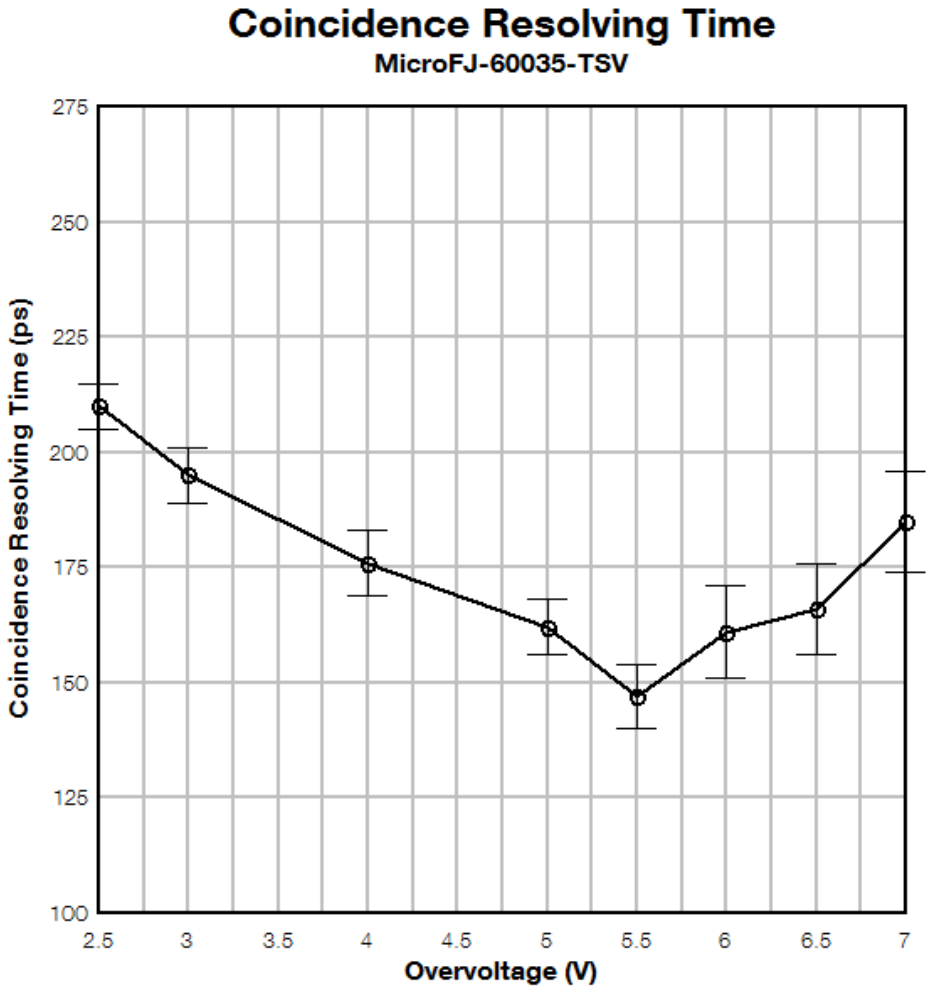
- Head-to-head configuration
- 4 separate readout channels for Fast and Standard Outputs



14-bit, 5GSps, 700MHz

Fast Output Amplification:
Amp 1: Minicircuits ZFL-1000
Amp 2: Minicircuits ZX60-43-S+
(Combined amplification of ~200x)

Coincidence Resolving Time (CRT)



Measurement conditions:

- 3 x 3 x 20 mm^3 LYSO:Ce
- 6 mm SiPM
- Head on test
- Folded measurement using 2 SiPM

Reliability Test Assessment Program

Test	Location	Ref.	Abbr.	Required Condition	Lot size	Status
High Temperature Operating life	Tyndall Institute	JESD22A 108	HTOL1	1000hr Ambient temperature = 125°C; bias>Vbr	3 lots / 77 units	at 500hr
High Temperature Operating life	Tyndall Institute	JESD22A 108	HTOL2	1000hr Ambient temperature = 85°C; bias>Vbr	1 lot / 77 units	at 500hr
Human Body Model ESD	EAG	JESD22-A114	ESD-HBM	Ta = 25°C	3 units	DONE
Moisture Level Definition	Tyndall Institute	J-STD-020	MLD	MSL treatment to levels set out in the standard; followed by solder simulation according to the specified solder conditions		Passed level 3
Preconditioning	Tyndall Institute	JESD22-A113	PRE	MSL3; 3 times reflow; peak body temperature 260°C	Applied to all parts prior to temperature cycling and thermal UHAST	DONE
Unbiased Highly Accelerated Stress	Maser	JESD22-A118	UHAST	110°C, 85%RH	3 Lots / 25 units	DONE
Temperature Cycling	Tyndall Institute	JESD22-A104	TC	500 cycles; -40C to 85C, 15 sec transition, 15 min dwell time	3 Lots / 25 units	DONE
High Temperature Storage Test	Tyndall Institute	JESD22-A103	HTS	504HRS HTS@125°C	3 Lots / 25 units	DONE
Characterisation	SensL	Functional Specification	CHAR	See Functional Specification	3 lots/ 10 units	DONE

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Characterisation Summary

Parameter	Abbr.	Unit	Notes	Target Specification	Specification Met
Breakdown voltage	Vbr	V	21°C	24.5	✓
Fill Factor	F	%		90%	✓
Photo-detection Efficiency	PDE	%	21°C , at max λ; Vbr + 2.5V	31%	✓
Gain	G		21°C , at Vbr + 2.5V	$3x10^6$	✓
Peak sensitivity wavelength	λp	nm	21°C, at Vbr + 2.5V	420	✓
Dark current	Idark	µA	21°C, at Vbr + 2.5V	3.2	✓
Signal rise time: fast mode	t_{rf}	ns	21°C, 10 to 90%	0.6	×
Pules width: fast mode	PW	ns	21°C, 90 to 10%	1.5	×
Microcell recovery time: standard mode	t_{re}	ns	21°C, 90 to 10%	180	✓
Temp dependence of Vbr	Vbr(T)	mV/°C	Various temperatures	21.5	✓
Optical cross talk probability	XT	%	21°C, at Vbr + 2.5V	10	✓

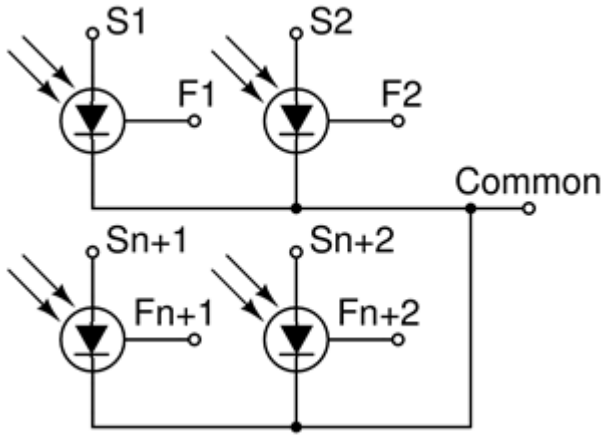
Modified Specification Acceptable to customers

TN3 Activity

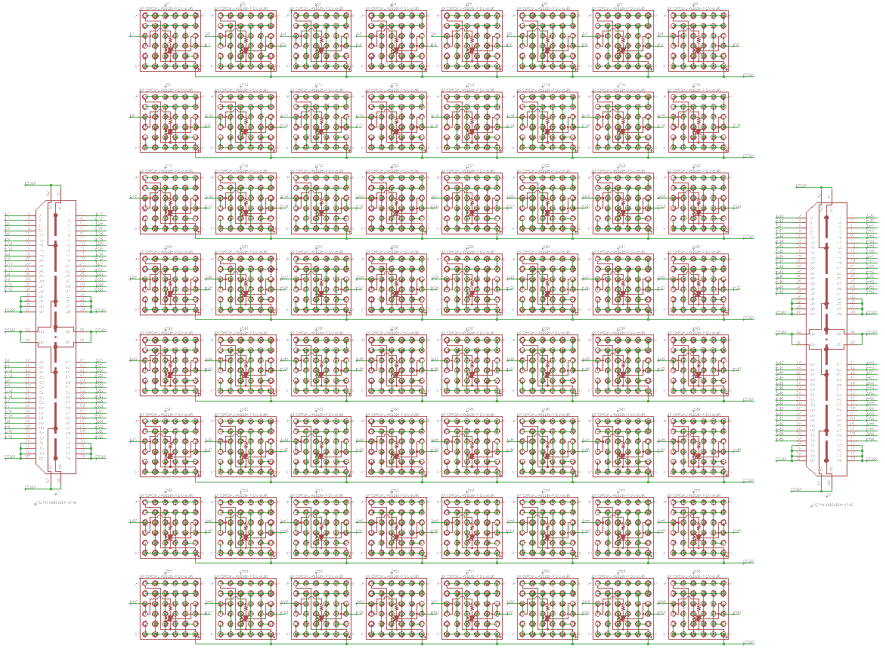
Array Development

8x8 Array Development

Internal Wiring Summary



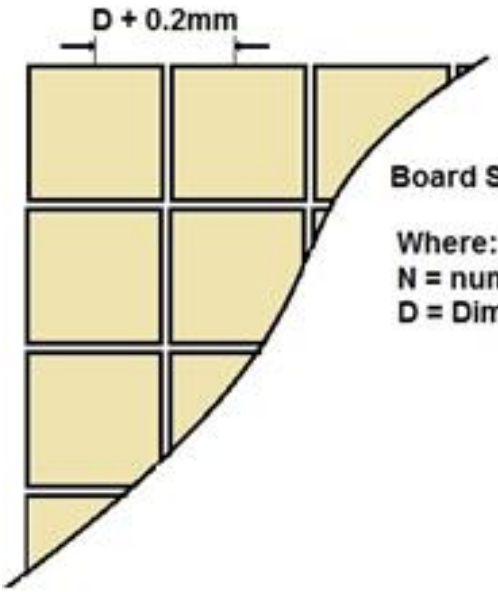
Schematic of 8x8 Array



- 64x Fast Outputs
- 64 x Standard Anode I/O
- 48 x pins connected to the common Cathode I/O

Design Rules and CAD of 8x8 Array

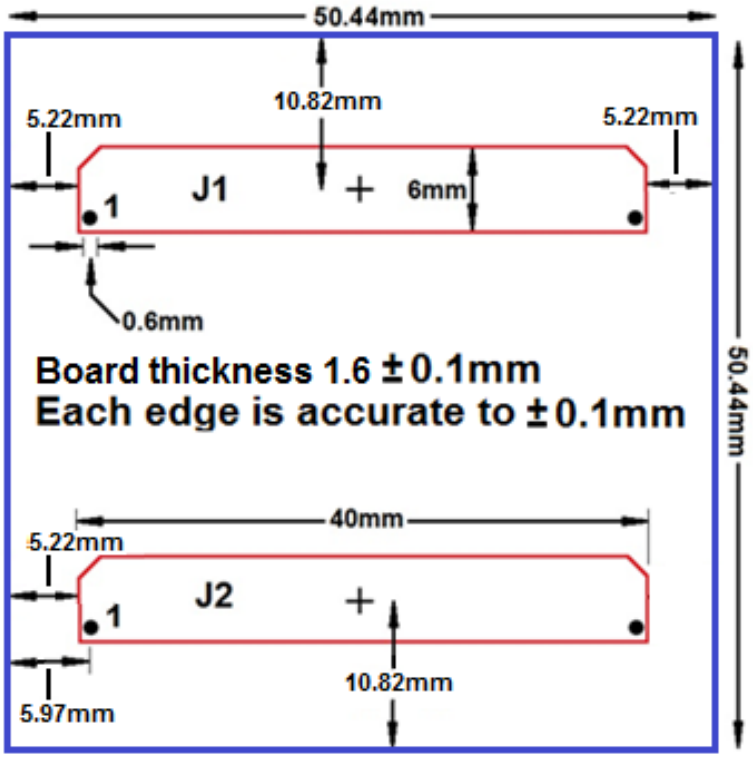
SiPM Spacing Design Rule



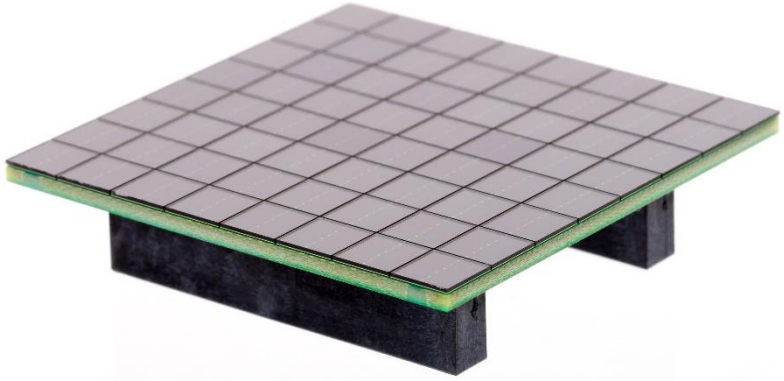
Board Size = (N x D) + ((N-1) x 0.2mm)

Where:
N = number of devices per side
D = Dimension of device

CAD of 8x8 Array

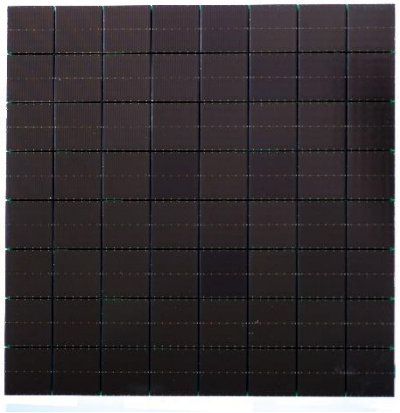


8x8 Array Images

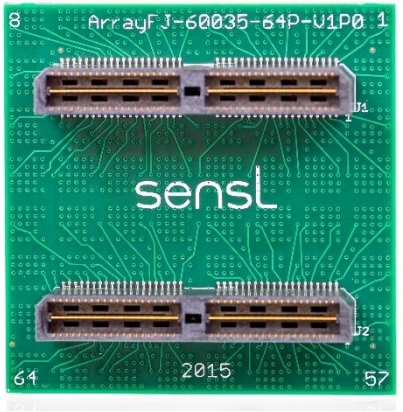


Side View

Top Side View



Back Side View



Conclusions

- A large area SiPM in a TSV process capability has been developed
- A large area SiPM in a TSV packaged product has been demonstrated
  - Reliability and qualification assessment has been carried out
- An 8x8 array of the large area SiPM has been developed
  - Reliability and qualification assessment has been carried out
- Customer validation has been performed with over 41 customers

Final Slide