caeleste

ADVAFAB

Deliverable

HYBRID-VIS

Executive Summary Report

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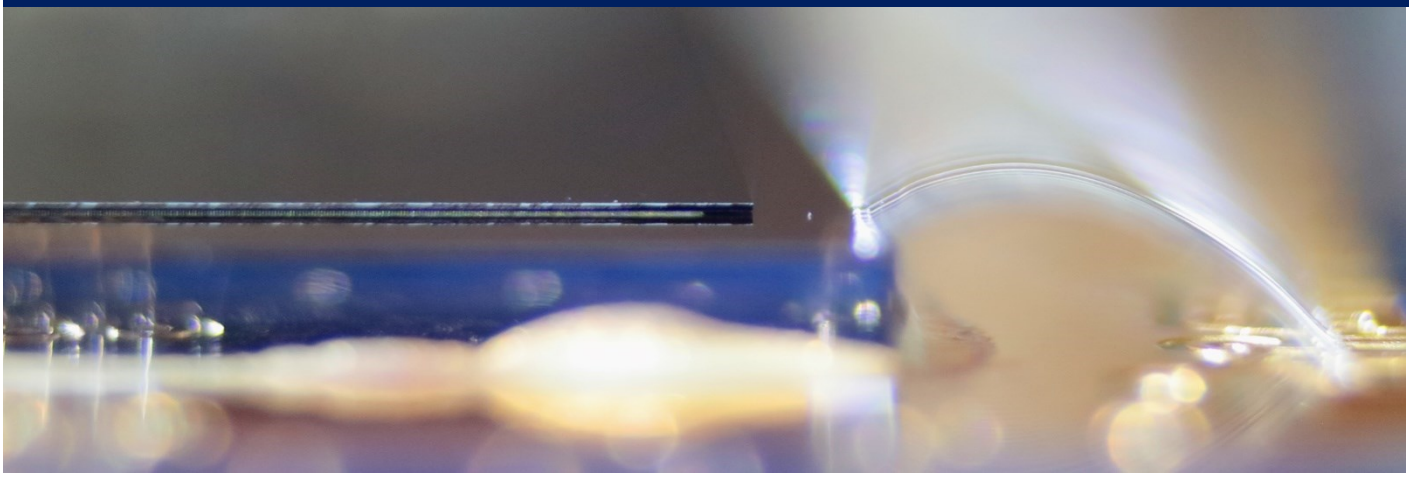

Hybridization, mechanically joining a photo-detector material to a (typically silicon) read-out integrated circuit (ROIC) using flip-chip-bonding, is a common manufacturing process for infrared (IR) detectors because those detector materials are not suitable as ROIC materials. This manufacturing method is rarely used for silicon visible-spectrum detectors, which can be manufactured monolithically (detector and electronics in the same silicon substrate) as front-side-illuminated (FSI) or back-side-illuminated (BSI) detectors; alternatively, as wafer-stacked (hybrid-bonding) composite devices. The latter is the dominant manufacturing method for high-performance, mass-produced silicon imagers and is similar to the flip-chip hybridization method but with key differences. In particular, wafer-stacking has a limitation on the thickness of the detector layer, through which a via must be etched; presently the detector layer is a few microns to a maximum of 10 µm. Die-to-die flip-chip hybridization enables much thicker detection layers fabricated with ideal technology without restrictions set by different wafer sizes, which makes them suitable for wider spectral response compared to both monolithic and wafer-bonded hybrids. Both hybrid approaches have higher manufacturing costs than monolithic detectors. Wafer-stacked hybrids are better able to realize small pixel (<15µm) arrays with higher expected yields than flip-chip hybrids but, as stated, with greater restrictions on the detector layer. This HYBRID-VIS research program intends to mature hybridization methods for large-format, high-performance visible detectors and demonstrate that small (20µm) pixels arrays can be reliably manufactured and the increased spectral range can be realized by virtue of the independent optimizations of detector and ROIC materials.

The Hybrid-VIS demonstration modules created in this research project have the following attributes:

- A 1024-by-1024 array of 20 µm square pixels, reaching a spectral response of >75% for 570-900 nm, see Figure 1.
    - 50µm thick detector layer fabricated using SOI technology.
    - The array is designed with a stitched schematic that makes future up-scaling possible in steps of 1K pixels in both directions, up to a maximum of 4k-by-4k pixels.
    - The Global Shutter pixels have three in-pixel gain settings for (synchronous) high dynamic range (HDR), corresponding to full well values of 58ke$^-$, 300ke$^-$ and 1Me$^-$.
- Programmable region-of-interest (ROI) on the Y-direction,
- Choice of operating modes: Read-While-Integrate (RWI), Integrate-Then-Read (ITR),
- Programmable analog gain (x1, x2, x4) in the readout,
- Programmable low noise modes, including non-destructive readout mode,
- Sensor global settings control by Serial Peripheral Interface (SPI),
- 50Hz frame rate,
- Radiation hardness: total ionizing dose (TID) up to 20krad, and proton fluence up to $1{\cdot}10^{11}$ Protons/cm^2.

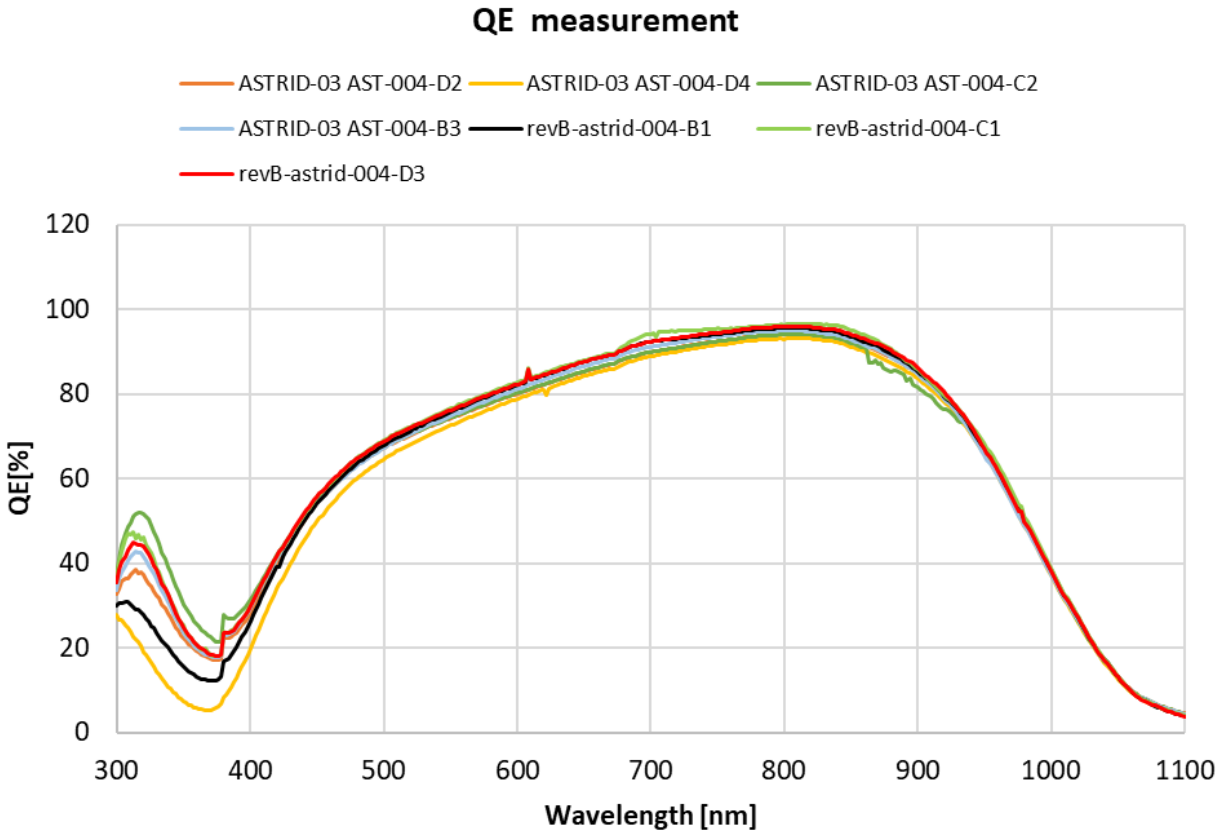

Figure 1: Quantum efficiency measurements of different hybrid modules.

The hybridization only allows for a PIN diode at the detector layer and a single pillar at 20µm pixel pitch. To read this structure out, the core of our pixel topology must be a 3T pixel. For this hybrid design, the pixel schematic must also account for the two distinct semiconductor properties and the copper pillar interconnects in the signal path. Furthermore, this pixel must support both the global shutter and (synchronous) HDR features. The designed hybrid pixel schematic is shown in Figure 2.

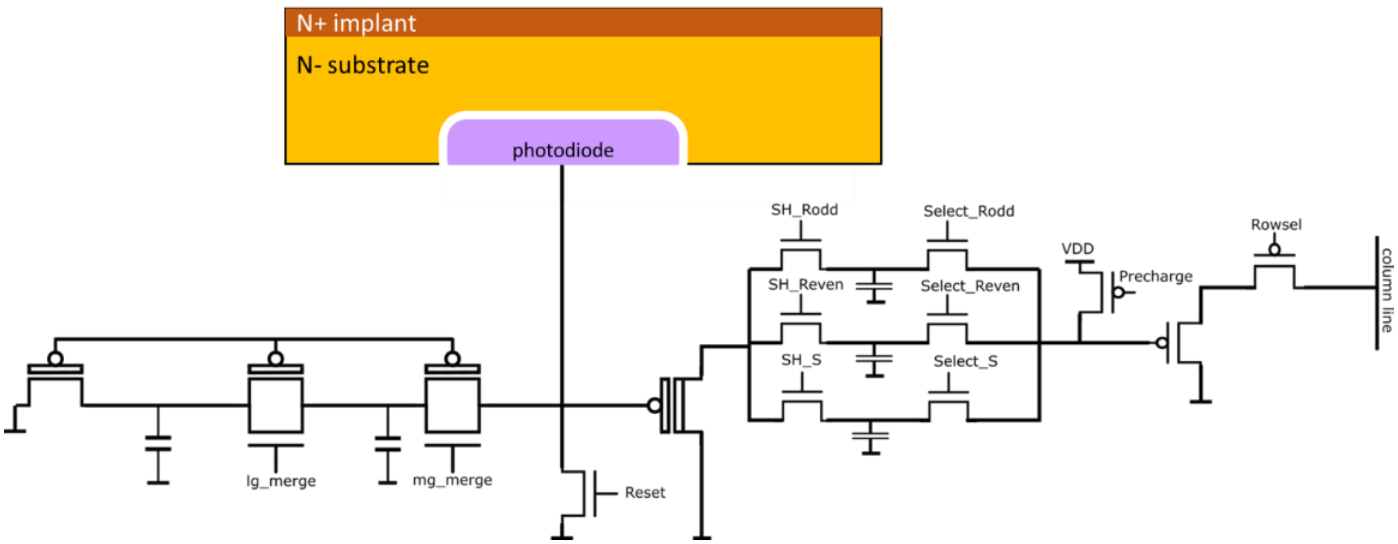

Figure 2: The hybrid 3T pixel schematic.

The circuit of this pixel is entirely located on the ROIC-side, in CMOS technology; this enables the properties of this circuit, like overall gain from photodiode to column line, to be fully simulated. The property with greatest uncertainty was the value of overall parasitic capacitance at the photodiode, mainly created by the junction at the detector side and the copper pillar. A first order estimation of this

capacitor was made, based on approximating the pillars and junction with parallel plate capacitor theory. The initial estimations during the architecture phase were revised at the end of layout phase and were adjusted with a factor 10 increase. This change of floating diffusion capacitor reduced the Charge-to-Voltage (CVF) factor and increased the input referred noise above the specified value. The produced devices showed, based on the full-well and CVF, that the final parasitic capacitance estimations were correct. This parasitic capacitance influences noise significantly.

In this project, we were pushing the existing processes to new limits on multiple fronts. Making large - area detectors with a-50µm thick sensors with 20µm pixels, front side biasing and using an atomic layer deposited (ALD) anti-reflection coating (ARC) to top it all. The flip-chip bonding creates a rear-illuminated hybrid detectors, which have virtually 100% fill factor.

The deposition of the ARC was done with ALD and consist of TiO2:Al2O3 stack. This stack was considered to be sufficient to meet the requirements on quantum efficiency and the fill factor.

The Flip-Chip Bonding (FCB) of the thin sensor chip was seen as the major challenge because of the unknown bow of the sensor layer. The hybridization approach was based on the Cu/Ni/InSn pillar type of interconnects. Those pillar bumps come with many advantages; e.g., less solder is required compared to typical ball like bumps, reducing the chance on solder bridges between pixels, it adds stand-off between the ASIC and sensor, it compensates for bow of the sensor chips and those bumps can be soldered at low temperature (~120°C). The bow of the sensor chip is caused by the metal layers, all located at the pixel side of the sensor, thermally expanding during the solder reflow step. During the solder reflow step, the module is required to stay flat. To realize this, a carrier technology was required. This process is shown in Figure 3.

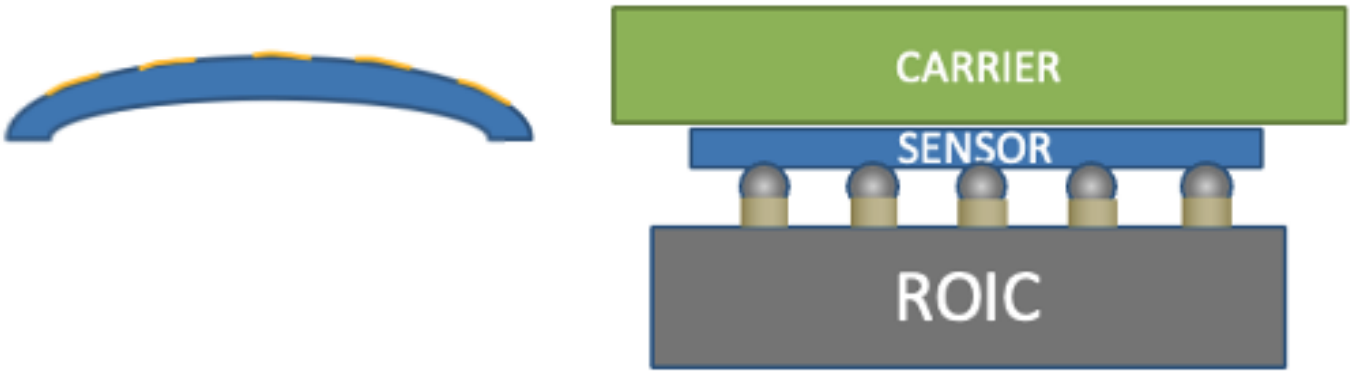

Figure 3: Illustration of using a carrier to support the sensor. On the left: free standing sensor chip with huge bow (not to scale). On the right: carrier attached to the sensor prior to solder reflow step. The carrier technology is proprietary information of Advafab.

Four batches of modules were produced and the total number of delivered modules was 29 pcs. The failures could be divided into three categories: 1) flip chip bonding failure, 2) delamination of the fringe bias contact bumps, and 3) sensor with very high leakage current. The fringe bump array structures were way too small to tolerate the external stress caused by the film stresses on the sensor chips. In this respect the simplest development improvement action is just to add mechanical bumps to support the corners and edge areas of the sensors.

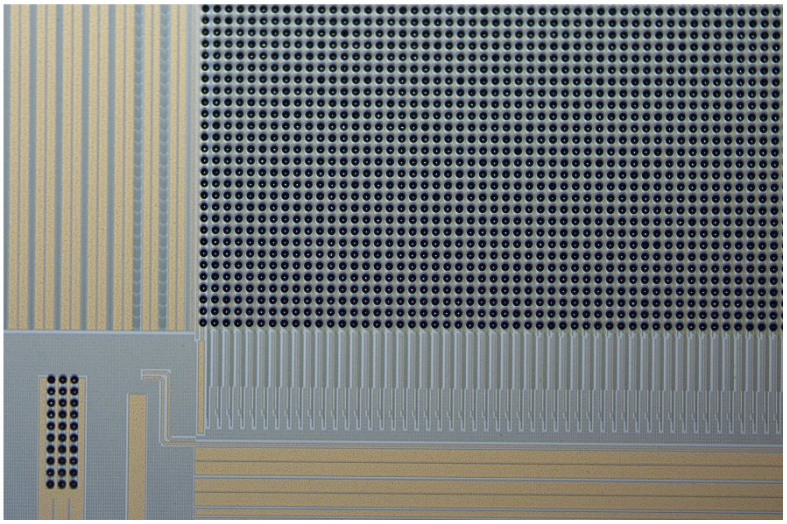

Figure 4: Image of the ASIC with bumps. The fringe bumps can be seen at the bottom left corner of the images.

Table 1. Manufacturing yields of detector modules attached to PCB.

Batch	#No of modules	#FC bonding issue	#Sensor issue	#Fringe (bias) issue	Yield %
1	6	1	1	0	67%
2	7	6	0	1	0%
3	6	6	0	3	0%
4	10†	0	0	2	67%‡
Total	**29**	**13**	**1**	**6**	**32%**

† Only 6 of these 10 were mounted on PCB for testing

‡ only mounted counted in

The first and the fourth delivery batches corresponded to the expected results, but the batches in between were failures. Many improvements have been made between the first and last batch to optimize the process. There are two major contributors to the flip chip bonding quality that can be improved: 1) die-level solder bump uniformity and 2) wetting of the UBM pads on the sensors.

The ROIC wafers were fabricated at XFAB using their XH018 technology node as it accommodates all required devices to realize the complex pixel schematic. It also allows a flat passivation option to facilitate the pad openings and hybridization. Each 200mm wafer resulted in 37 dice each; no defective ROICs were found among all devices tested.

The ROIC development grafted many features on the 3T pixel detector layer, to enable a global shutter readout of the 1k x 1k pixel array at a frame rate of 50Hz, with fully programmable integration time. Furthermore, it provides complete freedom in the programmability of the y-direction windowing. It provides the 3T pixel with three charge handling capacities that can be employed for synchronous HDR operation.

The ROIC layout must take account of the mechanical hybrid requirements. Each ROIC-side pixel must have its own electrode, allowing a connection to the detector-side photodiodes. Furthermore, the ROIC must route and supply the required bias for the substrate of the detector at the correct position. This bias enables us to fully deplete the 50µm thick silicon detector layer.

The pixel electrode is created by a top-metal hexagonal, as shown in Figure 5. The inner circle of this hexagon has a diagonal of 10µm. To route and supply the substrate bias of the detector layer, the same sized hexagonal electrodes are repeated in a 10x3 array at the top-left and top-right, just outside the pixel array. The top right-side of the pixel array is shown in Figure 6, annotating the effective locations of the bias electrodes.

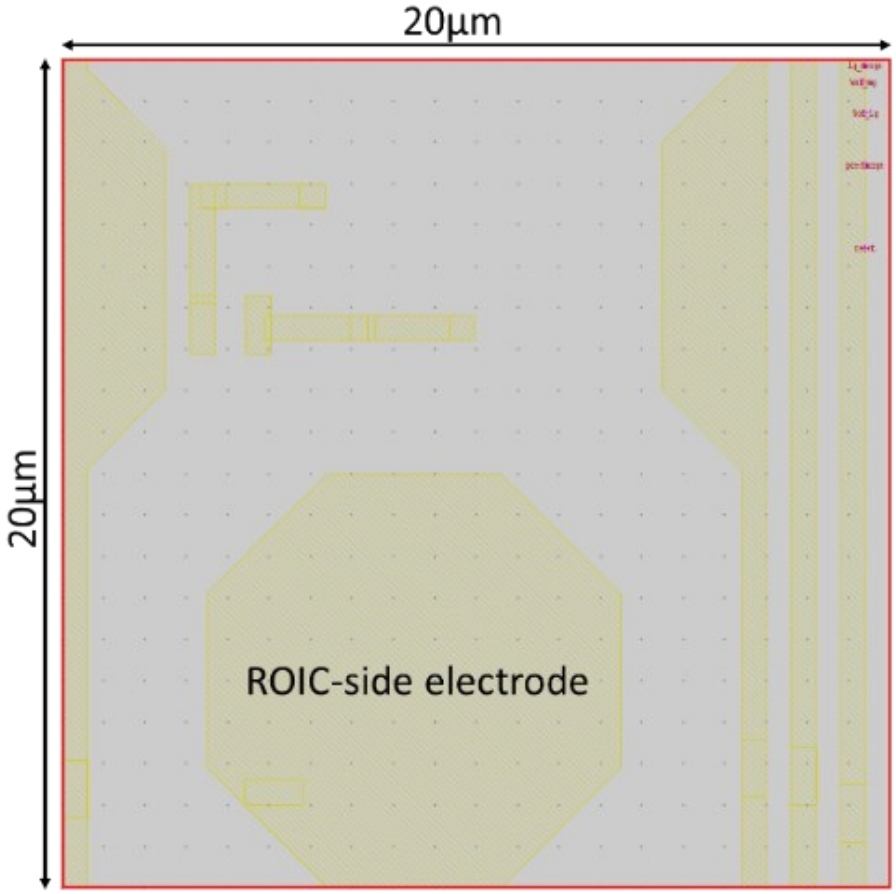

Figure 5: A top metal only view of a ROIC-side pixel (yellow shaded is top metal). The hexagonal electrode is located at the bottom center.

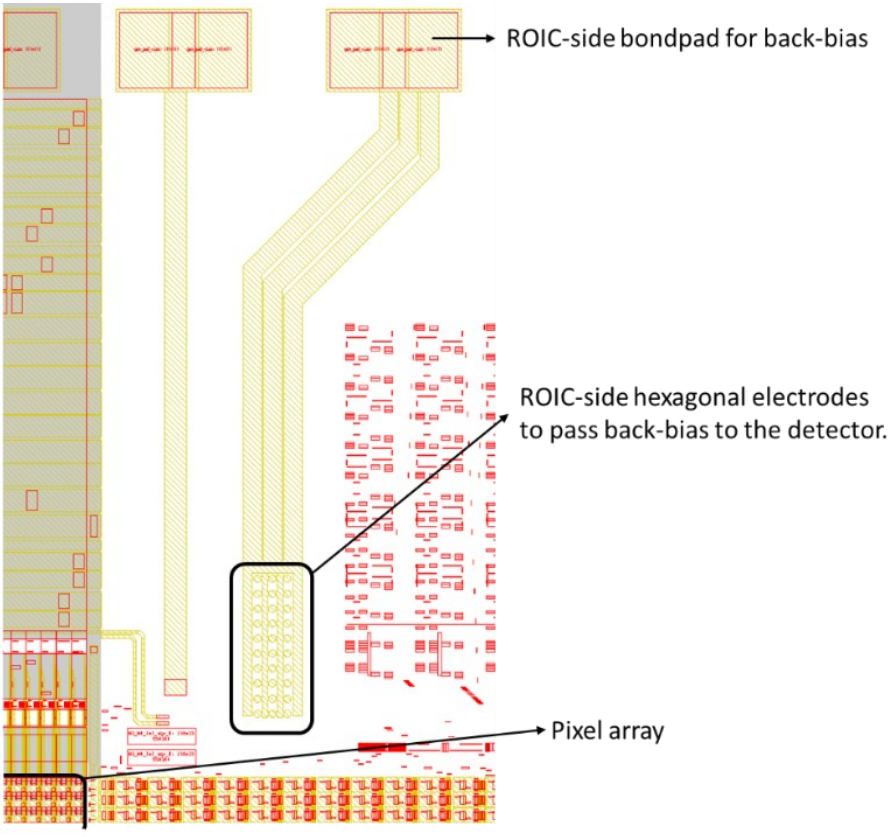

Figure 6: A snapshot of the top right side of the ROIC layout, showing only top-metal.

The foundry delivers a passivated wafer, covering all electrodes. The foundry had no technology available to etch Through Passivation Vias (TPV) as small as the 20µm pixel pitch. Additional post processing by a third-party was required to open the passivation accurately on top of the electrodes. This task was performed successful by Fraunhofer IZM, Germany.

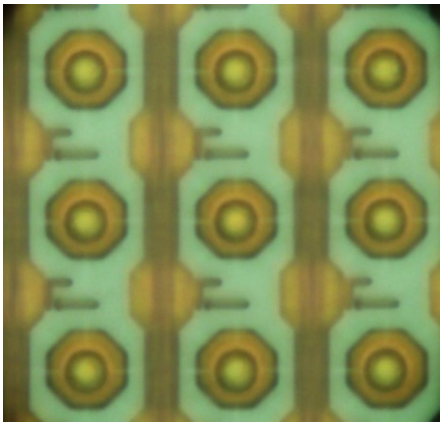

Figure 7: Pixel oxide opened in the array.

The top-level block diagram of the ROIC is shown (not to scale) in Figure 9 and may be compared with a photograph of the ROIC die in Figure 8, that was COB-mounted and wire-bonded for electrical testing, to see the correct scale. This top-level is composed of different blocks in such a way that it allows scalability of the pixel array up to a 4k-by-4k imager.

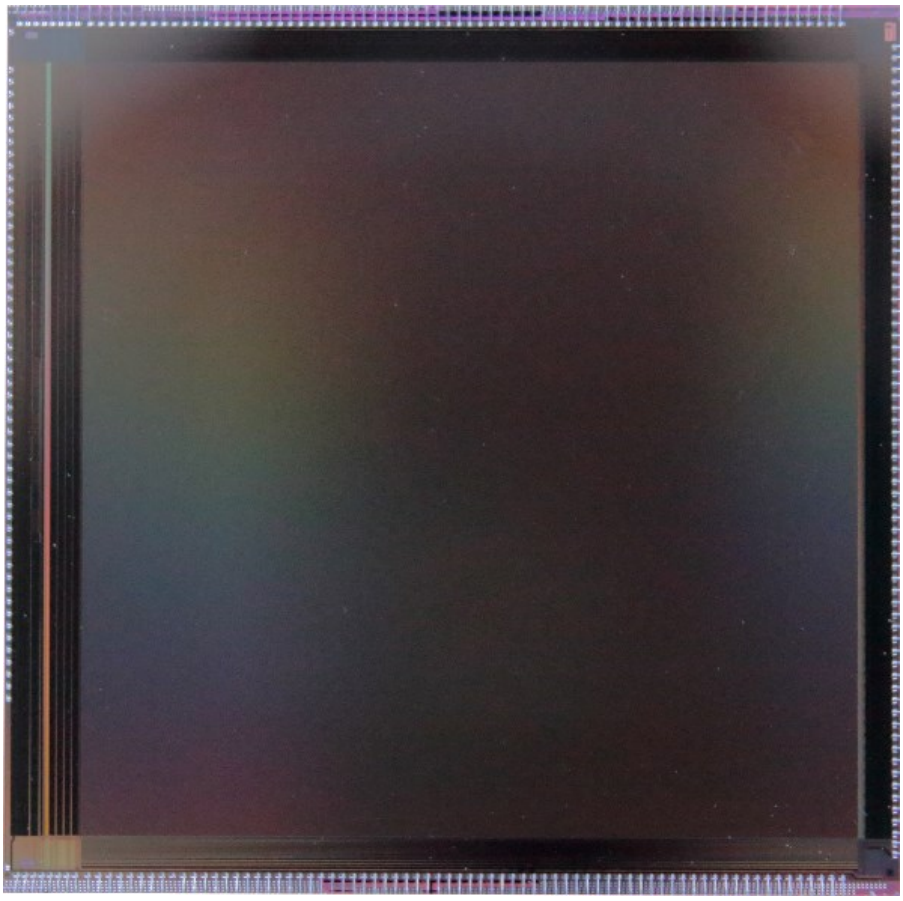

Figure 8: ROIC die without array open, wire-bonded for electrical testing.

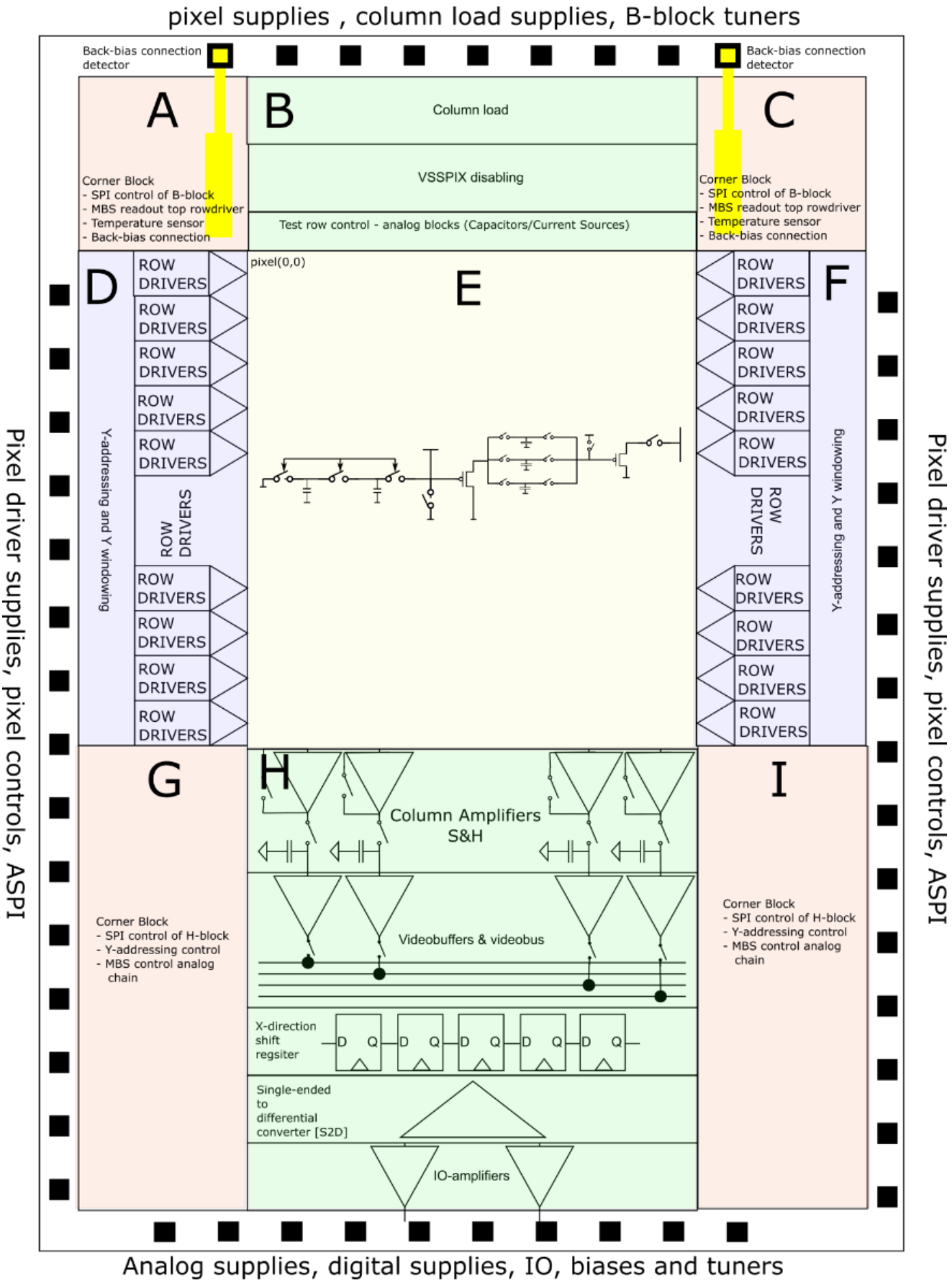

Figure 9: Block diagram of the ROIC indicating locations of the major blocks; not to scale.

Through this ESA-funded research and development effort, Caeleste and Advafab co-designed and manufactured a large-format Hybrid Visible Image Sensor (a matched-pair silicon ROIC and silicon detector combination) to demonstrate the advantages, to improve the design methodology and manufacturing of visible-NIR silicon-silicon flip-chip bonded hybrid imagers, and to advance the state of the art.

The design methodology of this novel matched-pair hybrid centered on the functionality of the pixel circuit and the analysis and simulation of uncertain pixel properties, that are physically located in two separate dies, later joined by pillar-and-bump interconnects. This shared electrical pathway introduces, in particular, parasitic capacitances for which little empirical data is available, none of which is directly applicable as this design is unique.

The pixel circuit design and the ROIC control introduce several novel operational features for a 3T pixel, including: fast frame rates up to 50Hz, Global Shutter readout; and programmability for the integration time, windowing and full well. This ROIC stitched schematic design makes it scalable to arrays as large as 4k-by-4k pixels.

This novel, proprietary hybridization process introduces advantages over typical bump-to-bump flip-chip bonding as it is based on growing Cu/Ni pillars of 12.5µm height on top of the ROIC, with a deposited InSn solder cap. This method reduces the likelihood of creating solder bridges between adjacent pixels, provides high stand-off height between the chips and improves flatness of the focal plane—especially for thinned detectors that may bow due to mechanical, thermal, and layer-stresses. Improving the evenness, composition, and geometry of these features at this small scale was a significant advancement of this research and demonstrates its practicality and risks for future products.

More than 25 hybrid modules were assembled on PCBs. The device properties measured were consistent across batches and may be relied on as a basis for future hybrid designs. Not all the challenging design specifications were met in this first design. Where underperformance was found, the root causes are understood and mitigations are documented to ensure any future design incorporates the improvements.

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