Hybrid visible image sensor

Final Presentation

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ESA Contract: 4000130176/20/NL/AR
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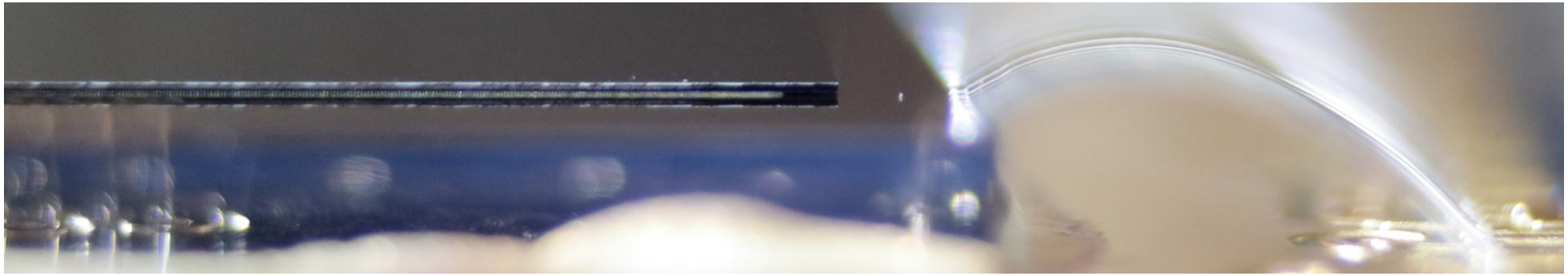
Agenda

1. **Background & motivation**
   1. Challenges, accomplishments
2. **Approach / design strategies**
   1. ROIC
   2. Detector
   3. Module
3. **Measured results**
   1. Characterization of device
   2. Radiation (Proton, TID)
4. **Conclusions & recommendations**
5. **Acknowledgements**



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Background & motivations

- **Thick-silicon detectors uniquely suited to certain applications**
  - Hyperspectral range with high (>75%) QE between 450-900nm
  - Also ideal for X-RAY and particle detectors
  - …but monolithic and wafer-stacking manufacture top-out around 25µm
- **Flip-chip bonded (FCB) hybridization has unique advantages**
  - Independent materials and processes for detection and read-out chips
  - Established tools, methods, and processes…for IR detectors with big pixels…
- **Outcome of this R&D:**
  - The maturation of FCB hybridization manufacture for large-format, high-performance visible detectors with small (20 µm)pixel pitch
  - A methodology for designing the matched-pair Detector and ROIC
  - Foundational measurement and insights for future designs
  - Characterized and operable demonstration / test devices

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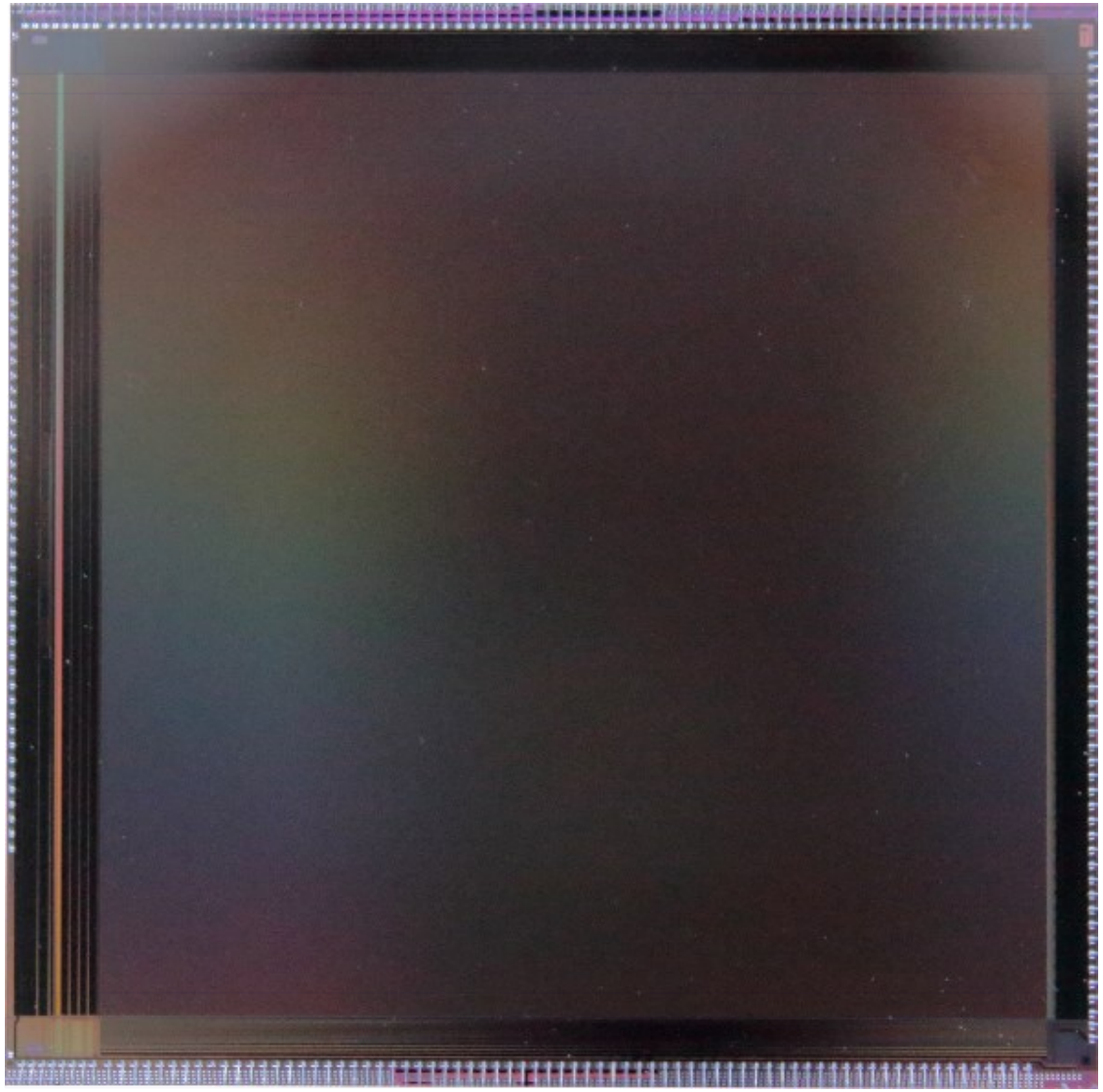
Features

- **50µm thick detector layer for high QE, fabricated using SOI technology.**
- **A 1024-by-1024 pixel array of 20 µm square pixels,**
- **50Hz frame rate**
- **Global Shutter pixels**
- **3 in-pixel gain settings for (synchronous) high dynamic range (HDR), corresponding to full well values:**
  - 58ke-
  - 300ke-
  - 1.2Me-.
- **Choice of operating modes:**
  - Read-While-Integrate (RWI),
  - Integrate-Then-Read (ITR).
- **Configurable by Serial Peripheral Interface (SPI):**
  - Region-of-interest (ROI) on the Y-direction,
  - Two low-noise modes:
    - analog gain (x1, x2, x4) in the readout
    - non-destructive readout mode (averaging)
- **Radiation tested: total ionizing dose (TID) up to 20krad, and proton fluence up to $1 \cdot 10^{11}$ Protons/cm^2.**



Detector – manufactured by ADVAFAB
ROIC – manufactured by XFAB in XH018 tech.

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WEST, Pixel Array, and EAST blocks {D,E,F}

Center Block E
Pixel Array

Edge Block D
- Row drivers, Y-addressing window control

Edge Block F
- Row drivers, Y-addressing window control

Bondpads for: Pixel driver supplies, pixel controls, ASPI

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NORTH blocks {A,B,C}

Bondpads for: pixel supplies, column load supplies, B-block tuners, detector bias voltage connections

Center Block B

Column load | VSSPIX disabling | Test row controls | Analog blocks (capacitors, current sources)

Corner Block A

- SPI control of B-block
- MBS readout top row-driver
- Temperature sensor
- Bias connection

Corner Block C

- SPI control of B-block
- MBS readout top row-driver
- Temperature sensor
- Bias connection

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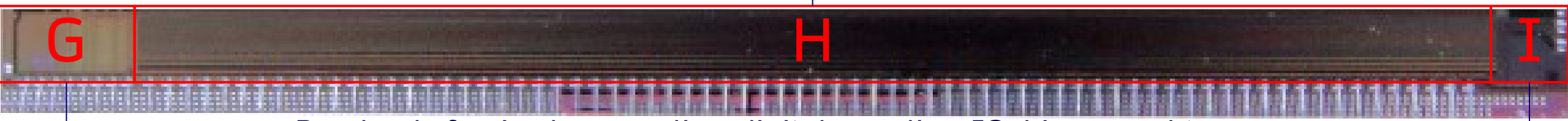
SOUTH blocks {G,H,I}

Center Block H
Column Amplifiers | Video-buffers & Video-Bus | X-Direction Shift Register | S2D converter | IO Amplifiers



Bondpads for Analog supplies, digital supplies, IO, biases and tuners

Corner Block G
- SPI control of H-block
- Y-addressing control
- MBS control of analog chain

Corner Block I
- SPI control of H-block
- Y-addressing control
- MBS control of analog chain

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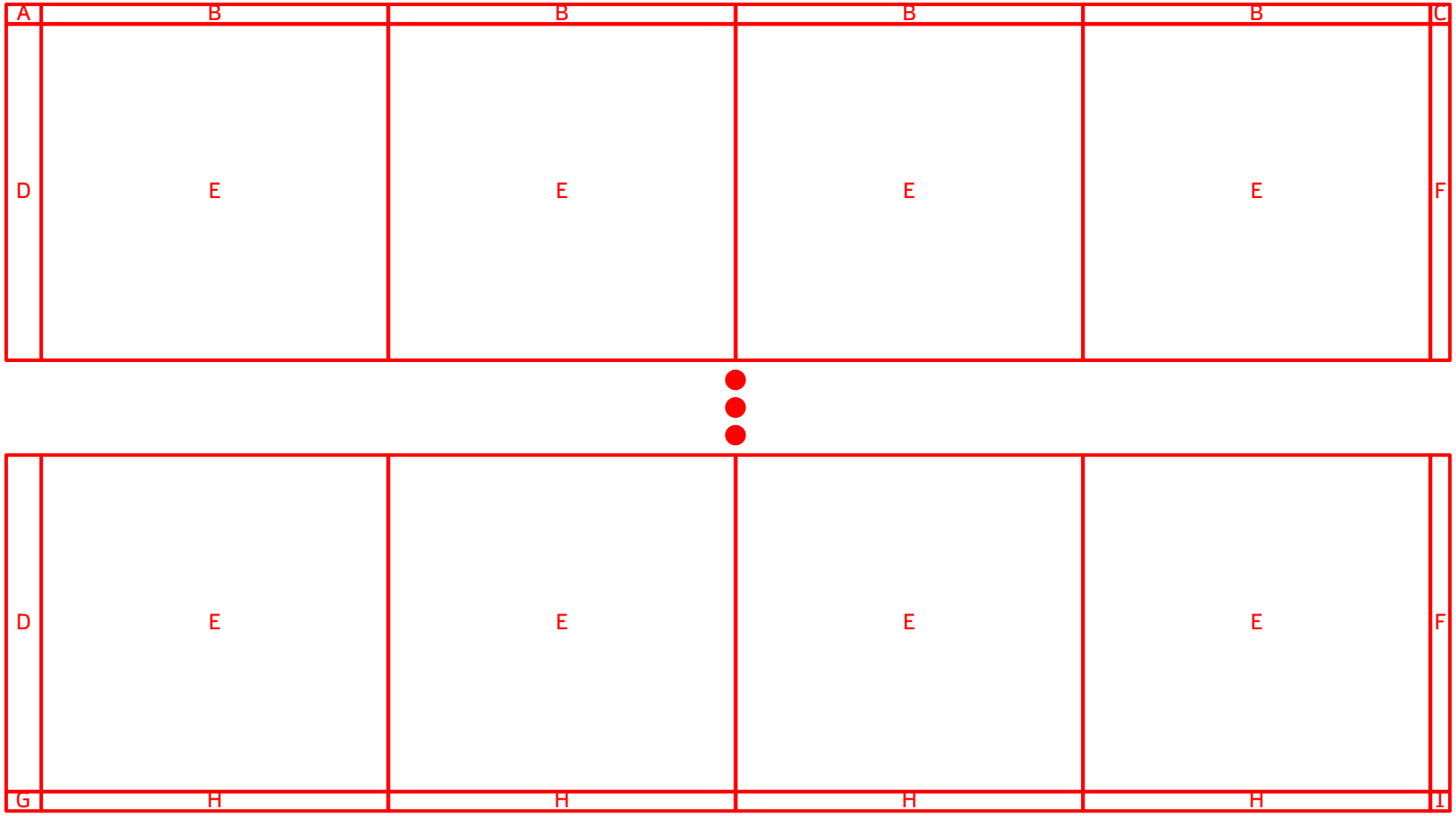
Extensible design can stich to 4k x 4k array



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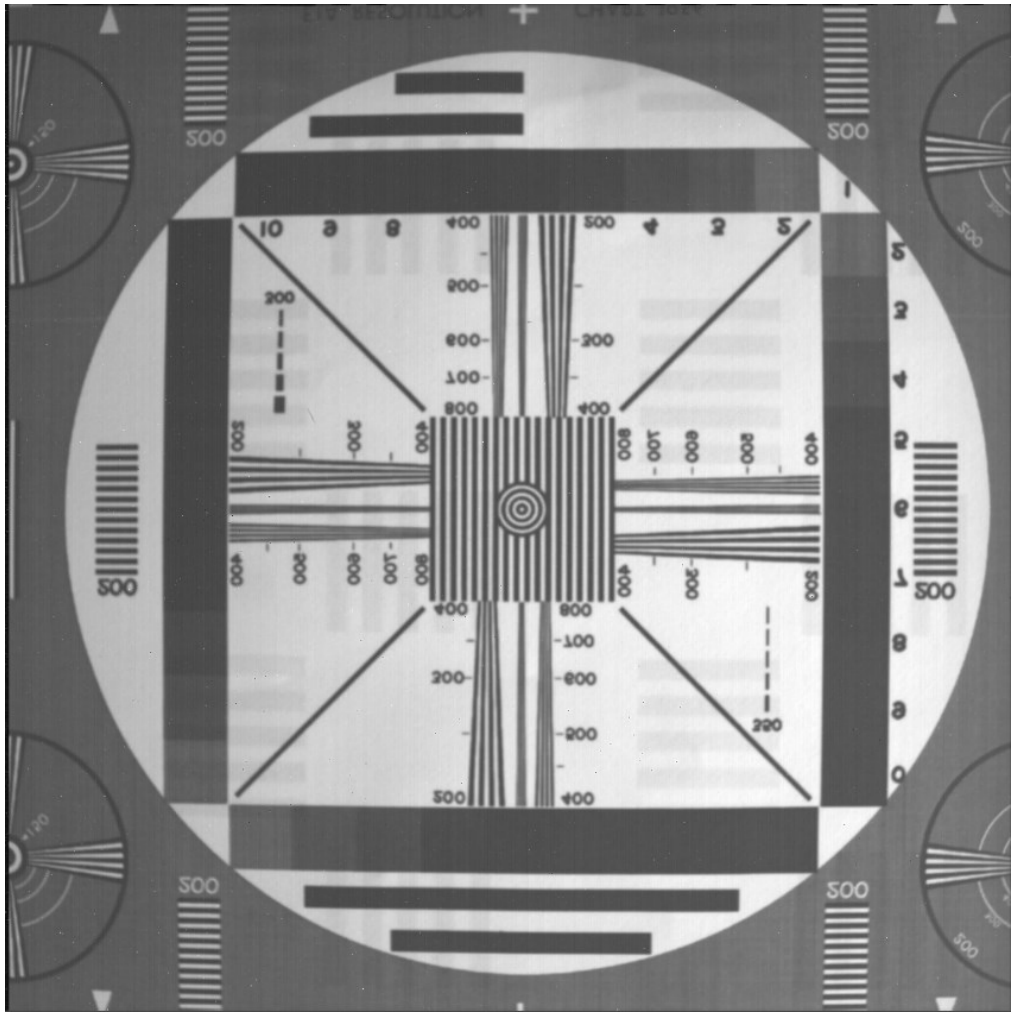
Real images from working hybrid



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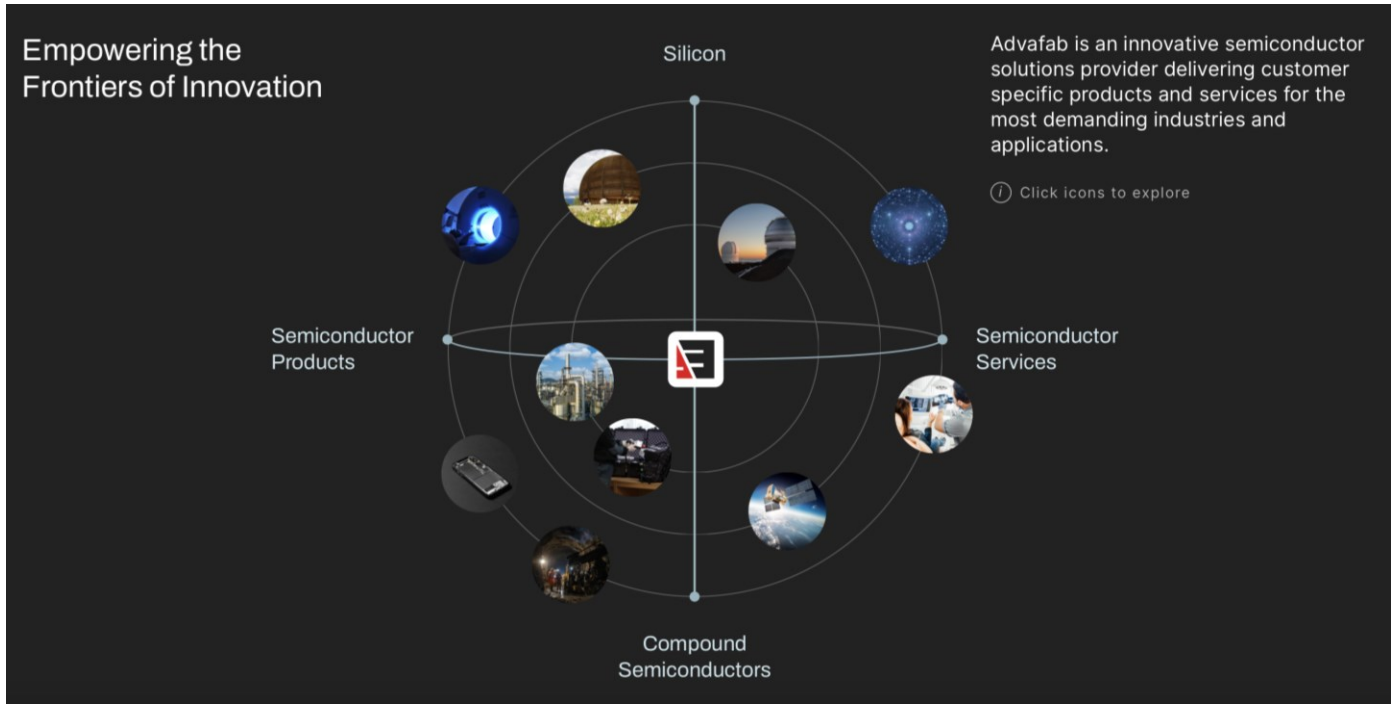
Advacam is now Advafab

- Company's name was re-branded to Advafab Oy in June 2023
- No changes in ownership or operation
- Company focused on semiconductor solutions instead of detector products
- Agnostic provider of radiation sensors
- Purpose for the change to attract new customers
- www.advafab.com



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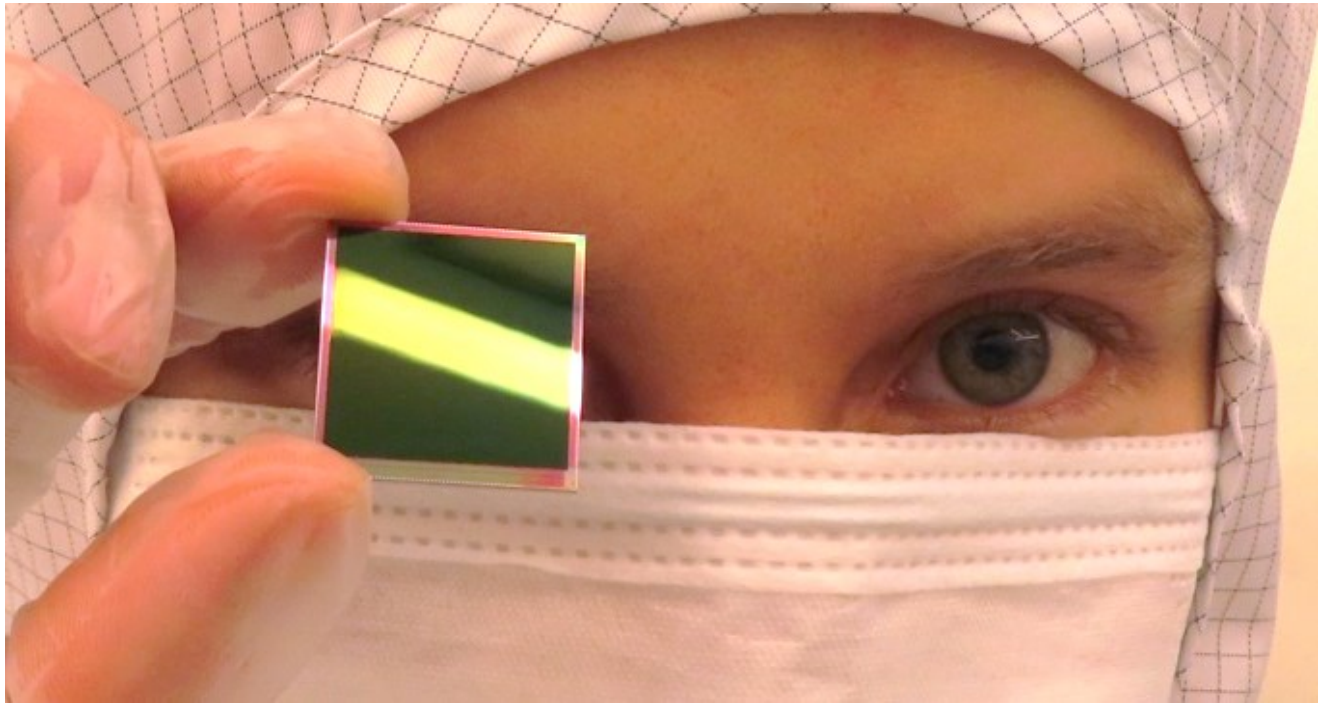
Sensor fabrication

- Detector thickness = 50µm
- ARC optimized 450-900nm with roll off more pronounced at shorter wavelengths
- N-type Si sensors used for manufacturability purposes



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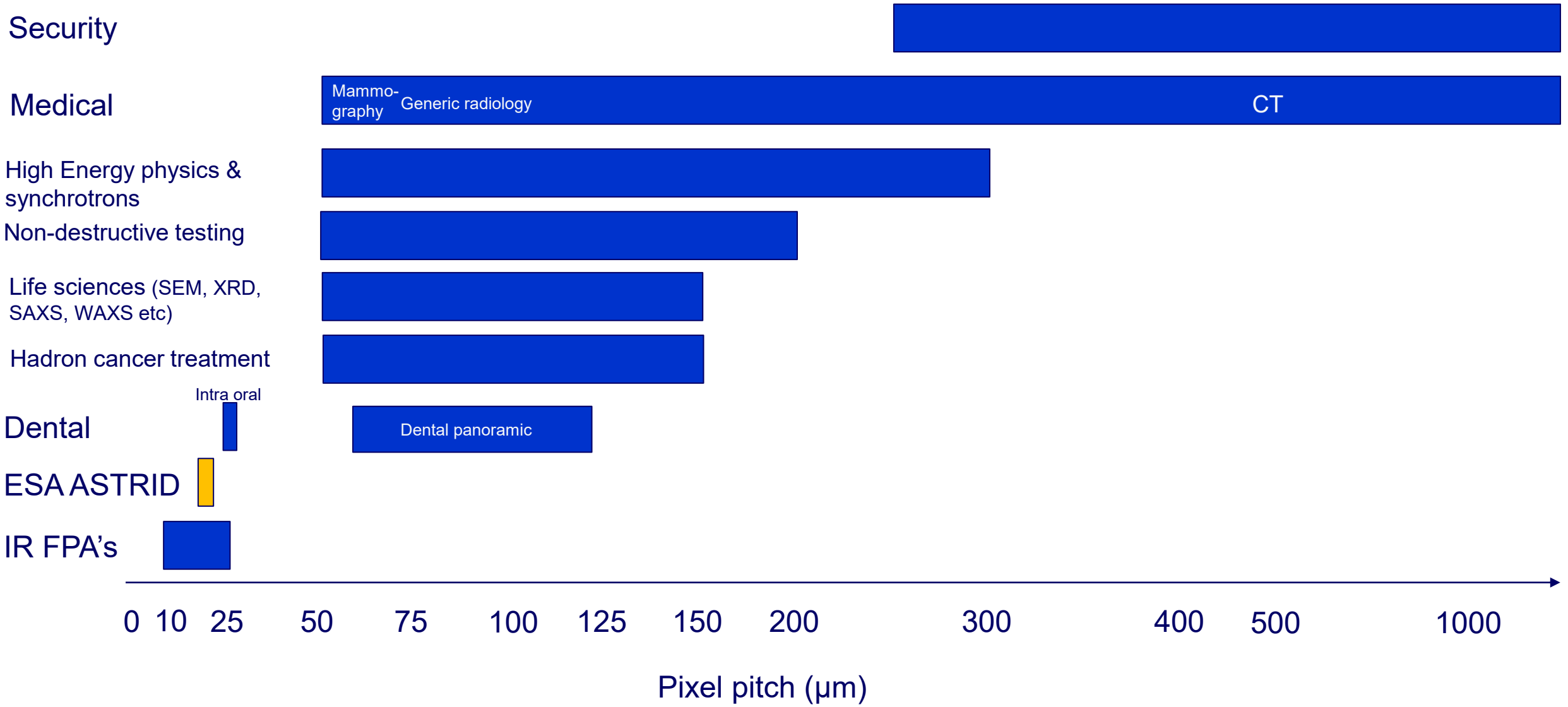
Subjective view on pixel pitch vs. applications in hybrid pixel detectors



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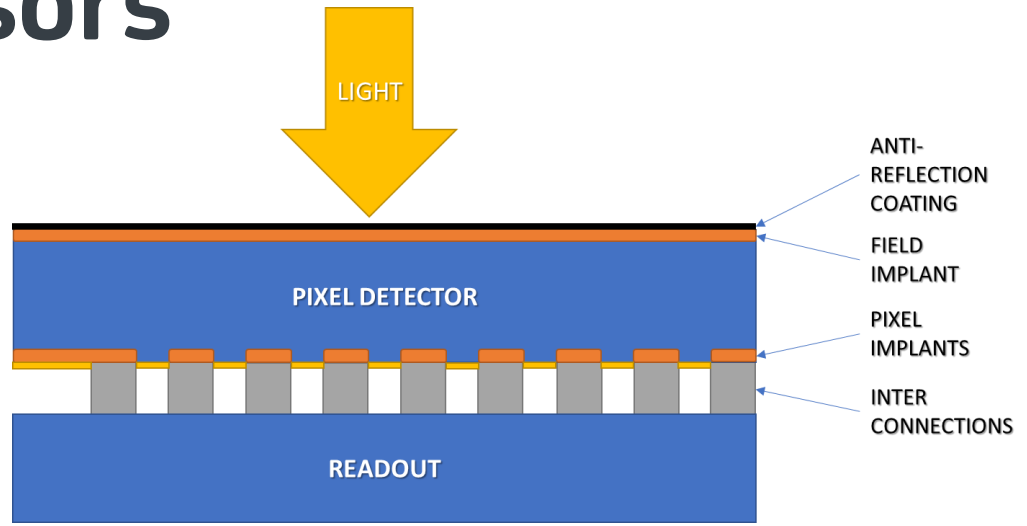
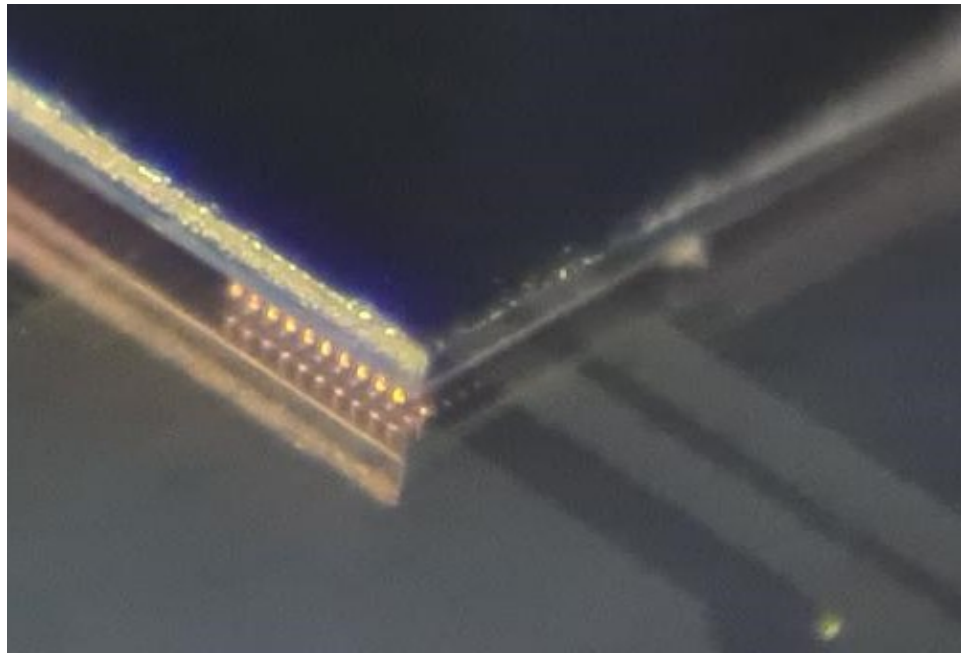
Hybridization of thin pixel sensors

- **Why it's not trivial?**
  - First time going for pixels or bumps at 20 um pitch
  - No previous experience in depositing ARC layer on 50 um thick sensor wafer
  - Solder bumping had been previously demonstrated at 26 um pixel pitch on 9cm²
  - Sensor biased through the ASIC at the edge of the pixel array
  - Bow of the sensor makes the FC bonding challenging





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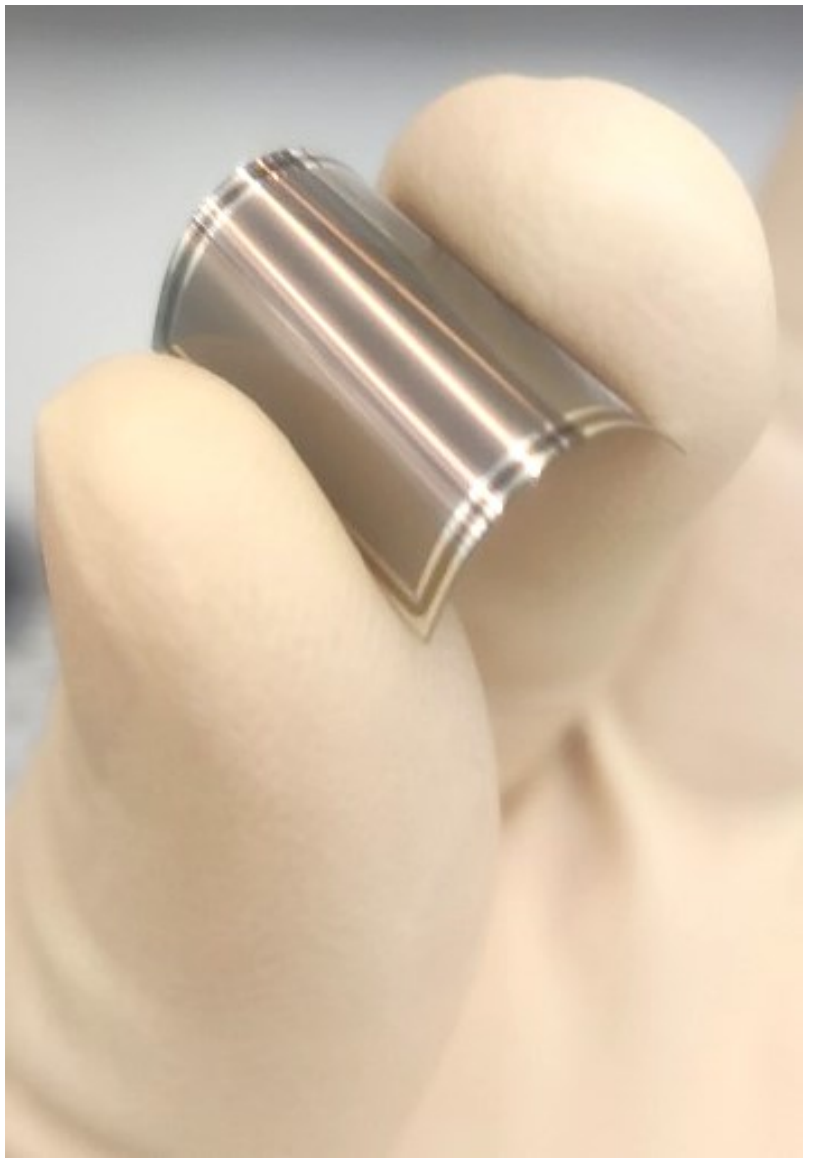
Detector – sensor chip

- **50 um thick P-on-N sensor fabricated on SOI wafers**
- **High-resistivity silicon wafer (15 kOhm-cm) used with biasing through chip (fringe) structure at the edge of the sensor**
  - Estimated depletion voltage ~14V
- **ARC layer based on multi-layer ALD coating on a very thin sensor wafer**
  - Al2O3:TiO2



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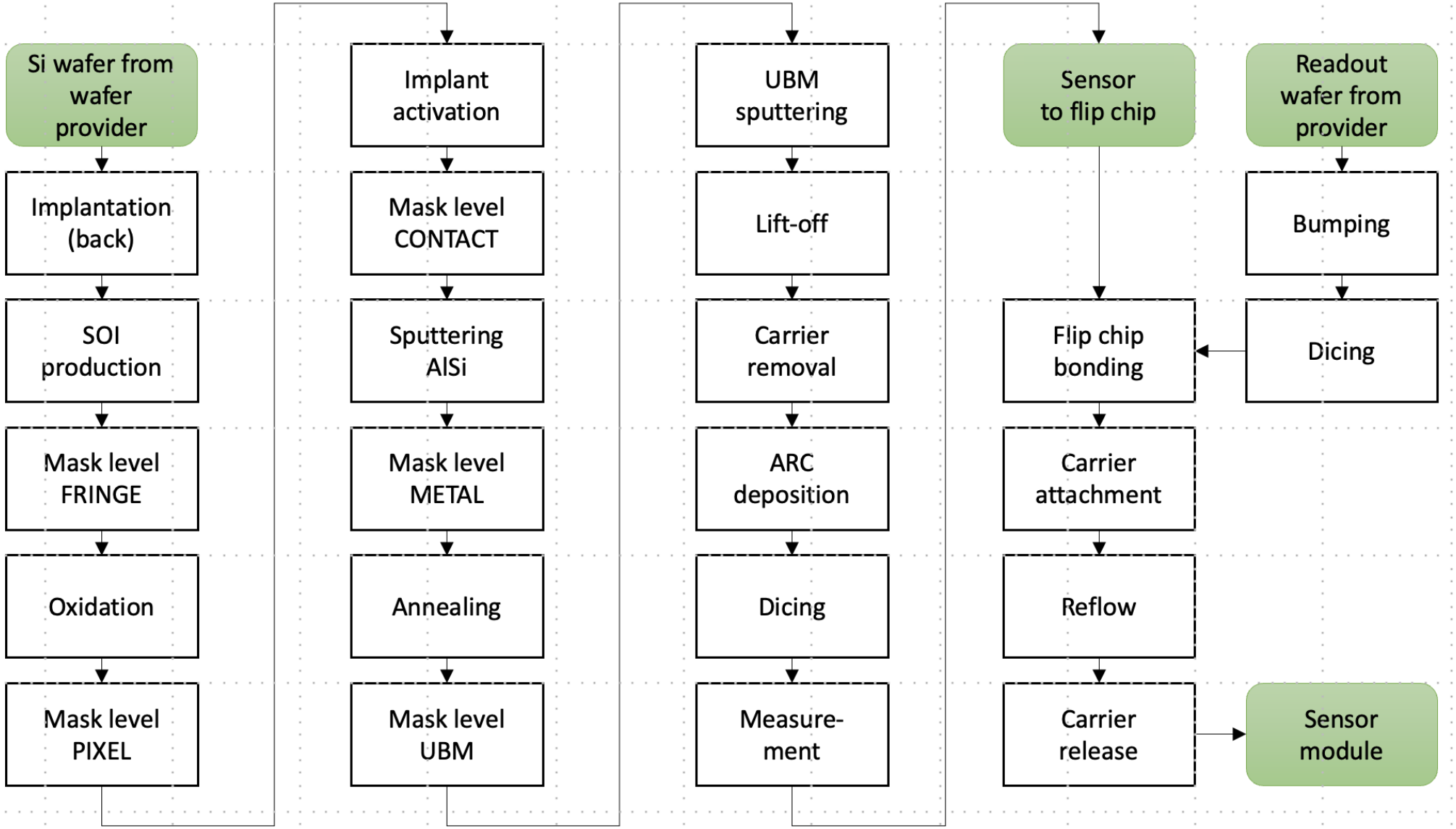
Detector – fabrication process flow



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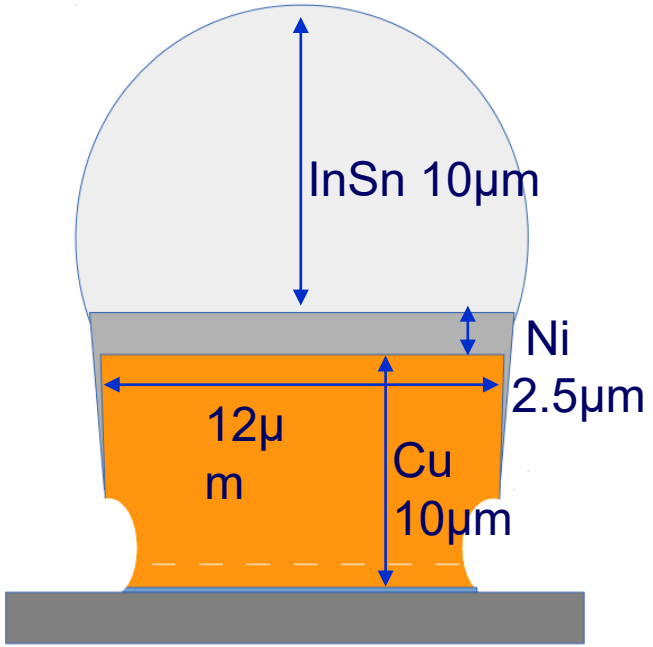
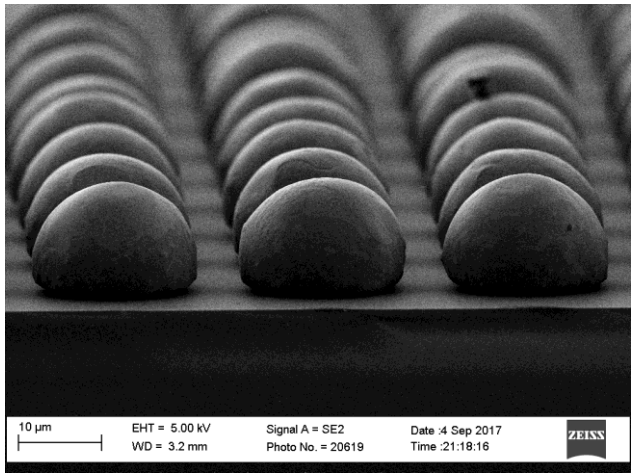
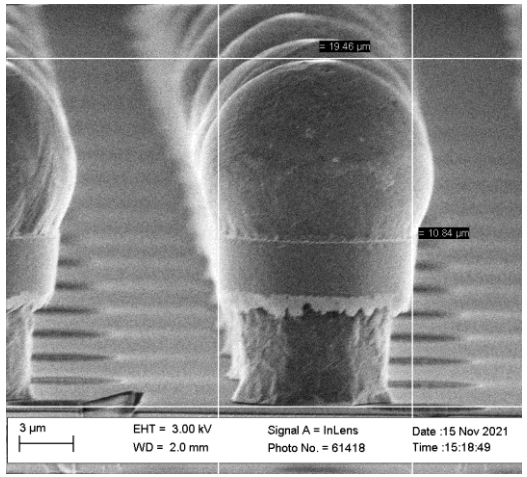
Detector – wafer bumping

- **Opening of the ROIC passivation at the pixels at Fraunhofer IZM**
  - 6 µm openings were not supported by the CMOS foundry
- **Cu pillar bumps (Cu/Ni/InPbSn) solder interconnects deposited at Advafab**
- **Cu pillars enable ultra-fine pitch bumping and minimize the solder bridges in flip chip bonding**
- **Uniformity of the bump deposition was a known challenge**



Conventional collapsible bumps placed at 25 µm pitch will form solder bridges during FC bonding because of high solder volume





Cu pillars have only rather small solder ball on top and the risk of forming solder bridges during FC bonding is greatly reduced

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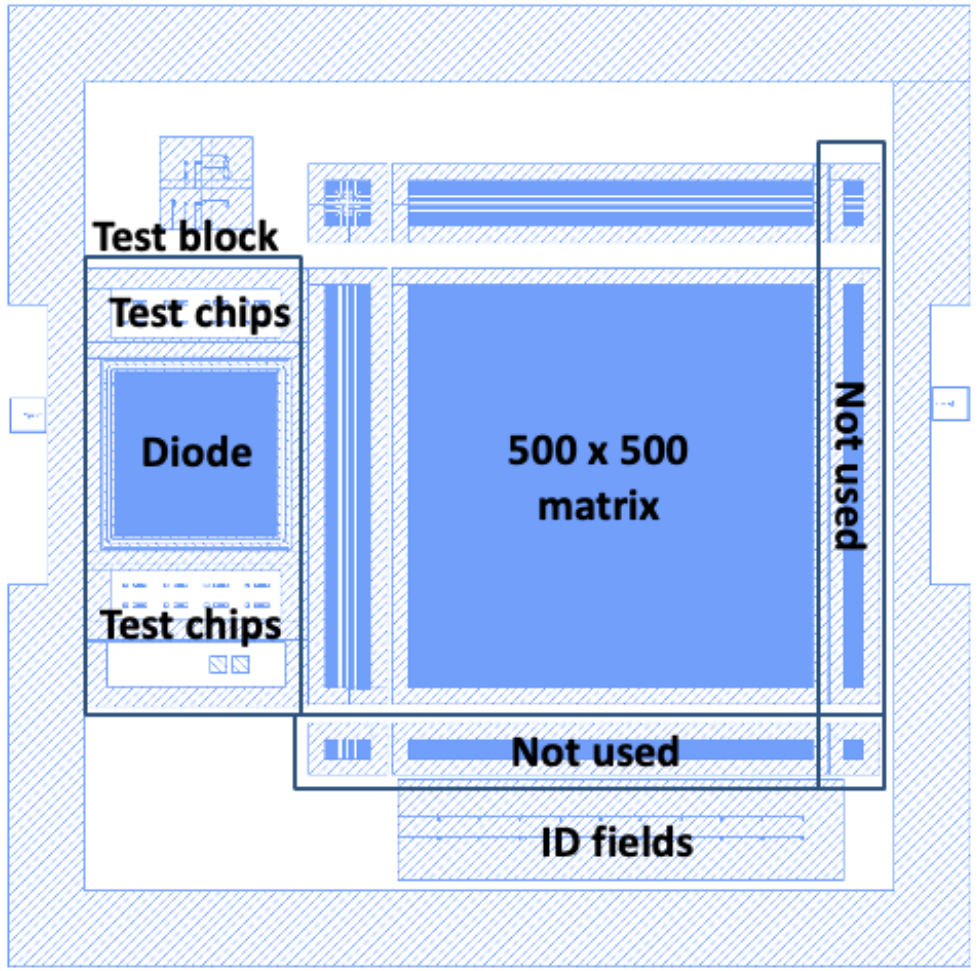
Process flow of sensor fabrication

- High resolution Si pixel sensors were manufactured with pixel array of 1024 x 1024 and pixel pitch of 20 µm.
- Total area: 21,080 x 21,080 microns including 300 microns edge on all sides.
- Stepper lithography used with the reticle design that gave an option to scale up (stitch) the sensor side for larger detectors
- P-on-N process is suitable for prescribed radiation conditions



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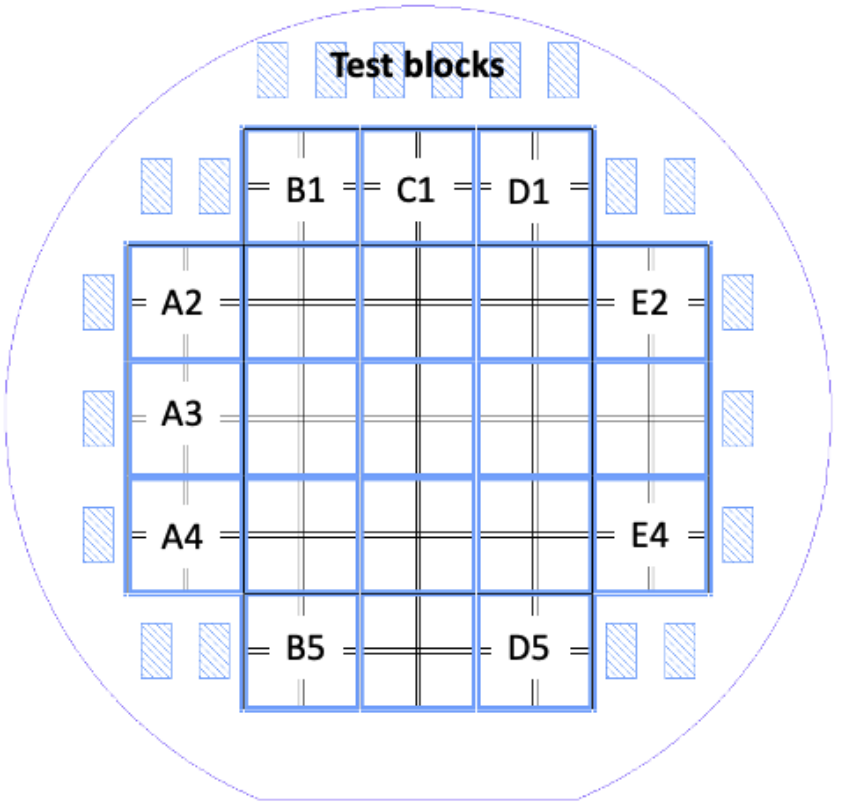
Process flow of sensor fabrication

- Sensors were manufactured on 150 mm high resistivity Si wafers (~15 kOhm-cm) on SOI wafers.
- Silicon On Insulator (SOI) technology was used for bonding sensors wafer to the carrier wafer
- Carrier wafer was removed from the sensor wafer after the UBM deposition
- ARC layers were deposited by ALD at low temperature (~120°C) on thin wafers TiO_2/Al_2O_3
- Wafers were diced into dies, the dies were visually inspected and the good chips were flip chip bonded.



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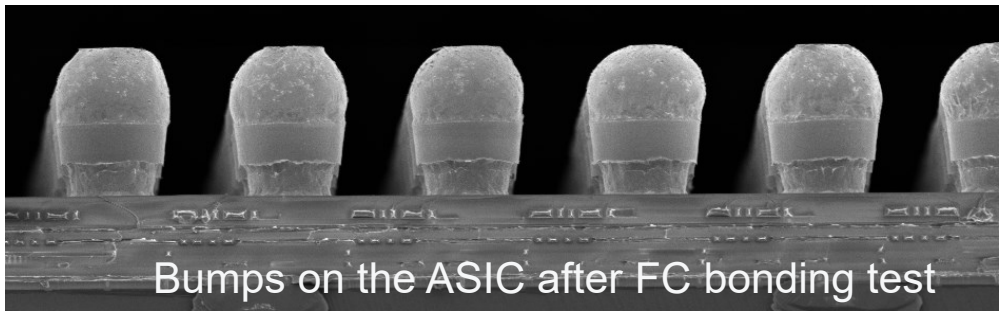
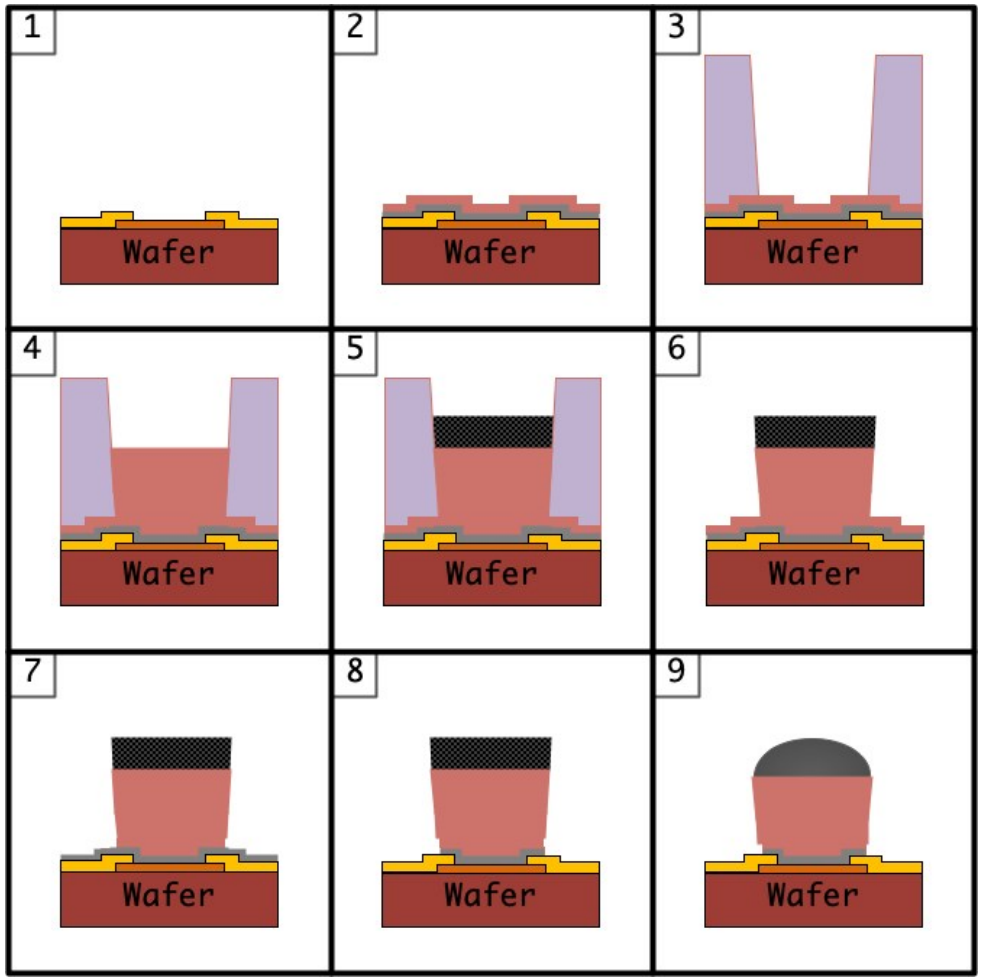
Process flow of wafer bumping

- **Solder bumps were deposited on the 200 mm CMOS wafers by electroplating**
- **12 µm bumps in diameter were patterned in the lithography**
- **Cu pillar with Ni layer formed the foot of the bump**
- **InSn based solder alloy was deposited on the pillars**
  - Low melting point alloy is favorable for managing thermo-mechanical stresses





1) wafer cleaning, 2) deposition of TiW/Cu adhesion/seed layers, 3) photolithography, 4) plating of UBM (i.e., Cu pillar), 5) deposition of In and Sn metal layers, 6) removal of the photoresist, 7) etching of Cu seed layer, 8) etching of TiW layer, 9) Solder reflow

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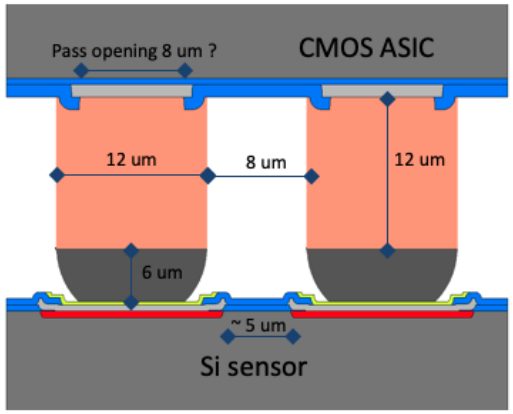
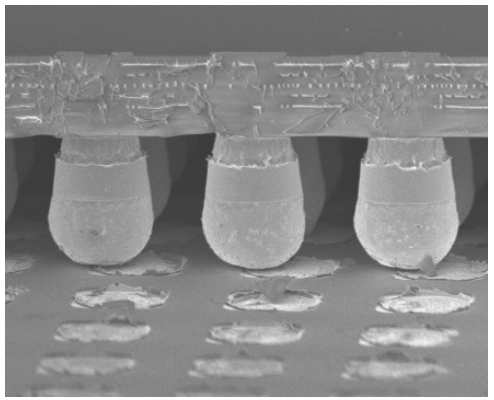
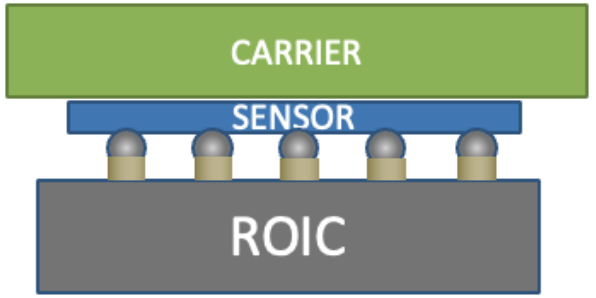
Flip chip bonding of hybrids

- Flip chip bonding was done on high-accuracy bonder
- Tack bonding + reflow in separate furnace
- ASIC (full thickness) and sensor were set parallel before starting the soldering process
- Process was set up using real dies and performing destructive tests
- White light optical profilometer was used for measurement of the bow of the modules

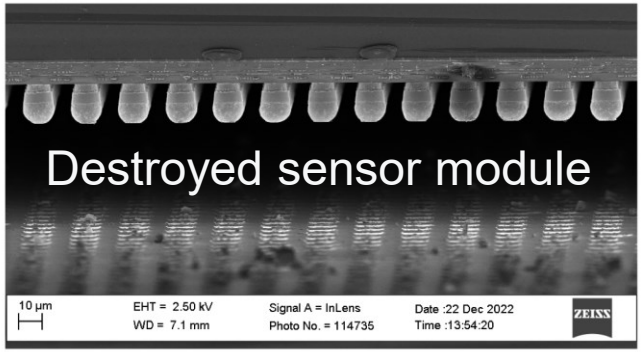




Profile of a sensor chip



Principle of using carrier substrates



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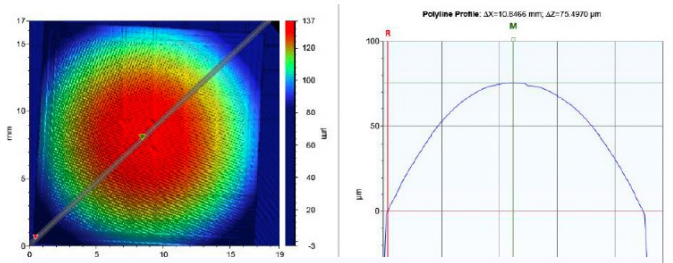
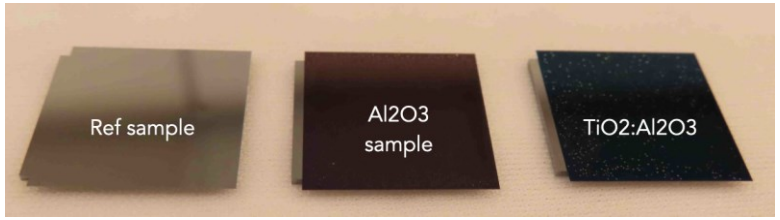
Optical profilometer measurements

- **White light optical profilometer was used as a tool measure the bow of the chips and**
  - Gives an indication of magnitude of the bow

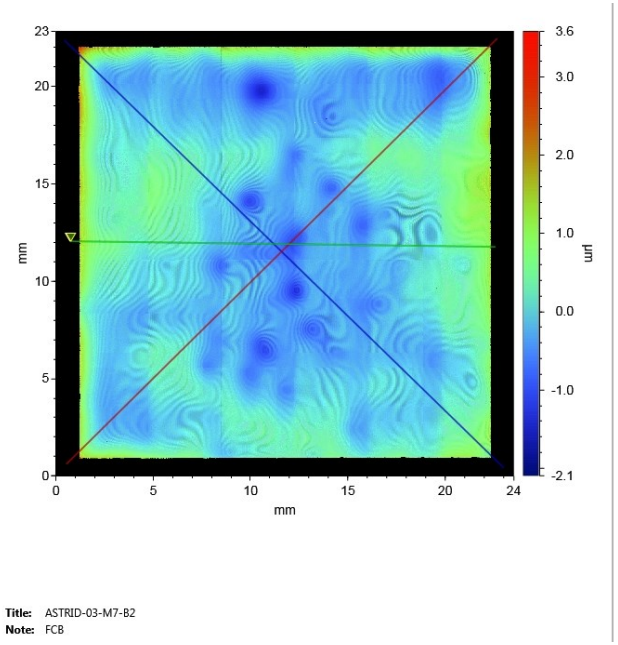


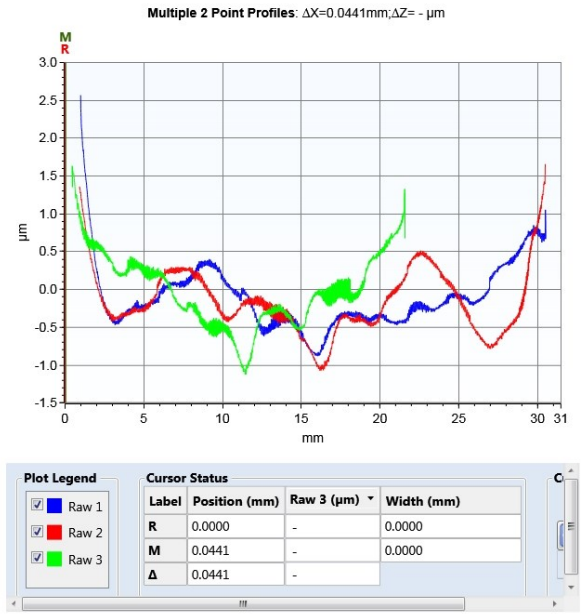
Sensor chips have a convex profile (pixels heading up)

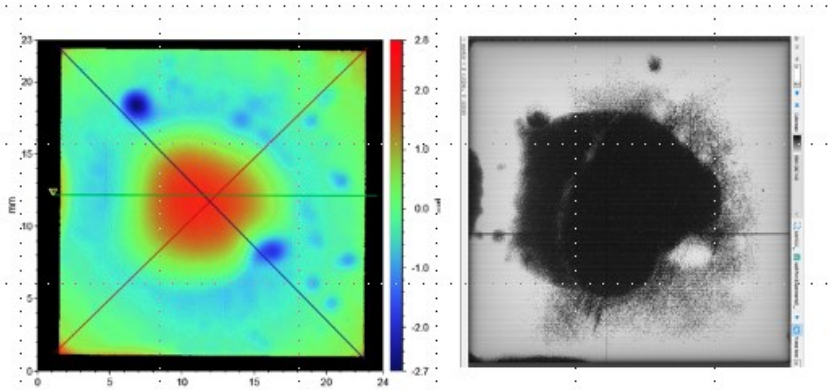
Sample	Front (um)
Si reference sample w/o ARC	44
ALD-Al_2O_3 Sample-01	62
ALD-TiO_2/Al_2O_3 Sample-01	75



Bow increased across the mechanical sensor after deposition of the ALD layers







Left: delamination on the optical profilometer image.
Right: test image acquired by illumination

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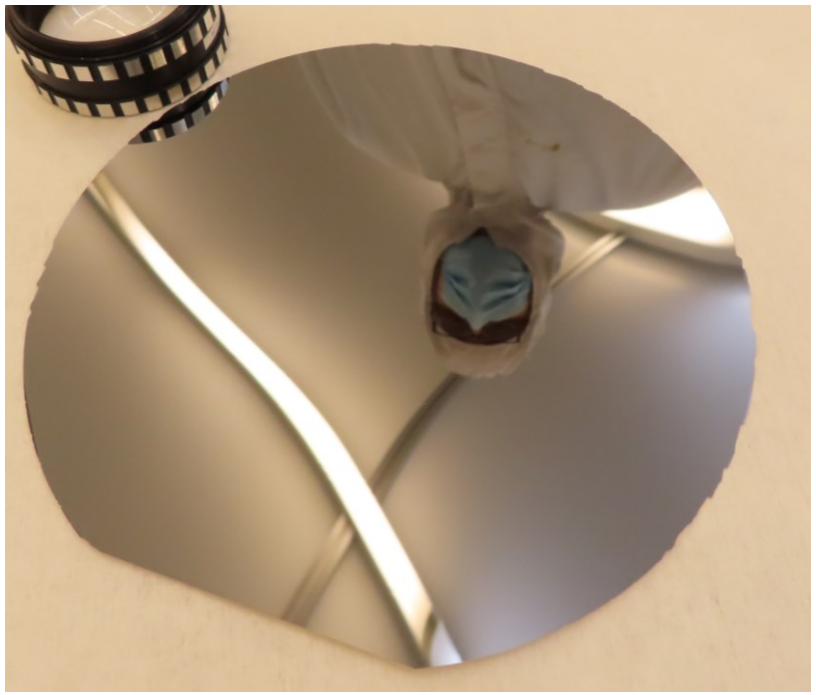
Challenges in sensor fabrication

- **Small pixel size – stepper-based lithography worked well**
  - High pixel patterning yield
- **Imbalanced thin film stresses – several metal layers at the pixel side and only ARC layer at the entrance window**
  - Wafers were too curved to be measured for the bow
  - ARC layers increased the bow of the sensor
- **Thin wafer handling (ARC coating and dicing steps)**
  - Some of the wafers were cracked
  - Three fabrication runs were helpful for sorting out the issues



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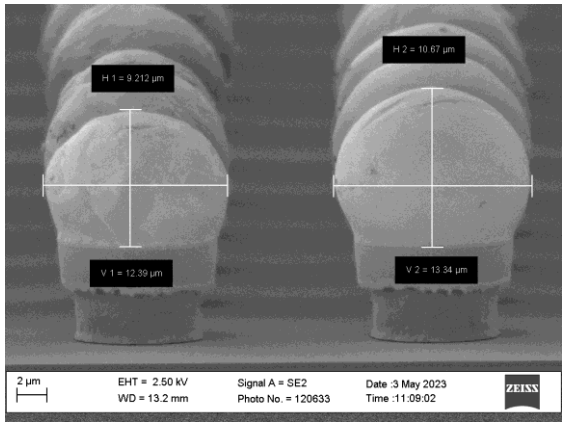
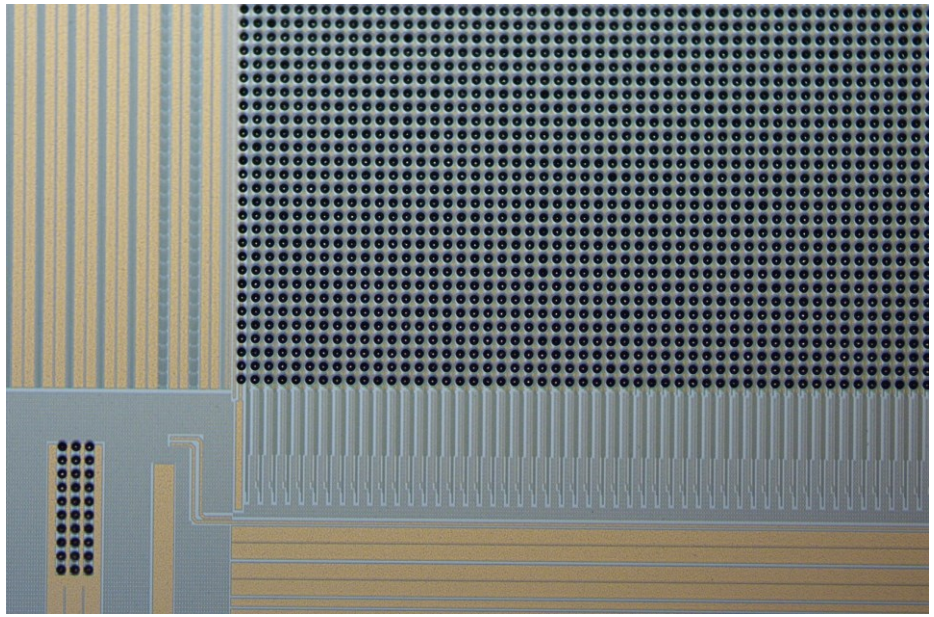
Challenges – wafer bumping

- **Good height uniformity of the solder bumps is critical for FC bonding**
- **Deposition of 12 µm bumps seemed to be at the low end of the process window**
- **Wet etching of the seed layers isn't trivial**
- **Issues especially with In deposition**
  - Issues with the chemistry
  - Time dependent shift in the process
  - Wetting in small resist openings





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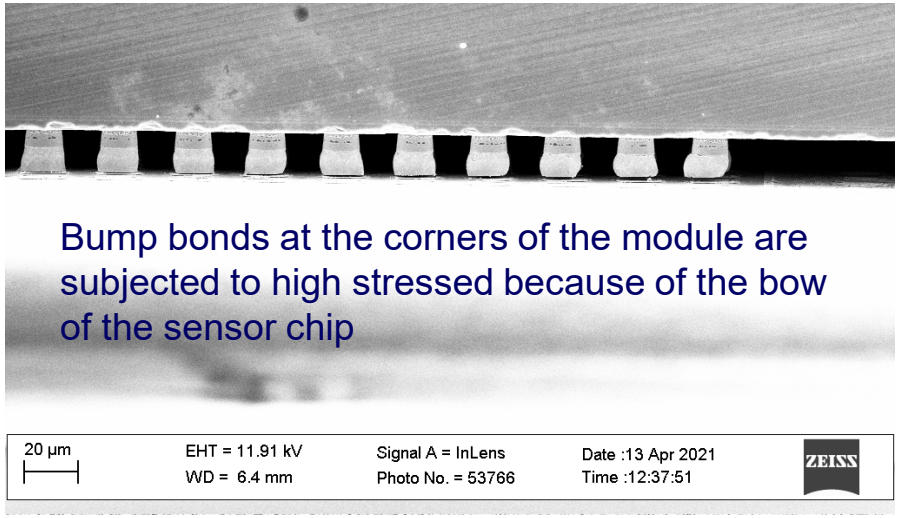
Challenges in FC bonding

- **FC bonding of thin chips has shown to be challenging**
  - Metal layers thermally expand with temperature
- **Project started with well bonded detectors, but the FC process drifted during the project leading to failures**
- **Thin sensor chips bow ~ 90 µm over the die and the Cu pillars are only 22 µm high**
- **Noble Under-Bump Metallization (UBM) was used in combination with indium (In) based solder**
  - Limited amount of interdiffusion between the metals during the FC bonding process
- **Thin hybridized modules may be strong but they are also very fragile**



Bump bonds at the corners of the module are subjected to high stressed because of the bow of the sensor chip

Outlook for future fabrication

- Thinner entrance window
- Thicker sensors
- Other sensor materials GaAs, Cd(Zn)Te for higher energies
- GaAs sensor manufacturing in-house
- More reactive UBM material (Ni/Au) on sensor wafers

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Summary of HYBRID measurements

1. Intro to analog chain
2. Photoresponse
3. Noise
4. Quantum Efficiency
5. MTF & Cross-talk
6. Radiation effects
7. Summary of results ←→ specifications

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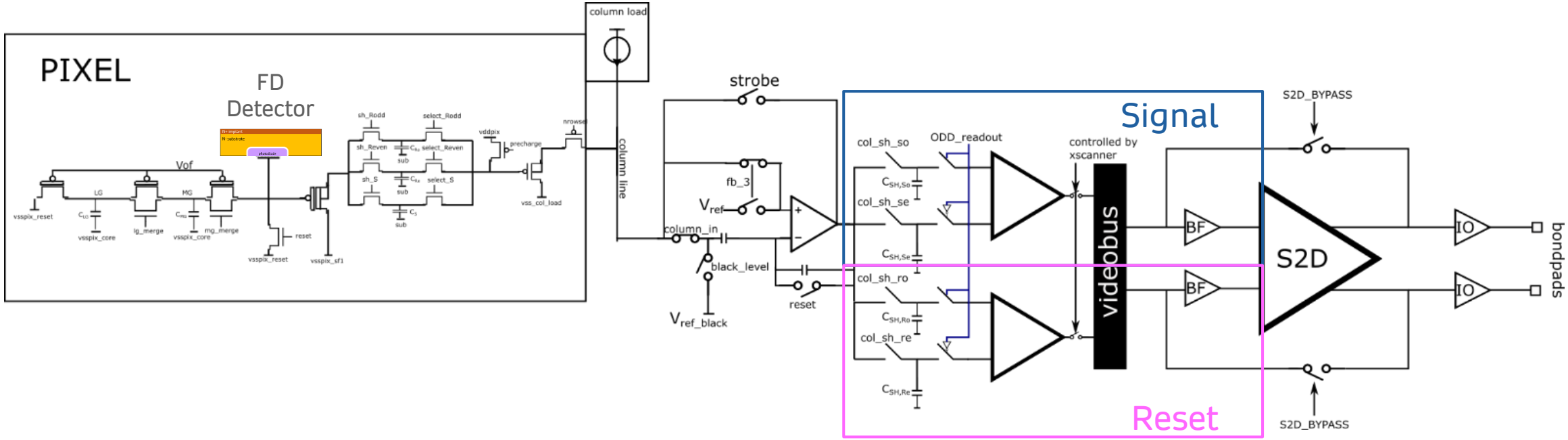
ROIC development – Analog Chain

- **Reads out all pixels to 4 analog differential output channels**
  - 4 reset video busses and 4 signal video busses
  - Internal conversion pseudo-differential to fully differential
  - 50Hz frame rate for full frame (1k x 1k pixels)



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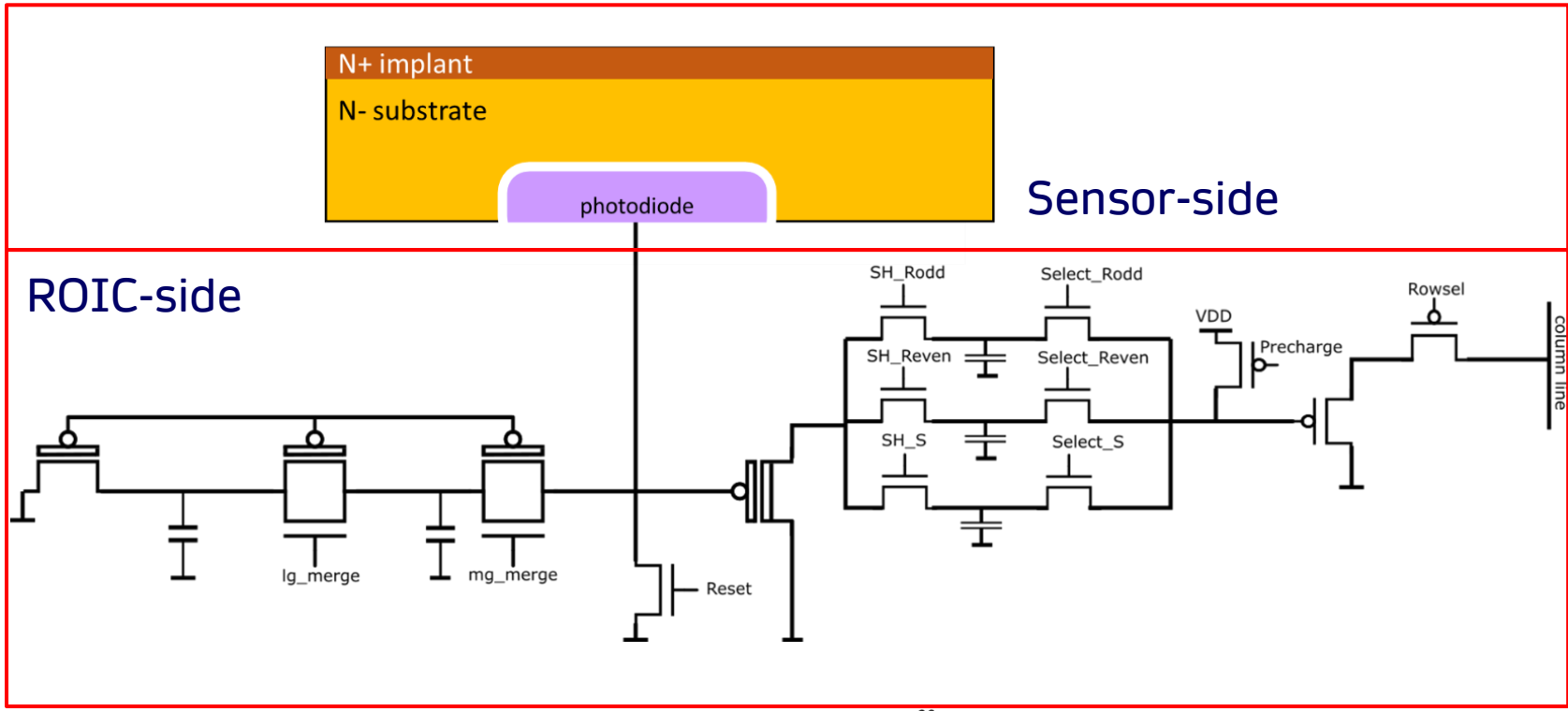
Pixel Schematic

- **CMOS technology**
- **Features**
  - Global Shutter
    - 3 in-pixel memories
  - 3 Charge Handling Capacities
    - 3 in-pixel gains
    - Synchronous HDR
  - Fully programmable integration time
- **Uncertainty**
  - Parasitic capacitance at photodiode



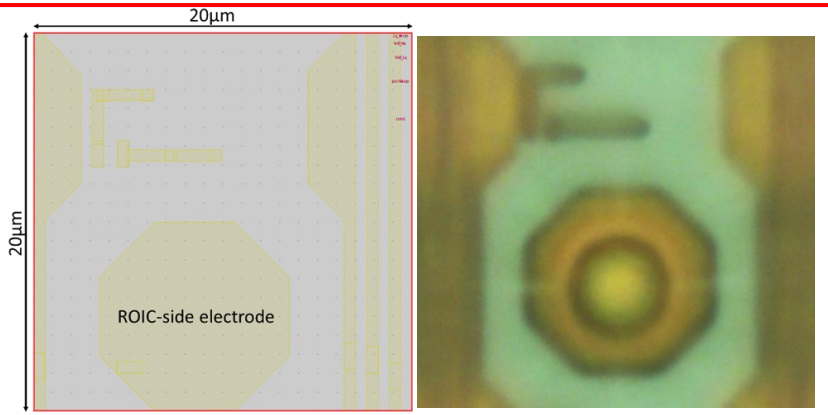


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Photo Response

1. Methodology
2. Different column gains
3. Test pixels and black columns
4. RWI CDS and ITR HDR photo response and mean variance
5. Non-linearity
6. Charge Handling Capacitance (full well)
7. PRNU investigation
8. Charge-to-Voltage conversion factor (CVF)
9. Response vs. integration time

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Methodology

- **Purpose: to optimize sensor operation via tunable parameters**
  - Back bias voltage
  - Pixel reset voltage
  - Column load
  - VDDPIX pre-charge voltage
  - Overflow voltage
- **Conditions:**
  - Dark Chamber at room temperature (uncontrolled)
  - Controlled light source of 525nm

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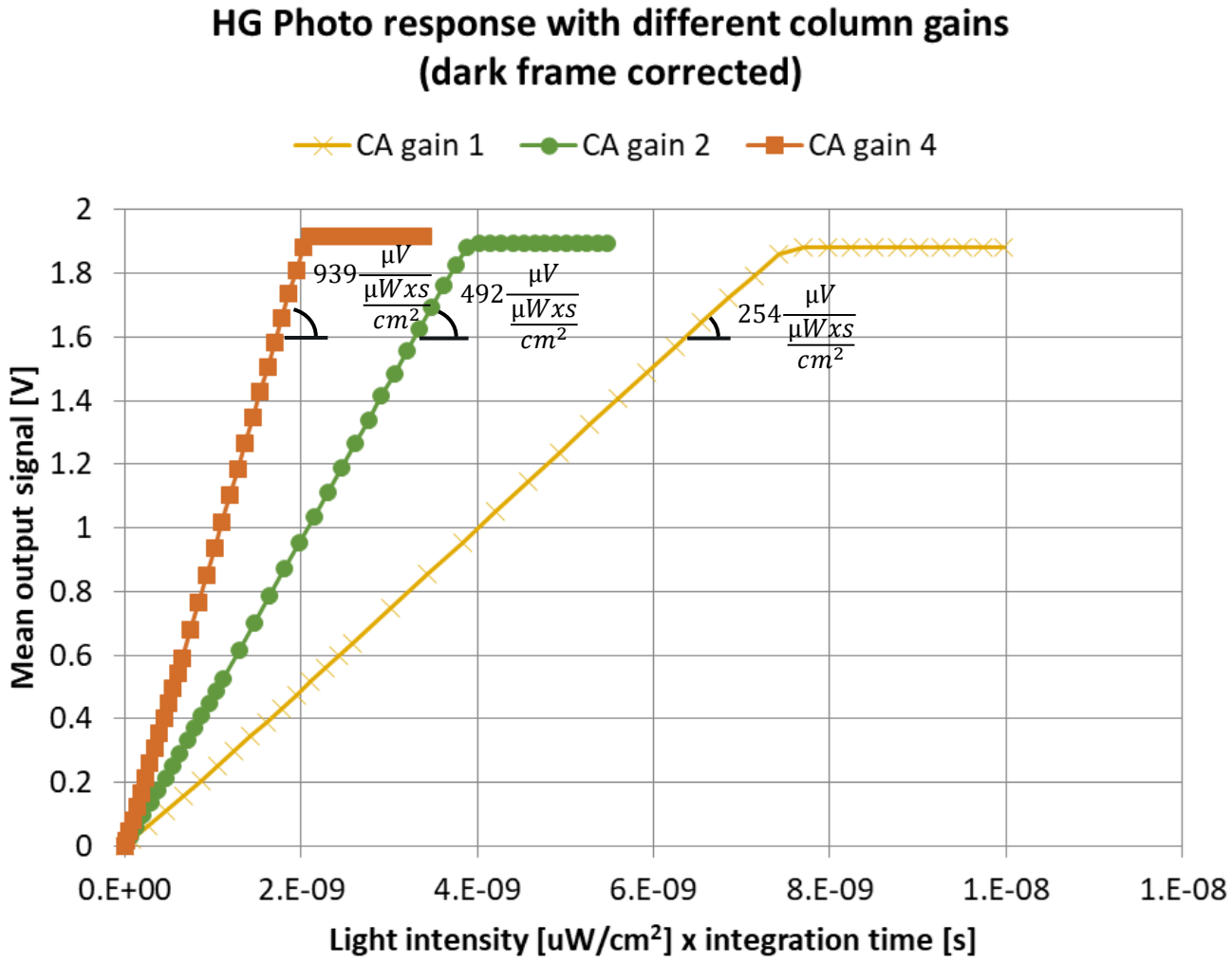
column gains response

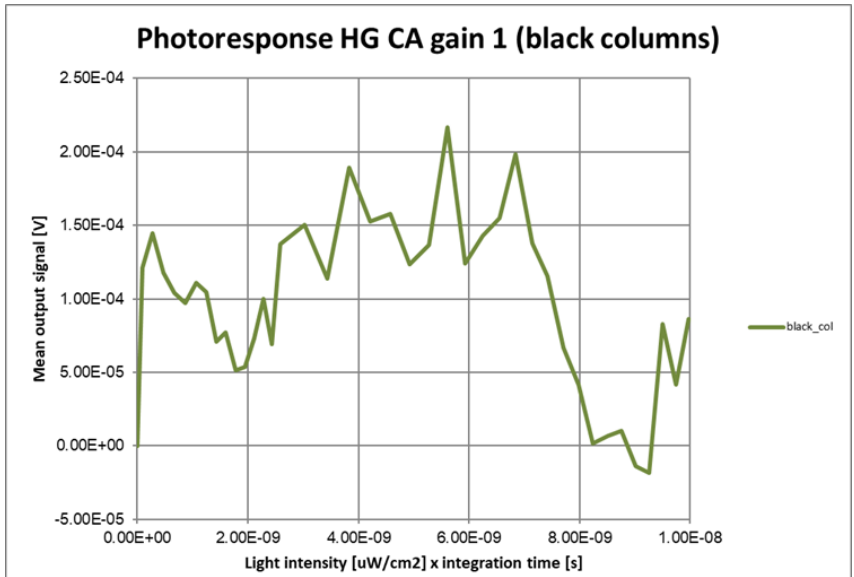
- **Measured gains match designed values**

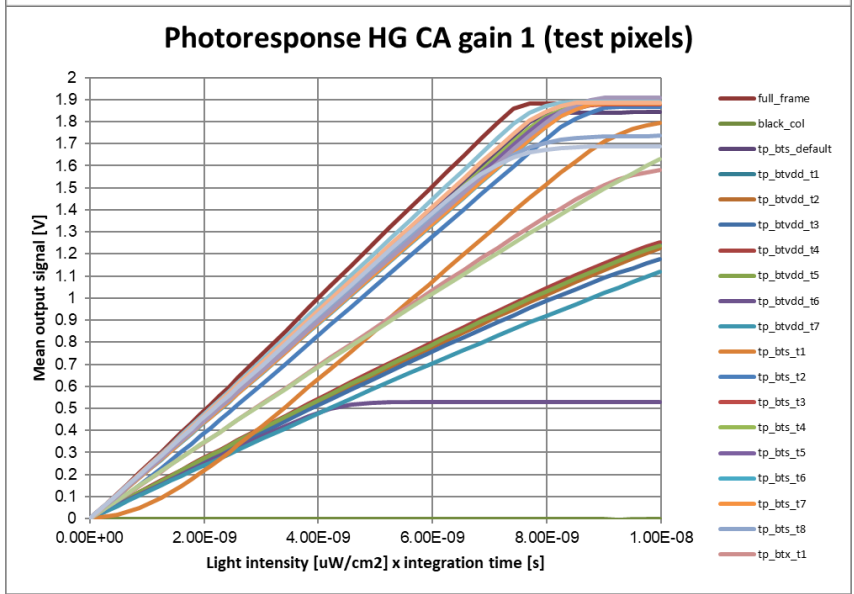


Ideal CA gain setting [V/V]	Column amplifier gain Simulated [V/V]	Column amplifier gain Measured [V/V]
2	1.98	1.93
4	3.85	3.68

Test pixel variants and black columns response

- **Black pixel column photo response**
  - Electrical black pixels
  - As designed, no light sensitivity
- **22 Test pixel variants photo response**
  - Default pixel outperforms others for linearity & gain
  - Variants
    - Different types,
    - Different W/L sizing of source followers,
    - Simplified structures,
    - Different connectivity in the schematic (e.g., bulk-to-supply source followers).





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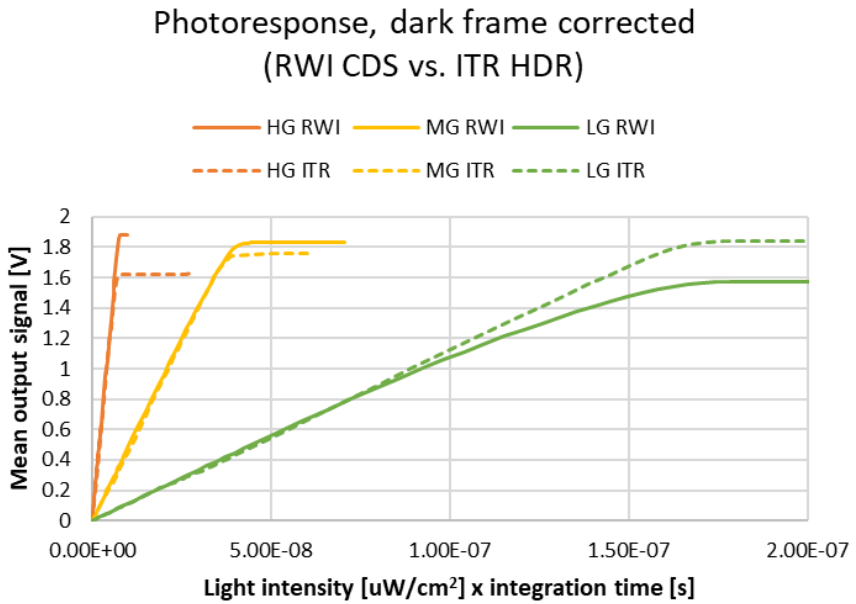
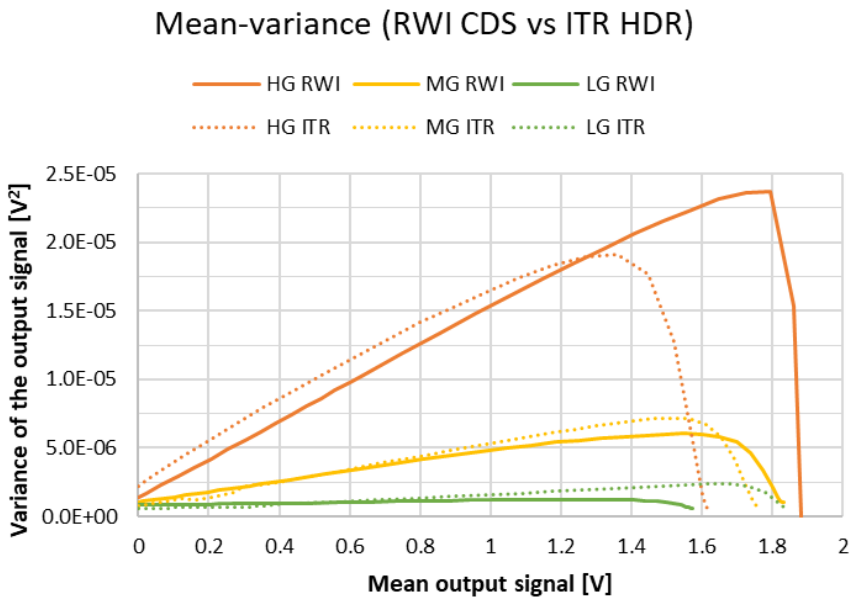
RWI CDS and ITR HDR response

- **Read While Integrate CDS**
  - HG, MG, LG
- **Integrate Then Read non-CDS**
  - HG, MG, LG
- **Programmable full well matches design values**
- **ITR provides synchronous HDR in 3 ranges**

High Gain (HG)
Medium Gain (MG)
Low Gain (LG)





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RWI CDS and ITR HDR response

Charge Handling Capacity –Charge accumulation at saturation

Read out mode	In pixel gain	Column gain	Full Well	Specification
RWI CDS	HG	1	58 ke^-	<100 ke^-
		2	30 ke^-	
		4	16 ke^-	
	MG	1	300 ke^-	
	LG	1	1.2 Me^-	>1 Me^-
ITR HDR	HG	1	52 ke^-	<100 ke^-
	MG	1	293 ke^-	
	LG	1	1.2 Me^-	>1 Me^-

The programmable full wells reach the requested specifications.

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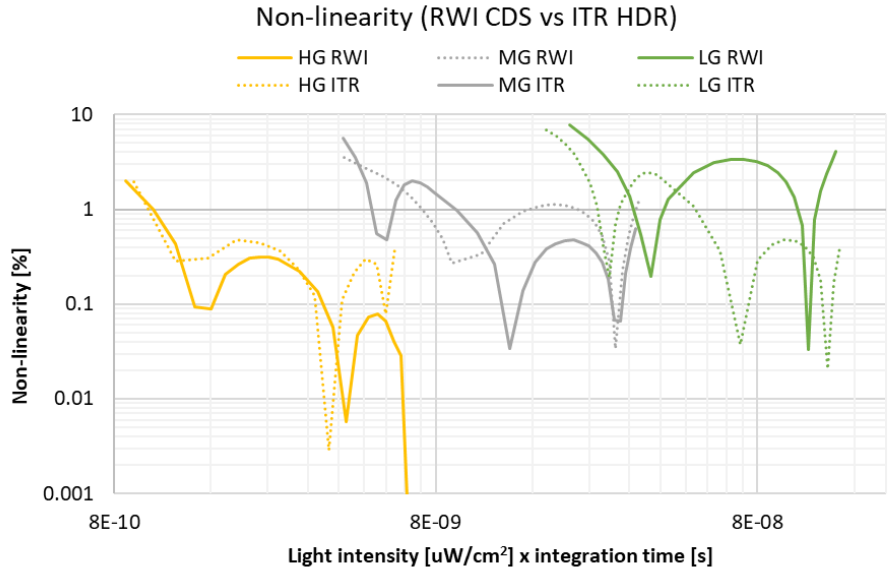
RWI CDS and ITR HDR response

- **Non-linearity calculated from photo response**
  - $NL_i(\%) = 100 * \frac{y_i - (Ax_i + B)}{Ax_i}$
  - $NL\ error\ (\%) = \max_i NL_i - \min_i NL_i$
    - With $Ax_i + B$ the best linear fit in 10-90% of saturation region
    - With y_i the actual detector response
- **Off-chip calibration required to reach <1% NL**

The measured non-linearity is within expectations from design.



Read out mode	In pixel gain	Column gain	Non-linearity error [%]
RWI CDS	HG	1	1.98
		2	2.61
		4	2.55
	MG	1	3.53
	LG	1	7.73
ITR HDR	HG	1	1.97
	MG	1	5.56
	LG	1	6.83

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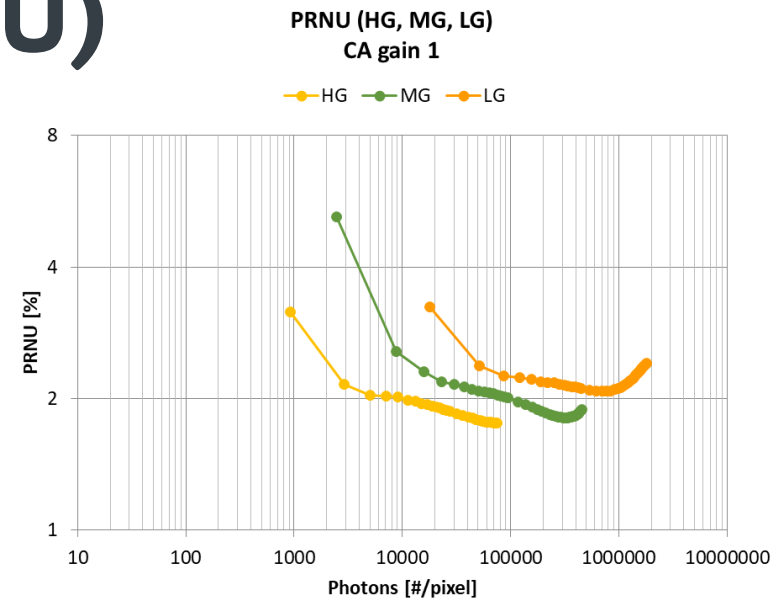
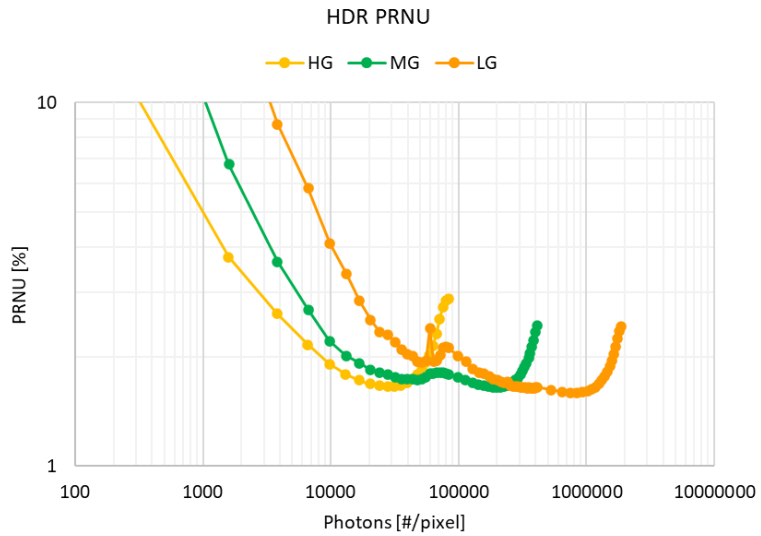
Photoresponse non-uniformity (PRNU)

Spatial noise of imager vs. illumination

$$PRNU_{\%} = \frac{stddev(grey - dark)}{avg(grey - dark)}$$

Read out mode	In-pixel gain	Full frame PRNU at 50% [%]	6x6 windows PRNU [%]
RWI CDS	HG	1.8	1.7
	MG	1.8	1.7
	LG	2.0	1.9
ITR HDR	HG	1.7	1.5
	MG	1.6	1.5
	LG	1.6	1.4





The full frame PRNU reaches specification.
The 6x6 windows PRNU is higher than expected.

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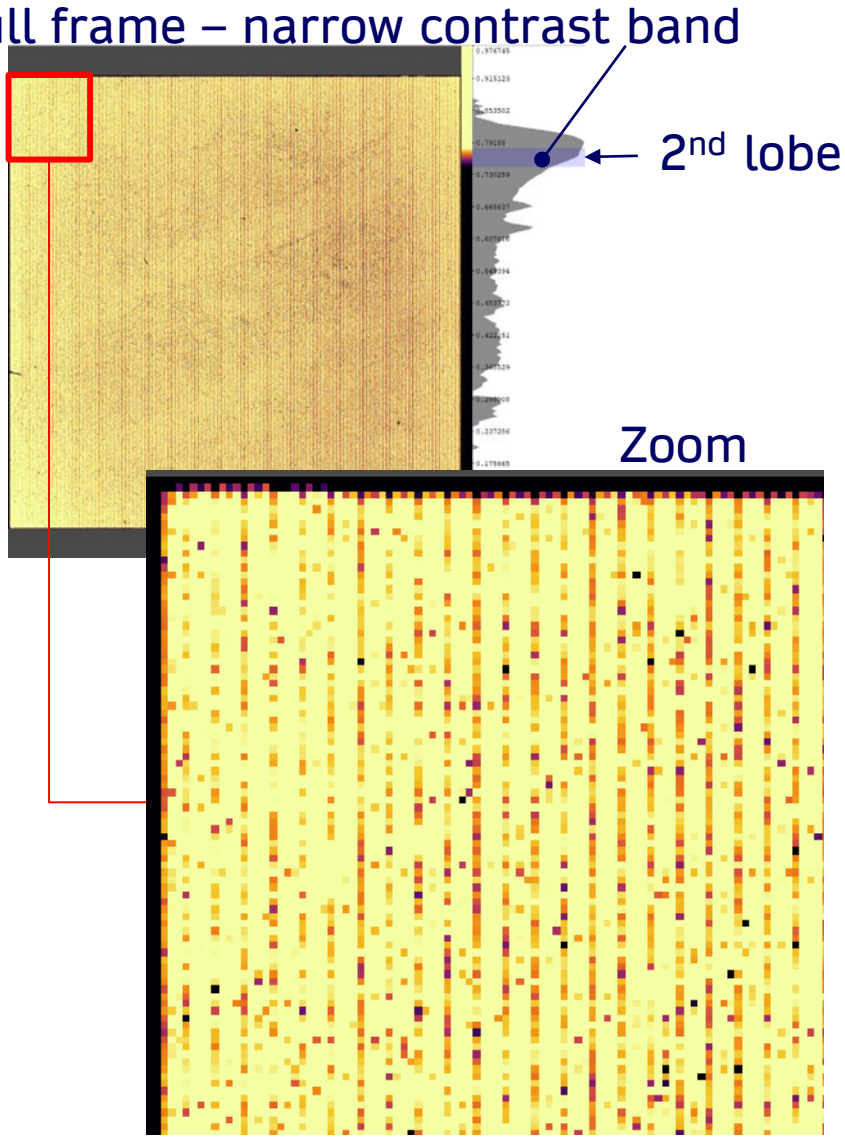
Photoresponse non-uniformity (PRNU)

- **Second lobe visible in histogram plot**
  - FPN on 1 out of 4 columns
  - Correlates with 1 out of 4 video busses
- **Pre-charge timing issue**
  - Pre-charge pulls signal darker while S2D is sampling



Timing issue in one of the 4 channels causes an increase in the overall PRNU, explicitly in the 6x6 windowed PRNU.

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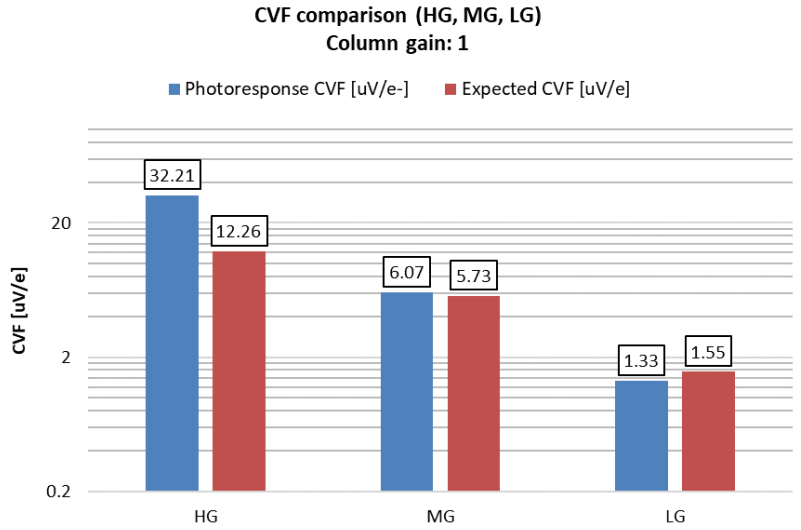
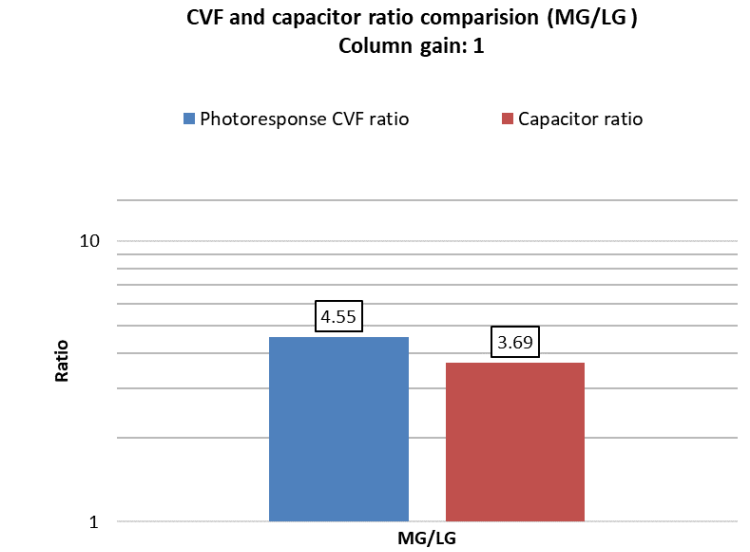
Charge-to-Voltage Conversion factor (CVF)

- **Photo response curve + QE ➔ CVF**
- **CVF ratio (LG/MG) is in line with capacitor ratio (C_{LG}/C_{MG})**

Read out mode	In pixel gain	Column gain	CVF [µV/e-]
RWI CDS	HG	1	32.2
		2	62.2
		4	119.0
	MG	1	6.0
	LG	1	1.3
ITR HDR	HG	1	31.0
	MG	1	6.0
	LG	1	1.4





Measured CVF matches design values, calculations in LG, MG
HG deviates due to overestimation of parasitic capacitances

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Photo response vs. integration time (T_{int})

- **RWI, non-CDS readout**
  - Meets expectations above 50µs
  - Extremely short (<50µs) T_{int} exhibits:
    - Loss of gain
    - Loss of linearity
- **Shutter efficiency is light dependent**
- **Still able to reduce exposure time by factor of 400 (20,000:50)**

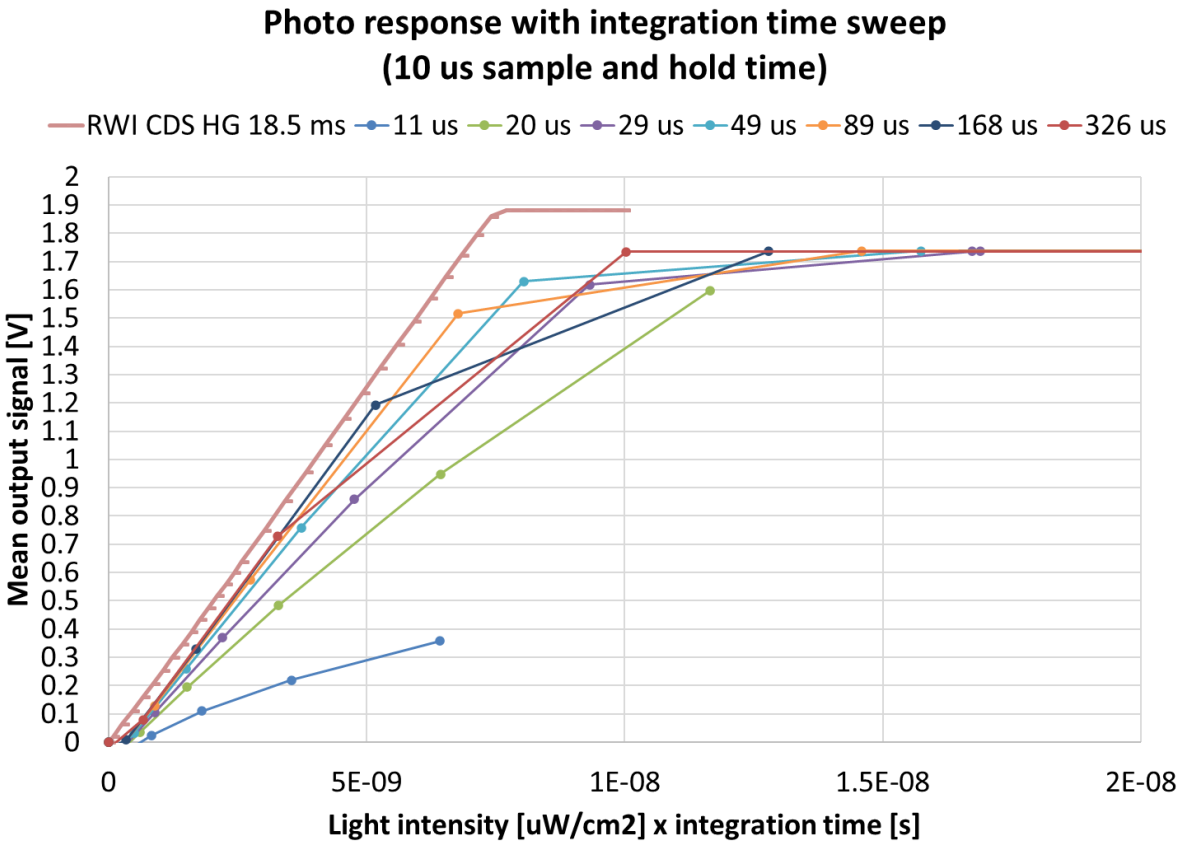

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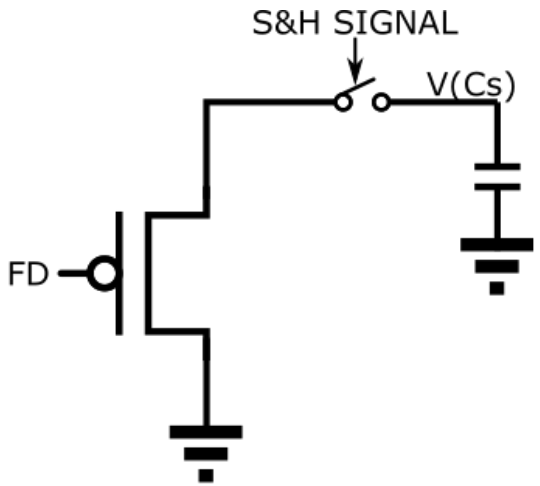
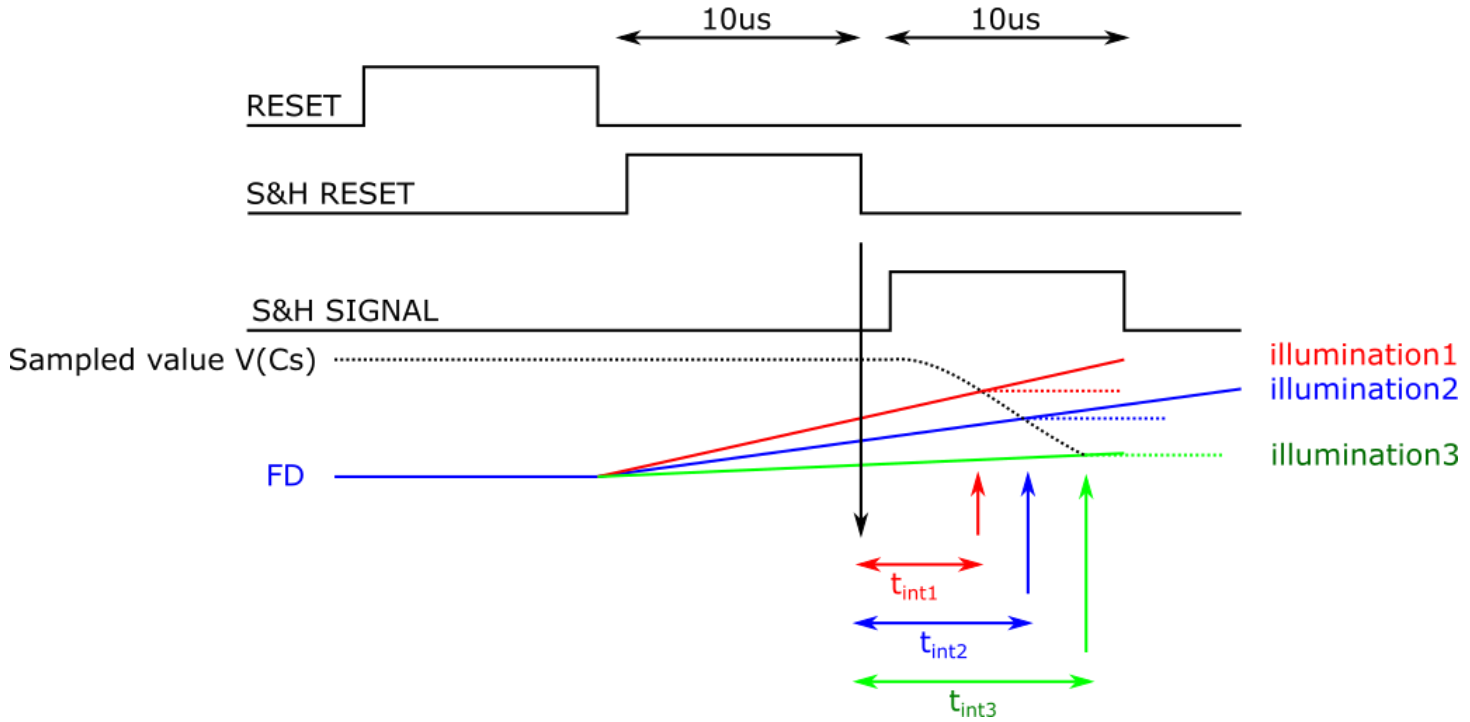
Photo response vs. integration time (T_{int})

- The true end of integration time depends on the illumination, not on the end of S&H signal.
- Exposure time is shorter than the programmed integration time, and the delay is light dependent





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Noise

1. Methodology
2. Summary results
3. Noise histogram analysis
4. Noise measurements per channel
5. Noise contributors within analog chain

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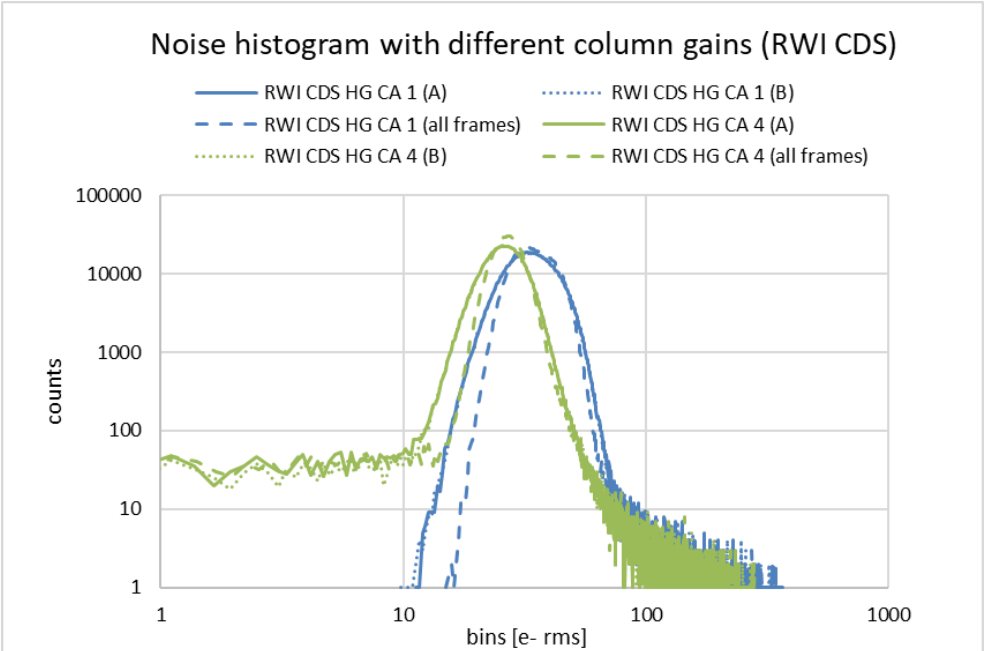
Methodology

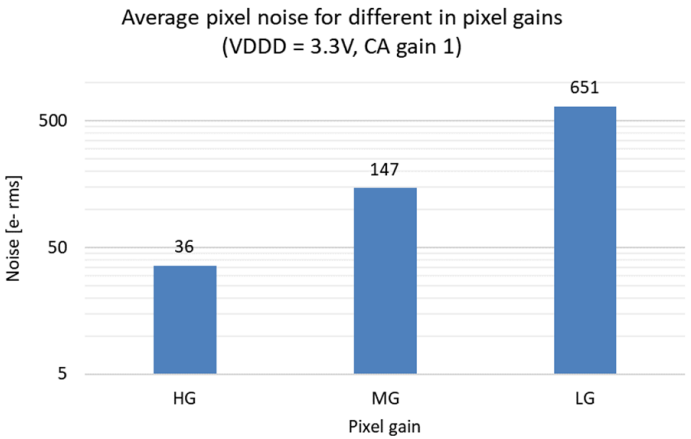
- **Purpose:**
  - Measure the noise in the image (V_{RMS}) for the following different modes:
    - Read While Integrate (RWI) with Column Amplifier (CA) gain 1.
    - Read While Integrate (RWI) with Column Amplifier (CA) gain 4.
- **Conditions**
  - Dark chamber at controlled temperature ~22°C
  - 3 noise histograms are derived:
    - For all frames
    - For only Odd frames (Frames A)
    - For only Even frames (Frames B)

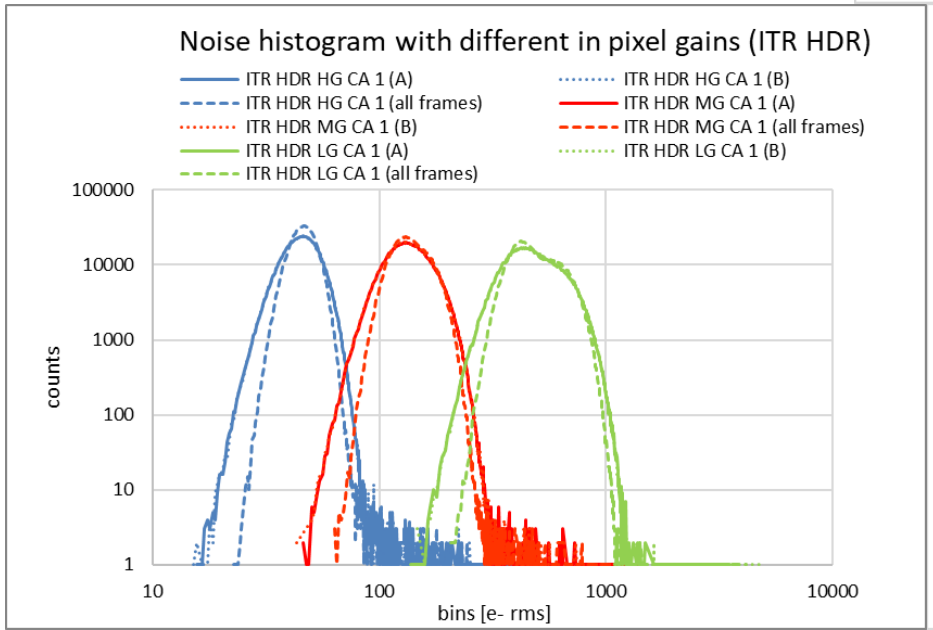
Summary of Noise Results

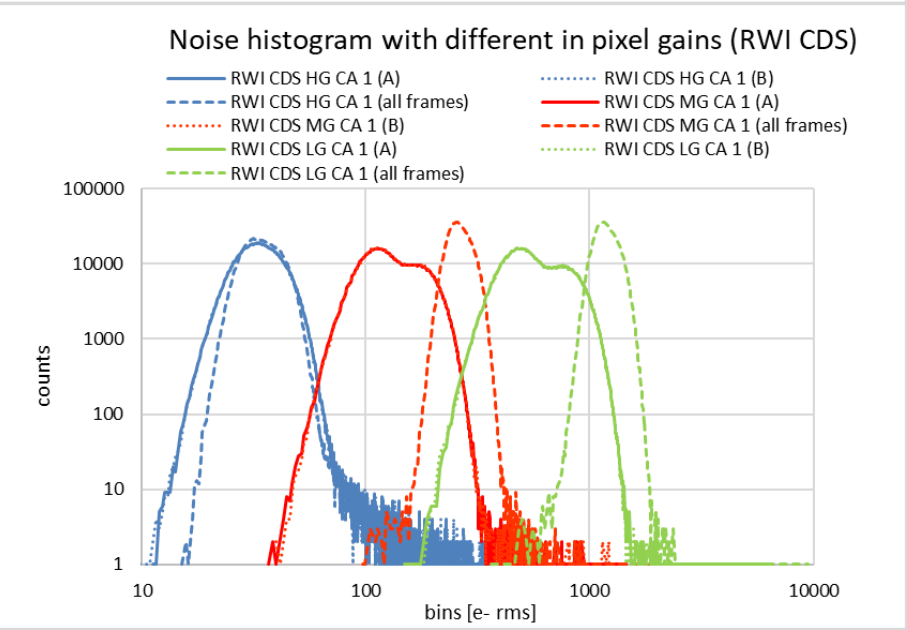
Read out mode	In pixel gain	Column gain	A-Frame noise [e^-_{rms}]	B-Frame noise [e^-_{rms}]	All frames noise [e^-_{rms}]
RWI CDS	HG	1	36	36	37
		4	28	28	28
	MG	1	147	148	269
	LG	1	651	652	1214
ITR HDR	HG	1	47	47	47
	MG	1	144	144	145
	LG	1	527	527	529

Noise measurements show deviating (too high) results.



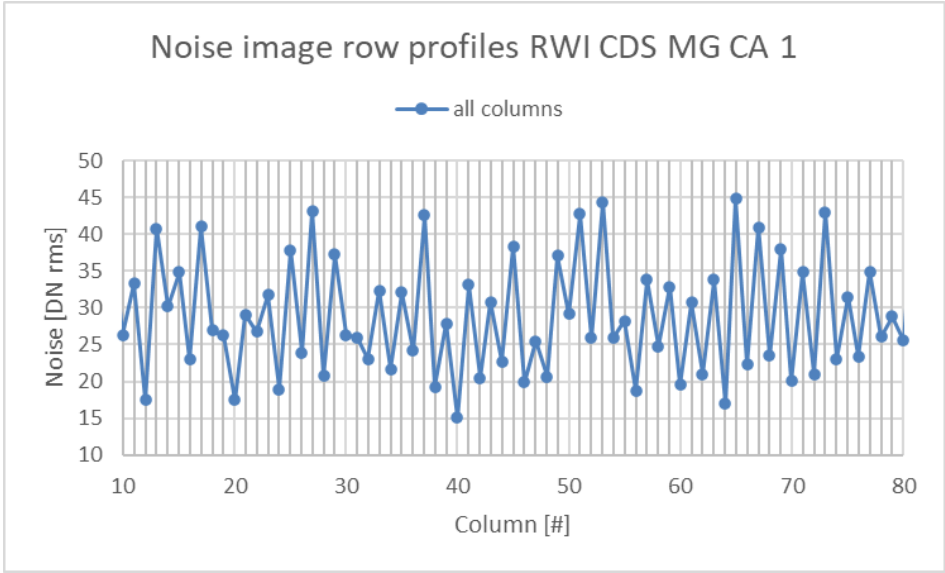




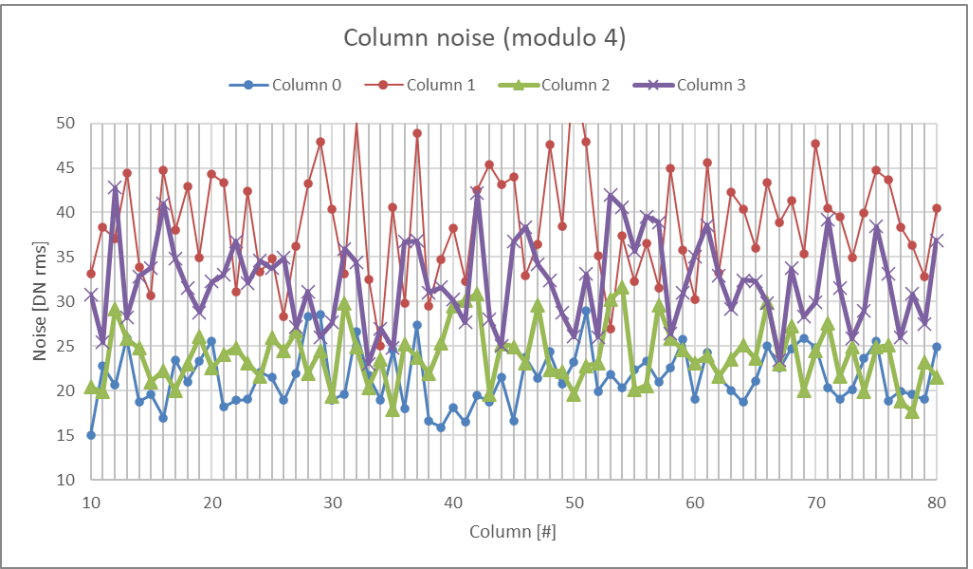


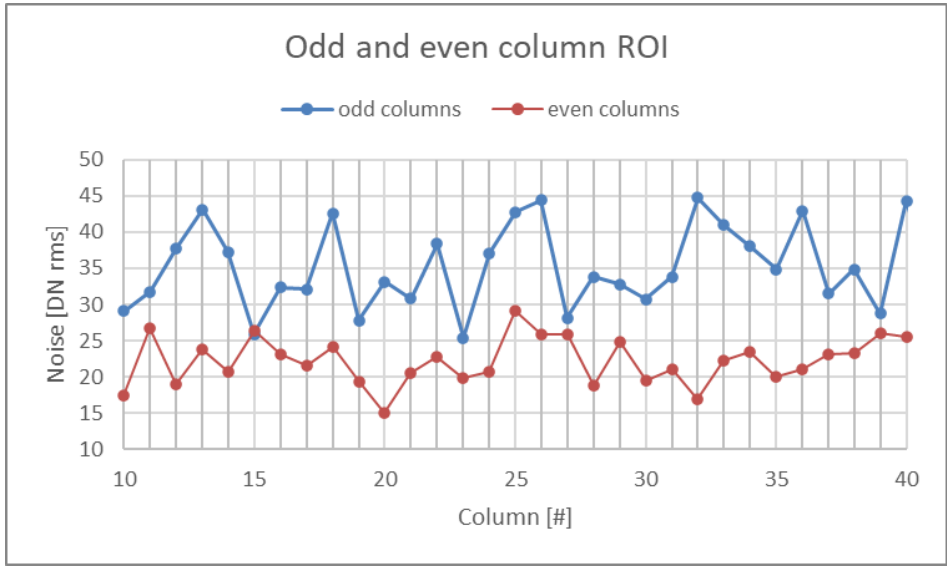
Histogram analysis

- **RWI CDS noise histogram shows two regions for MG & LG**
- **MG noise is further analyzed**
  - Dominant source is videobus in analog chain



The odd columns are showing consistently higher noise.
1 of the 4 channels shows highest noise.





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Quantum efficiency

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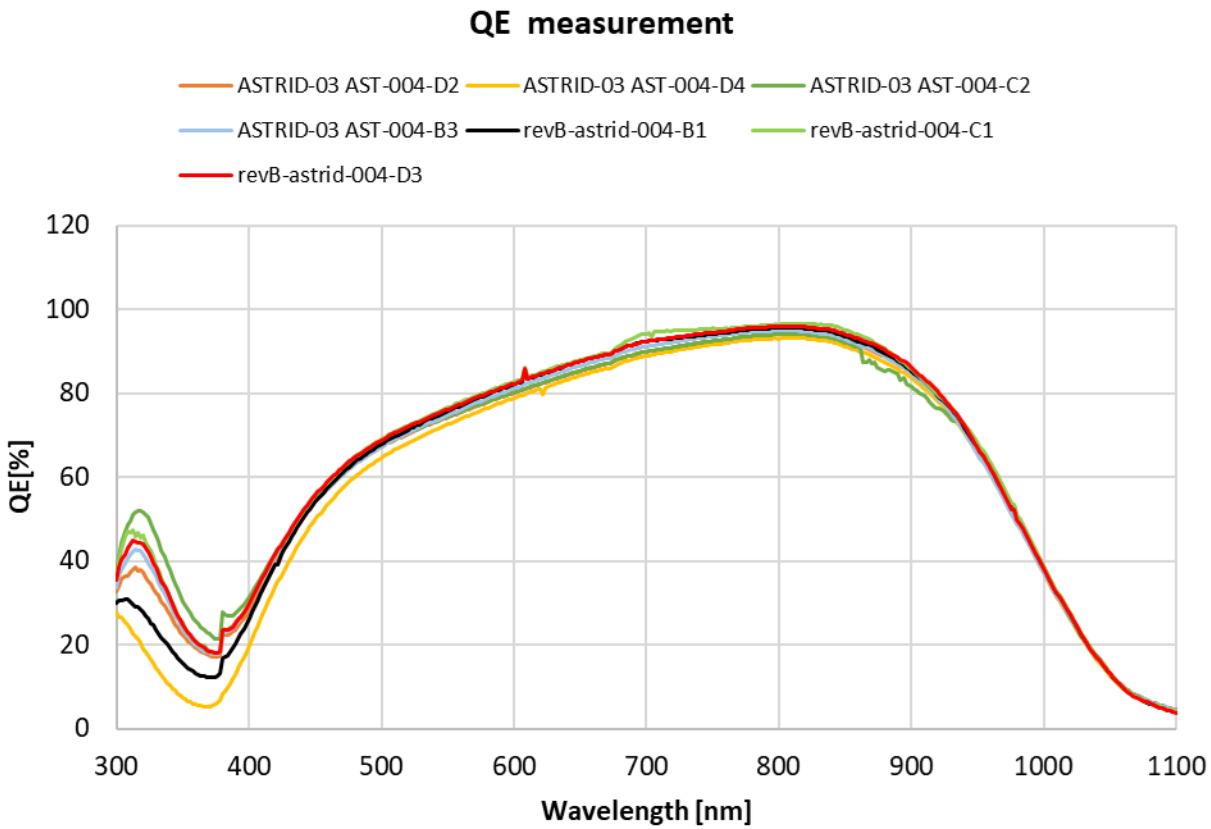
QE: Results, Conclusions

- QE > 75% [570nm – 930nm]
- Peak QE_{810nm} = 95%
- QE_{450nm} = 56%
- QE_{900nm} = 85%



QE shows a strong response in the Near InfraRed (900 nm)
A strong decrease of QE towards the Ultra Violet (450 nm)

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Dark Current

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Dark current: Method, results

- **Read While Integrate (RWI) non-CDS mode**
- **4 different devices**
- **CVF of 32µV/e⁻ to calculate from output signal back to #e⁻ on the FD**
- **The dark current density:**
  - $J_{dark}[pA/cm^2] = \frac{I_{dark}*q}{A} * 10^{20}$
    - I_{dark} the PPD dark current [e⁻/s]
    - q: charge of an electron ($1.602e^{-19}$C)
    - A: pixel area in µm²

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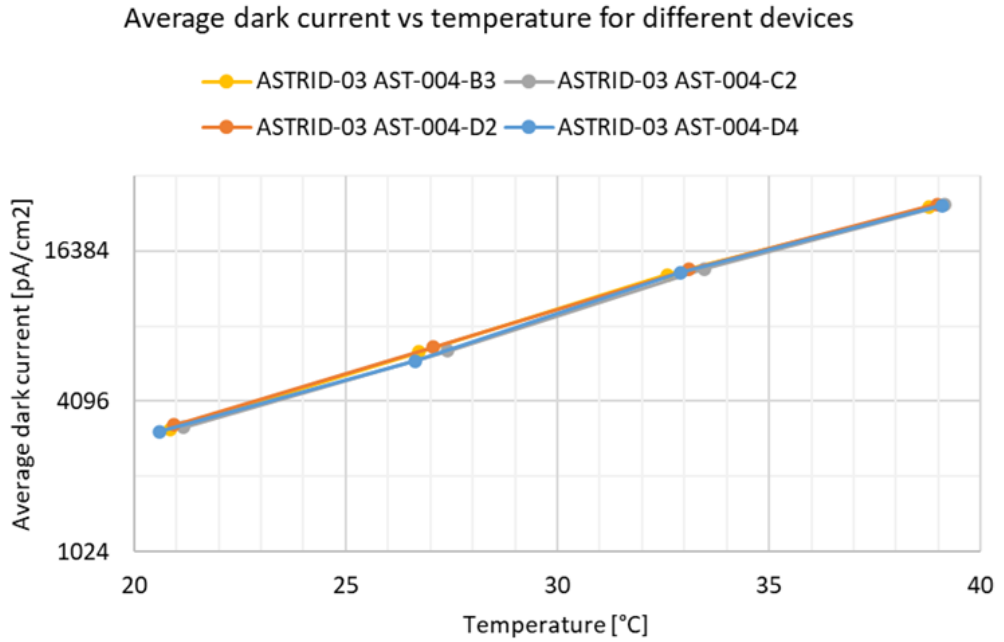
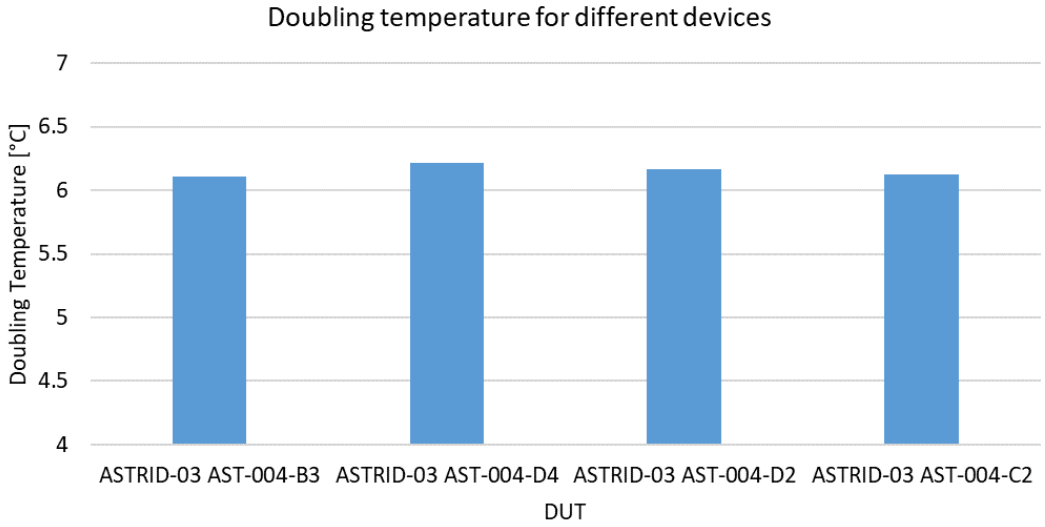
Dark current: Conclusions

- At 21° a high dark current of 3110 pA/cm²
- All devices show a doubling temperature of about 6.1°C

Dark current is far out of specification (800pA/cm²)
Doubling temperature shows the expected ~6°C of silicon





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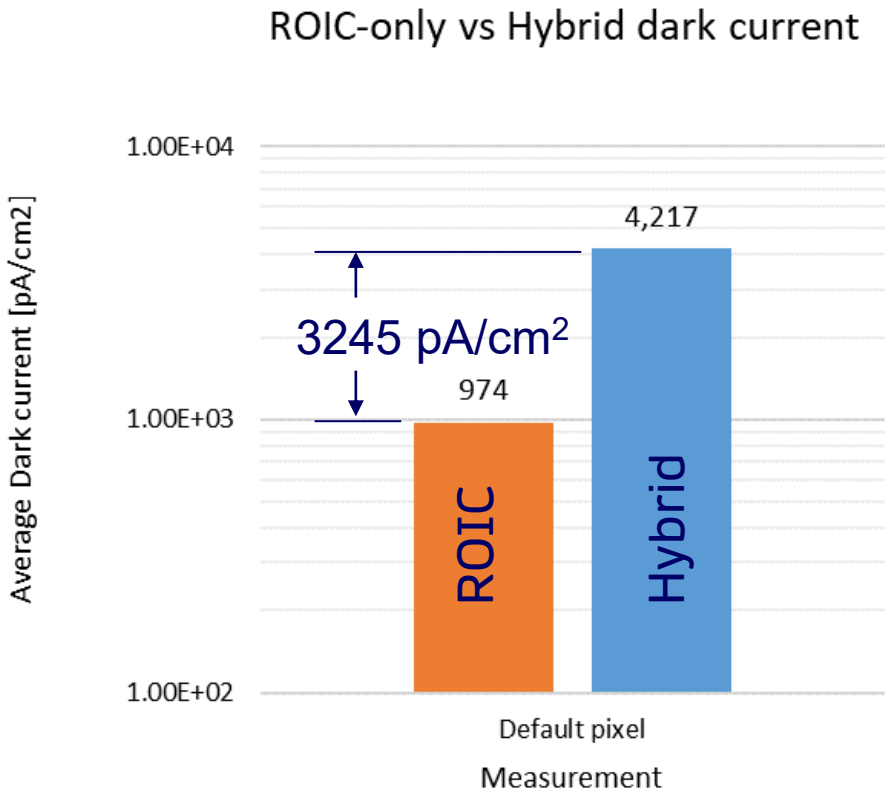
Dark current (I_{dark}) dominant source is the detector

- **Dark current at room temperature**
  - Detector produces >80% I_{dark}
  - ROIC Major contributor is HDR circuit ~940pA/cm²
    - Leak of the HDR pMOS bulk responsible



Detector represents largest contributor to dark current
ROIC itself can improve through simplified HDR circuit

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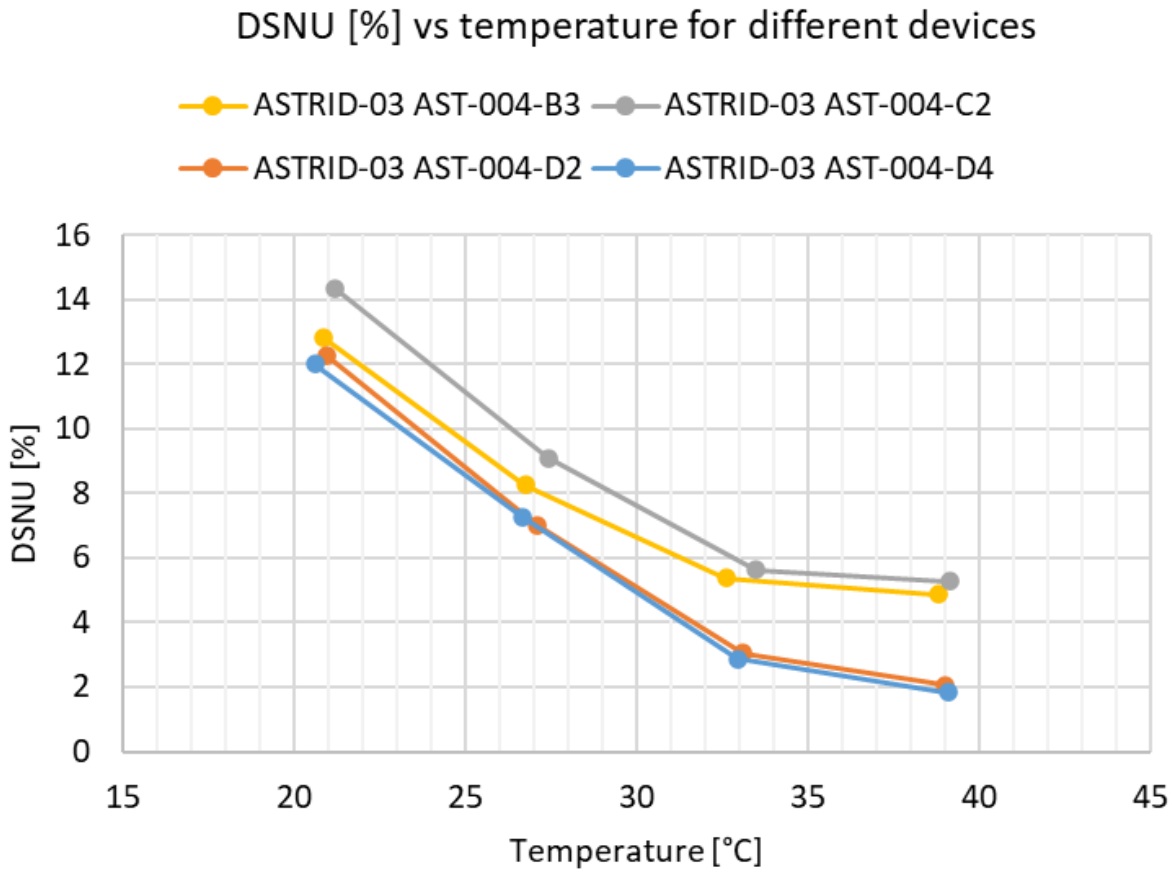
Dark current: Dark Signal Non-Uniformity (DSNU)

- **Two ways to interpret DSNU**
  - [%] of signal level ➔ $0.36\%_{RMS}$
  - [%] of dark signal ➔ 13%
    - This is our standard definition



DSNU is within expectation

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Modulation Transfer Function (MTF) and crosstalk

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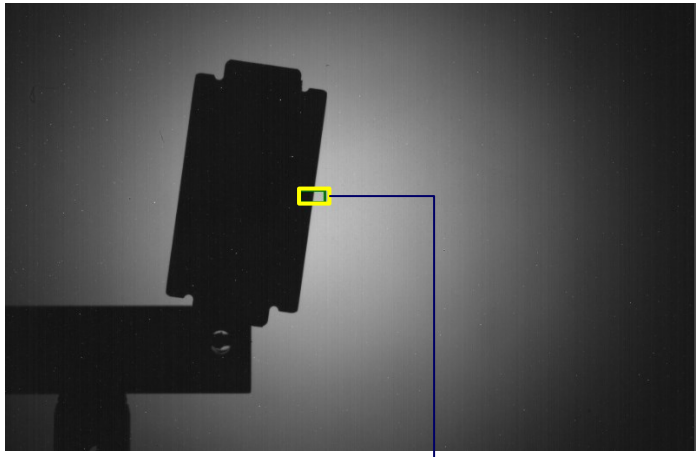
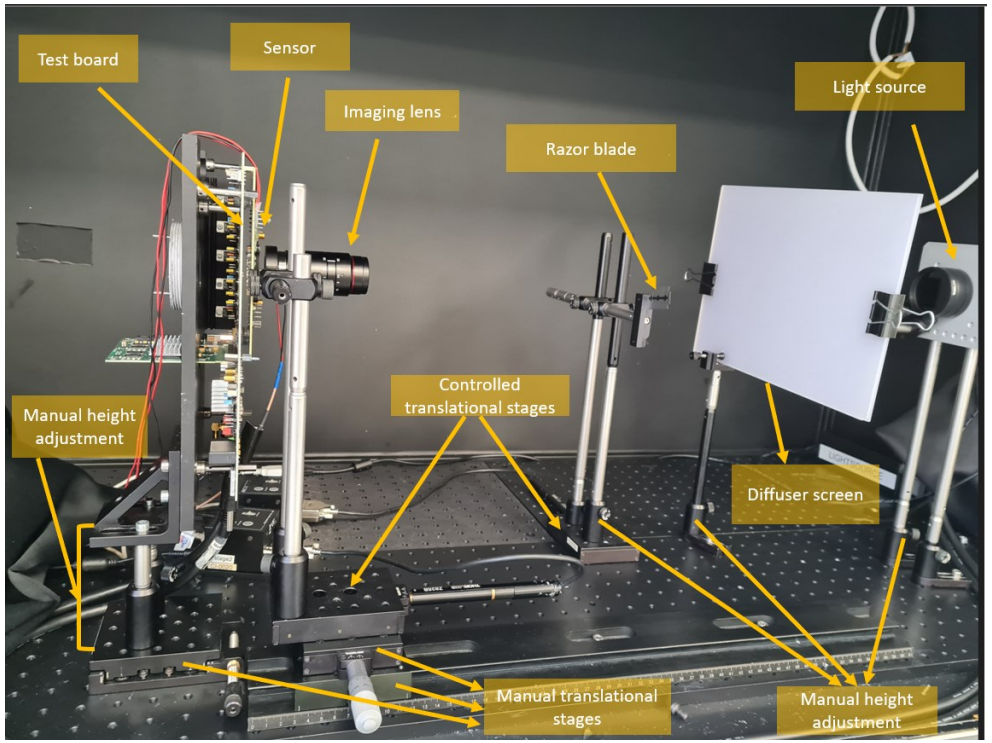
MTF and crosstalk: Test procedure and setup

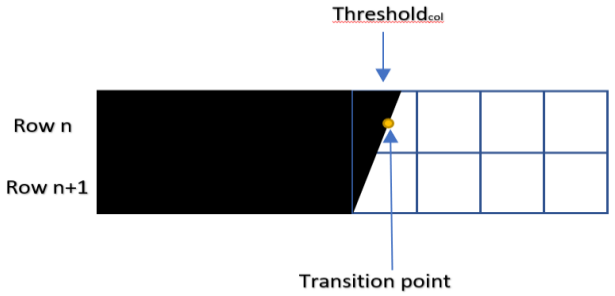
- **Standard measure of image contrast**
- **Based on Slanted Edge Method**





$$Normalized\ image = \frac{edge - dark}{light - dark}$$

$$Col_{intersept} = Threshold_{col} + \frac{(col_0 - 0.5)}{(col_1 - col_0)}$$



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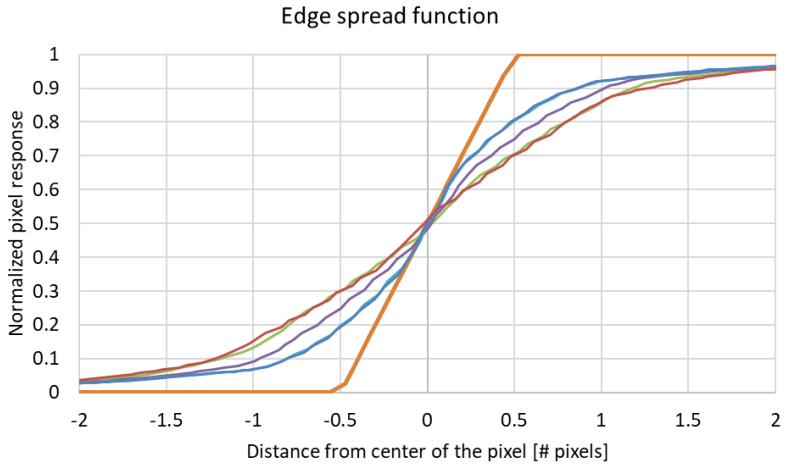
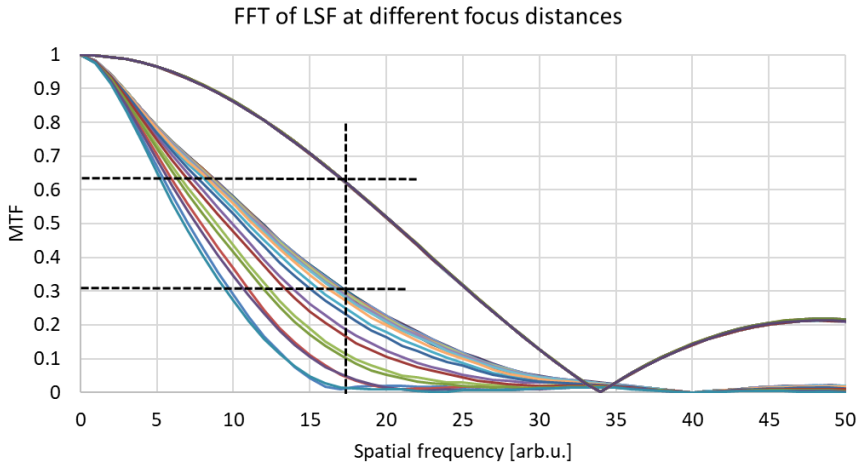
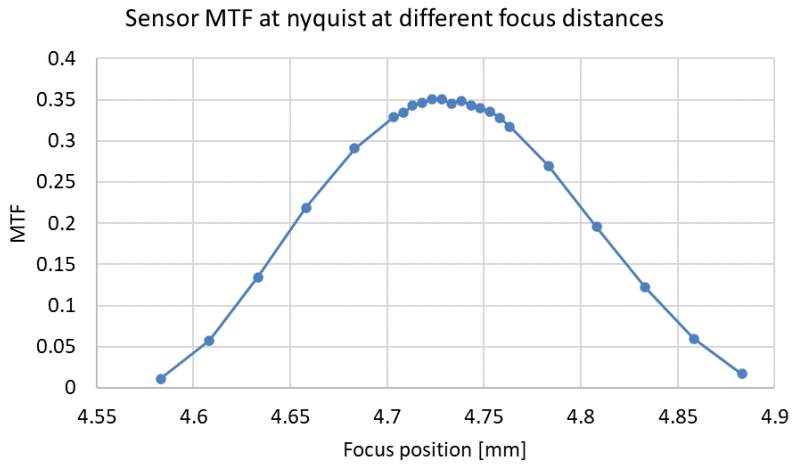
MTF and crosstalk: Test procedure and setup

- Lens at *f#* = 1/2.8 for which calibration data is known, and factored out of calculation
- MTF = 0.35 against a target of 0.55







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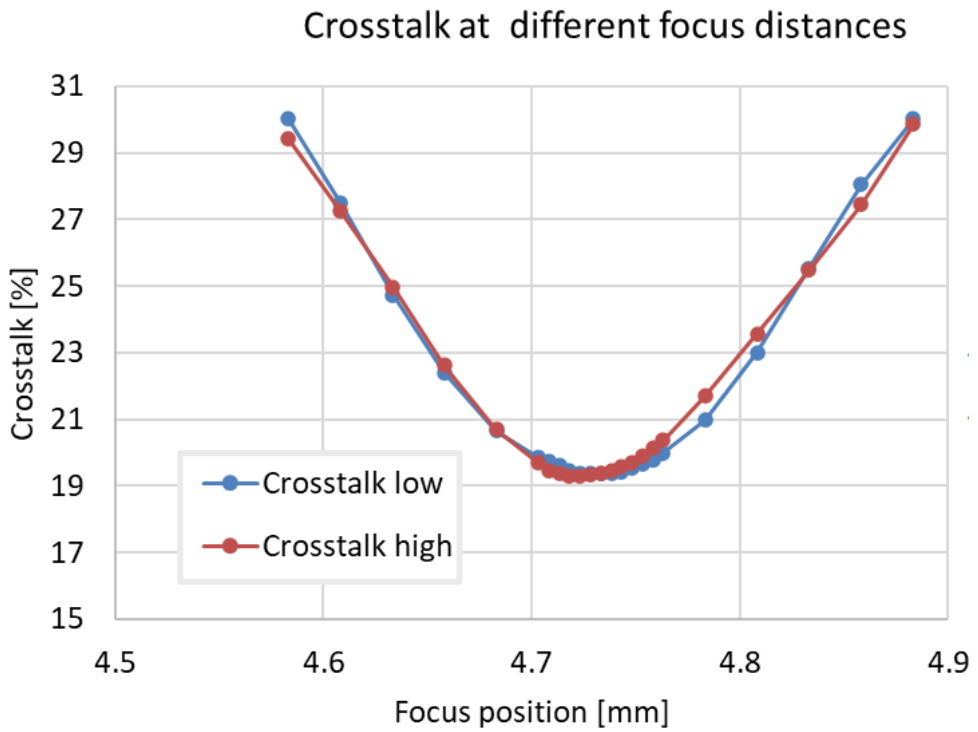
Crosstalk: Results

- **Based on the Edge Spread Function curve**
- **Uses principle that at position -/+0.5, pixel is fully covered by edge**
  - Any deviation from 0/1 is crosstalk



DUT	Cross talk [%]
AST-004-D4	17.6
AST-004-D2	18.9
AST-004-B3	18.0

Worst case crosstalk measurement shows 18% against target of 4%. (lens MTF not subtracted)

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Image Lag

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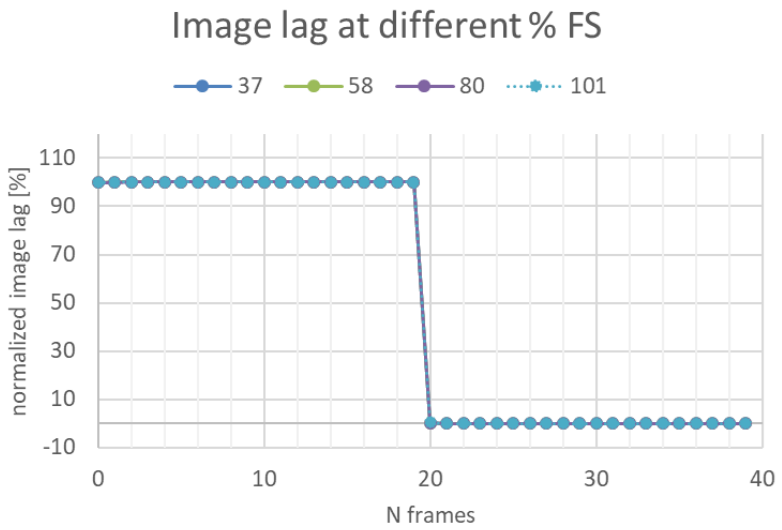
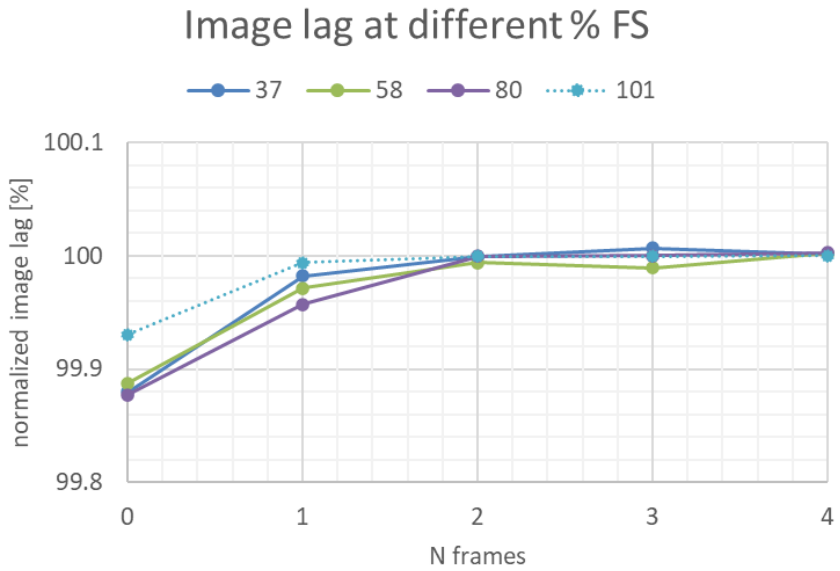
Image Lag: Results

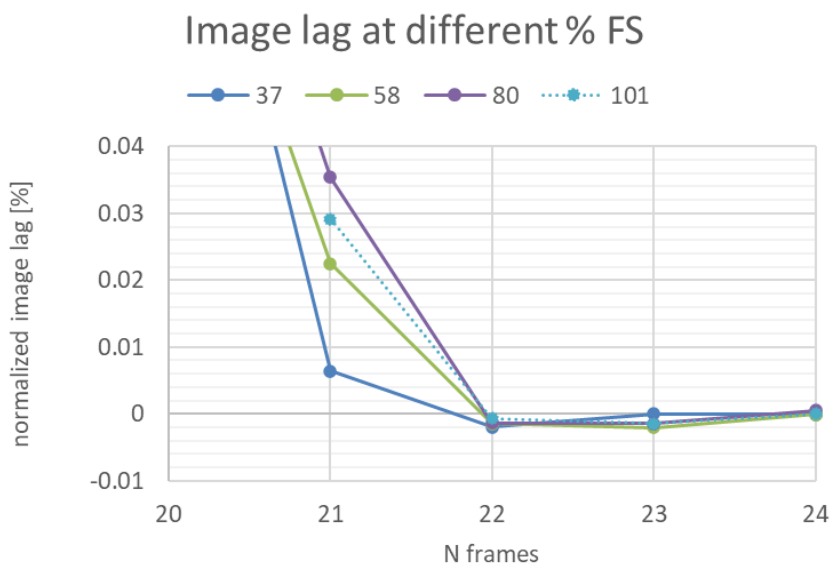
- Expressed as [%] of Full Scale [%FS]
- 50%FS = output half of saturation level
- Measurements shows image lag of 0.1%.



Zoom to dark-to-light part of image lag plot



Zoom to light-to-dark part of image lag plot



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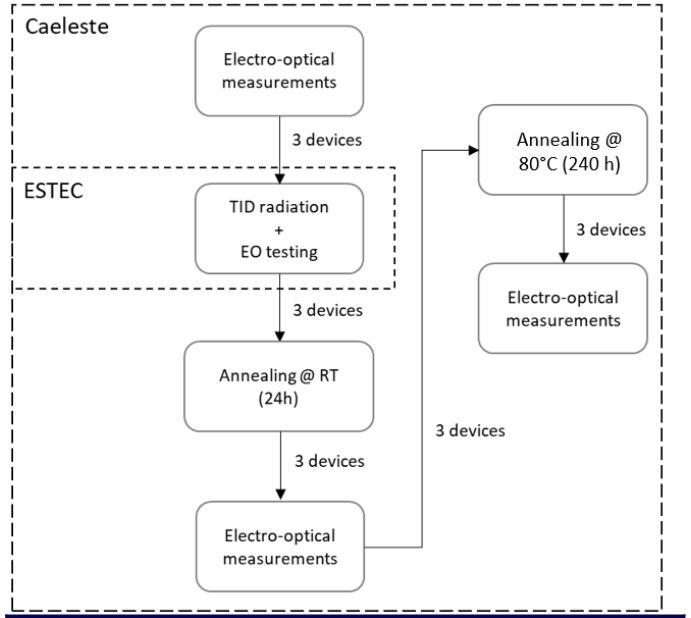
Total Ionizing Dose (TID) radiation

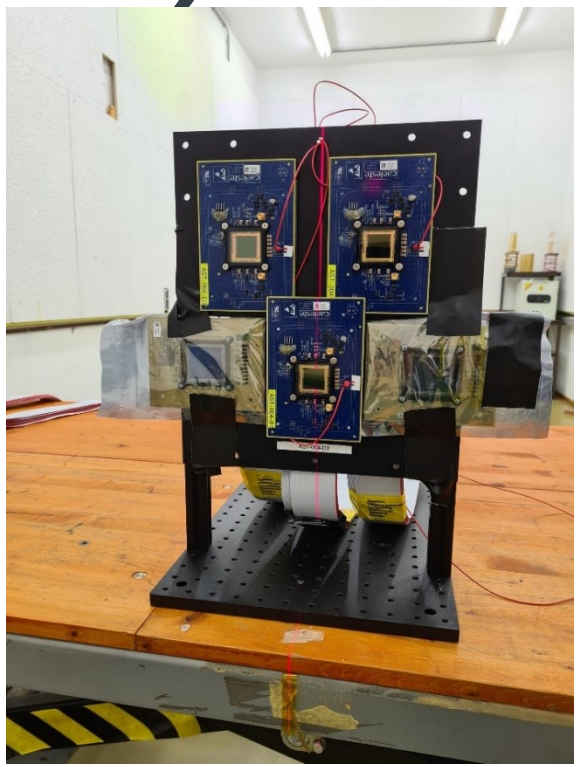
ESA Contract N° 4000130176/20/NL/AR

Total Ionizing Dose (TID) Radiation (ESTEC)

- **ESTEC Co-60 Facility**
- **3 (+ 1 reference) devices**
  - Biased & operated radiation
- **Room temperature**
- **RWI CDS HG**
- **Test executed in portable stand-alone tested**
  - Calibrated light source



No.	Parameter
12	Defects
13	Dark Current
14	DSNU
15	Read noise
20	RTS
16	Charge Handling Capacity
17	Non-linearity
19	PRNU



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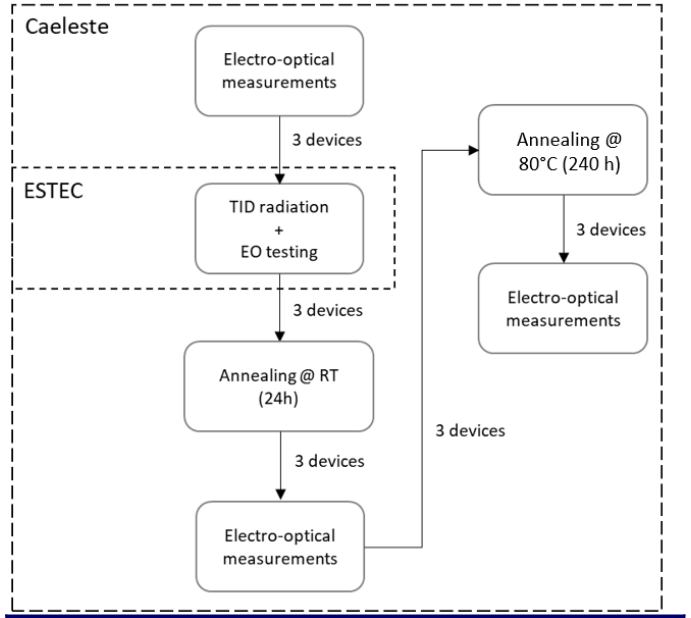
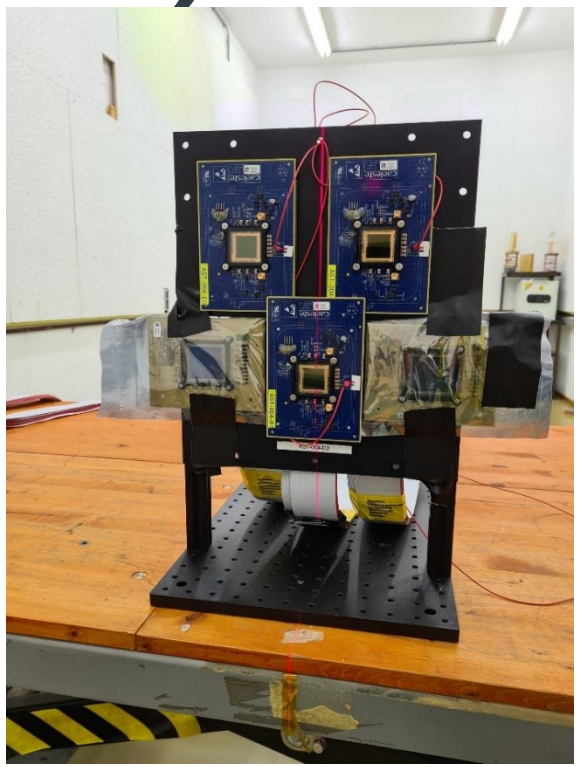
Total Ionizing Dose (TID) Radiation (ESTEC)

- **Dose rate of 1.2 krad/hr**
  - Step 1: 5.5 krad
  - Step 2: 19.1 krad
  - Step 3: 31.0 krad
- **1 device had greater exposure:**
  - Step 4: 55.6 krad



No.	Parameter
12	Defects
13	Dark Current
14	DSNU
15	Read noise
20	RTS
16	Charge Handling Capacity
17	Non-linearity
19	PRNU



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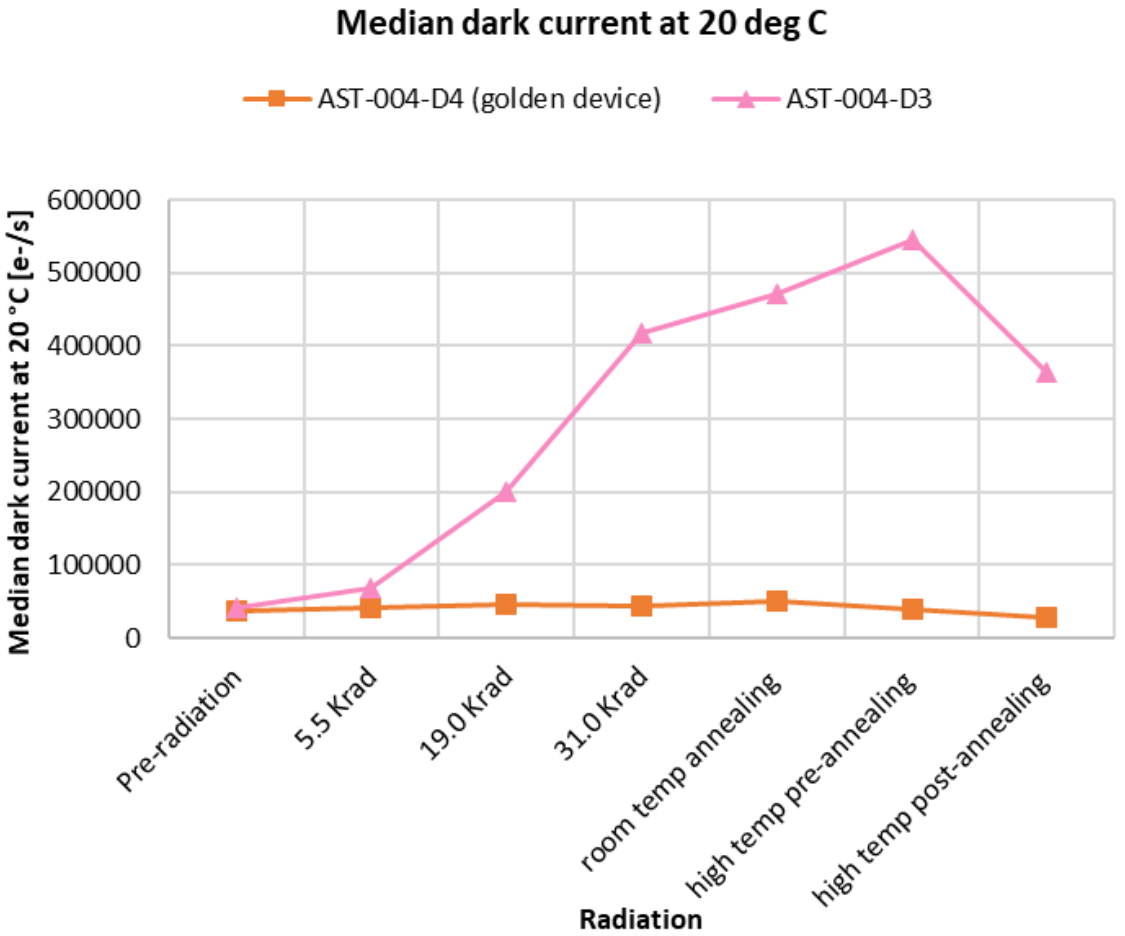
TID - Dark current

- **The expected effect from TID radiation is dark current**
- **Radiation creates defects in silicon**
  - Increasing the dark current generation centers



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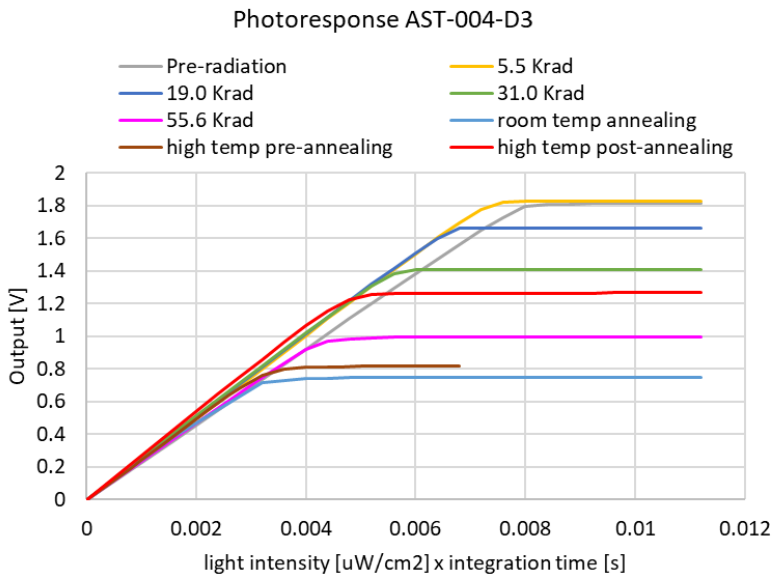
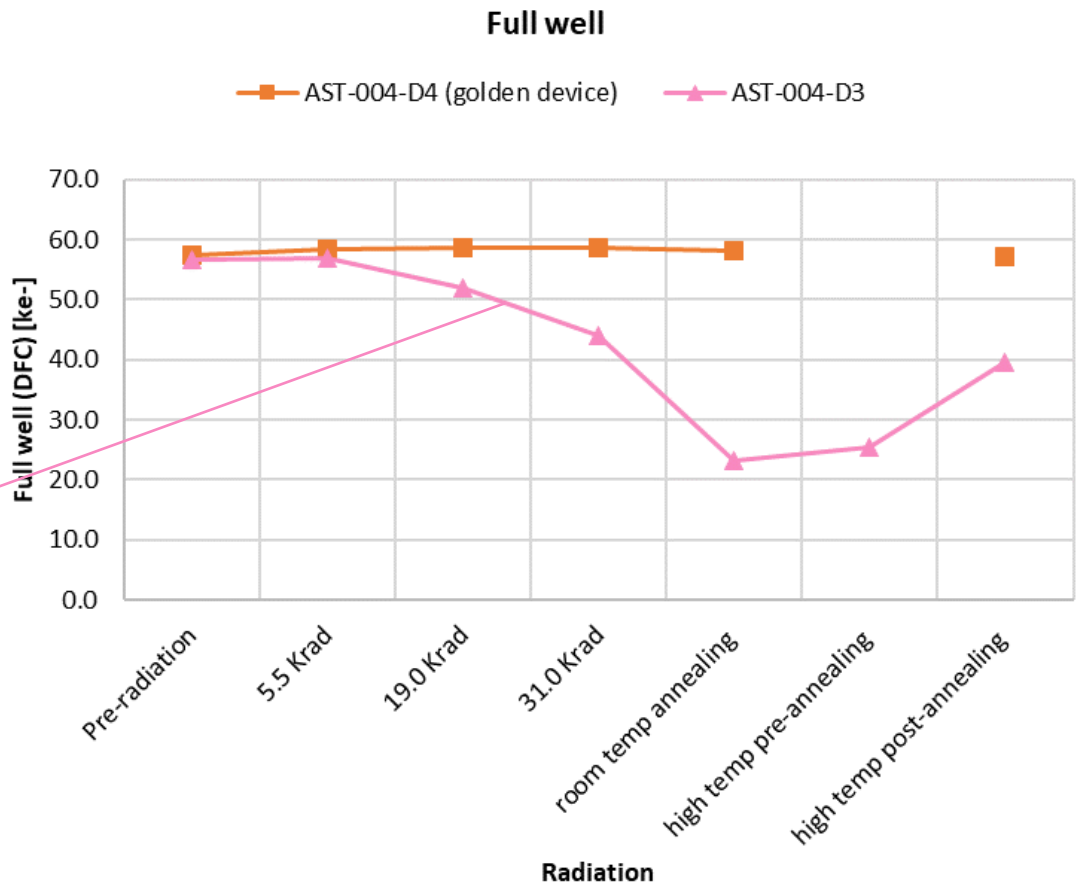
TID - Photo response – Sensitivity & Full Well

- Reference device + radiated device shown
- Pre-radiation had temperature deviation
- Sensitivity is irresponsive to radiation
- Dark Frame Corrected full well reduces due to increase of dark current





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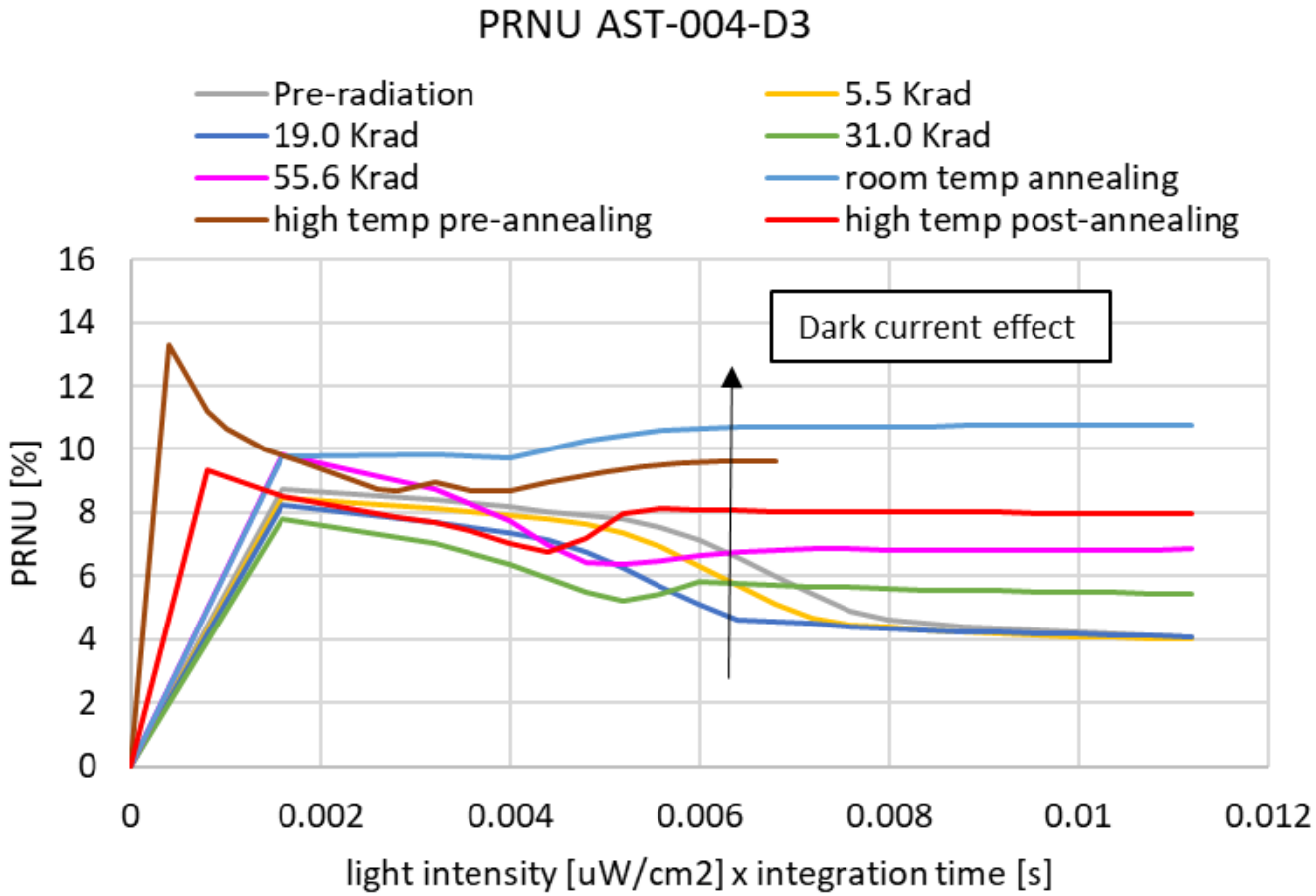
TID - Photo response – PRNU

- **Reference device + radiated device shown**
- **PRNU increases with dark current**
- **PRNU restores with high temperature annealing**



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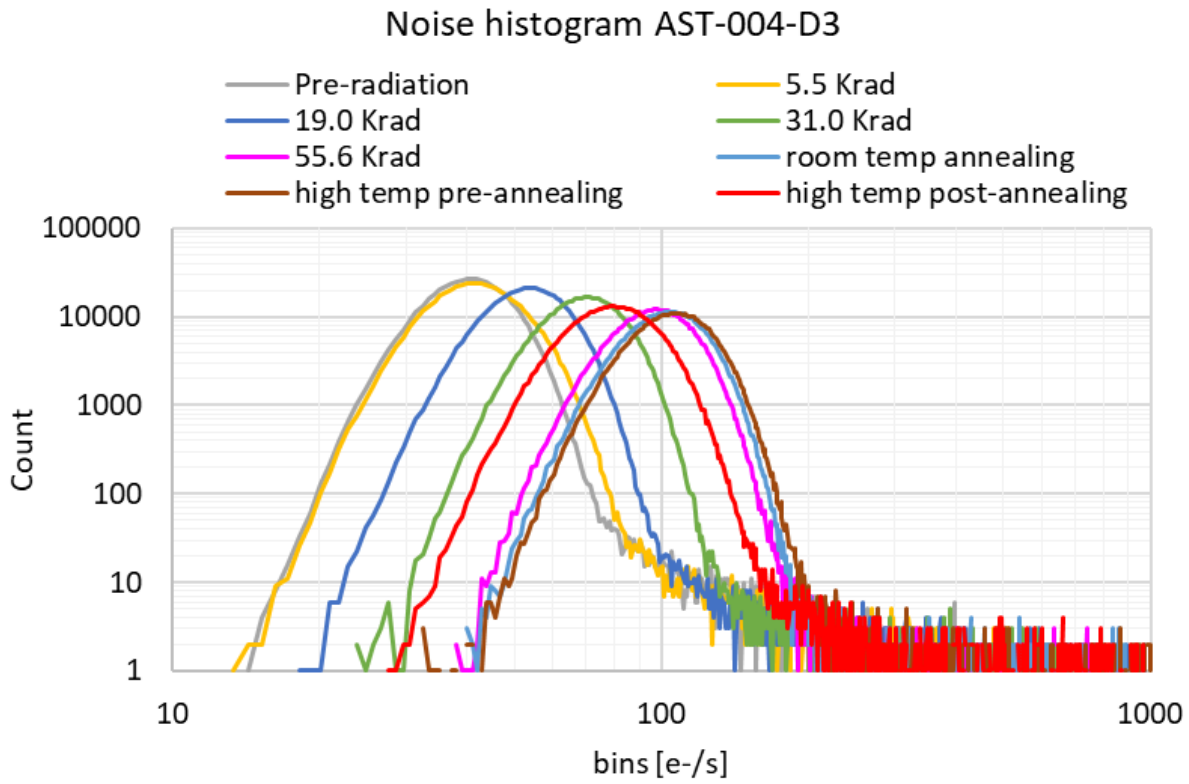
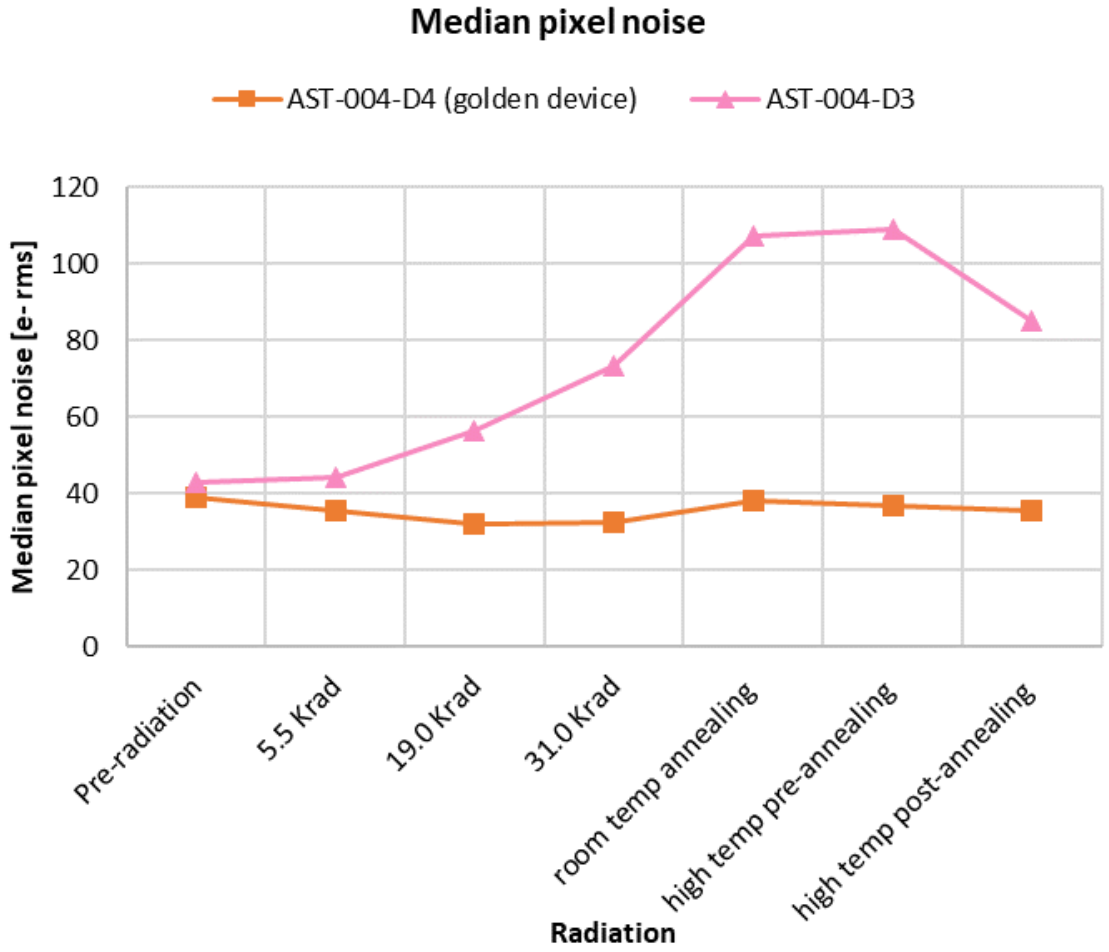
TID - Noise

- **Read noise increases**
  - Dark Current Shot Noise (DCSN) increase





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Proton radiation

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Proton radiation (UC Louvain, BE) - procedure

- **2 (+ 1 reference) devices**
- **Devices left unbiased during radiation**
- **Intermediate test are performed at room temperature**
- **Same set of specifications tested as TID**
- **Total fluence of $1e^{11}$ protons/cm^2**
  - beam energy of 60MeV
  - 6 dosage steps at flux rate of $5e^7$ p/cm^2/s
    - $2.5e^9$p/cm^2
    - $2.5e^9$p/cm^2
    - $2.5e^{10}$p/cm^2
    - $2.5e^{10}$p/cm^2
    - $2.5e^{10}$p/cm^2
    - $2.5e^{10}$p/cm^2

No.	Parameter
12	Defects
13	Dark Current
14	DSNU
15	Read noise
20	RTS
16	Charge Handling Capacity
17	Non-linearity
19	PRNU

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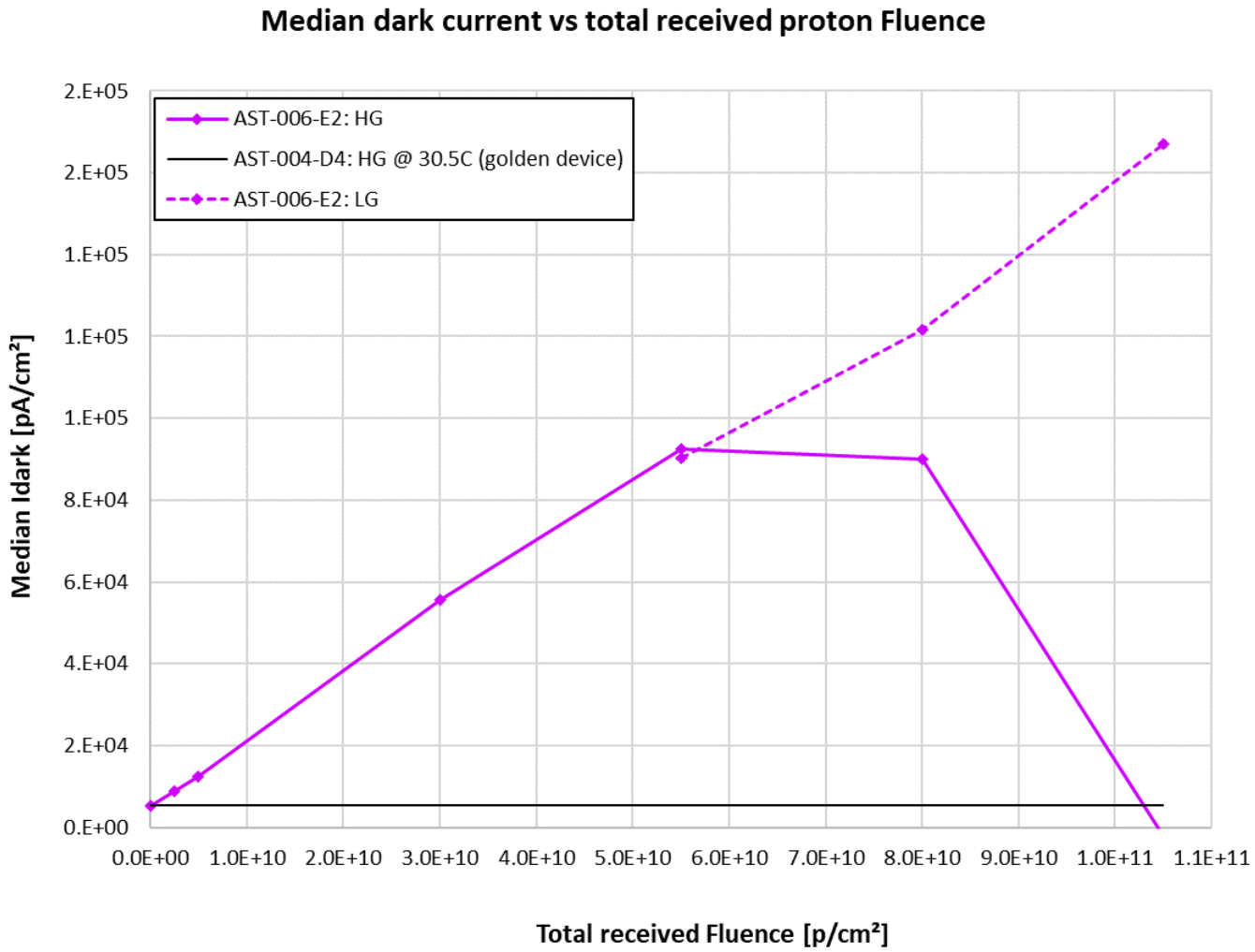
Proton radiation - Dark current

- **Effect of proton radiation is dark current**
- **Radiation creates defects in silicon**
  - Increasing the dark current generation centers
- **From 5.5e^{10}p/cm^2 on**
  - HG measurements saturate
  - LG measurements reported



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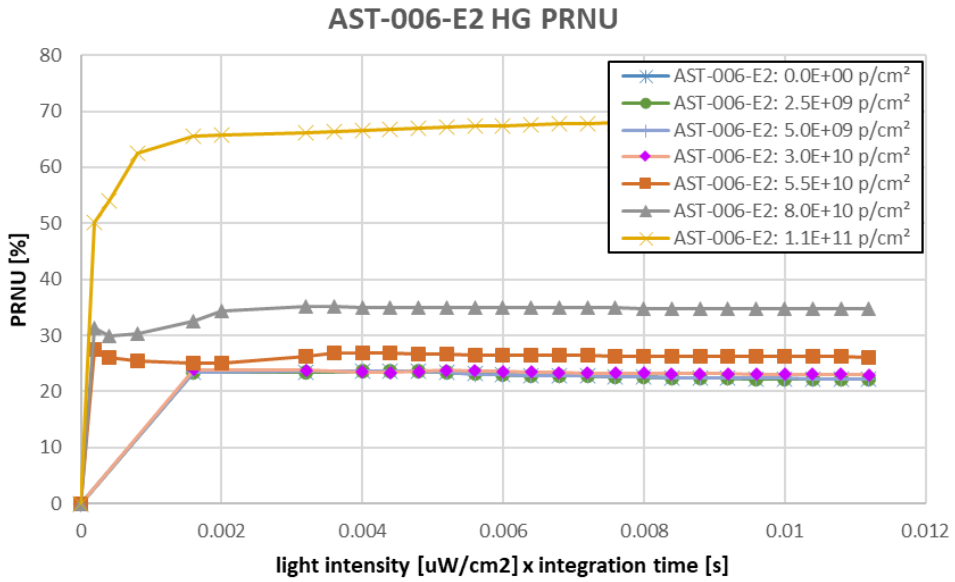
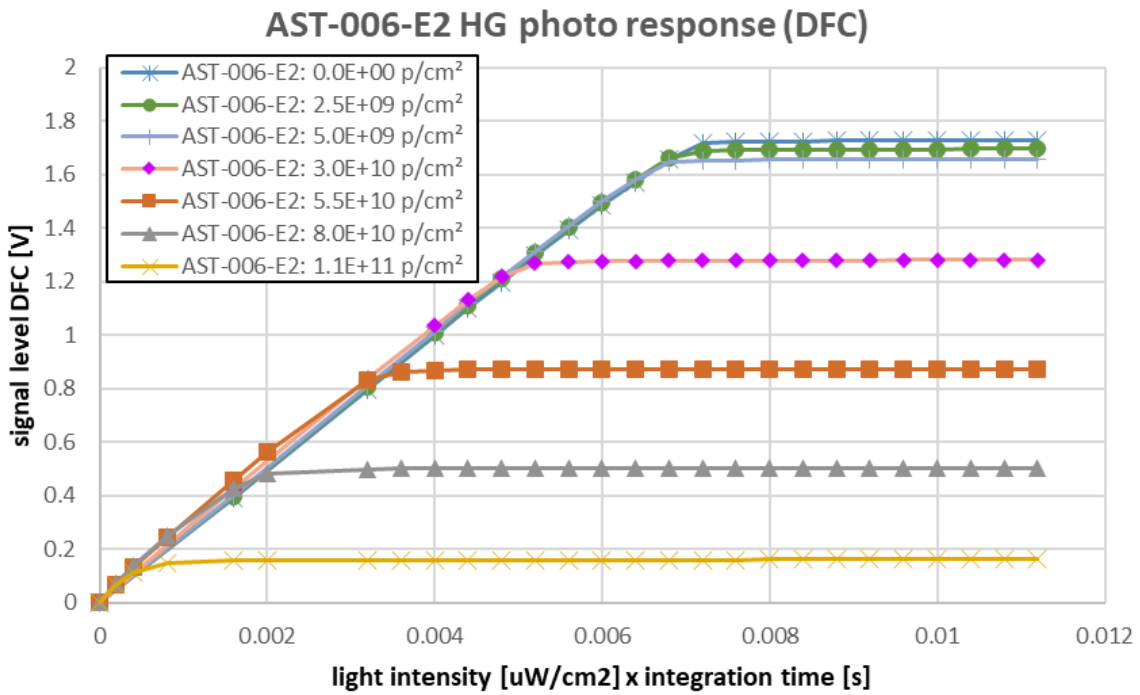
Proton radiation - Photo response

- **Sensitivity invariant to radiation**
- **Dark Frame Corrected full well drops with increased radiation**
- **PRNU increases from 5.5e^{10} p/cm^2 on**





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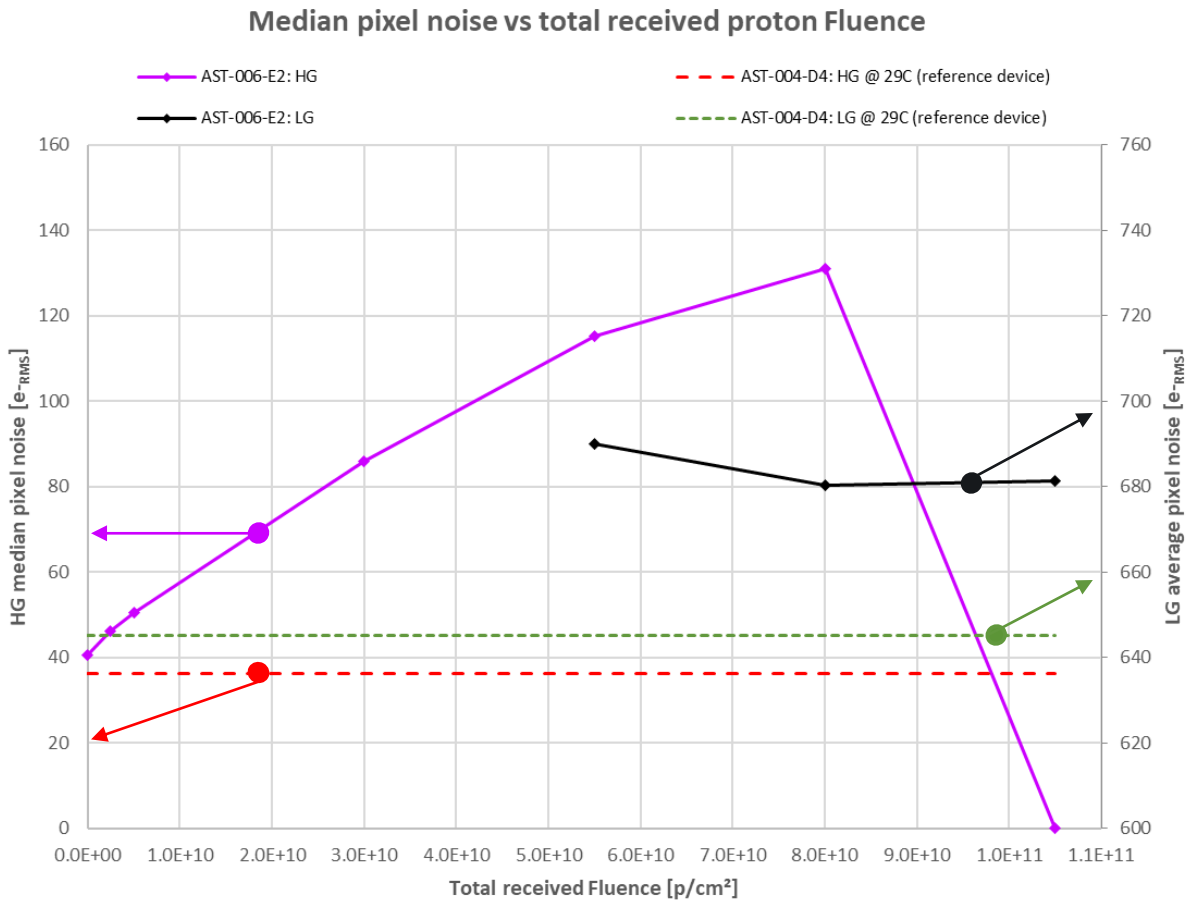
Proton radiation - Noise

- **From 5.5e^{10}p/cm^2 on**
  - HG measurements saturate
  - LG measurements reported
    - Relative invariant to radiation
    - Analog chain is dominating the overall noise



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Specification Compliance Matrix (1/2)

Req. ID	Property	Requirement	Test result	Compliance assessment
5	Read-out mode	Global Shutter	Functional	Compliant
6	Frame Rate	>40Hz	~50Hz	Compliant
7	Integration time	Min: 10µs Max: no limit	Min (poor linearity & gain): 10µs Min (decent linearity & gain): 50µs Max: No limit	Partially compliant
8	Windowing	Required only in Y-directions	Fully programmable y-direction window sizes	Compliant
9	QE x FF	>75% [450-900nm]	>75% [570-930nm]	Partially compliant
10	Crosstalk	<4%	~18%	Not compliant
11	MTF	>0.5 (at Nyquist)	~0.34	Not compliant
12	Defects	<0.01% dead pixels <0.1% bad pixels 0 column defects 0 row defects 0 block defects	0.8% dead pixels 0.1% bad pixels 7 column defects 9 row defects 55 block defects	Not compliant

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Specification Compliance Matrix (2/2)

Req. ID	Property	Requirement	Test result	Compliance statement
13	Dark current	<800pA/cm^2 at 293K	4217pA/cm^2 at 293K	Not compliant
14	DSNU	<5%$_{RMS}$	13%$_{RMS}$	Not compliant
15	Read noise	<10e$^-_{rms}$ <100e$^-_{rms}$	28e$^-_{rms}$ 591e$^-_{rms}$	Not compliant
16	Charge Handling Capability	<100ke$^-_{High\ Gain}$ >1000ke$^-_{Low\ Gain}$	58ke$^-_{High\ Gain}$ 300ke$^-_{Medium\ Gain}$ 1.2Me$^-_{Low\ Gain}$	Compliant
17	Non-linearity	<1%	2% (uncalibrated)	Partially compliant
19	PRNU 6x6 pixels Whole array	 <0.3%$_{RMS}$ <3%$_{RMS}$	 1.6%$_{RMS}$ 1.8%$_{RMS}$	Partially compliant
20	RTS	Not specified.	~0.5%	Compliant
21	PLS	<0.02%	-	Not measured
23	TID	20krad	Radiated	Compliant
24	Proton fluence	1x10^{11} Pr./cm^2 at 60MeV flux 10^7 ions/cm^2 •s	Radiated	Compliant

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Conclusions

- **Established a design methodology for silicon-silicon flip-chip bonded hybrid imagers**
  - Architecture proven, improvements studied and documented
  - Design parameters and trade-offs are known, quantified
  - Models and simulations improved by measured results
  - Stitched design scalable to 4k x 4k pixels
- **Demonstrated, improved manufacture of small-pixel-pitch FCB Hybrid devices**
  - Advanced state of the art for pillar interconnect processing
  - Cu/Ni pillars of 12.5µm height with InSn solder cap, resulting in uniform height, composition
  - Improved manufacturing yield, reduces risk of solder bridges between pixels (compared to In bumps)
  - Improved methodology for new hybrid module designs
- **Produced high-quality Hybrid modules featuring:**
  - Small pixels (20 µm)
  - Fast frame rates up to 50 Hz
  - Global shutter readout
  - Programmable integration time
  - Programmable region of interest
  - High QE at Near Infrared spectrum (900nm and above)

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Future work for this design could include

- **ROIC**
  - Deeper analysis of video channel noise
- **Detector**
  - Investigate different silicon processing
  - examine other ARCs
  - Goal: Improve QE at UV, I_{dark}, MTF
- **Hybrid and manufacture**
  - Various design changes (Detector and ROIC) to improve mechanical strength, electrical connectivity
  - Process refinements for small-pixel devices

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Acknowledgements

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