

Development of an automatic failure analysis tool for space applications: SFailSIM

Abstract—A new idea to be developed by Power Smart Control S.L. (PSC) in collaboration with the European Space Agency (ESA) is to create a software tool (SFailSIM) for executing and optimizing FMECA (Failure Modes Effects and Criticality Analysis), which is a standard methodology in the field of reliability and failure analysis. The company acknowledges the possibility of improving and simplifying tasks associated with FMEA (Failure Modes Effects Analysis) / FMECA (evolution of FMEA, including Criticality Analysis). Although there have been efforts and different companies are exploring the automation of FMEA/FMECA standard outcomes, their results do not explicitly focus on calculating an accurate FMEA/FMECA for electronic systems, and, therefore, PSC has identified the need for improving the robustness, accuracy and reliability of failure analysis, mainly in the aerospace sector.

In this project, PSC has clarified some critical technical and economic issues associated with the potential development of the software tool, which will guide follow-on activities. In addition, as part of this project, PSC has developed a first prototype version of SFailSIM.

Keywords—FMEA, FMECA, simulation, automation.

I. INTRODUCTION

This project (Development of an automatic failure analysis tool for space applications: SFailSIM) aims to be an initial step for evaluating the feasibility and specifications of a future software tool, SFailSIM, focused on improving in terms of accuracy and efficiency the failure analysis process applied to complex electronic systems on space applications, which is currently covered by analysis methodologies such as FMEA/FMECA (Failure Modes Effects and Criticality Analysis). SFailSIM will improve the quality and feasibility of existing FMECA analysis.

During the project, relevant proofs of concept and identification of critical technical and economic issues associated with the potential development of the tool have been carried out, in order to guide the potential creation of SFailSIM.

The following figure summarizes the baseline engineering approach for the future SFailSIM.

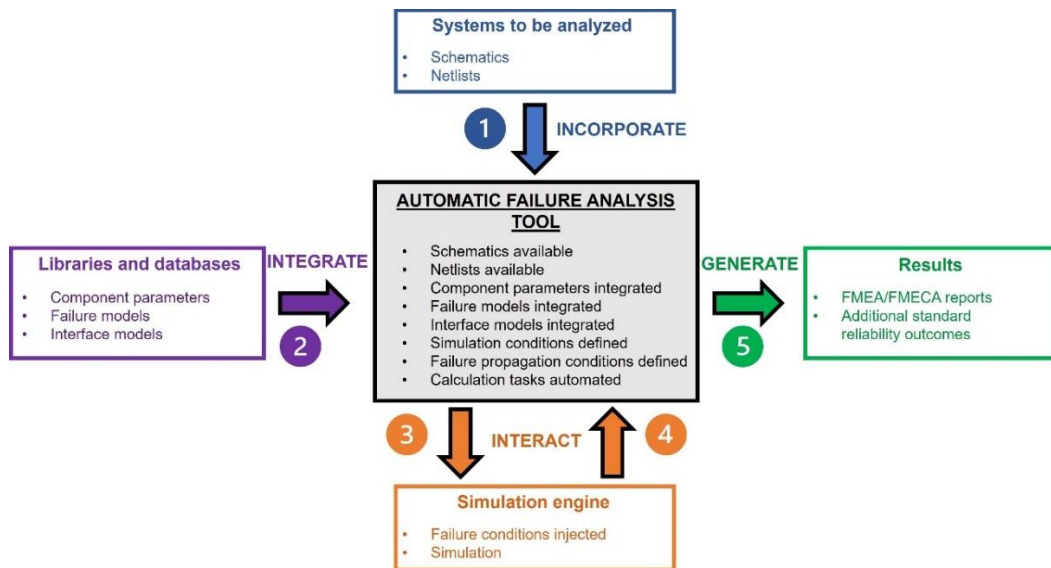


Figure 1: Baseline engineering approach for SFailSIM

It can be observed the overview of the workflow between the different main blocks that will make up the future product SFailSIM. All of them have been preliminary tested and researched from the technical point of view during this project by means of different approaches, tests, and software tools. A prototype version of SFailSIM has been generated as a key output of the project, as well as an study of the development schedule and economic viability.

Section II includes a general overview of the previous research and references in FMEA/FMECA. **Section III** briefly describes the main issues related to the methodology nowadays. **Section IV** shows the fundamentals of the economic viability study, as well as the highlights of the prototype version of SFailSIM generated during the project. **Section V** collects the most relevant conclusions extracted from the developed work. **Section VI** shows the identified future works for SFailSIM.

II. PREVIOUS RESEARCH AND REFERENCES

FMEA/FMECA is a required task for reliability, and the technology developers need to implement it in their roadmaps. However, this is a complex and time-consuming task, especially in the case of systems containing a large number of components, whereby several simplifications have to be assumed, and the quality of the results is drastically affected due to subjectivity and lack of depth of the analysis.

In recent years, several efforts have been carried out to develop processes and strategies for improving and simplifying tasks associated with FMEA/FMECA. Moreover, new software tools have emerged, looking for the automation of FMECA/FMECA standard outcomes (reports, templates, etc.) and integrating additional reliability analyses (Markov Analysis, Fault Tree Analysis, Reliability Block Diagrams, etc.). However, the application of these tools is not explicitly focused on calculating an accurate FMEA/FMECA for electronic

systems. Thus, improving the robustness and reliability of the results is still considered an issue to be solved.

Some reference standards in failure analysis for the target applications of SFailSIM are:

- ECSS-Q-ST-30-02C [ECSS - Q - ST - 30 - 02 Working Group, ECSS-Q-ST-30-02C - Failure modes, effects (and criticality) analysis (FMEA/FMECA), Noordwijk, 2009.]
- MIL-STD-1629A [Department of defense USA, Procedures for performing a failure mode, effects and criticality analysis - MIL-STD-1629A, Washington DC, 1980.]
- MIL-HDBK-217F [Department of Defense USA, «MIL-HDBK-217F,» Washington, D.C., 1991.]

III. PROBLEM FORMULATION

The future software SFailSIM will be focused on dealing with current problems identified in state of the art of failure analysis (specifically of FMEA/FMECA), mainly from the point of view of applicability, identification of causes and effects, risk analysis, and problem solving [C. Spreafico, D. Russo y C. Rizzi, «A state-of-the-art review of FMEA/FMECA including patents,» Computer Science Review, vol. 25, pp. 19-28, 2017] .

A. Applicability

- Lack of automation and a significant amount of time and human resources spent on complete the analysis.
- Difficulty in partitioning systems containing a high number of components accurately and in a standard way.
- Subjectivity due to different degrees of knowledge and approach of the analysts.
- Difficulty in integrating FMECA with other processes and tools.
- Difficulty in executing FMECA in the design phase, where it would be really effective.

B. Identification of causes and effects

- Difficulty in modelling specific failure modes and determining their causes and effects.
- Lack of integration with commercial simulation tools to obtain quantitative and robust results.

C. Risk analysis

- Difficulty in associating failure modes with specific risks.
- Lack of consistency due to ambiguity and subjectivity.

D. Problem solving

- Lack of reliability and standardization in quantifying the results.
- Difficulties in problem definition, methodology application, and feasibility of the proposed solutions.

IV. METHODS AND RESULTS

In this project, a global study of the technical and economic viability of SFailSIM has been carried out in order to improve the ability to evaluate and decide between the alternatives and reduce the critical uncertainties associated with the feasibility of developing the final product.

Regarding the study of economic viability, it has provided relevant information and conclusions about the development schedule and the associated costs of the future software SFailSIM, as well as the conditions/restrictions/risks regarding the economic feasibility of the final product, and the assessment of critical aspects to enhance its chances of success as a real product in the market. It has been focused on:

- SWOT analysis (Strengths, Weaknesses, Opportunities, Threats) and differentiation strategy.
- Competition Analysis and determination of the potential market.
- Resource planning and project costs.
- Analysis and selection of the business model.
- Identification and evaluation of financing strategies.
- Demand forecasting.

Regarding the study of technical specifications and development, this project has been an early proof of concept to research and test the key aspects of the implementation approach for the final software. A software structure for a prototype version of SFailSIM (based on PYTHON scripts and LTSPICE simulation) has been proposed to set an initial reference for the final product development and allow early test/experiments for identifying critical aspects regarding, among others, accuracy and time of automatic failure simulations.

The general workflow of the prototype version of SFailSIM has been the following:

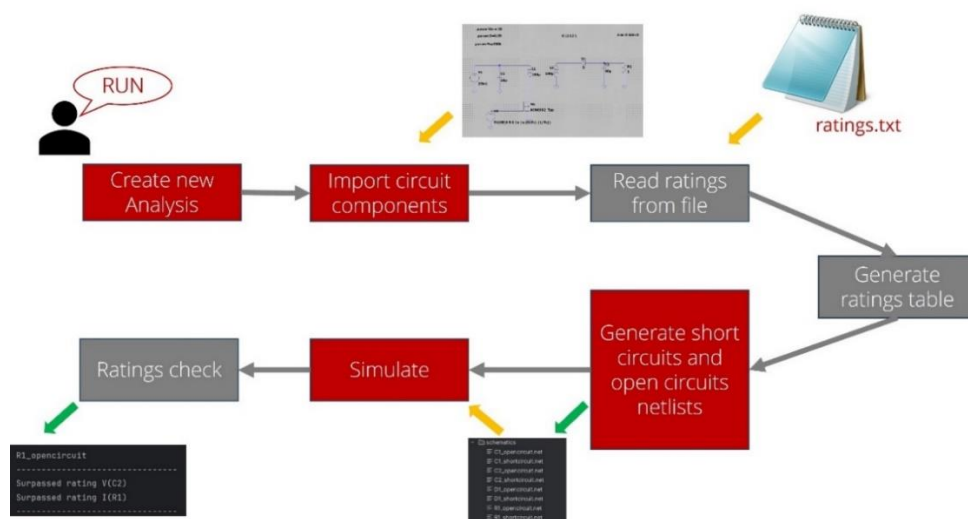


Figure 2 Flowchart for the proof of concept of SFailSIM (PYTHON script)

In this project, the main failure modes (Short-Circuits and Open-Circuits) of an interesting group of components (two-terminal components, transistors, transformers, and integrated circuits) have been modelled to be injected in LTSPICE by means of the modification of the original netlist of the circuit (as a text format file).

Example of short circuits injection on a component with three terminals: MOSFET

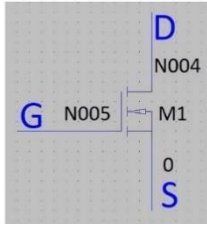
Nominal schematic	Netlist description												
	<table border="1"> <tr> <td>M1</td> <td>N004</td> <td>N005</td> <td>0</td> <td>0</td> <td>AON6992_Top</td> </tr> <tr> <td>Designator</td> <td>Drain</td> <td>Gate</td> <td>Source</td> <td>Substrate</td> <td>Model</td> </tr> </table> <p>The source and the substrate are connected internally even if the symbol only has three terminals.</p>	M1	N004	N005	0	0	AON6992_Top	Designator	Drain	Gate	Source	Substrate	Model
M1	N004	N005	0	0	AON6992_Top								
Designator	Drain	Gate	Source	Substrate	Model								

Table 1 MOSFET Netlist in LTSPICE (nominal conditions)

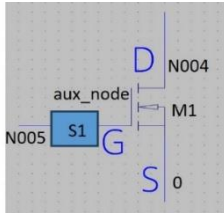
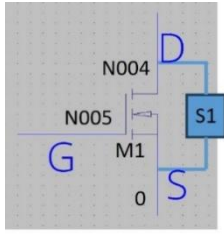
Failure schematic	Failure mode	Netlist description *S1: Failure Injection Structure
	Open-Circuit (Gate)	<pre>M1 N004 aux_node 0 0 AON6992_Top S1 aux_node N005 SW+ 0 SW</pre>
	Short-Circuit (Drain-Source)	<pre>M1 N004 N005 0 0 AON6992_Top S1 N004 0 SW+ 0 SW</pre>

Table 2 MOSFET Netlists in LTSPICE (failure modes injected)

In addition, as a proof of concept using the prototype version of SFailSIM, an automatic failure analysis has been carried out in a flyback converter designed with space specifications. The complete automatic failure analysis and reporting of fifty failure modes took around one hour, and a double-check of the results obtained with LTSPICE has been developed against PSIM (another reference tool for simulation).



Figure 3: SFailSIM prototype version: initial menu

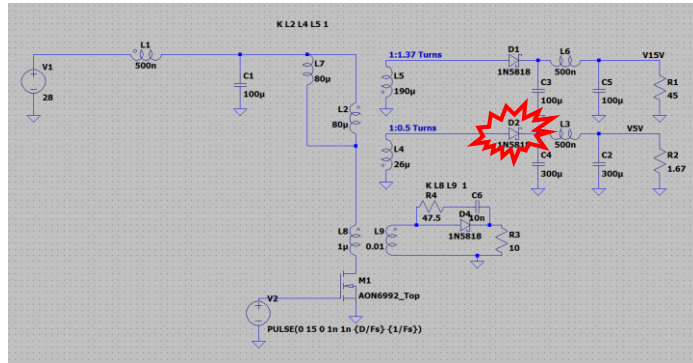


Figure 4: D2 Open-Circuit failure mode overview

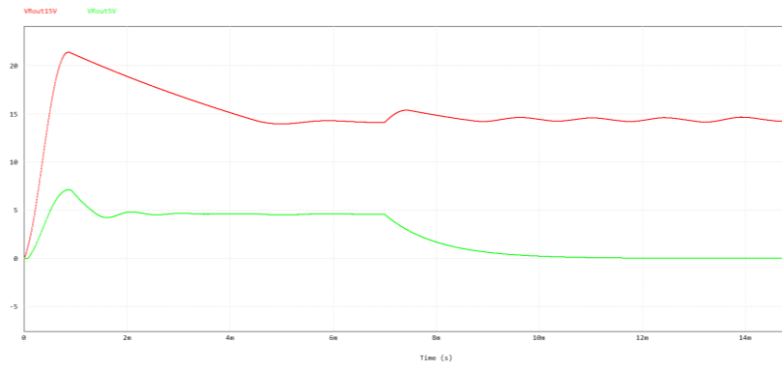


Figure 5: D2 Open-Circuit failure mode simulated in PSIM (outputs 15VDC and 5VDC, open loop)

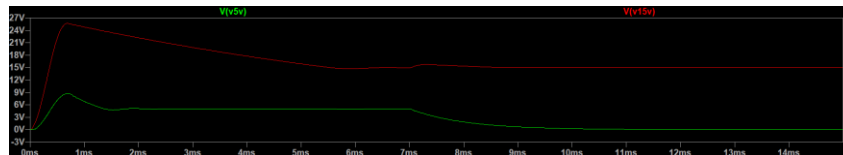


Figure 6: D2 Open-Circuit failure mode simulated in LTSPICE (outputs 15VDC and 5VDC, open loop)

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Experiment: C1_shortcircuit
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Surpassed ratings: 1
I (L1)
Time:0.004030137618090404
Max value: 2546.167
Rating: 3.0
    
```

Figure 7: SFailSIM prototype version: .txt results

Finally, it should be highlighted that this project has covered additional studies regarding failure analysis and future enhancements of SFailSIM, mainly associated with system partitioning, system redesign, identification of steady-state, simulation engines, and time steps

V. CONCLUSIONS

Regarding the development schedule and economic viability:

- 1) *SFailSIM appears to address a pressing and relevant business need, potentially providing significant value added above existing solutions.*
- 2) *Given the proposed risk management plan is properly implemented, no insurmountable risks or hurdles have been identified.*
- 3) *Nevertheless, barriers to entry, change resistance and a somehow limited reachable market lead to an uncertain financial attractiveness/viability for SFailSIM's development project, highly dependent on ESA's support or assistance in various facets, as detailed in the following considerations.*
- 4) *It is critical for the project's financial viability that PSC succeeds in securing further financial support, i.e. through Compendium in the short term and then through successive MAKE programs supporting development until final product's TRL is reached.*
- 5) *Given the results of the preliminary viability analysis and target prices, it is key to verify whether the threshold of a stable customer base of 50-75 license-paying customers (not 50-75 licenses) can be reached, and how.*
- 6) *ESA's level of support/prescription of the tool, upon its validation, will critically influence the viability of successfully surmounting the Aerospace sector's high entry barriers.*

Regarding the technical development and proof of concept with SFailSIM prototype:

- 1) *Component data and information sources for failure analysis (such as failure modes parameters and voltage/current/power ratings) have been collected.*
- 2) *Different workflows for automating failure analysis have been explored using PSIM and LTSPICE as reference simulation tools. In this proof of concept, the connection between PYTHON and LTSPICE using scripts has been selected for the prototype version of SFailSIM due to the high capabilities and advantages identified for automating failure analysis with minimum user intervention and input data by means of netlists (only original schematics/netlists are required for their subsequent, systematic, and automatic modification for injecting failure modes in all components).*
- 3) *A relevant group of components and failure modes have been considered in the scope of this project. The failure modes of all components, mainly associated with open circuits and short circuits, have been generated by modifying their associated netlist in LTSPICE and replacing components by failure injection structures. The proposed strategies for failure modes injection*

have been approached since the beginning to be easily extended in future works to other components and failure modes.

4) A prototype version of SFailSIM has been coded in PYTHON, using libraries such as PYLTSPICE for enabling fast proofs of concept by means of ready-to-use functionalities (using LTSPICE as simulation engine). In addition, for the future implementation of SFailSIM as a final/commercial software product, different approaches of licensing have been explored and proposed.

5) Different partitioning strategies have been explored. In terms of failure analysis, partitioning at subsystem level is recommended and could be considered in future developments. However, partitioning lower than subsystem level is not recommended due to complexity and loss of accuracy issues, which imply more disadvantages than benefits. In addition, two different strategies for exchanging information between partitions at subsystem level have been explored, both with advantages and disadvantages regarding traceability and efficiency depending on the application.

6) A flyback converter (both in open and closed loop) has been proposed for the failure analysis simulation with the prototype version of SFailSIM (script).

7) The standard conditions for the input schematics, ratings files and component libraries for the correct functioning of the prototype version of SFailSIM have been provided.

8) A sample of the output information provided by the prototype version of SFailSIM have been presented, both the output information available during the execution of the script and the final report produced by it.

9) A full execution cycle of the failure analysis script has been executed and reported in an open loop flyback converter (spending around one hour for the complete analysis and reporting of fifty failure modes).

10) A comparison of the simulation results in PSIM and LTSPICE has been presented for double checking. The differences between simulation results have been analyzed and reported, opening new research lines in failure modes modelling for failure analysis with SFailSIM.

11) A redesign of the analyzed flyback converter has been proposed following the results from the failure analysis. The redesign of the converter has been carried out by the use of both component and system redundancy. The fault tolerance of the proposed system has been checked.

12) An algorithm for finding the steady state of DC/DC power converters has been proposed and tested in various application cases successfully. This algorithm may be useful in future stages of the project to minimize simulation times and may lead to a more precise ratings analysis.

13) Different methods for omitting or reducing the simulation time until the system reaches a steady state have been initially proposed, which may lead to reduced simulation times.

VI. FUTURE WORKS

- 1) Study the feasibility of incorporating other simulation tools (in parallel with LTSPICE and PSIM), such as NGSPICE, within the development of SFailSIM, both for interaction (import/export) and for acting as simulation engine.*
- 2) Extend the scope and data amount of the databases included in SFailSIM progressively in next stages, as the future product may deal with the widest possible scope of components and failure modes.*
- 3) Research simulation parameters such as time step (optimum values) and time to steady-state (automatic identification and strategies for skipping it) for optimizing the simulation time spent for failure analysis without losing accuracy.*
- 4) Include additional considerations about other component parameters such as temperature.*
- 5) Model additional existing components and failure modes.*
- 6) Implement advanced component models for simulations (e.g., PSIM model Level 2 for MOSFET).*
- 7) Extend the scope of failure analysis to be included in SFailSIM from one-failure approach to multiple failure and cascade failures.*
- 8) Intensify and improve the processing of information generated during the simulation of failure modes with software tools (such as LTSPICE or PSIM), and extend the scope of reporting to design recommendations and standard outcomes such as FMECA (Severity Number, Detection Number, Probability Number, Criticality Number, Criticality Matrix, and other associated reports) for increasing the safety and design robustness/quality of electronic systems.*
- 9) Test and include, in future developments, the automatic exchange of information between partitions under failure conditions, considering partitioning at subsystem level and the strategies explored in this project.*
- 10) Continue the research line regarding the influence of the component models and the switches used for failure modes injection, which has been initially studied and tested in the scope of this project, and it remains open for future works associated with failure modes modelling within the scope of SFailSIM development.*
- 11) Inject failure modes in experimental tests on hardware prototypes for validating the results of the failure simulations executed with software tools such as LTSPICE and PSIM.*
- 12) Generate more complex and complete proofs of concept to evolve the TRL until SFailSIM becomes a real software product (full-documented, software-licensed, quality-tested, market-approached, standardized, ESA-recommended).*

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MAIN REFERENCES

- [1] C. Spreafico, D. Russo and C. Rizzi, "A state-of-the-art review of FMEA/FMECA including patents," *Computer Science Review*, vol. 25, pp. 19-28, 2017.
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- [4] *Reliability prediction of electronic equipment*, MIL-HDBK-217F, 1991.