REFERENCE	Customer	Date
900802-100-007	ESA	04/10/2024
Project	**Revision**	
OCMO - High Performance MEMS Oscillator	1.0	
Title	**Author**	
Executive Summary - OCMO	L.GUINGOUIN	
Distribution ESA	ESA - ONERA	
SYRLINKS	LGN/JDT/CBY	

OCMO - High Performance MEMS Oscillator

Executive Summary - OCMO

	Name _ Function	Date	Signature
Prepared by:	L.GUINGOUIN	04/10/2024	Signature numérique de Guingouin Date : 2024.11.25 17:27:07 +01'00'
Approved by:		04/10/2024	
Level of confidentiality:	☒ Public ☐ Internal use ☐ Controlled ☐ Confidential	Document status:	☐ On working ☐ Preliminary ☒ Completed ☐ Approved

REVISION

Revision n°	Date	Author	Comments
1.0	04/10/2024	Louis Guingouin	Creation

APPLICABLE

AD 1	

REFERENCE

R - 1	
R - 2	
R - 3	
R - 4	

ACRONYM

Abbreviations	Signification
MEMS	Microelectromechanical systems
OCMO	Oven controlled MEMS oscillator
OCXO	Oven controlled crystal oscillator
UTP	Upper turnover point
USO	Ultra Stable Oscillator

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1. INTRODUCTION

The purpose of this project was to design, realise and test two engineering models (EM) of high-performance MEMS reference oscillators compatible with on-board telecom and navigation applications.

Accurate timing and low phase noise are critical parameters for on-board Navigation receivers and Telecom frequency converters respectively. Those two critical parameters, in many instances, are calling for high performance quartz oscillators namely Oven Controlled Crystal Oscillators (OCXO)

The major performance differences between standard quartz oscillators and high-end OCXOs are resulting from the careful choice of the quartz resonator (and the associated electrical components), as well as the fine sheltering of the quartz resonator itself which provides a very stable environment. The major drawback of this improved performance is significantly increased power consumption as well as larger mass and volume.

Most recent on the market, MEMS oscillators are already as good as temperature-controlled oscillator (TCXO) while being much smaller (single-chip integration as compared to hybrid assembly).

The purpose of this R&D activity was to aim at OCXO performance while reducing drastically the power consumption benefiting from the MEMS resonator properties. A footprint reduction was also expected as result of this development.

2. INITIAL REQUIREMENTS

Parameter	Telecom	Navigation
Design frequency	100 MHz	10 MHz
Phase noise max. @ 1 Hz offset		< -65 dBc/Hz
Phase noise max. @ 100 Hz offset	TBD	< -95 dBc/Hz
Phase noise max. @ 1 kHz offset	< -120 dBc/Hz	< -145 dBc/Hz
Phase noise max. @ 10 kHz offset	< -140 dBc/Hz	< -165 dBc/Hz
Phase noise max. @ 100 kHz offset	< -155 dBc/Hz	< -165 dBc/Hz
Phase noise max. @ 1 MHz offset	< -170 dBc/Hz	< -165 dBc/Hz
Noise floor	< -170 dBc/Hz	< -165 dBc/Hz
Harmonics	< -40 dBc	< -30 dBc
Spurious	< -80 dBc	< -100 dBc
Allan variance (over 1 s)	NA	$< 5\ 10^{-12}$
Output power	> +5 dBm	> +5 dBm
Temperature sensitivity (within operating range)	< 5 ppb	+- 20 ppb
Aging (over 10 years)	5 ppm	0.5-0.8 ppm

Figure 1. Functional and performance requirements

Telecom application refers mainly to electronic beam forming that uses oscillator signals to control the phases of the elements in a phased array antenna. Phased array antennas form beams by adjusting the phase of the transmission or reception signals of each antenna element. Unwanted phase variations due to phase noise can cause beam misalignment, meaning the antenna will no longer point precisely at the desired target or affecting the angular resolution. Phase noise can introduce errors in these adjustments, disrupting the direction and shape of the beam. Regarding general purposes radio links, phase noise degrades signal quality by introducing noise components that can mix with the desired signal. This reduces the signal-to-noise ratio (SNR), thereby affecting the link balance. Therefore, low phase noise floor is essential.

Navigation applications refer to positioning, navigation and timing applications in low earth orbit. LEO PNT applications currently enable positioning accuracies from centimeters to tens of centimeters. To achieve such performance, the onboard clocks must exhibit a stability representing a fraction of the system's total error over an integration time corresponding to the duration of one or more GNSS frames. This corresponds to stabilities on the order of 1E-12 to 1E-13 over integration times ranging from 1 to 120 seconds. In the coming years, LEO PNT constellations appear to be opening the doors to a high-volume market for Newspace USOs. Inter-satellite time synchronization and/or ranging as well as radio occultation also are navigation applications with similar needs for short term stability.

Parameter	Value
Operating temperature range	-30 /+70 °C
Radiation (TID)	100 krad
g-sensitivity	TBD

Figure 2. Environmental requirements

The radio front-ends of Mini & MicroSats, having low power efficiency, often have a very high power consumption compared to OCXO or other kind of local oscillator. Therefore, power consumption does not seem to be a critical factor for NewSpace applications. However, the emerging NanoSatellite platforms, which are more compact than Micro & MiniSats, have power allocated to oscillators of only a few hundred milliwatts. It is therefore essential to propose low power oscillators for both telecom and navigation applications.

Parameter	Value
DC power (steady state @ 25 °C)	< 250 mW
DC power (warm-up)	< 500 mW
Mass	< 25 g
Volume	< 25x25x17 mm^3

Figure 3. Physical and resource requirements

3. WORKFLOW

Tasks	Syrlinks / Onera / FemtoENG
Literature Review and Patent Survey	▪ Solutions of vacuum packaging: Cold Welding, Gold wafer level thermocompression, Silex wafer stacking and MEMS ▪ Presentation of IHR (Internally Heated Resonator) designs ▪ Solutions of oscillator external packaging ▪ Electronics topology ▪ Presentation of silicon oven first version ▪ Presentation of quartz MEMS design (HRL) ▪ Presentation of Silicon MEMS resonator ▪ Presentation of 2DLEM Quartz MEMS resonator
OCMO Preliminary Design	▪ Circuit design simulation ▪ Frequency accuracy and multiplication. Simulations and study of DDS and PLL synthesis ▪ Simulation and fabrication of 10MHz length extension resonator first batch ▪ First finite element simulation of 100MHz thickness shear mode resonator

Critical Building Blocks Detailed design & Test	▪ Measurement of 10MHz MEMS resonators in vacuum chamber ▪ 10MHz length extension resonator encapsulation in TO8 package ▪ Pierce gate with 10MHz MEMS breadboard and measurements ▪ Heating of the resonators and FreqvsTemp measurements ▪ LMX2594 simulations and measurements of 10MHz (accuracy) and 100MHz synthesis ▪ DDS development and measurement using ICE40LP8K FPGA
OCMO Detailed Design	▪ Presentation of the final architecture ▪ Simulation and fabrication of a 10MHz transimpedance discrete oscillator ▪ Thermal simulation and optimization of the silicon oven ▪ Oven control circuit ▪ Study of electrical resistivity of sputtering Ti/Au deposits ▪ 100MHz transimpedance amplifier oscillator simulation ▪ Silicon oven manufacturing flowchart definition
OCMO Performance Evaluation	▪ Fabrication of silicon oven ▪ Debug and investigation of 10MHz and 100MHz MEMS in silicon oven. ▪ Measurements of vacuum sealed 10MHz resonators from phase 1 + Onera TIA oscillator for characterization.
OCMO Future Developments	• Update about markets needs for telecom and navigation applications • Issues vs solutions table • Future developments roadmap

Table 1. OCMO project workflow

4. DEMONSTRATOR PRESENTATION

The development of the deep reactive ion etching (DRIE) of crystalline α-quartz has enabled to overcome drawbacks of standard chemical wet etching such as non-vertical etching facets and allows to etch along any crystal axis. This will pave the way for high-Q resonators and high-performance vibrating quartz MEMS devices and especially high-performance MEMS resonators for time references.

As part of this project and previous work, Onera has developed, manufactured using DRIE and measured a 10MHz length extension mode quartz MEMS resonator for navigation applications and a 100MHz thickness shear mode quartz MEMS resonator meant for telecom application.

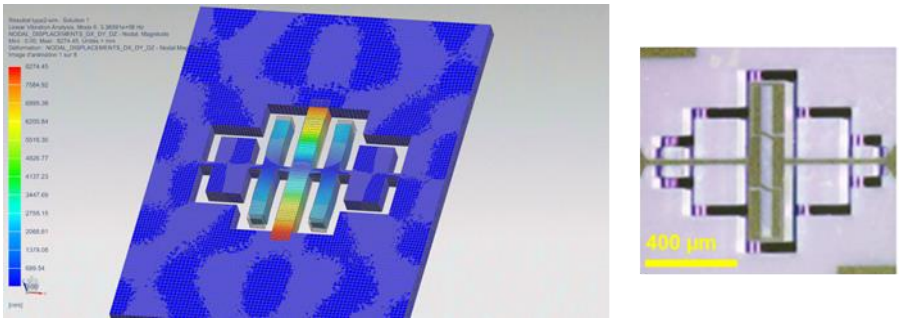

Figure 4. 10MHz length extension mode quartz MEMS resonator developed by ONERA

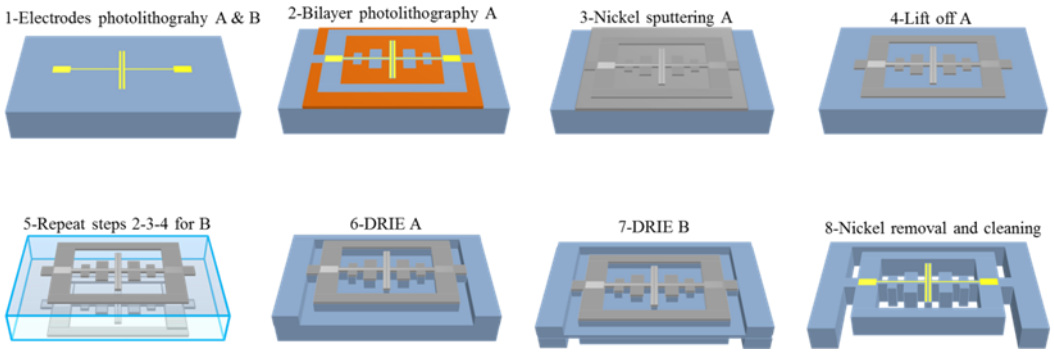

Figure 5. Manufacturing flowchart quartz MEMS resonator using DRIE

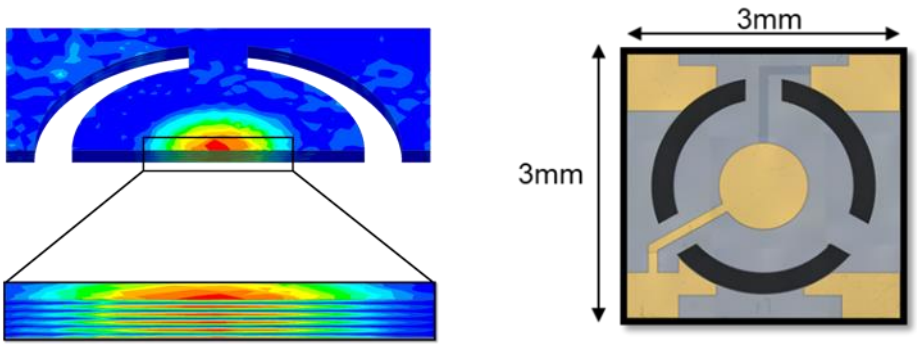

Figure 6. 100MHz thickness shear mode quartz MEMS resonator developed by ONERA

Those resonators have been integrated in an internally heated resonator design patented by Syrlinks and manufactured by FemtoENG. Two versions of this silicon oven were developed for respectively the 10MHz and the 100MHz resonators as their dimensions were slightly different.

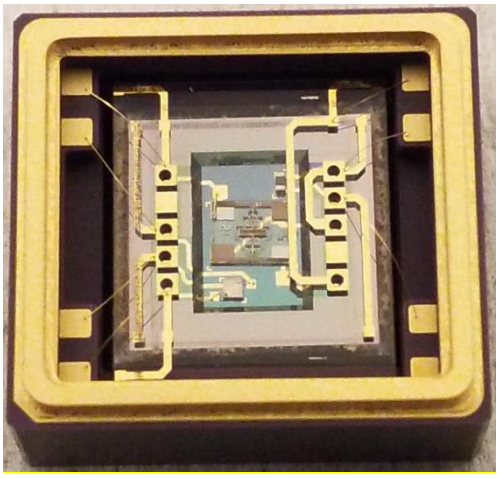

Figure 7. 10MHz quartz MEMS resonator & Silicon Oven

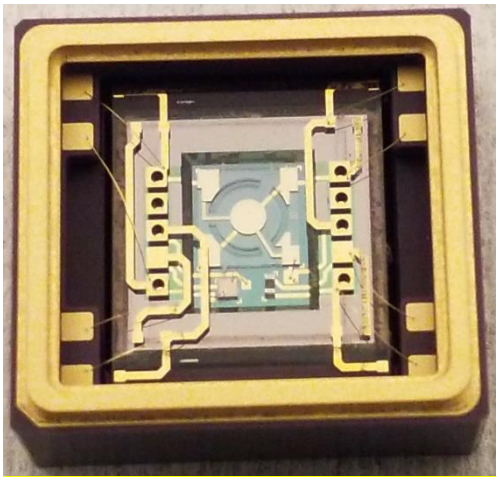

Figure 8. 10MHz quartz MEMS resonator & Silicon Oven

The demonstrator consists of a main PCB, the ceramic package which contains the quartz MEMS resonator as well as the heating element and temperature sensor. Main PCB electronics consists of a transimpedance oscillator, a buffer and an oven control circuit.

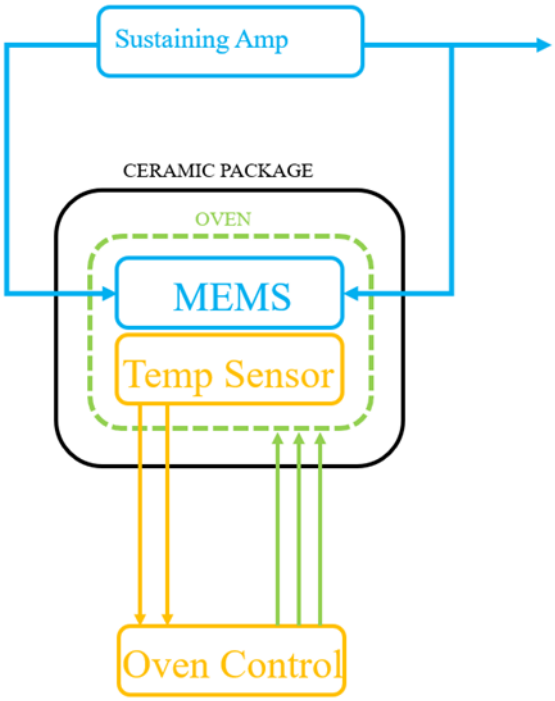

Figure 9. Architecture of the final OCMO demonstrator

5. RESULTS

Phase noise, ADEV and ageing have been measured on the final demonstrator. Measurement of the 10Mhz OCMO are depicted in the figures below. Phase noise floor level is related to low drive level into the resonator as well as the high noise factor of the transimpedance oscillator circuit. Close to carrier phase noise and ADEV levels are related to the intrinsic quality factor of the resonator that was lower than expected and the high motional resistance of the resonator that complexified the design of the oscillator and didn't allow to achieve high loaded quality factor.

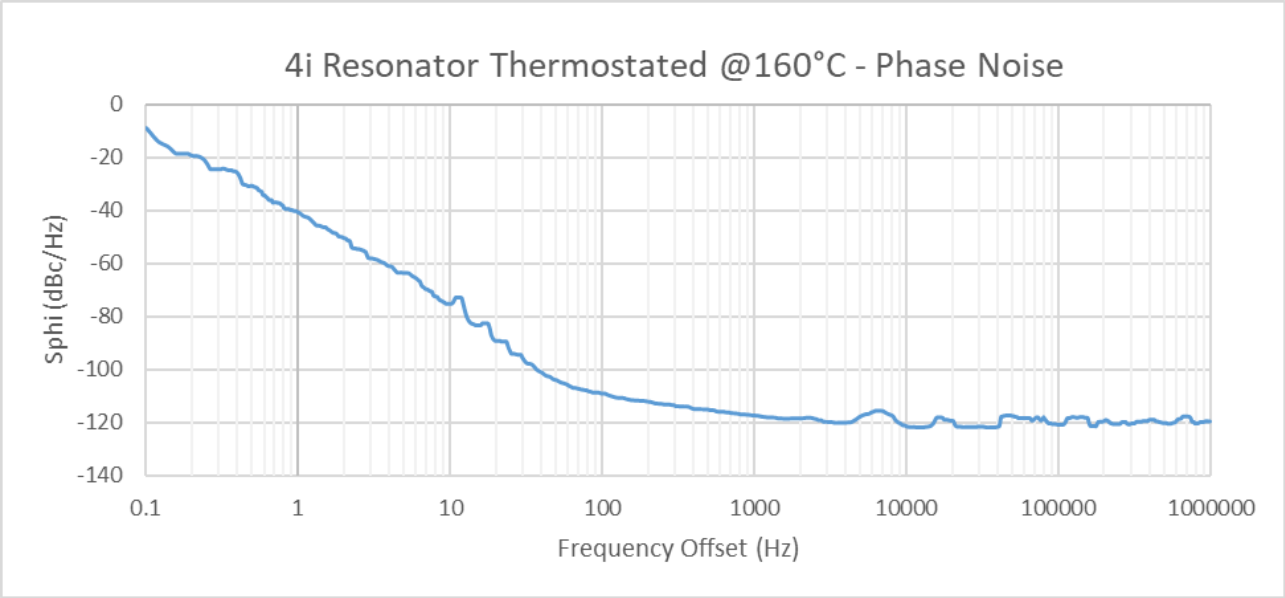

Figure 10. Phase Noise of a thermostated 10MHz length extension resonator with transimpedance oscillator circuit

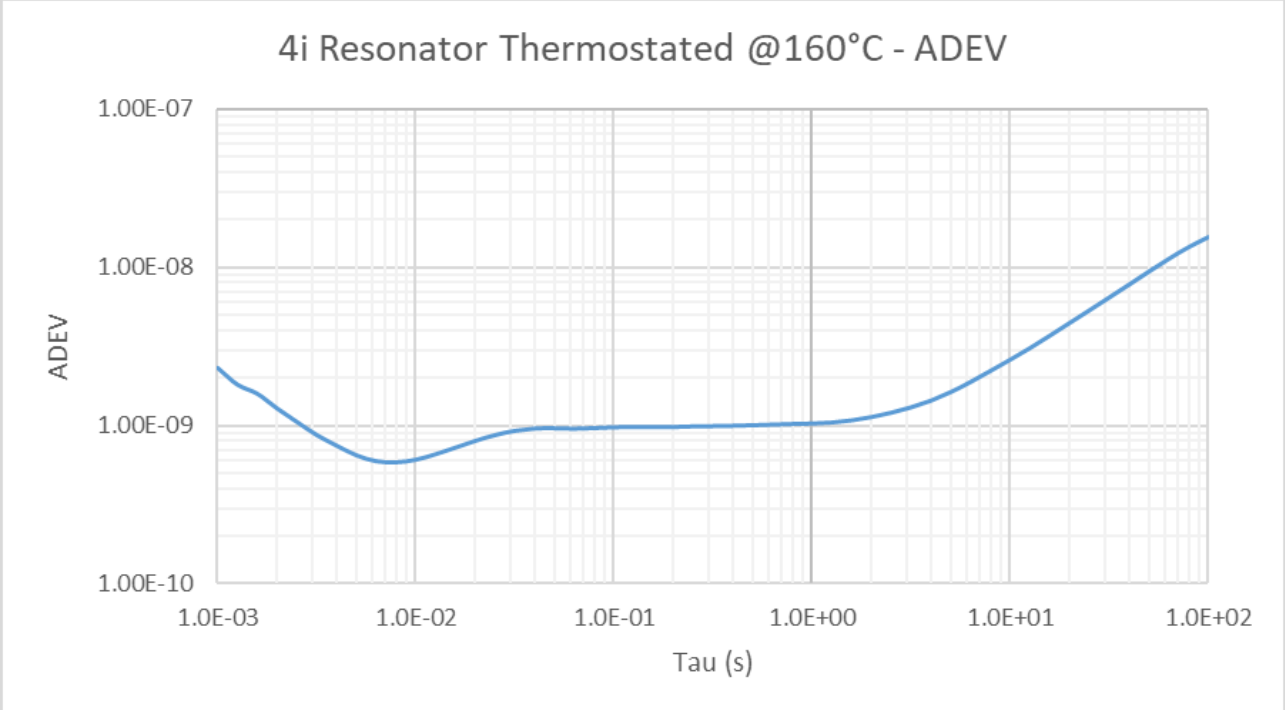

Figure 11. ADEV of a thermostated 10MHz length extension resonator with transimpedance oscillator circuit

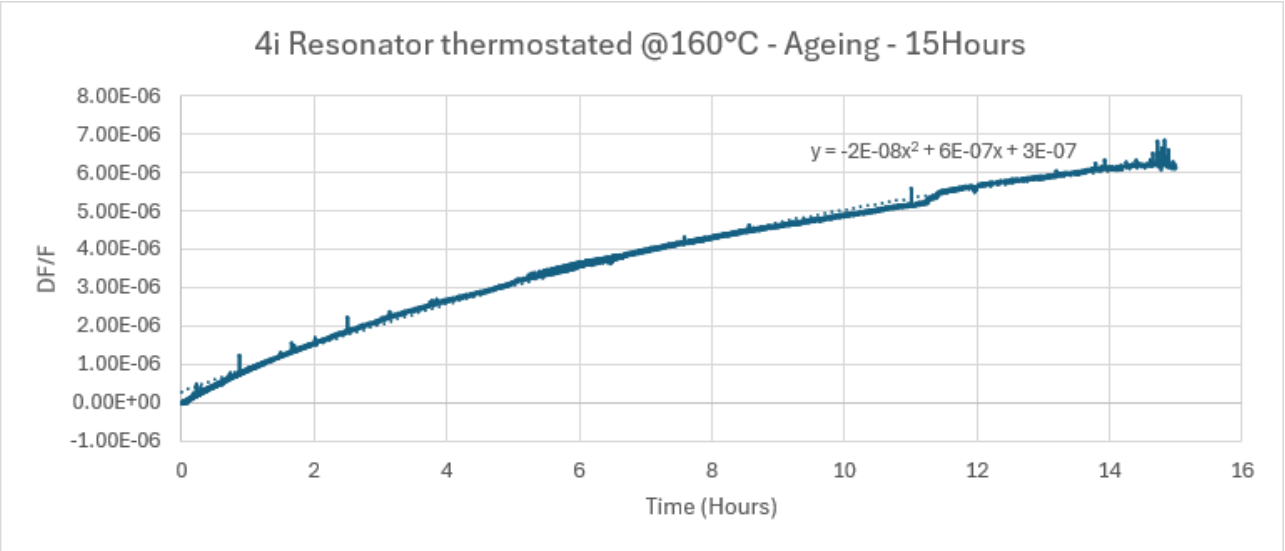

Figure 12. Ageing of a thermostated 10MHz length extension resonator with transimpedance oscillator circuit

The frequency drift that can be observed on the ADEV and ageing plot is directly linked to the bonding technique used for the resonator in the package and the associated stress release. Furthermore, thermal cycles for stress release have not been carried out on the packaged resonators. To improve frequency aging stability, the packaged induced stress on the resonators will have to be considered in future design, as well as the thermal cycles for stress release.

6. ISSUES & SOLUTIONS SUMMARY

Subpart	Issues	Solution
Silicon Oven	Resistivity of Ti/Au thin layer deposits	• Switch to electron beam physical vapor deposition for thicker deposition metal layers instead of sputtering to improve DC resistance conductive layers.
	Vacuum level inside the cavity	• Outgassing study of each material inside the cavity under vacuum to check the outgassing pressure level over the application duration. This study will allow us to define if a getter is needed or not what are the margins of vacuum level over the mission duration. • Definition and integration of a getter. Different types of getters and activation methods exists. The outgassing study as well as discussions with SAES are needed to define if a getter is needed and if so, what kind.
	Hermeticity of the cavity	• Gold/gold thermo-compression study. Changing metal with a lower diffusion temperature. And/or increasing the temperature without being incompatible from glues and components inside the cavity.

	Damaging the Ti/Au deposits at wafer cutting	• Go back to diamond saw instead of femtosecond laser for wafer cutting to avoid reflections inside the glass that destroys conductive layers. This solution nevertheless implies to design a silicon assembly that is immune to vibrations.
	Power consumption	• Decreasing the motional resistance will allow the use of standard low consumption electronics such as bipolar Colpitts or Pierce gate using low consumption unbuffered gate inverters. • ASIC. Reducing the size of the circuit by integrating it into an ASIC allows to reduce electrical interconnections length and therefore parasitic resistances and capacitance that can increase the power consumption a circuit. Furthermore, transistors sizes are reduced in ASIC compared discrete equivalent thus decreasing the power consumption of each transistor. Finally, ASIC are designed for a specific application which can be low power consumption. • Vacuum inside the ceramic package. That will allow to supress the convection losses and therefore reduce power consumption. • Thermal brakes in the glass layer. This will allow to reduce the conduction losses of the silicon oven. This is essential if vacuum is made inside the cavity or the ceramic package.
10MHz MEMS & 100 MHz	High motional resistance	• Use hybrid substrate to etch thinner resonators (thickness <20µm) will lead to improved resistance (<200Ω)
	Frequency aging	• The frequency aging stability can be improved by working on the resonator bonding technique in the packaging and by releasing residual stress by thermal cycles.

Table 2. Issues and solution table for silicon oven and quartz MEMS resonators

7. CONCLUSION

Silicon oven: Silicon oven manufacturing went well regarding the process that was defined. Some risks initially identified were successfully mitigate like the suppression of parasitic capacitance by introducing holes in the silicon cavity. However, measurements of the resonators inside the cavity showed that the silicon cavity was not under vacuum probably due to either a lack of pre-outgassing that led to outgassing inside the cavity or hermeticity due to gold/gold thermo-compression. Furthermore, femtosecond laser cutting at wafer level led to a deterioration of the conductive layers.

Quartz MEMS resonators: The main drawback of the resonators is their high series resistance that leads to high phase noise and oscillator design issues. The development of thin quartz resonators is under progress at ONERA and will enable to lower the series resistance down to 150 Ω for an AT cut thickness shear mode resonator of thickness 20µm.

10MHz TIA oscillator: Test of TIA 10MHz showed no improvement for loaded quality factor and phase noise floor compared to 1st design with pierce gate. Transimpedance amplifier current noise leads phase noise floor. However, state of the art and literature shows such sustaining amplifier must be used for MEMS oscillators. One way to improve power consumption of the TIA oscillator would be to develop a dedicated ASIC. Stability measurement showed high close to carrier phase noise, 1E-9 short term stability as well as very high rate. This design of resonator should be improved by one order of magnitude to compete with cheap AT-cut resonators.

100MHz TIA oscillator: No oscillation could be obtained from 100MHz TIA oscillator as the motional resistance of the resonator was too high. This is mainly due to the issues encountered during the manufacturing process where resonators only had one side of electrodes. Even if no performance of the 100MHz oscillator could be measured future development as described in the related documents should be oriented on high frequency (100MHz → 1GHz) MEMS resonators that are more integrated (less oven power consumption), low motional resistance (Standard electronics + good, loaded quality factor), high quality factor compared to SAW/BAW resonators.