

Health Monitoring of digitally controlled flexible converters

Final Review
25/04/2024



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Health Monitoring of digitally controlled flexible converters

Introduction

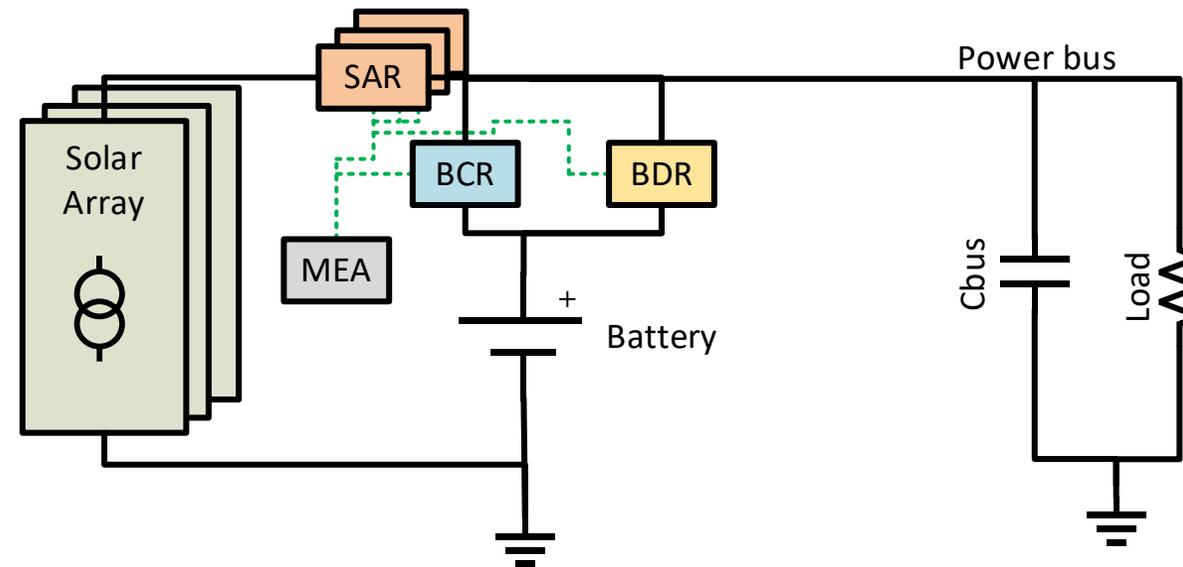


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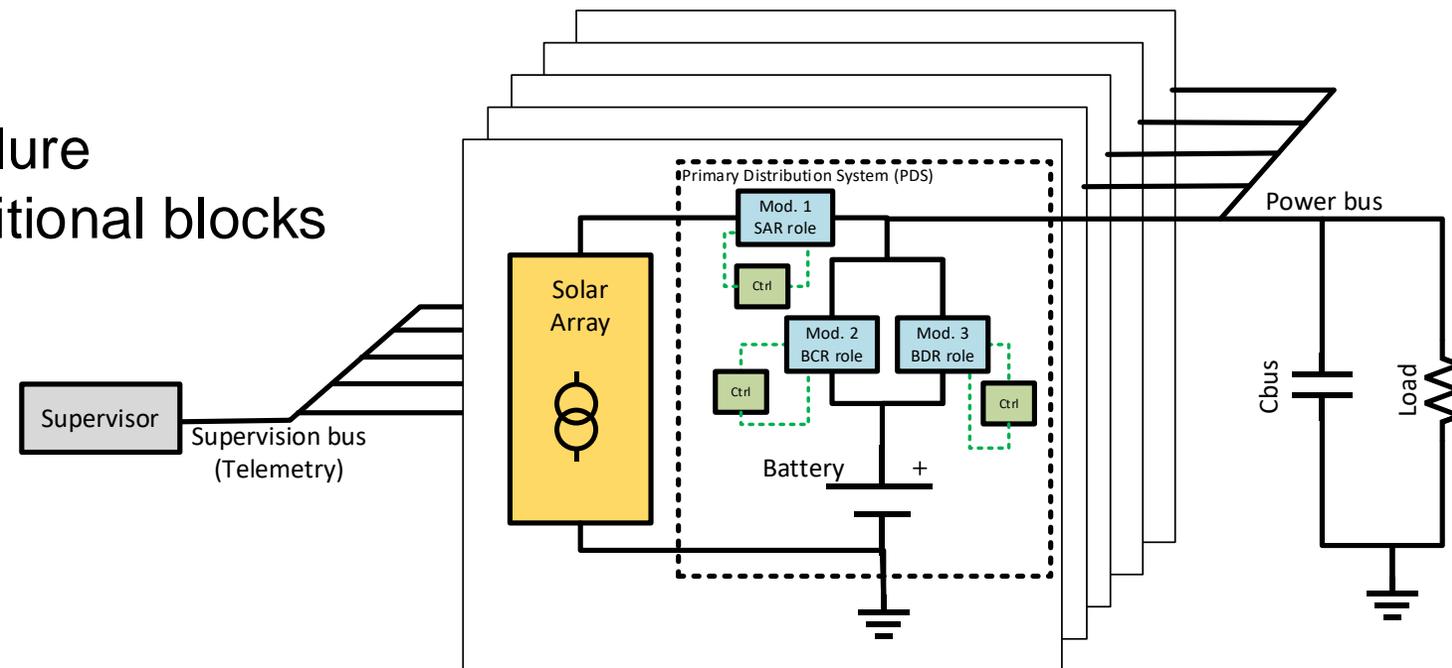


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- Each block is mission-dependent
- Long design times
- MEA is a centralized controller. Critical



- What if we could standardize and parallelize each main block (SAR, BCR, BDR)?
- Same hardware for each role (SAR, BCR, BDR)
- Control and protection local to each module
- Redundancy at module level
- Automatic power sharing
 - Failure recovery
 - Health monitoring to prevent failure
 - Power scale by introducing additional blocks
- No centralized controller
- Three branches to develop
 - Topology  Universidad de Oviedo
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 - Control  Universidad Carlos III de Madrid
 - Health monitoring  Universidad de Oviedo
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Health Monitoring of digitally controlled flexible converters

Topology



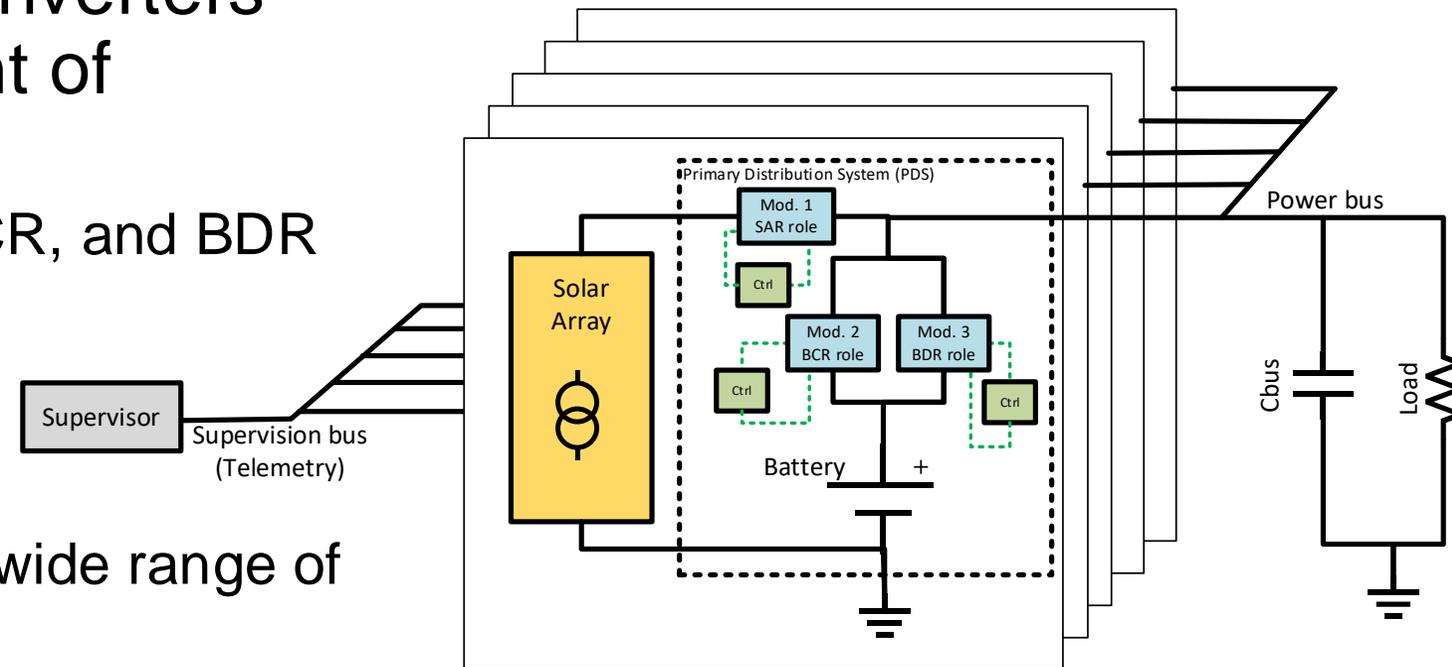
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1. New architecture is proposed. Smaller units (modules) that can be combined to satisfy power needs
2. Each module can work as SAR, BDR and BCR
3. No hardware reconfiguration needed. Digitally controlled.
4. Redundancy at module level
5. No communication between modules
6. Additional supervisor module interfaces between power system and rest of spacecraft

- Topology selection based on a comparison of optimised converters (lowest losses for each point of operation).
 - Each module includes SAR, BCR, and BDR capabilities.
- Two-method analysis.
 - Qualitative analysis explores a wide range of converters
 - Quantitative analysis selects the best based on a figure of merit



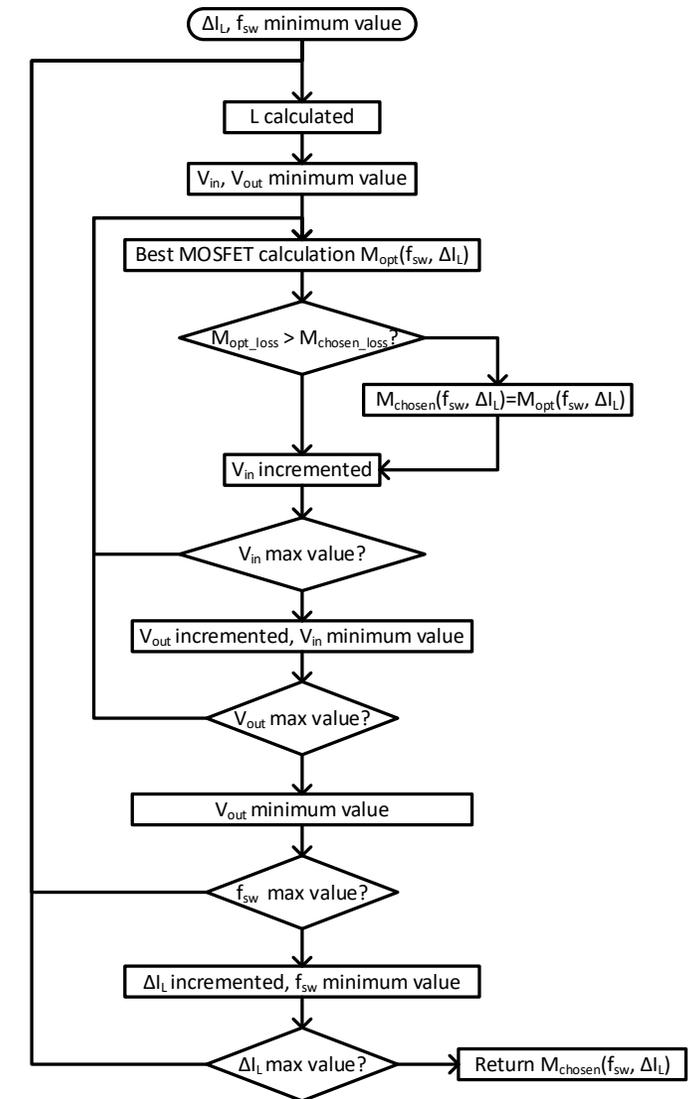
- **Qualitative analysis**
- Divided into: unidirectional, bidirectional and three-port topologies
- Evaluates adequacy of the topology (at module level) based on:
 - Number of semiconductor devices
 - Number of magnetic elements
 - Number of capacitors
 - Number of converters
 - Complexity of control
 - Bus limitations
 - Efficiency

Topology	Converters total	Semiconductor devices	Inductors	Capacitors	Control	Bus lim.	Efficiency
Buck or Boost	3	12	3	6	Simple	Y	Very High
Weinberg	3	21	6	6	Simple	Y	High-Very High
Non Inverting BuckBoost	3	18	3	6	Simple-Average	N	High
Full Bridge	3	24	6	9	Simple	N	High
Push Pull	3	18	6	9	Simple	N	High
Bidirectional 2-level Switched-Capacitor	2	16	2	8	Complex	Y	High
4-switch BuckBoost	2	12	2	4	Average	N	High
Bidirectional Buck/Boost	2	8	2	4	Average	Y	High
DAB	2	16	4	6	Complex	N	High
Bidirectional LLC	2	24	10	8	Complex	N	High
TAB	1	12	3	5	Very Complex	N	High
Interleaved Boosts with Full bridge (integrated)	1	9	4	3	Very Complex	Y	High
Three-port asymmetrical Half Bridge	1	8	2	4	Very complex	Y	Medium-High

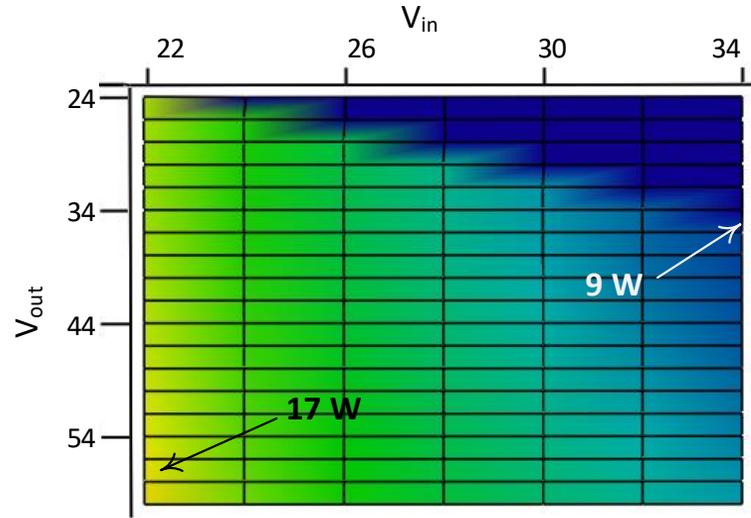
- **Unidirectional:**
 - Offer no real advantage
- **Bidirectional:**
 - More advantages at almost no cost
 - Reduce number of modules in one
 - Galvanic Isolation not a requirement. Increase in weight
- **Three port bidirectional:**
 - Reduction of components
 - Single control. More complex
 - Modularity more cumbersome
- Final candidates: Bidirectional buck and 4-switch buck-boost

- **Quantitative analysis**
- Used to obtain a final figure of merit to evaluate the best topology to choose.
- Converters optimized for lowest losses.
- Sweeping process.
- Optimised variables: fsw, current ripple.
- Topologies: Bidirectional buck and 4-switch buck-boost.
- Conditions:
 - Bus voltage: 28 V
 - Battery voltage 22 to 34 V
 - Solar array voltage: 30 to 60 V.
 - Power: 500 W.
 - Switching frequency: 30 to 200 kHz
 - Current ripple (relative): 0.05 to 0.45

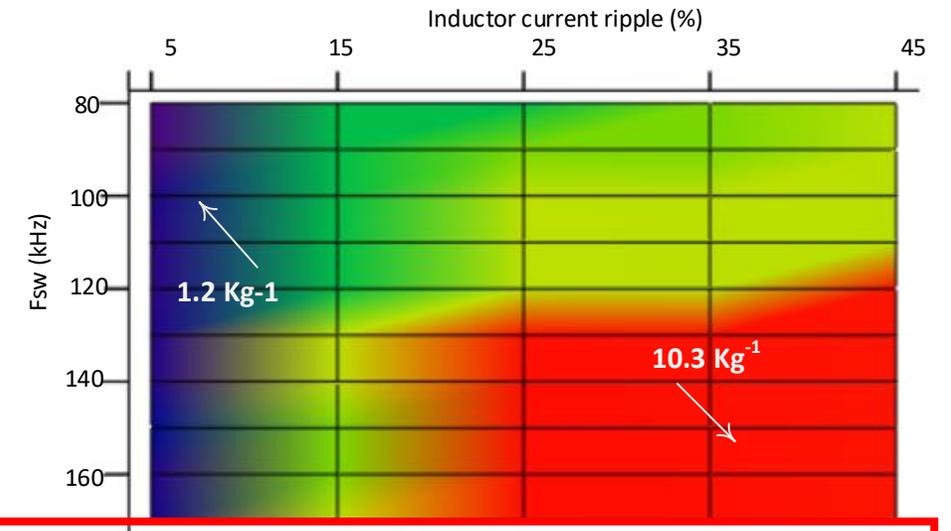
1. Definition of input variables (voltage range, power, switching frequency, current ripple, etc)
2. Minimum inductance value
3. Switch selection
4. Inductor design
5. Rough estimation of efficiency for each fsw-ripple pair
6. Accurate efficiency estimation
7. Figure of merit efficiency/weight



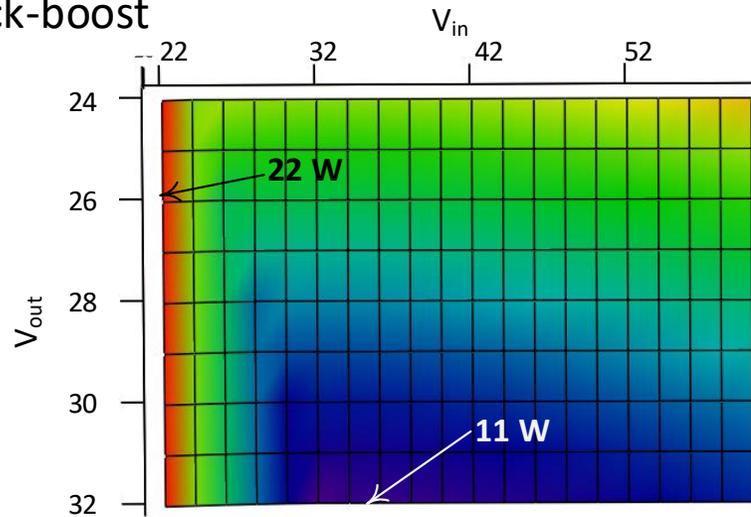
Losses



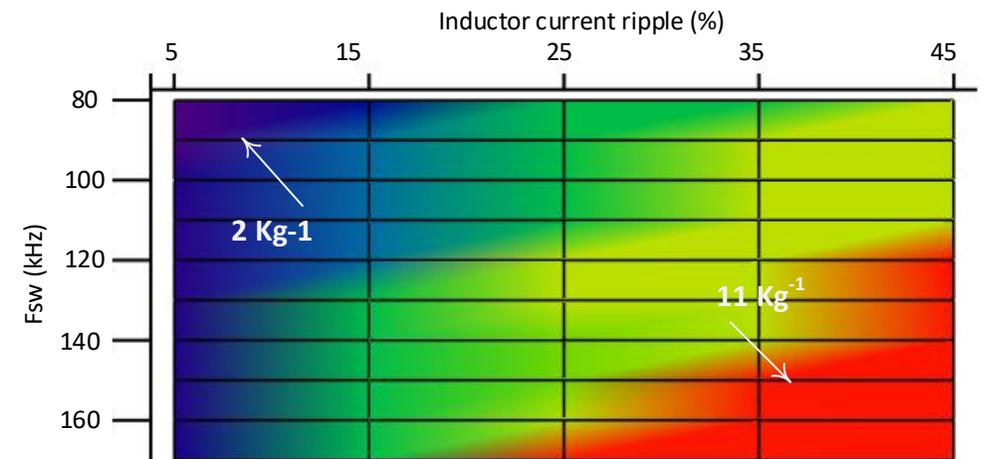
Eff/Weight



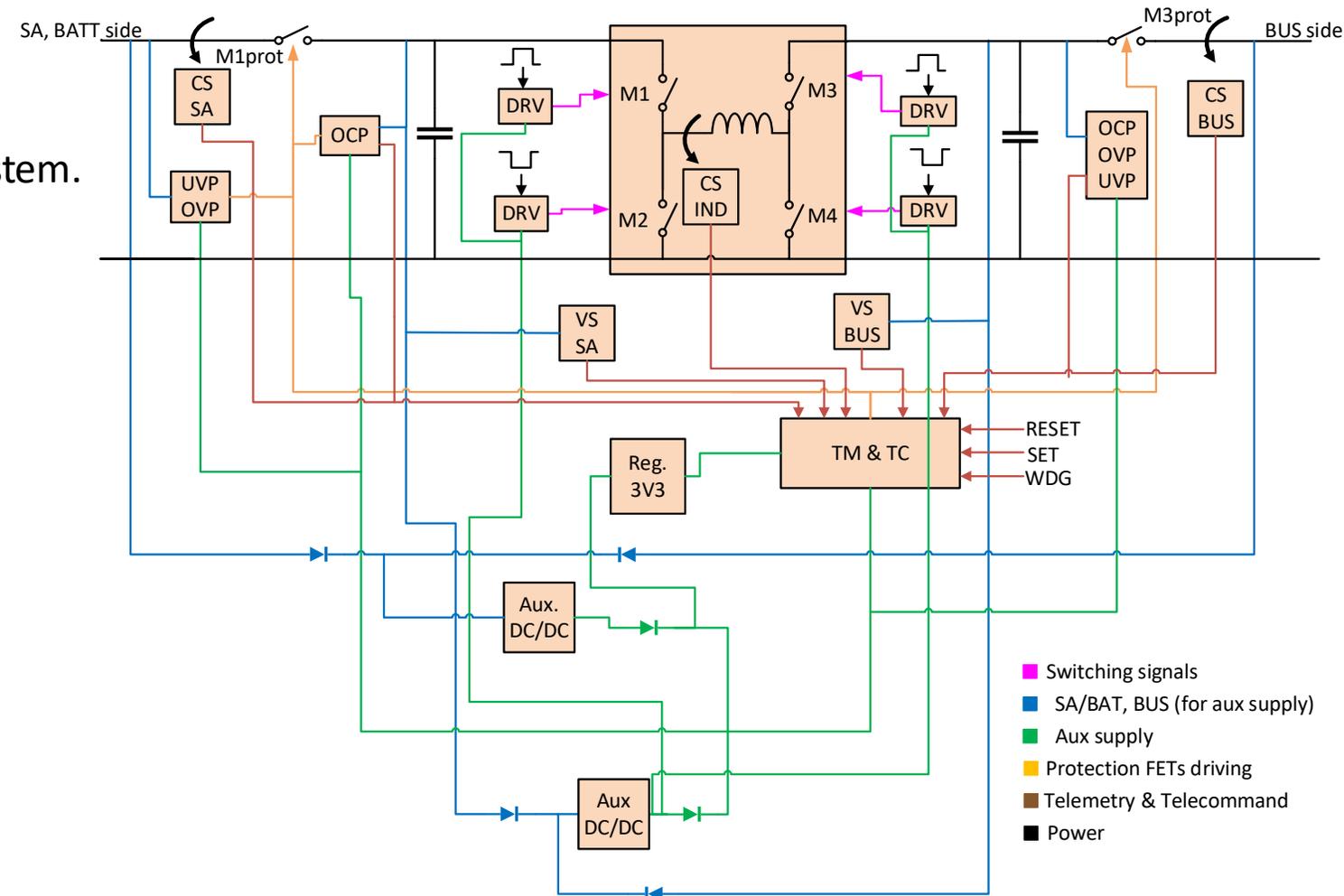
4-switch buck-boost



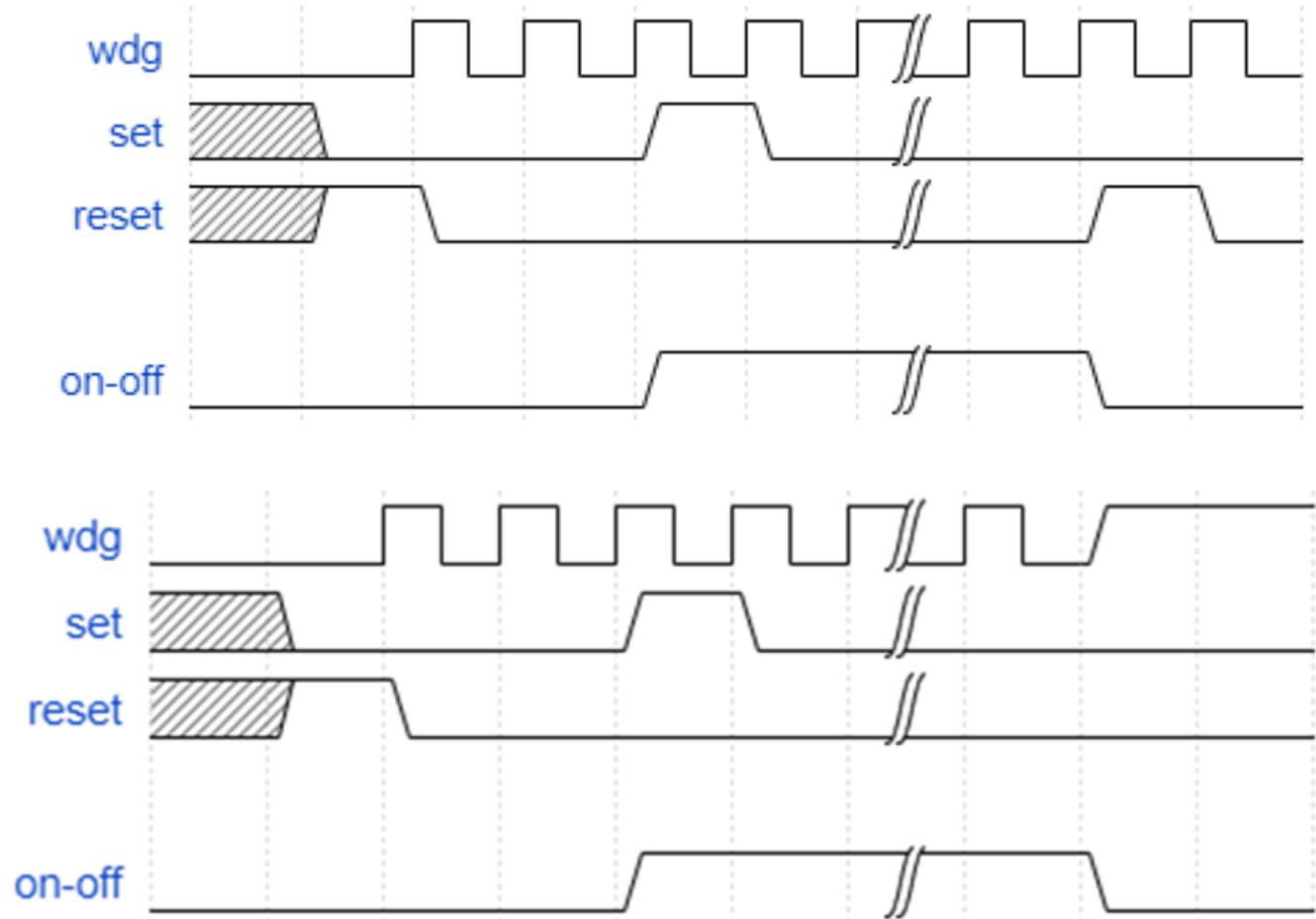
4-switch buck-boost



- Single point failure free
- Local OCP, UVP, OVP protections.
 - Protection FETs included.
 - In failure module isolates from power system.
 - Rest of the modules compensate
- Each module is digitally controlled by FPGA.
- Interface to control:
 - Analog
 - Input/Output voltage and current
 - Inductor current
 - Digital:
 - On/Off
 - Transistor driving
 - Watchdog

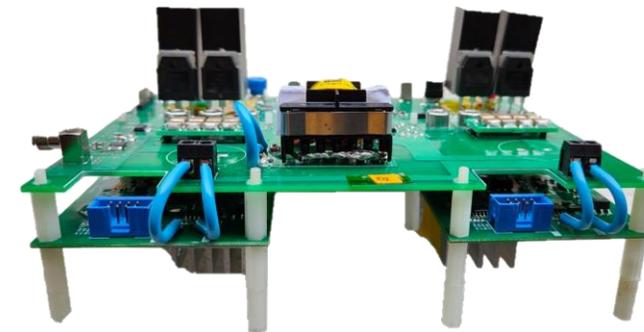


- Watchdog prevents digital controller failure.
- If stuck permanently High or Low module isolates.

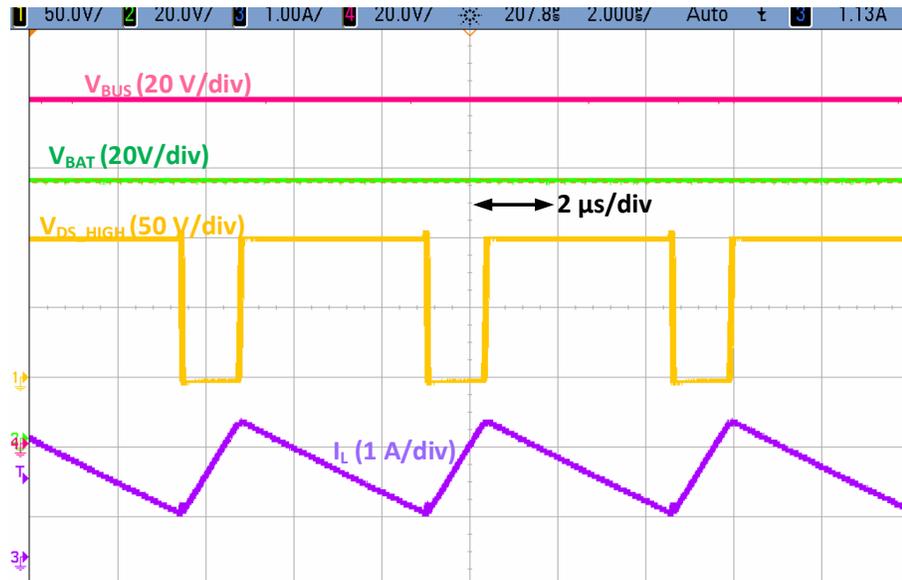


- Prototype built with COTS
 - Rad-hard equivalents available
 - Component availability
 - Switching elements: GaNSystems GS66516B

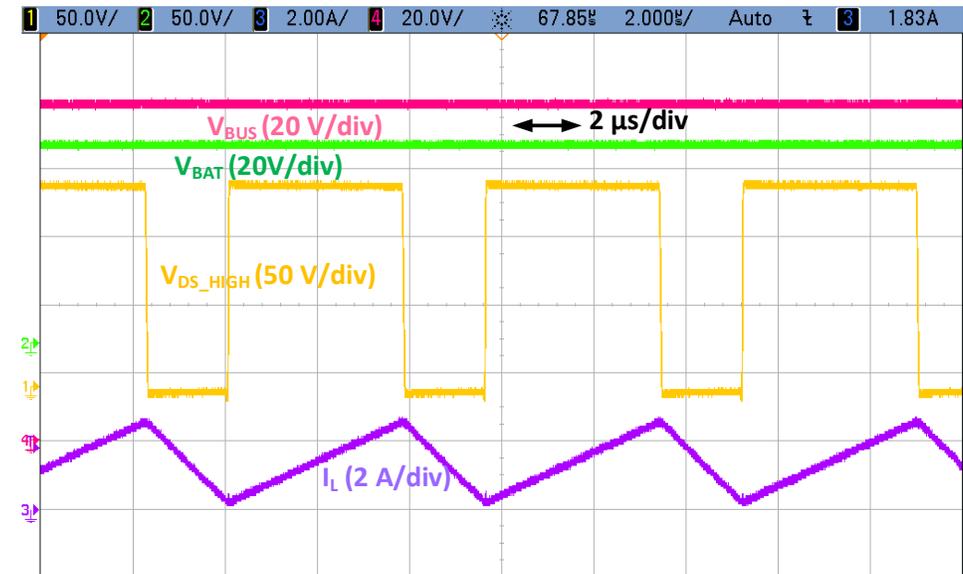
Bus voltage	100 V
Battery voltage	80 V
Solar array voltage	150 V
Output capacitor	35.2 μ F
Switching frequency	180 kHz
Inductance	83 μ H
Current ripple	2.5 A
Output current	5 A
Bus power	500 W

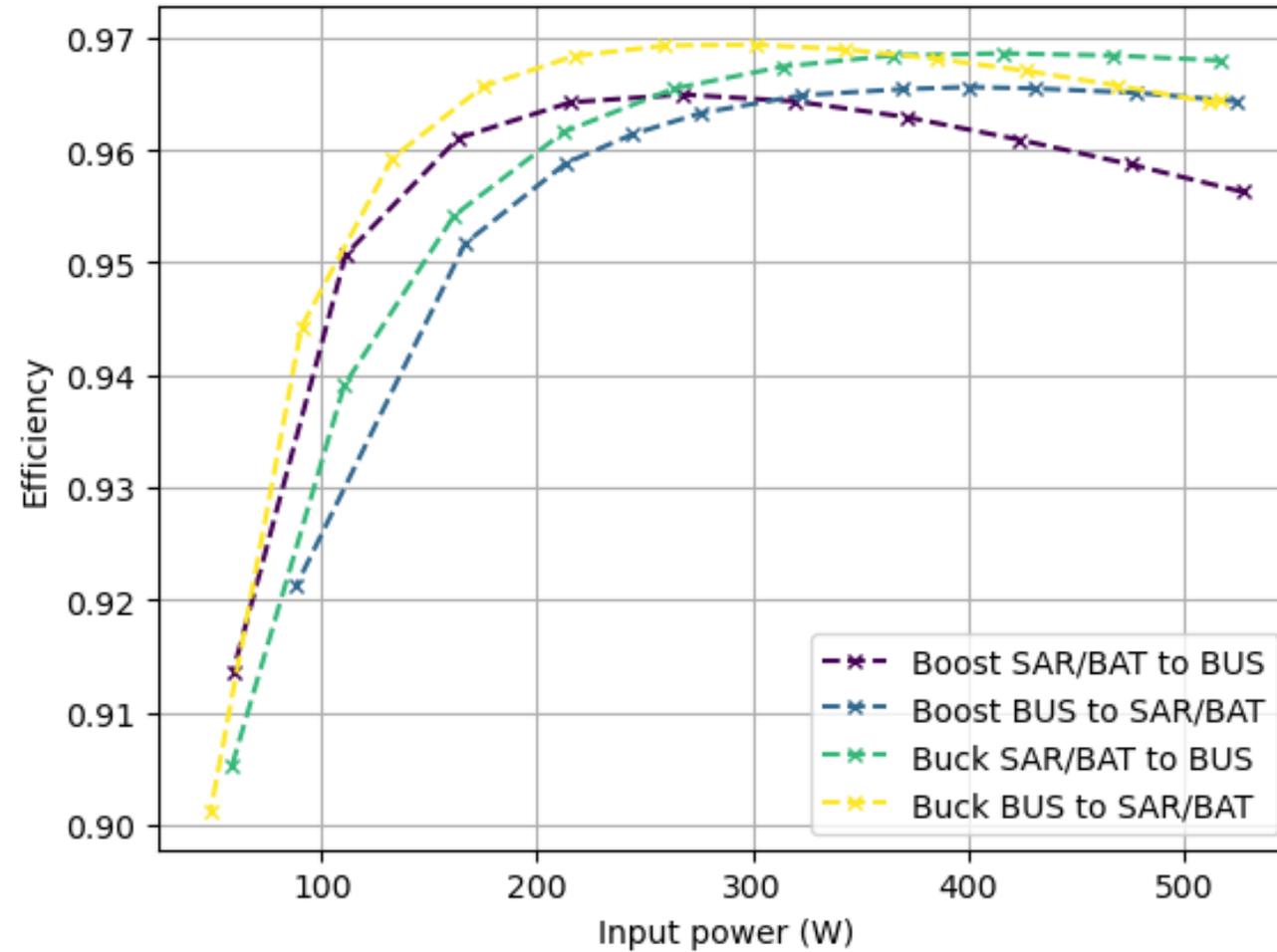


- Boost Mode
 - $V_{in}=80\text{ V}$
 - $V_{out}=100\text{ V}$



- Buck Mode
 - $V_{in}=150\text{ V}$
 - $V_{out}=100\text{ V}$





- Full power temperature response below 90°C .
- Full power efficiency: $\sim 96\%$



- New power architecture is presented
 - Hardware developed to test it
- Allows parallelization and adequate power scaling
- Allows decentralized control
- M. Fernandez, M. Arias, P. F. Miaja, J. Oliver, J. A. Fernandez and P. Z. Vaquero, "Four-Switch Buck-Boost Based Module Block for Highly Modular Power Architecture," 2023 13th European Space Power Conference (ESPC), Elche, Spain, 2023, pp. 1-6, doi: 10.1109/ESPC59009.2023.10412700.



Health Monitoring of digitally controlled flexible converters

Control

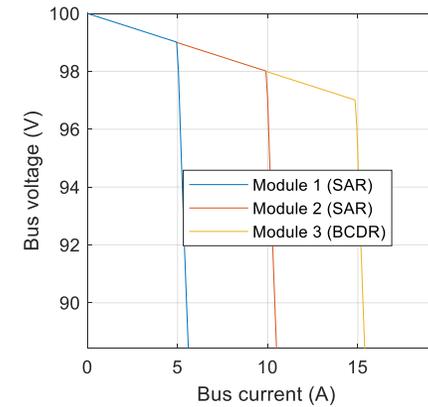


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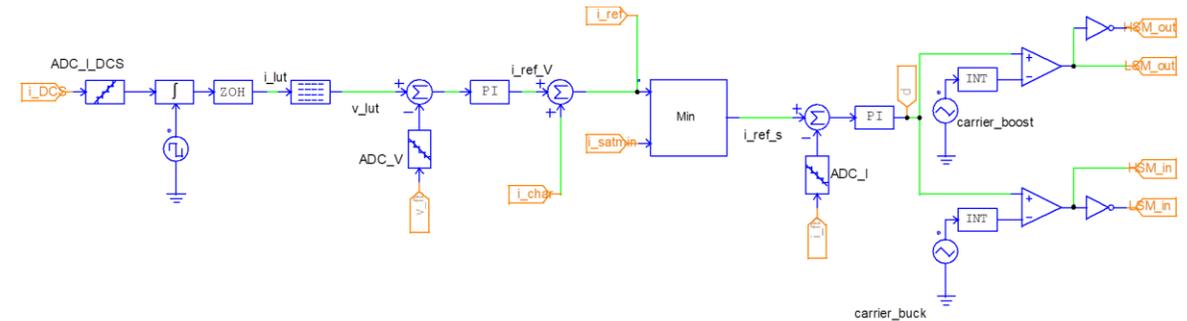


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- Control principle: droop control, DBS



- Control architecture and implementation



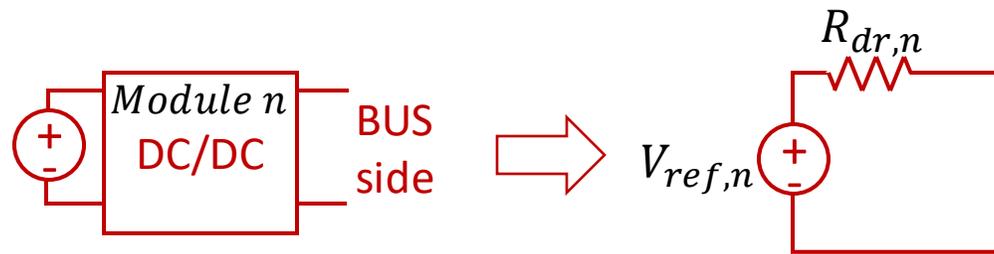
- Results



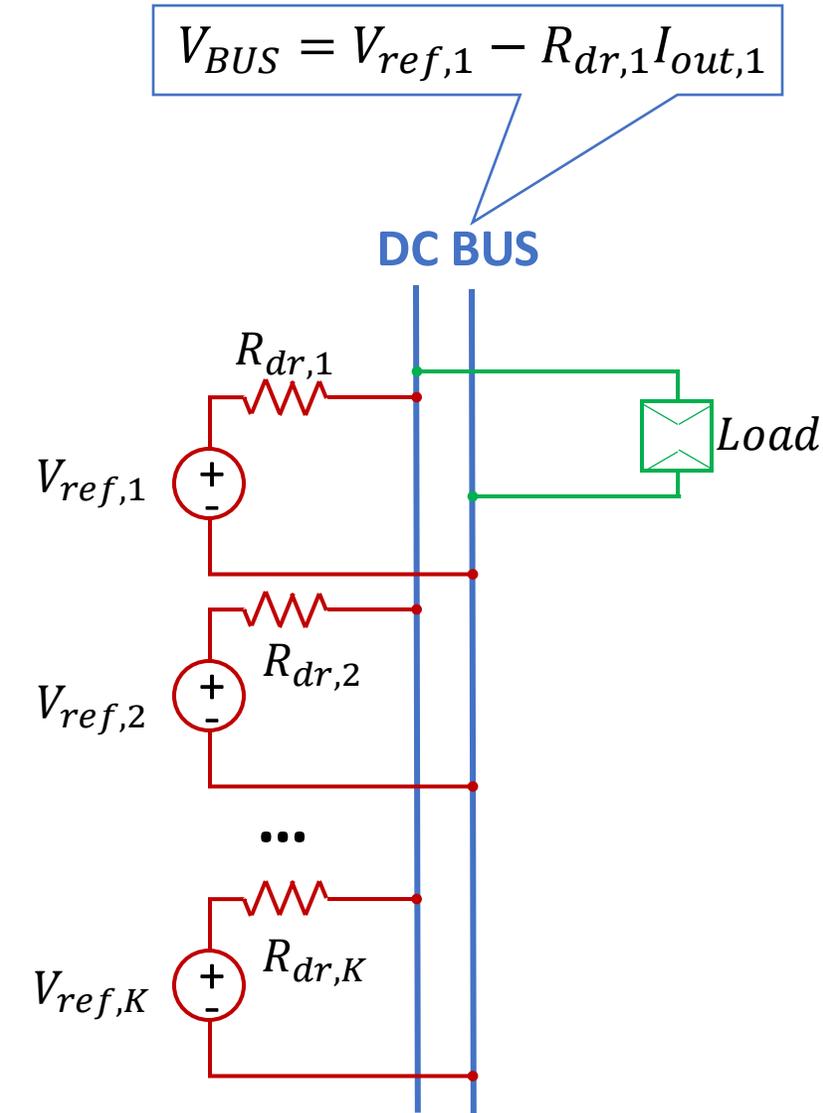
Control. Decentralized control in multiple converter architecture



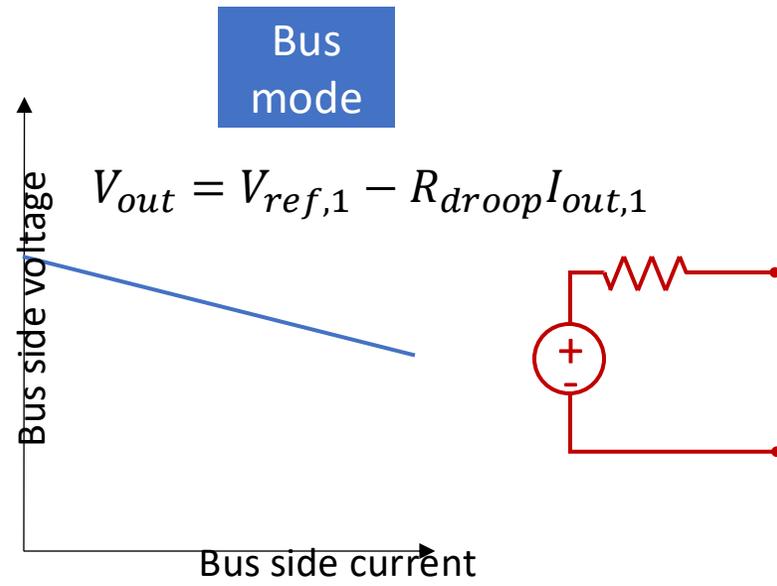
- Typical example in microgrids: droop control
- Droop resistance made by control
- It allows multiple converters connected to the same bus sharing load without any communication among them
- Limitations:
 - Every module provides current to the load according the control law: no power limitation per module
 - All modules regulate cooperatively the bus: no regulation of other quantities are allowed (input side of the module: battery, MPPT,...)



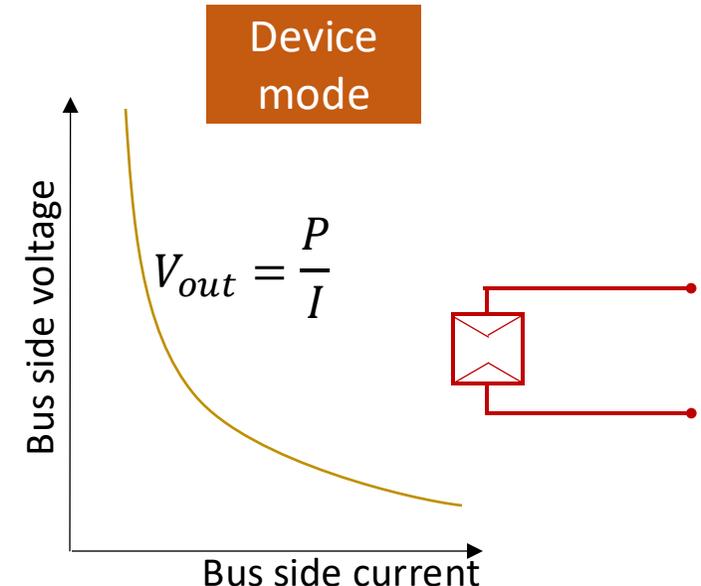
Equivalent circuit for module n



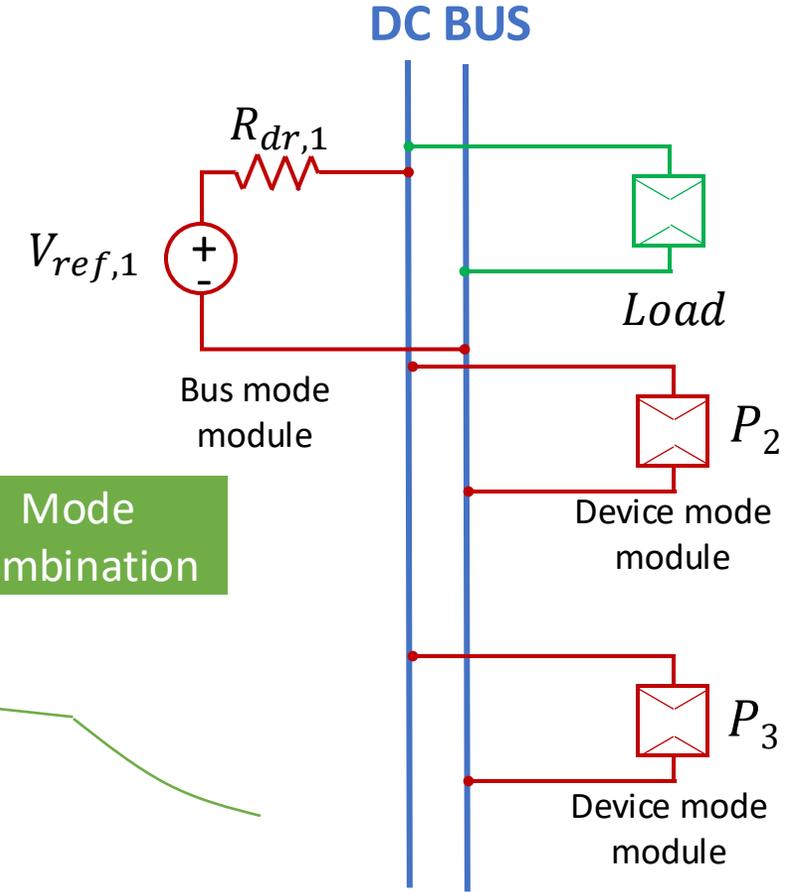
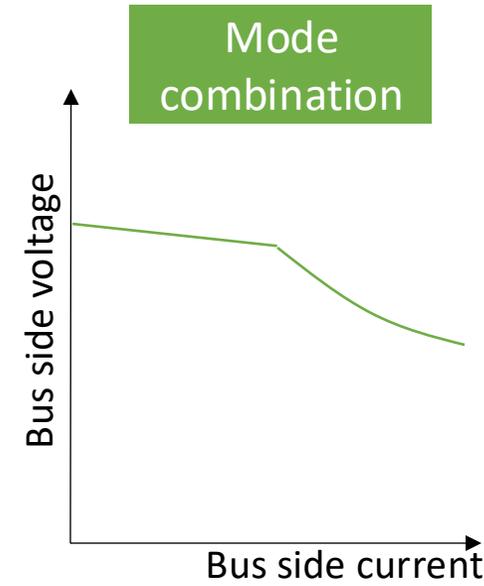
- Depending on the bus voltage, the modules have different operating modes:
 - Bus mode \rightarrow voltage sources + Rdroop (source or load)
 - Device mode \rightarrow regulates voltage or current at its no-bus side (device side)
- At least one module in bus mode to regulate bus voltage



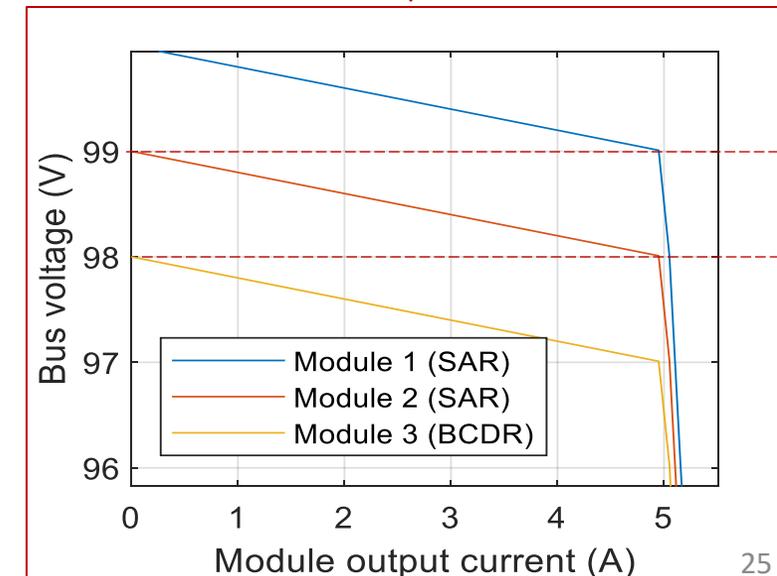
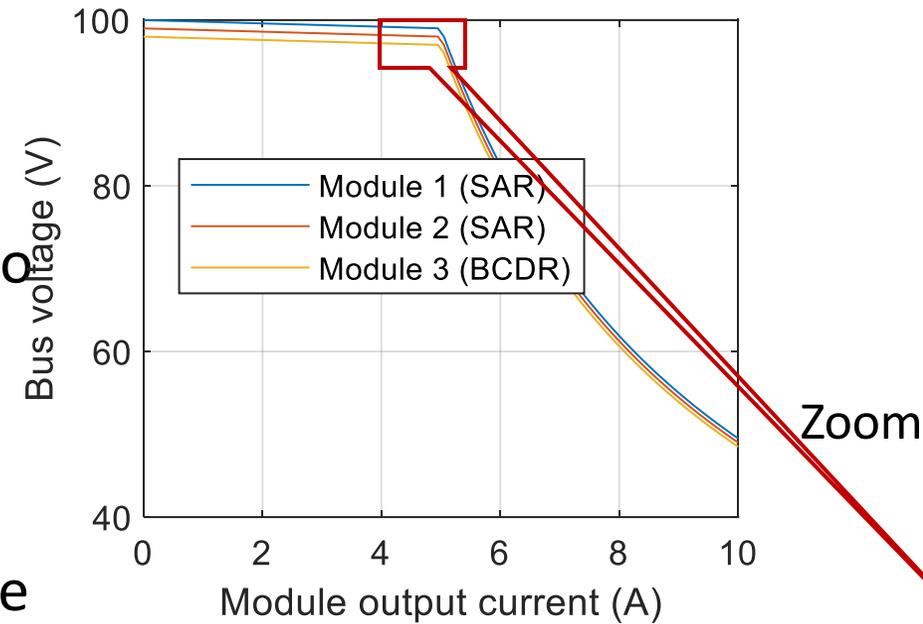
It regulates bus side voltage



It regulates device side current



- Every module has a slightly different bus reference voltage
- Only one module regulates the bus
- SAR modules priority vs. Battery modules to deliver power to the load
- SAR modules have the higher reference voltages
- When a module has a bus reference voltage lower than the actual bus voltage, it delivers the minimum output current: 0A for SAR, 0A or negative current for BCR
- When a given module reaches its maximum output current, it enters device mode

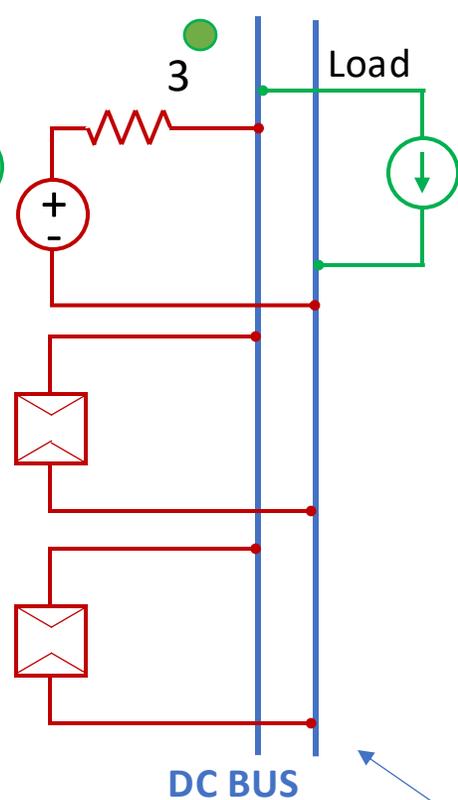
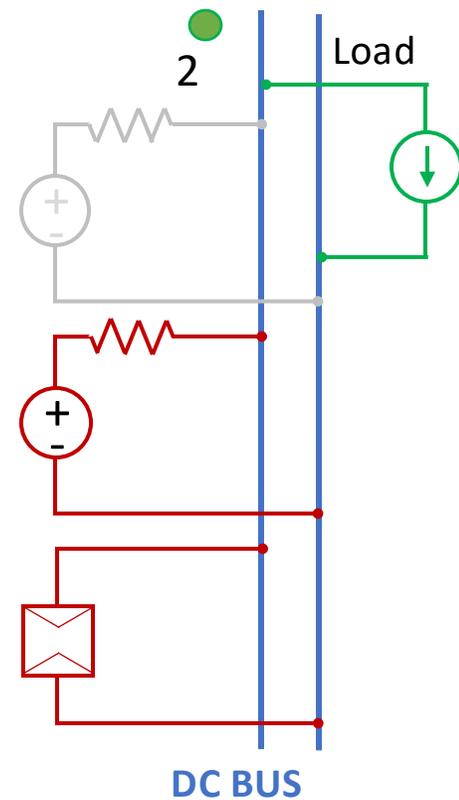
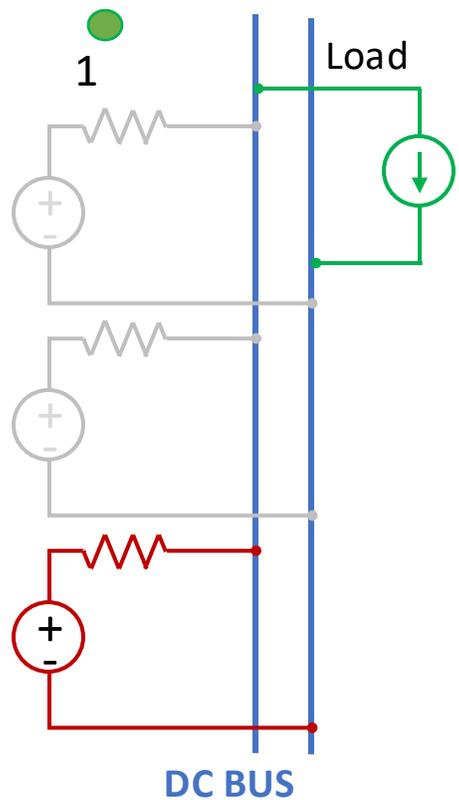


DC-Bus Signaling: A Distributed Control Strategy
for a Hybrid Renewable Nanogrid

John Schönberger, *Student Member, IEEE*, Richard Duke, *Member, IEEE*, and
Simon D. Round, *Senior Member, IEEE*

Control. Example of DC bus signalling

MODULE 1
MODULE 2
MODULE 3



Light load:

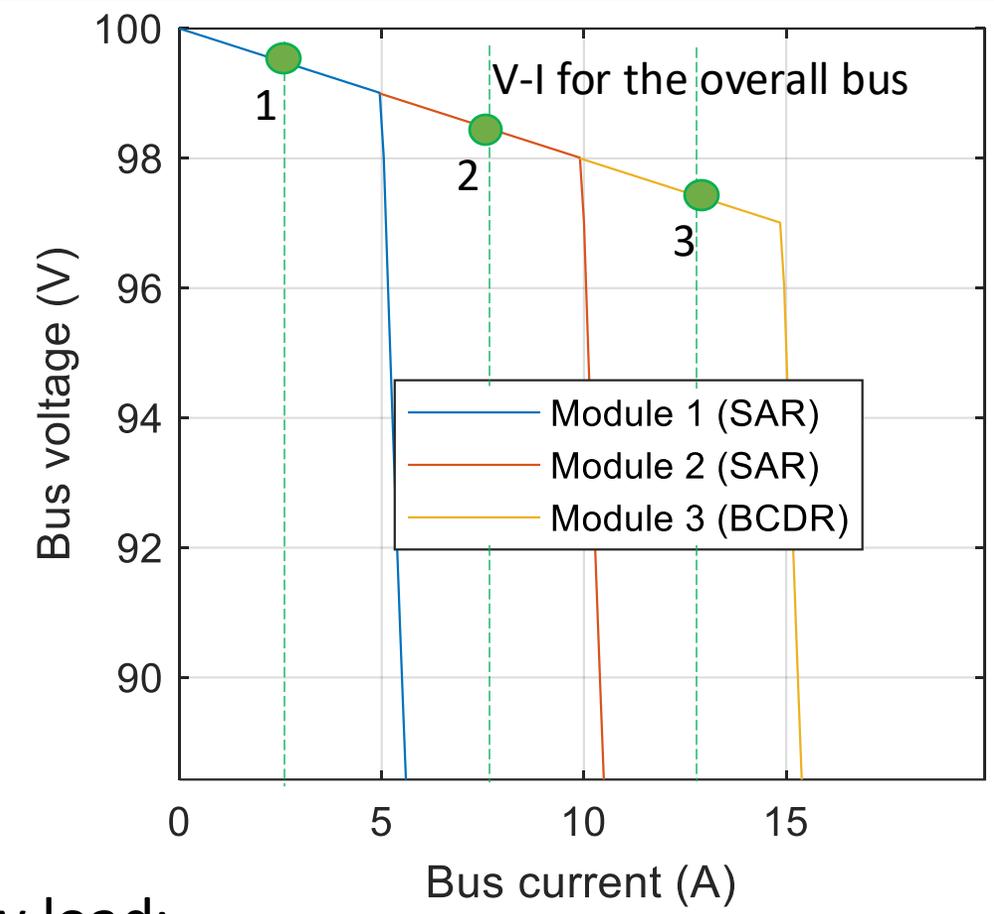
- Module 1 provides the load power → bus mode

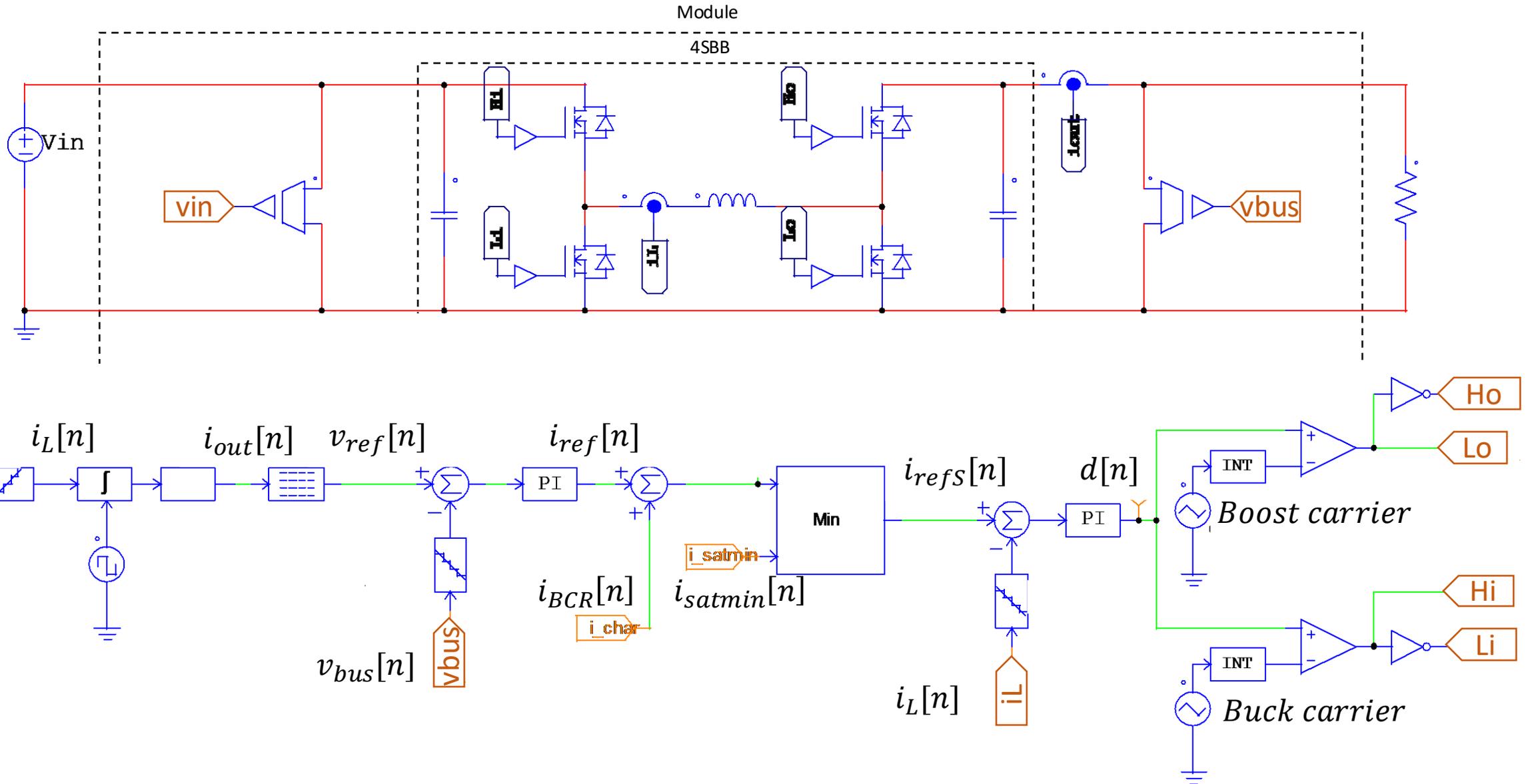
Medium load:

- Module 1 reached its maximum power → device mode
- Module 2 regulates the bus and provides the required extra power → bus mode

Heavy load:

- Modules 1 and 2 reached their maximum power → device mode
- Module 3 regulates the bus and provides the required extra power → bus mode

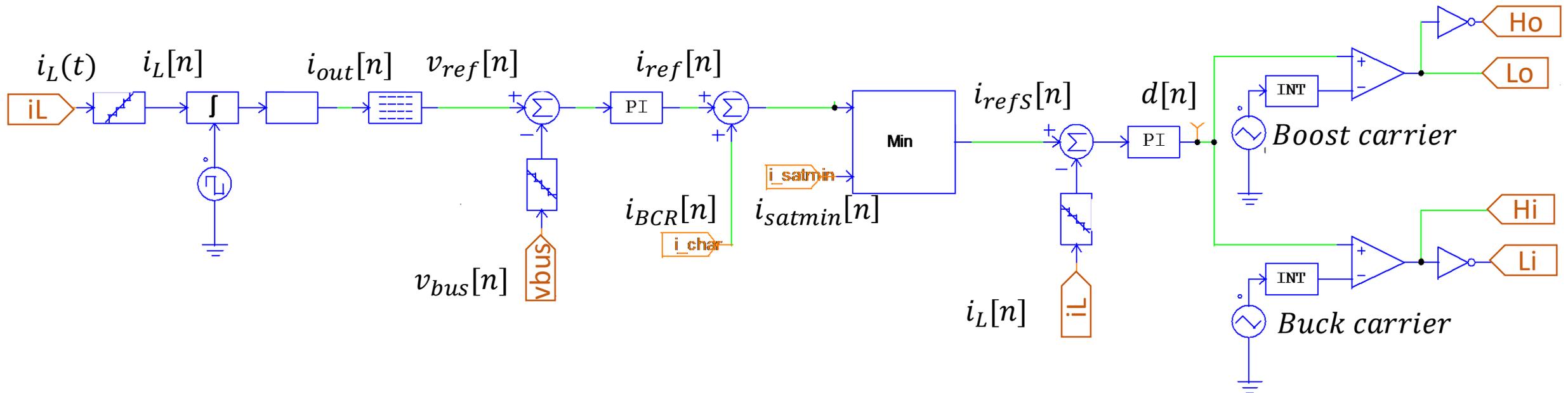




Control. Loop architecture



Output average current calculation DC bus signalling Outer voltage loop Saturator and mode selector Inner current loop Buck-boost DPWM



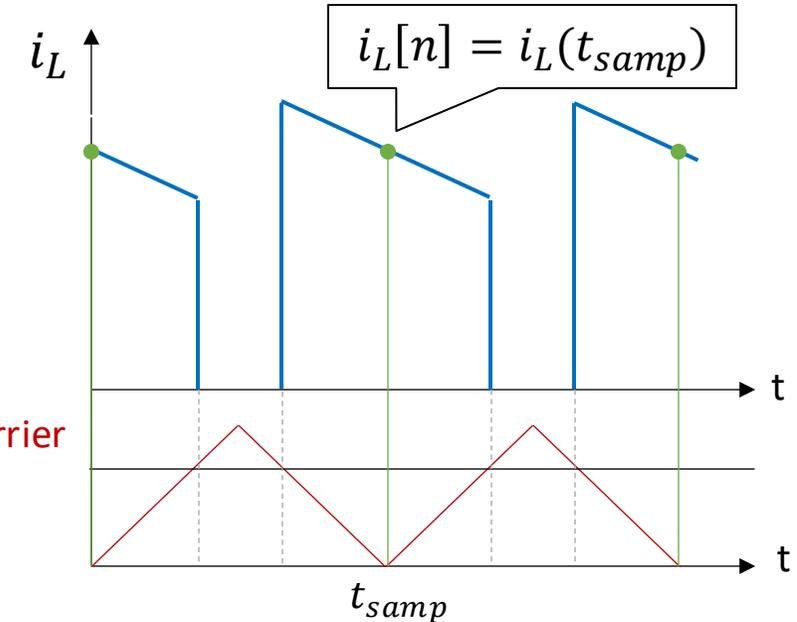
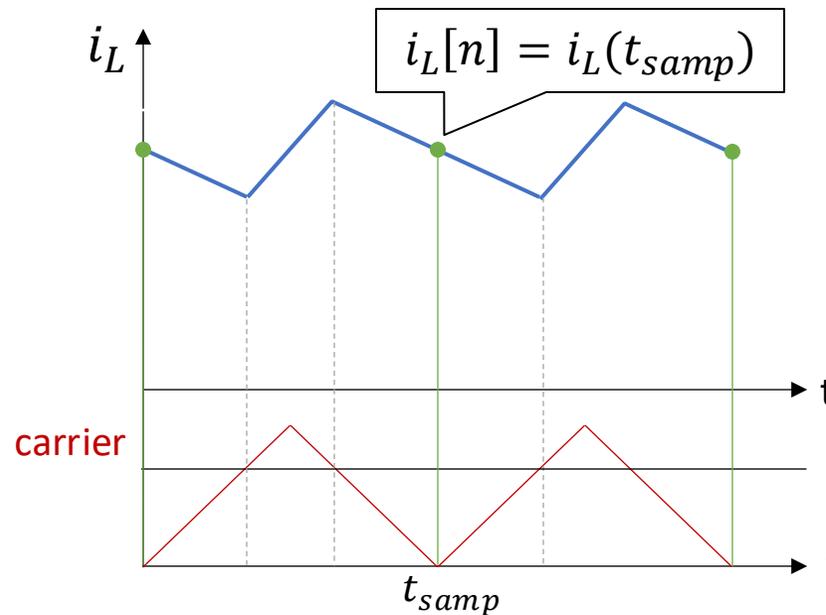
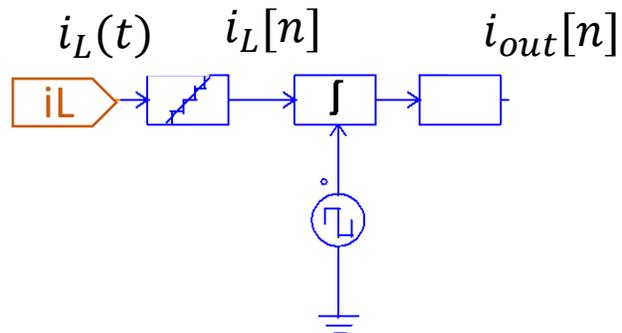
Buck mode

$$i_{out}[n] = i_L[n]$$

Boost mode

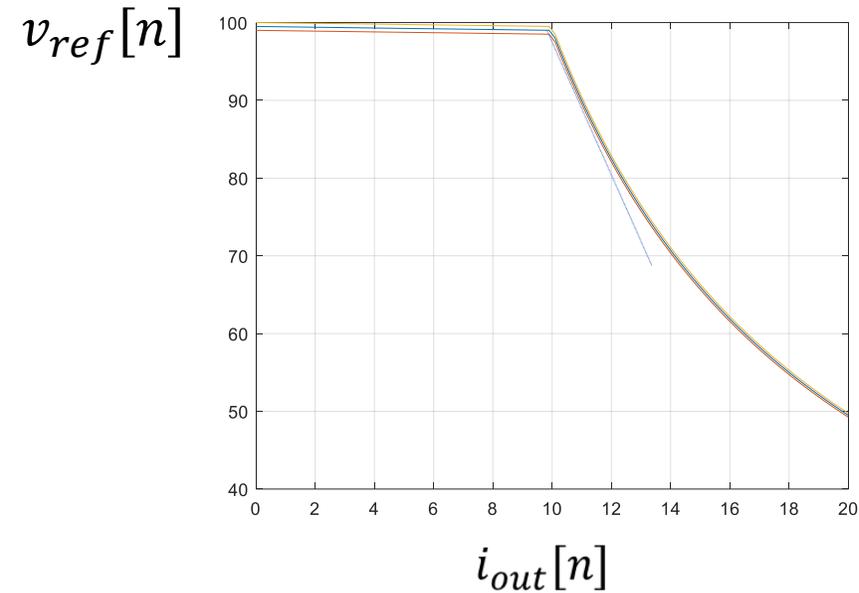
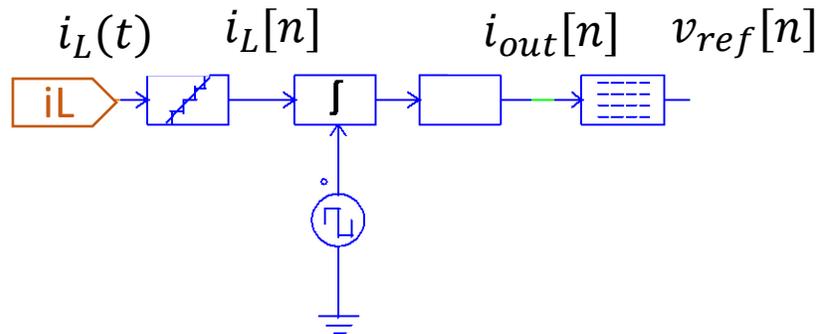
$$i_{out}[n] = i_L[n] \cdot (1 - d[n])$$

Output average current calculation



The output voltage is calculated from the sampled inductor current
ADC with standard SPI

Output average
current calculation DC bus
signalling

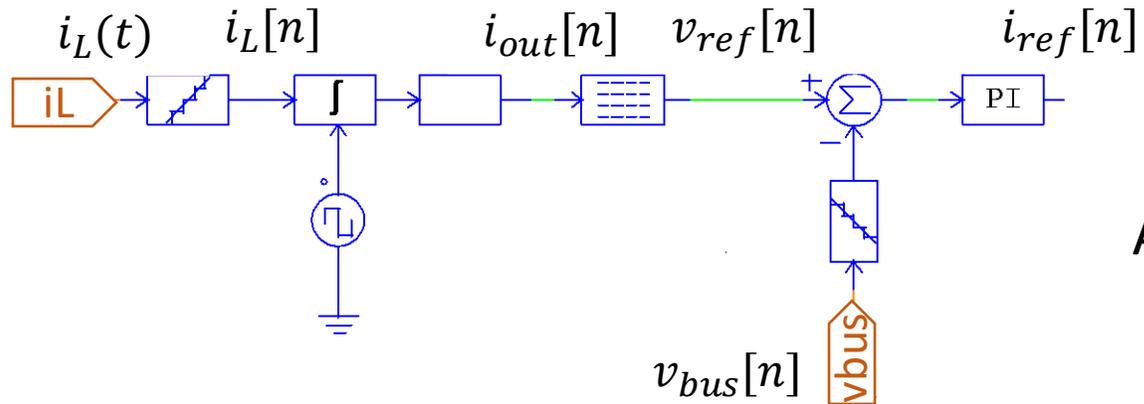


First order approximation to calculate
the voltage reference from the
calculated output current

Control. Outer voltage loop



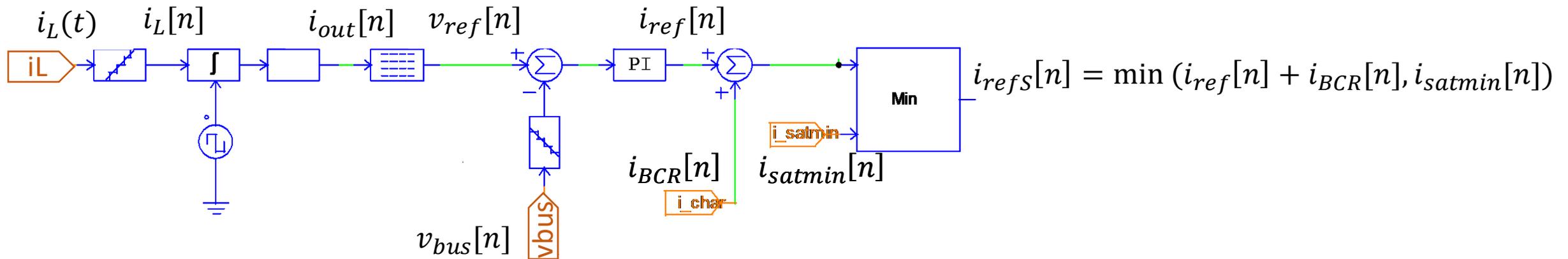
Output average current calculation DC bus signalling Outer voltage loop



Anti wind-up implementation (limits 0 and I_{max})

- The BCR charging reference current is provided by the supervisor using an additional block

Output average current calculation DC bus signalling Outer voltage loop Saturator and mode selector



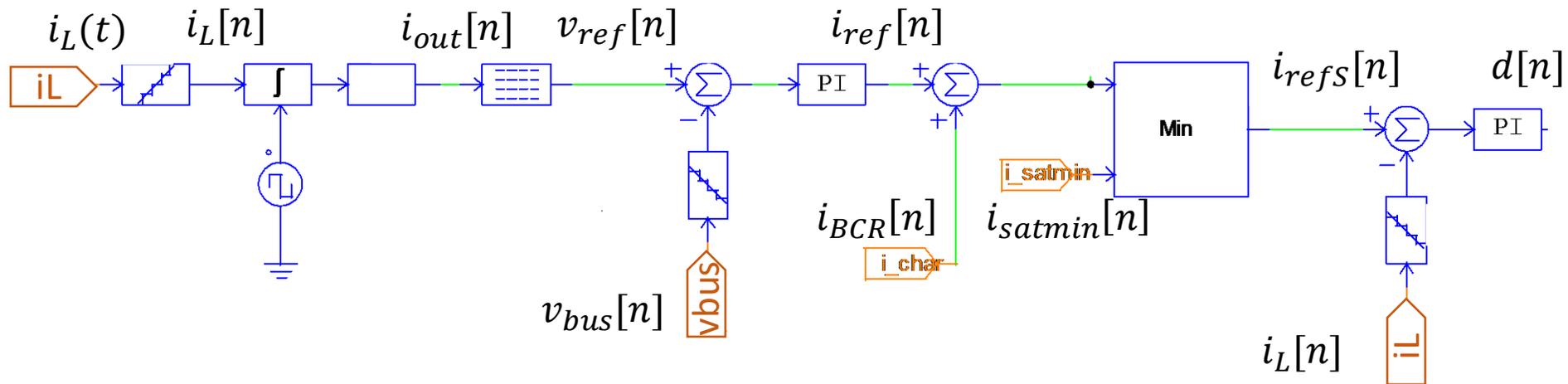
BCDR operation: $i_{BCR}[n] = \text{charging current reference}; i_{satmin}[n] = I_{max}$

SAR operation: $i_{BCR}[n] = 0; i_{satmin}[n] = i_{MPPT}[n]$

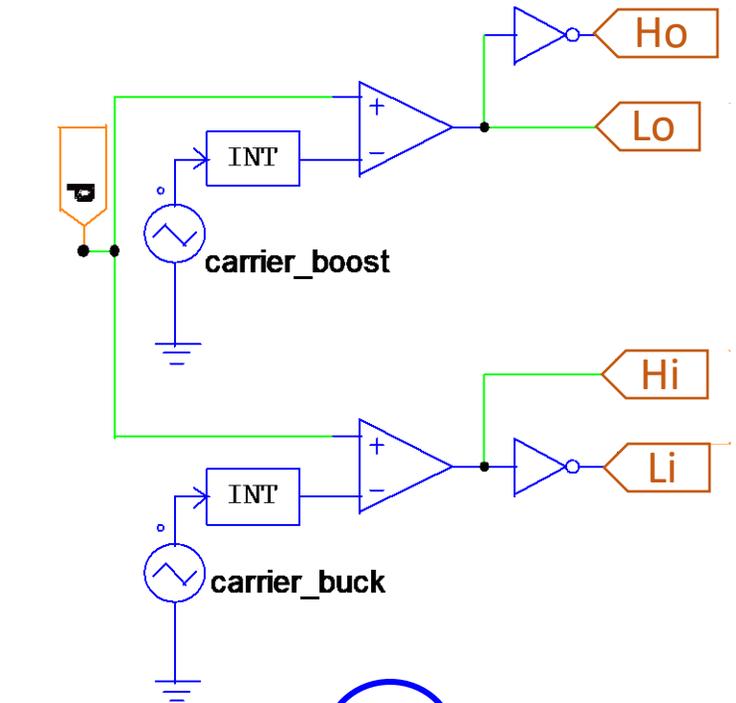
Control. Inner current loop



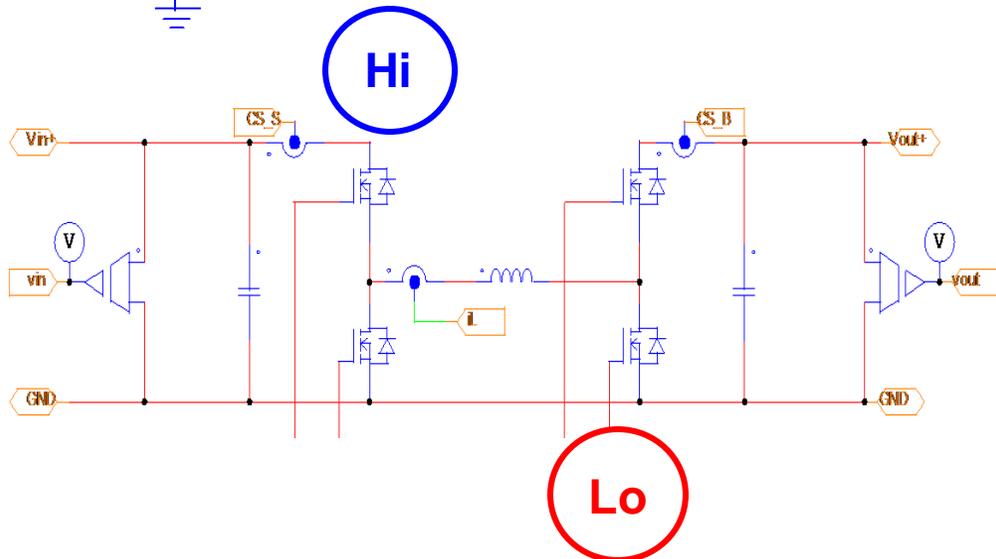
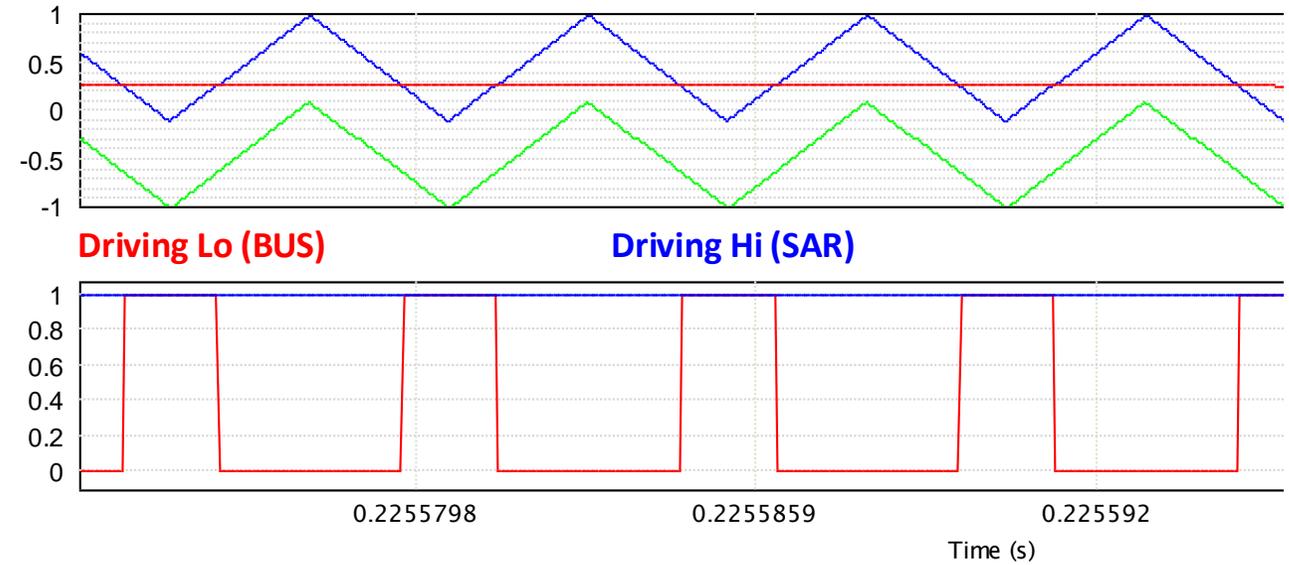
Output average current calculation DC bus signalling Outer voltage loop Saturator and mode selector Inner current loop



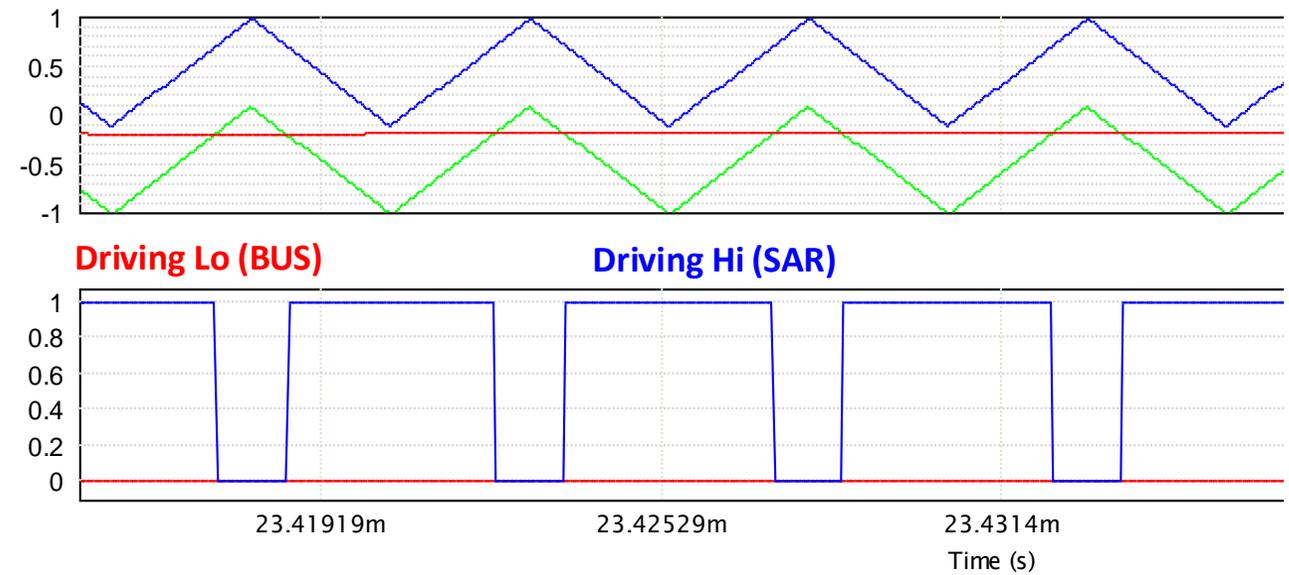
Control. Seamless PWM, buck and boost



Boost: **Control signal** **Carrier buck** **Carrier boost**



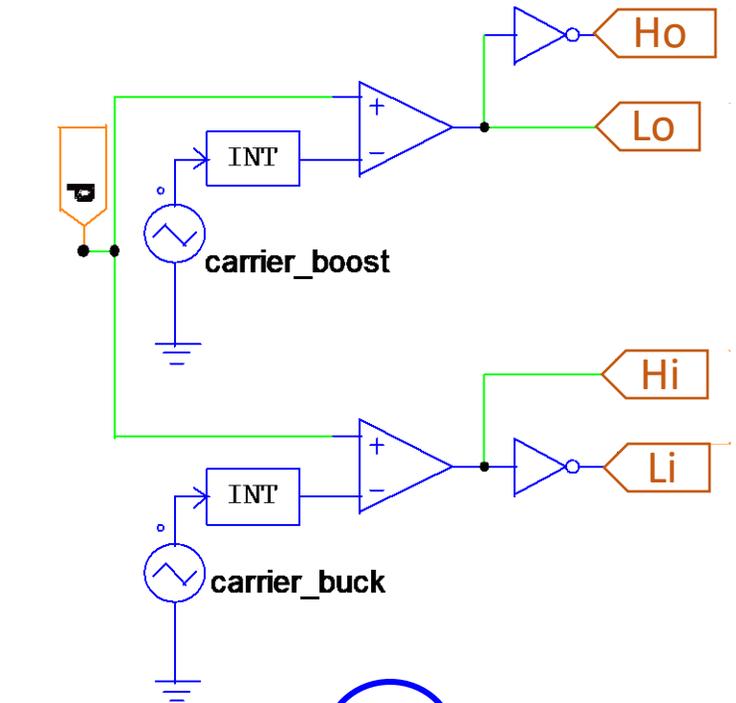
Buck: **Control signal** **Carrier buck** **Carrier boost**



Control. Seamless PWM, transition



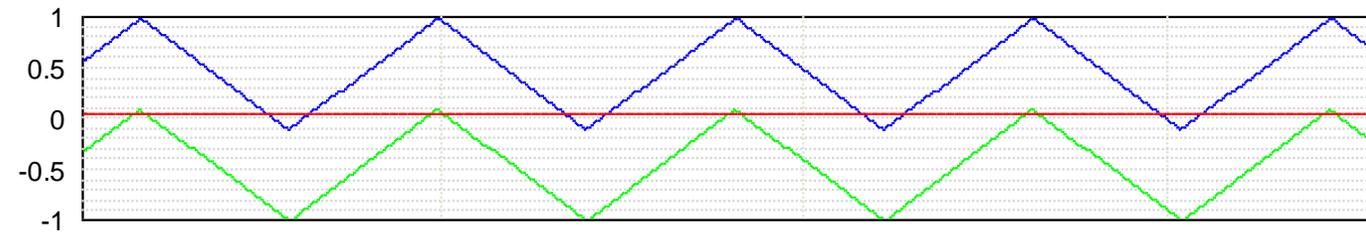
Transition between buck and boost:



Control signal

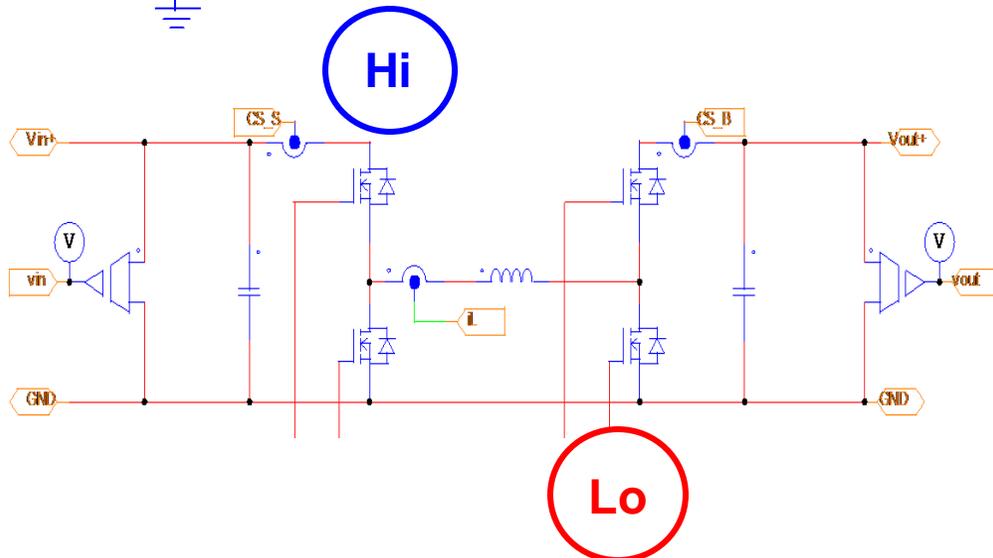
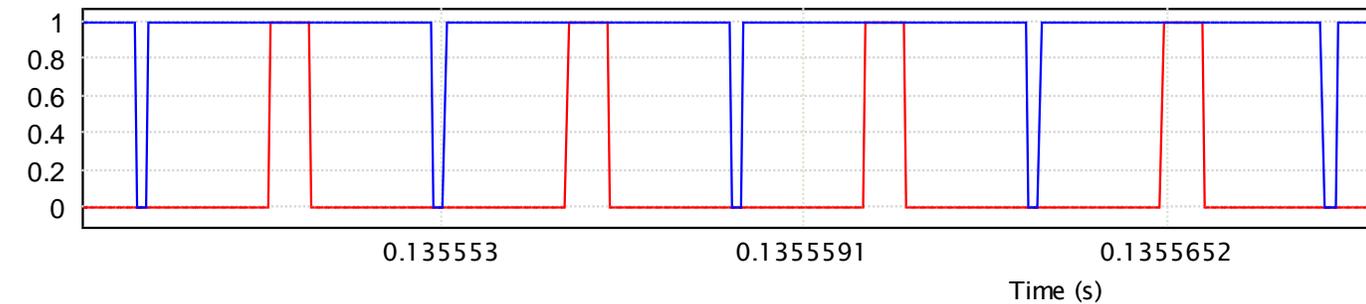
Carrier buck

Carrier boost



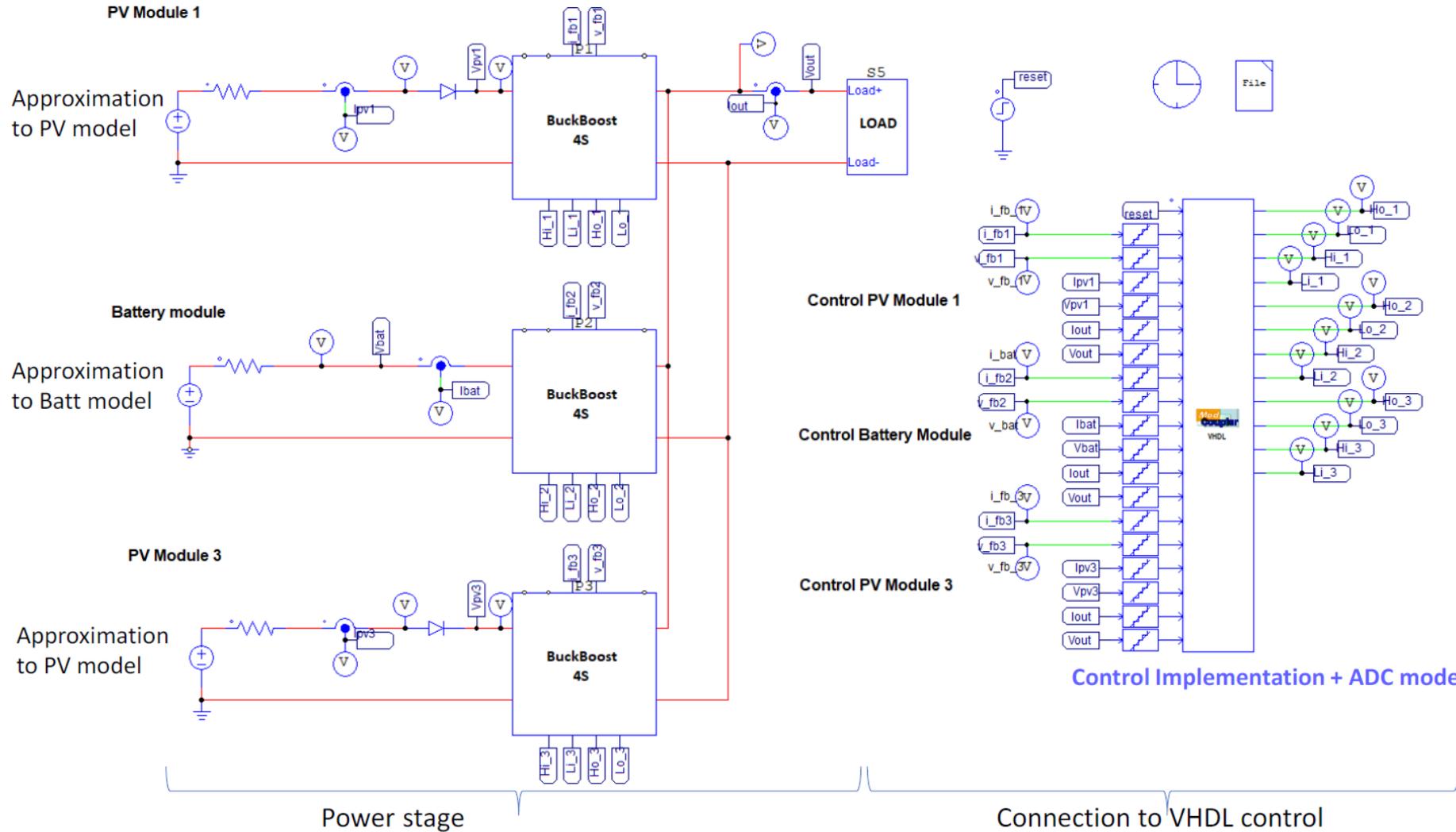
Driving Lo (BUS)

Driving Hi (SAR)



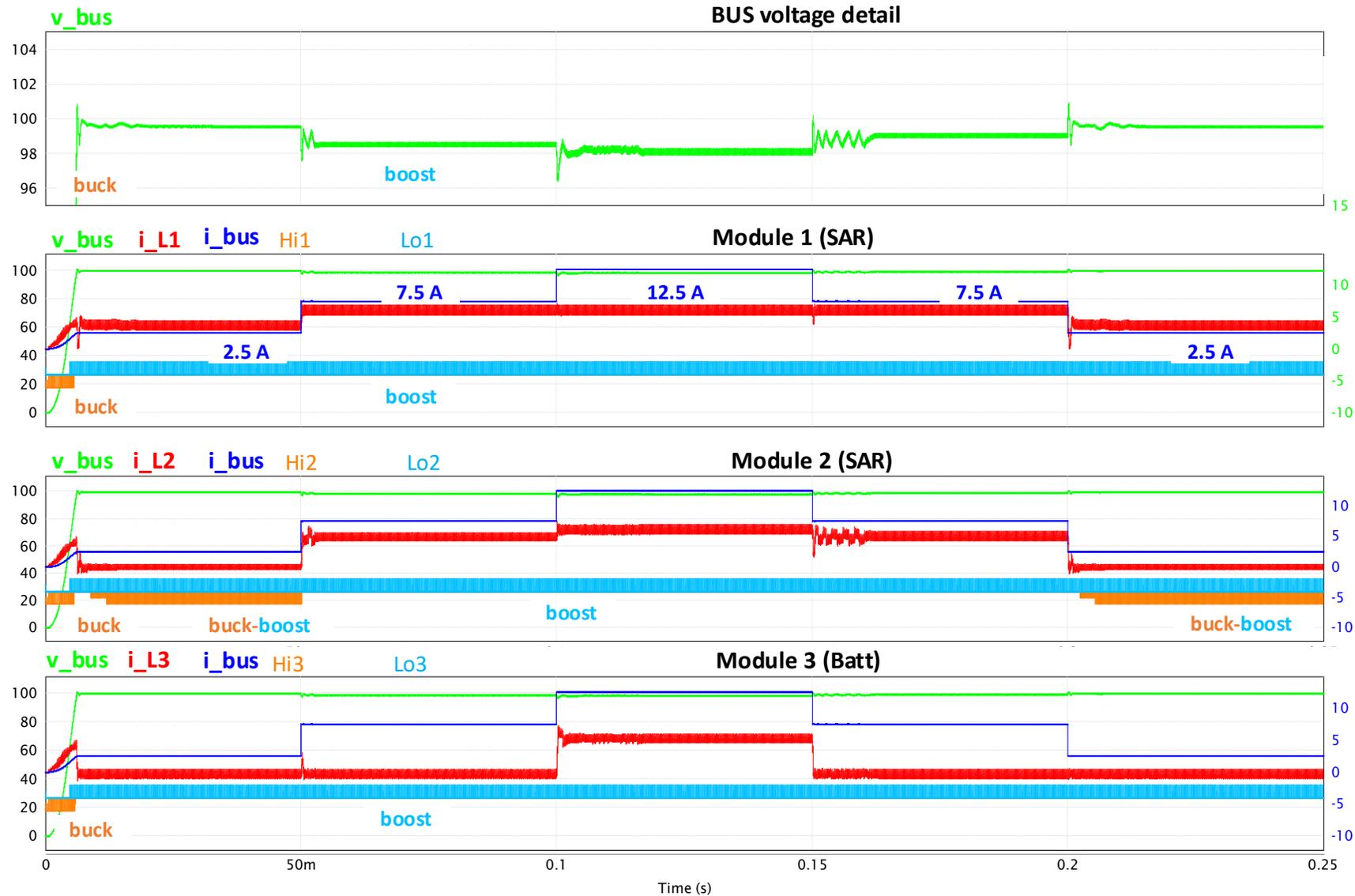
Power stage *PSIM simulator*

Control stage *Modelsim simulator*



- Design debugging using co-simulation PSIM-Modelsim
- All control blocks implemented in VHDL
- Synthesis code included in simulation
- ADC model included in VHDL blocks

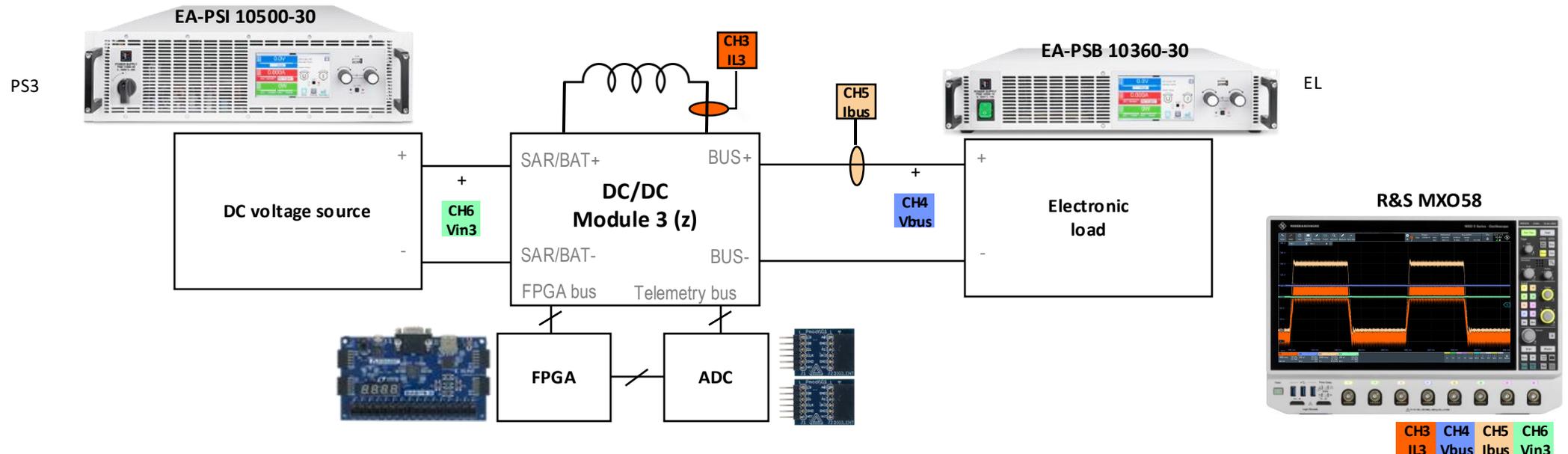
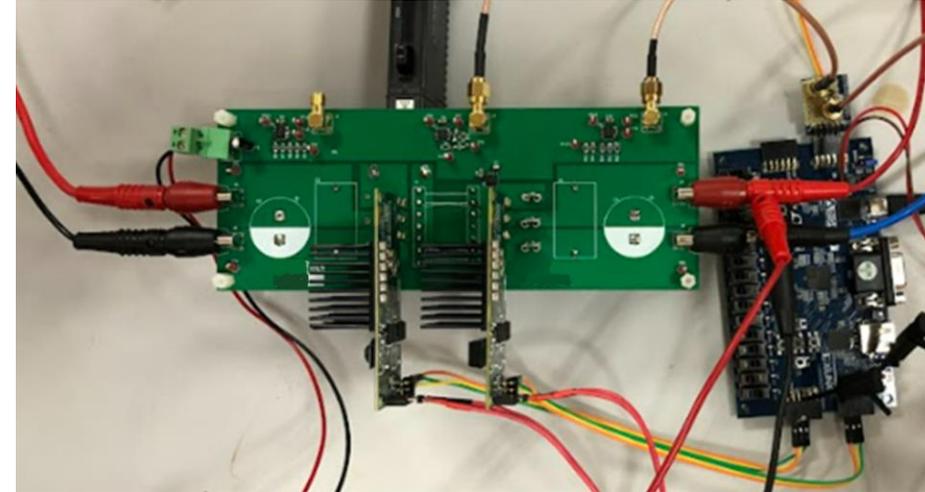
- Cosimulation has been essential to debug the control implementation



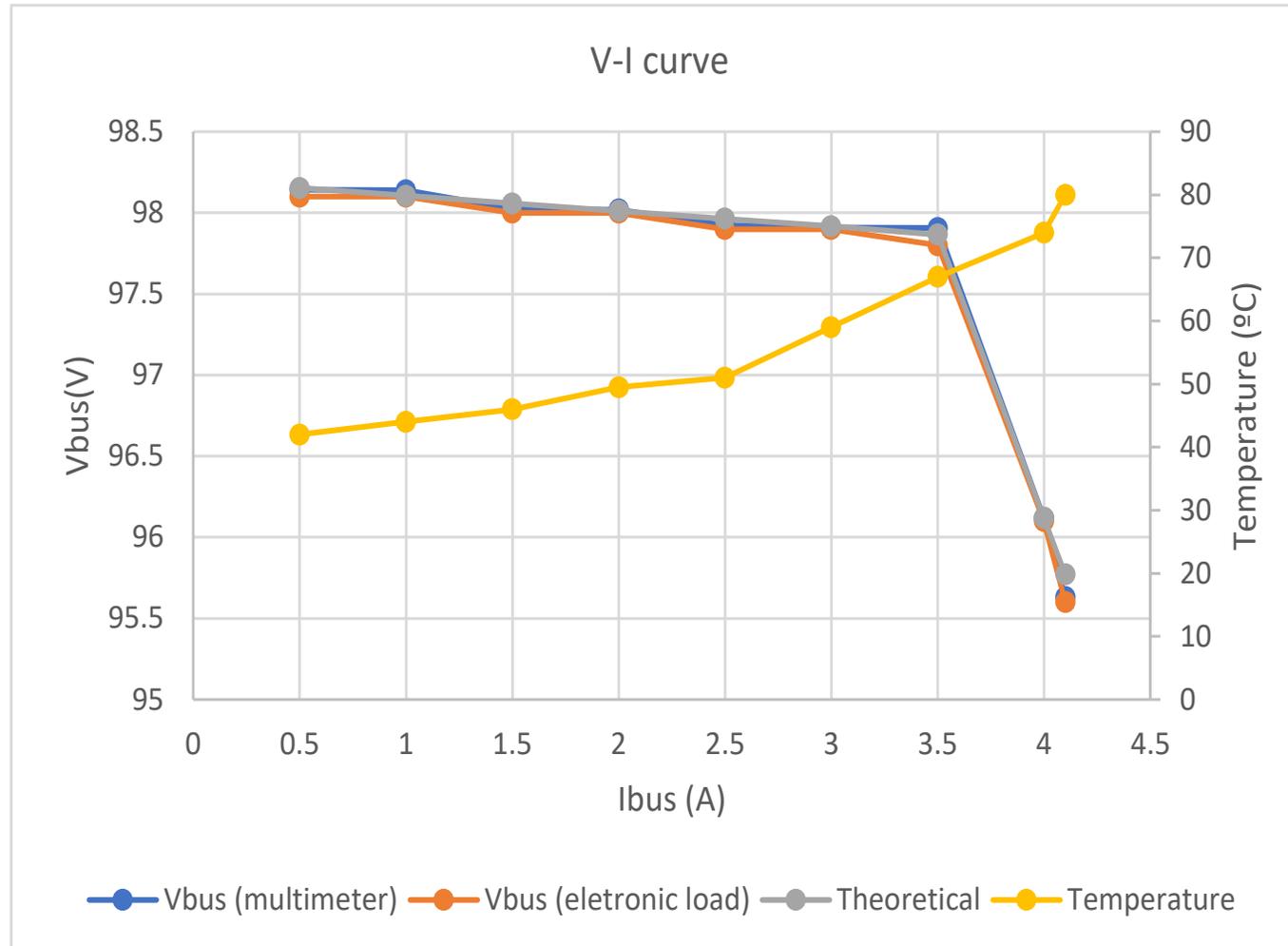
Control. Experimental set-up for single module



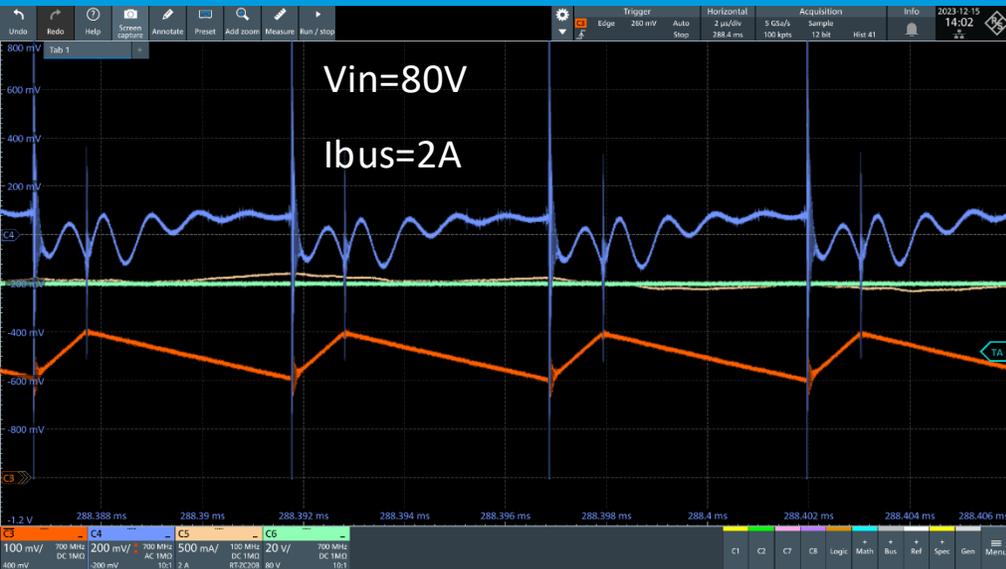
- A simplified power stage has been used:
 - Because of shortage of original GaN modules, replacement for other equivalent
 - No auxiliary circuitry and protections



- V-I curve as expected
 - Droop control and DC bus signalling implemented
 - Admissible temperatura rise

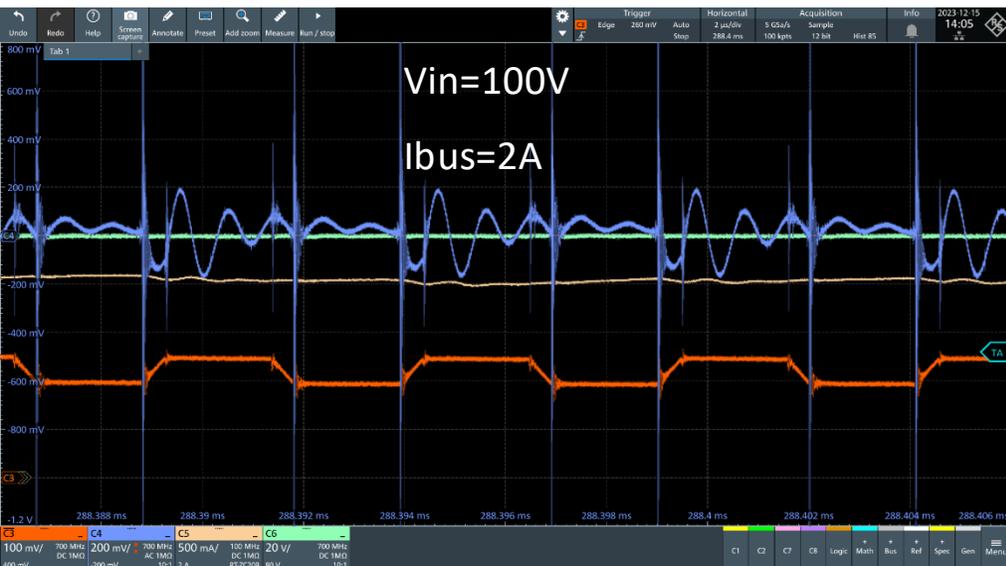


Control. Single module: different input voltages

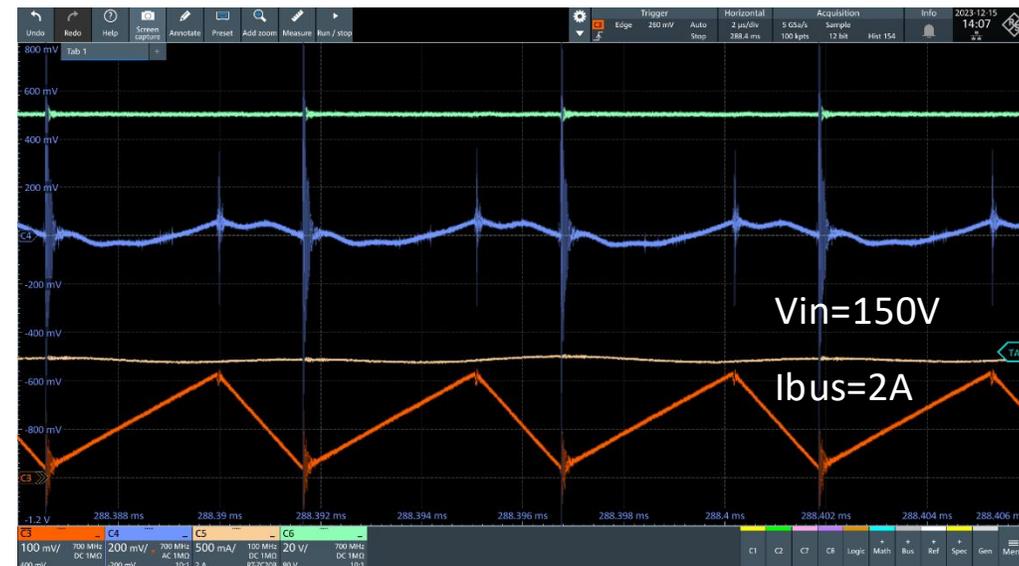


CH3: IL3
CH4: Vbus
CH5: Ibus
CH6: Vin

Different input voltage
Medium bus current
Modulator demonstration

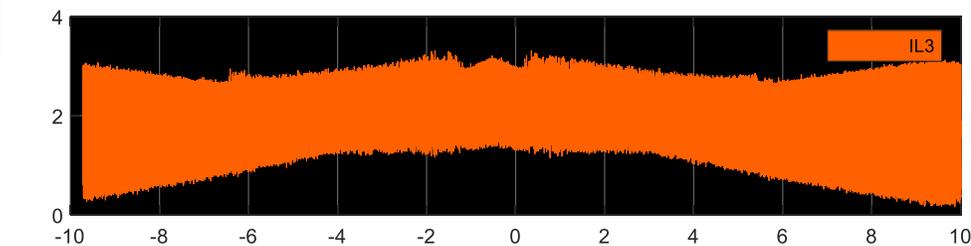
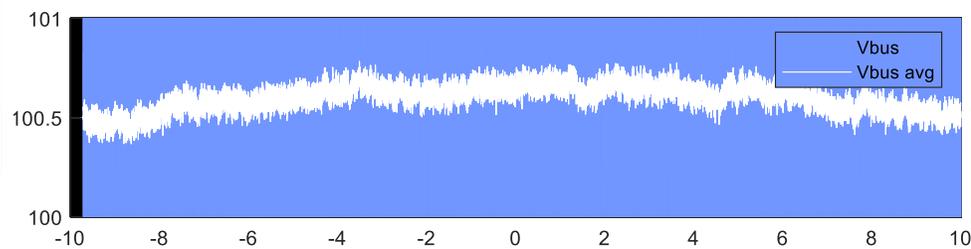
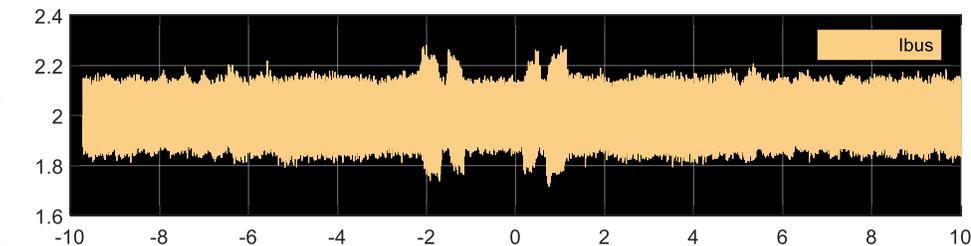
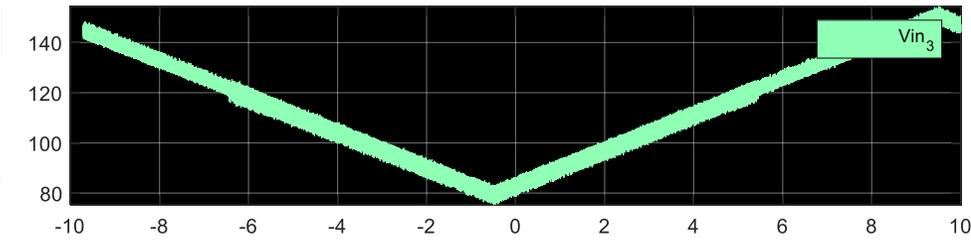
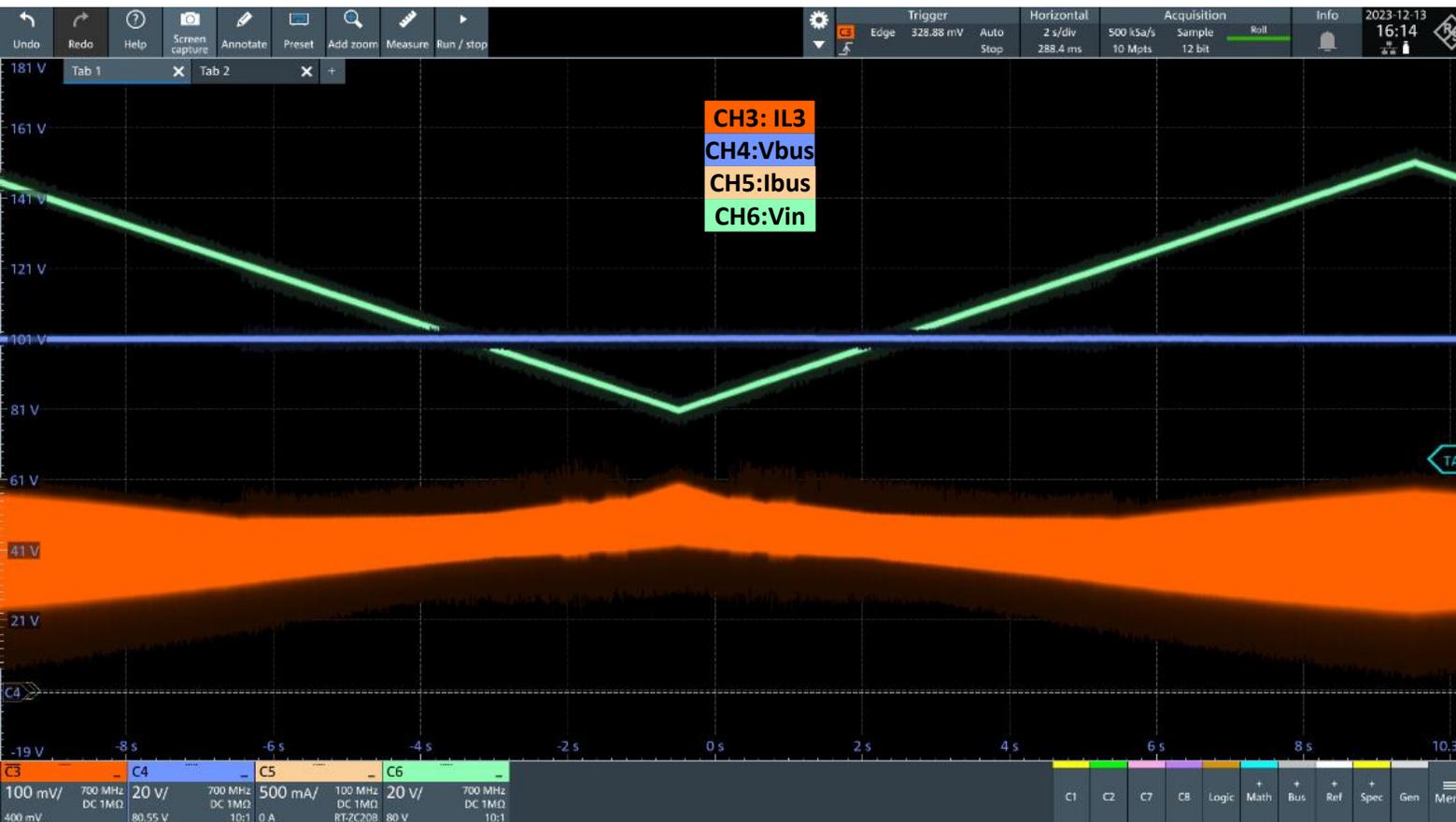


CH3: IL3
CH4: Vbus
CH5: Ibus
CH6: Vin



CH3: IL3
CH4: Vbus
CH5: Ibus
CH6: Vin

Control. Single module: input voltage sweep



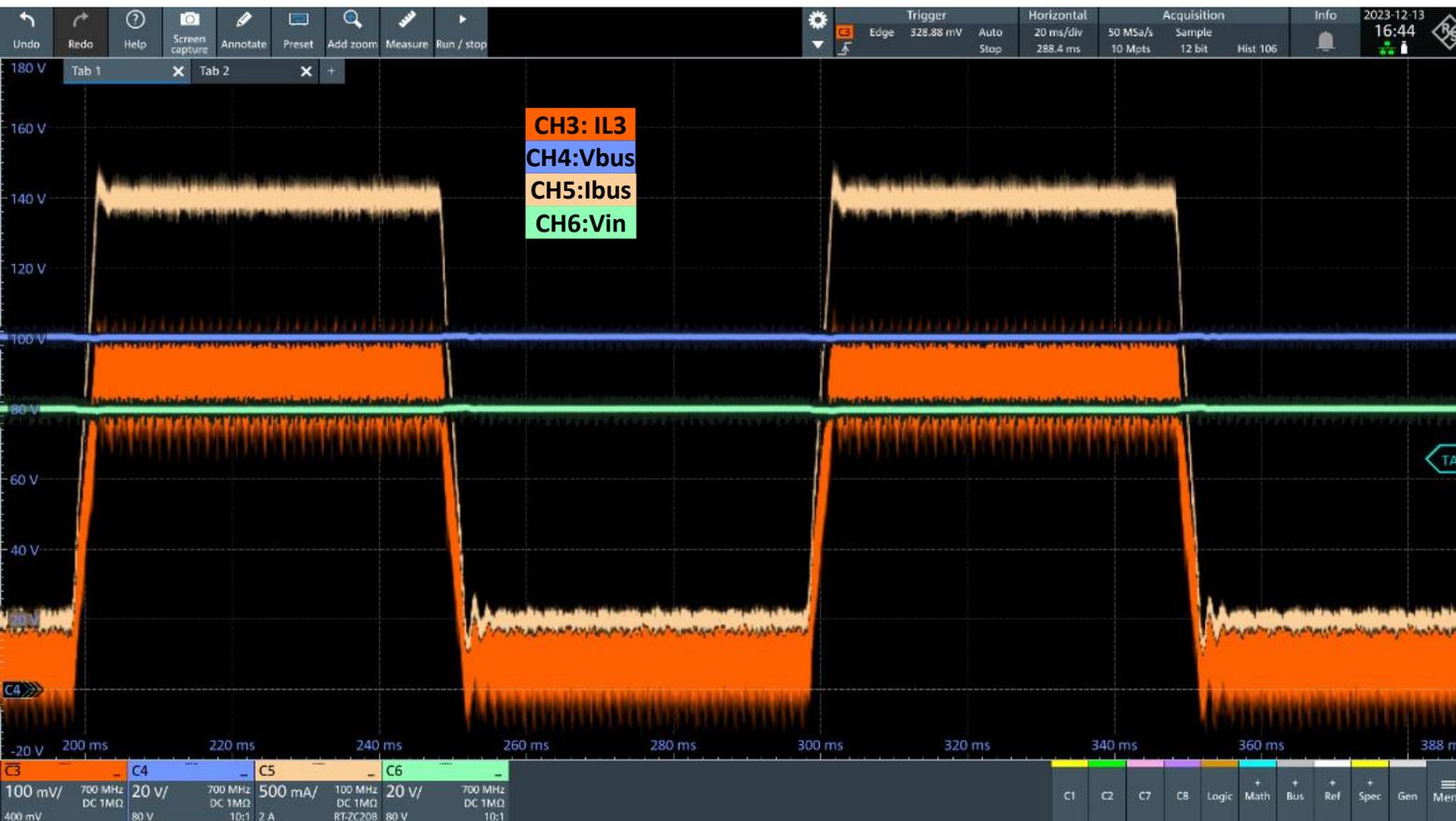
Test C1.7

Vin=80V-150V

Ibus=2A

Bus voltage is properly regulated under input voltage slow variation

Control. Single module: load current steps

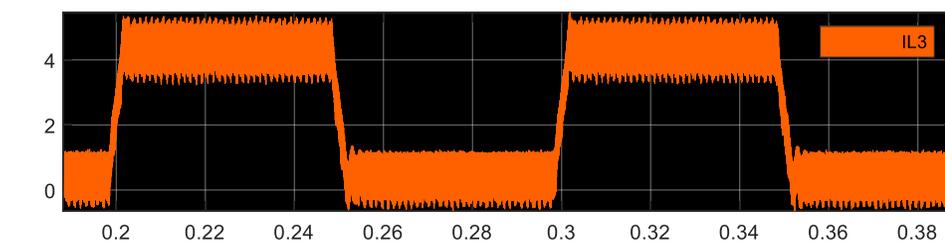
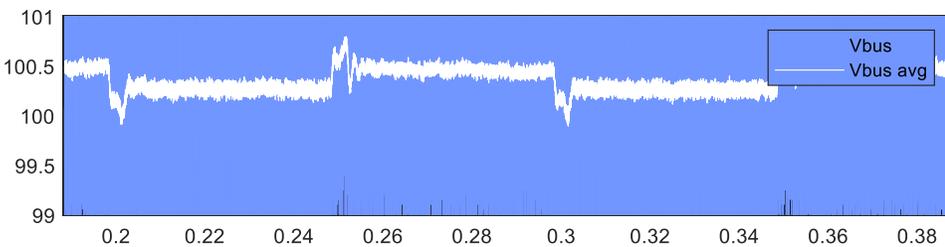
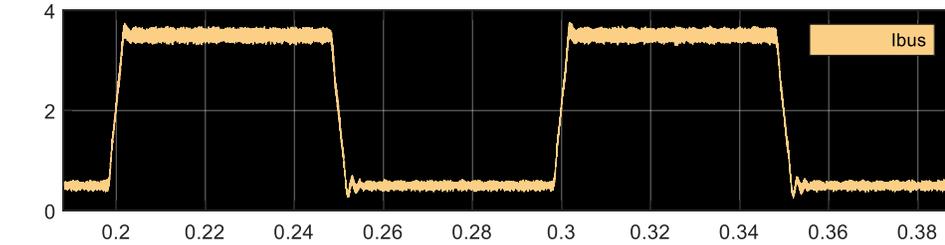
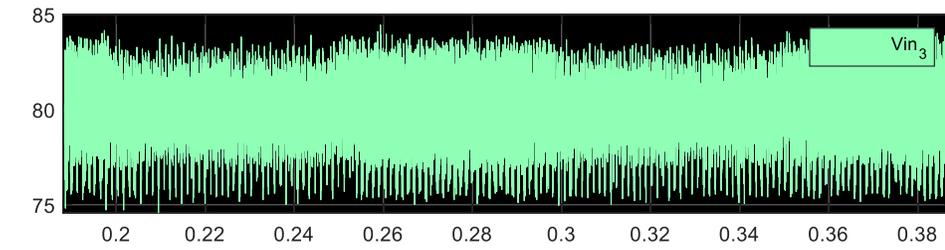


Test C1.12

$V_{in}=80V$

$I_{bus}=0.5A-3.5A$

Bus voltage is properly regulated under current steps (droop effect)



Control. Single module: MPPT

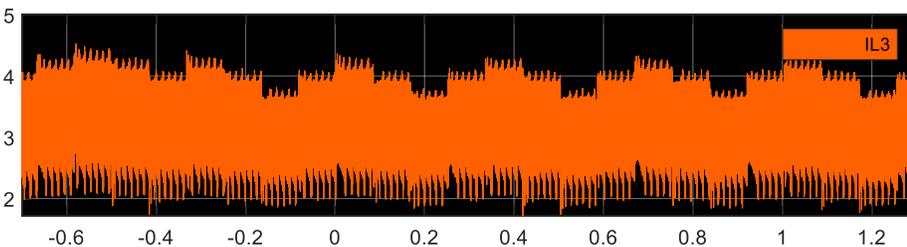
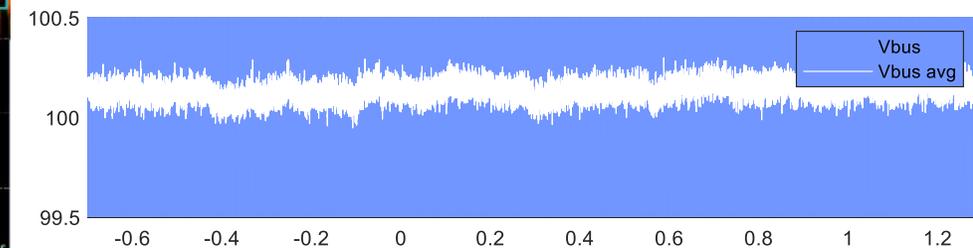
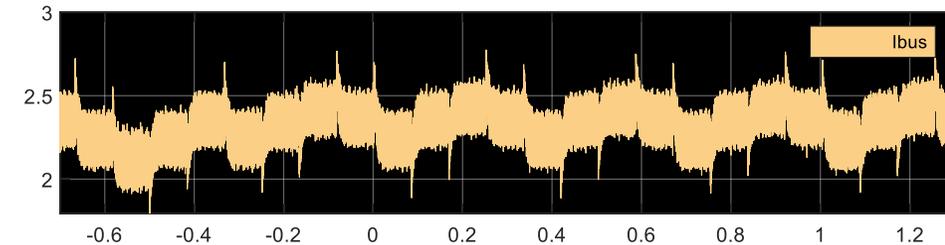
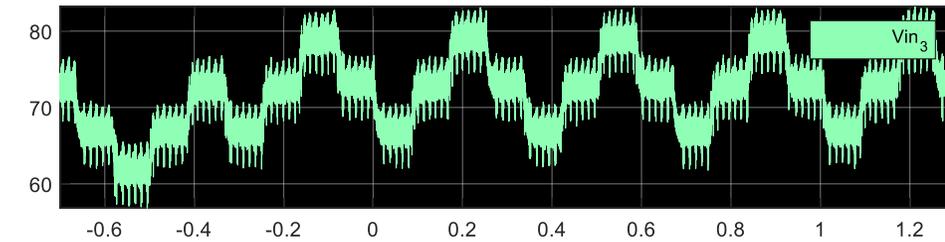


Test C1.16

Vin=PV panel emulator (MP=240W)

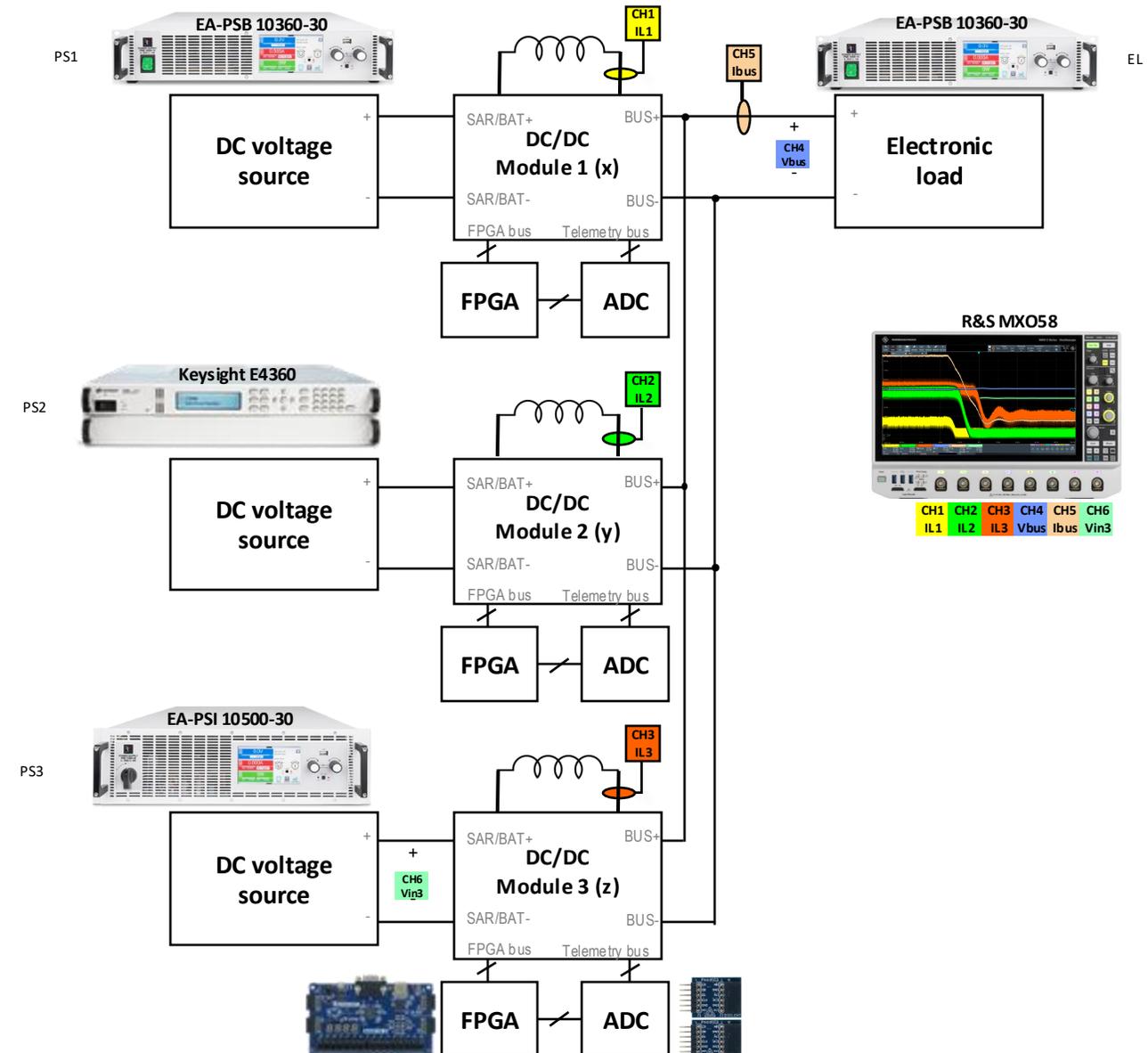
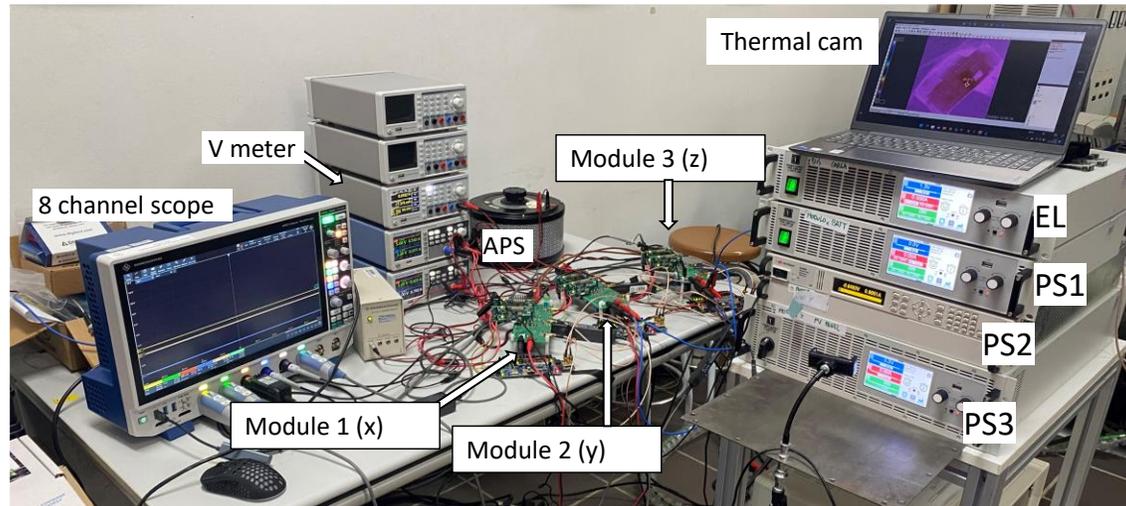
Vbus=100V (regulated by the load)

MPPT produces expected input voltage variations

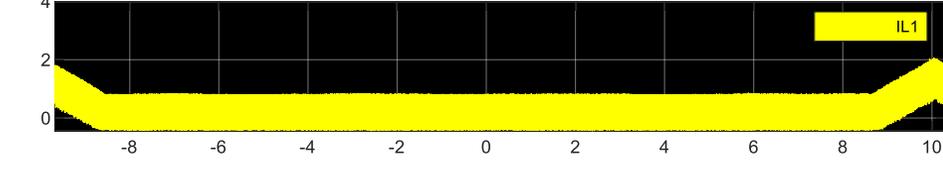
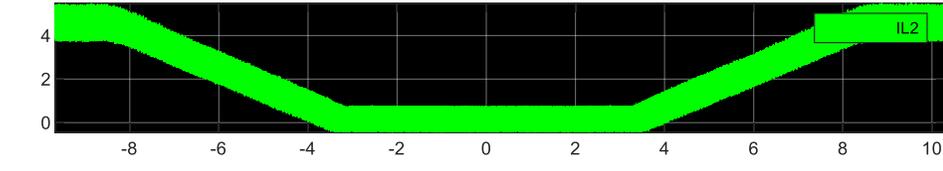
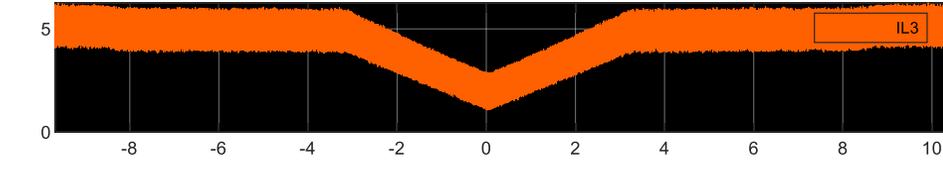
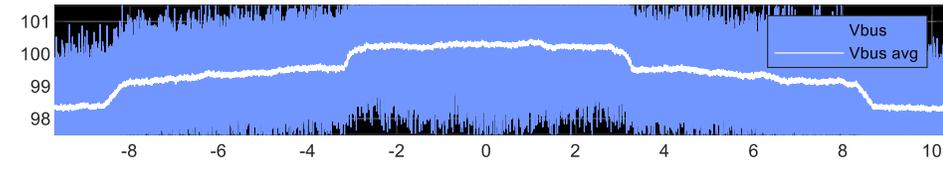
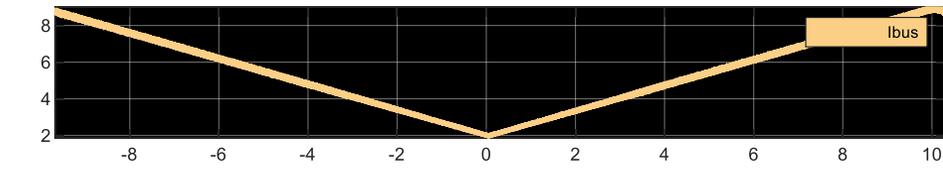
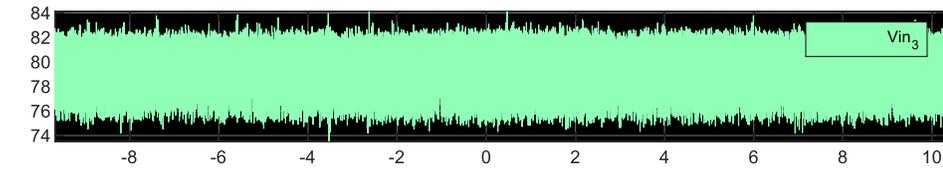
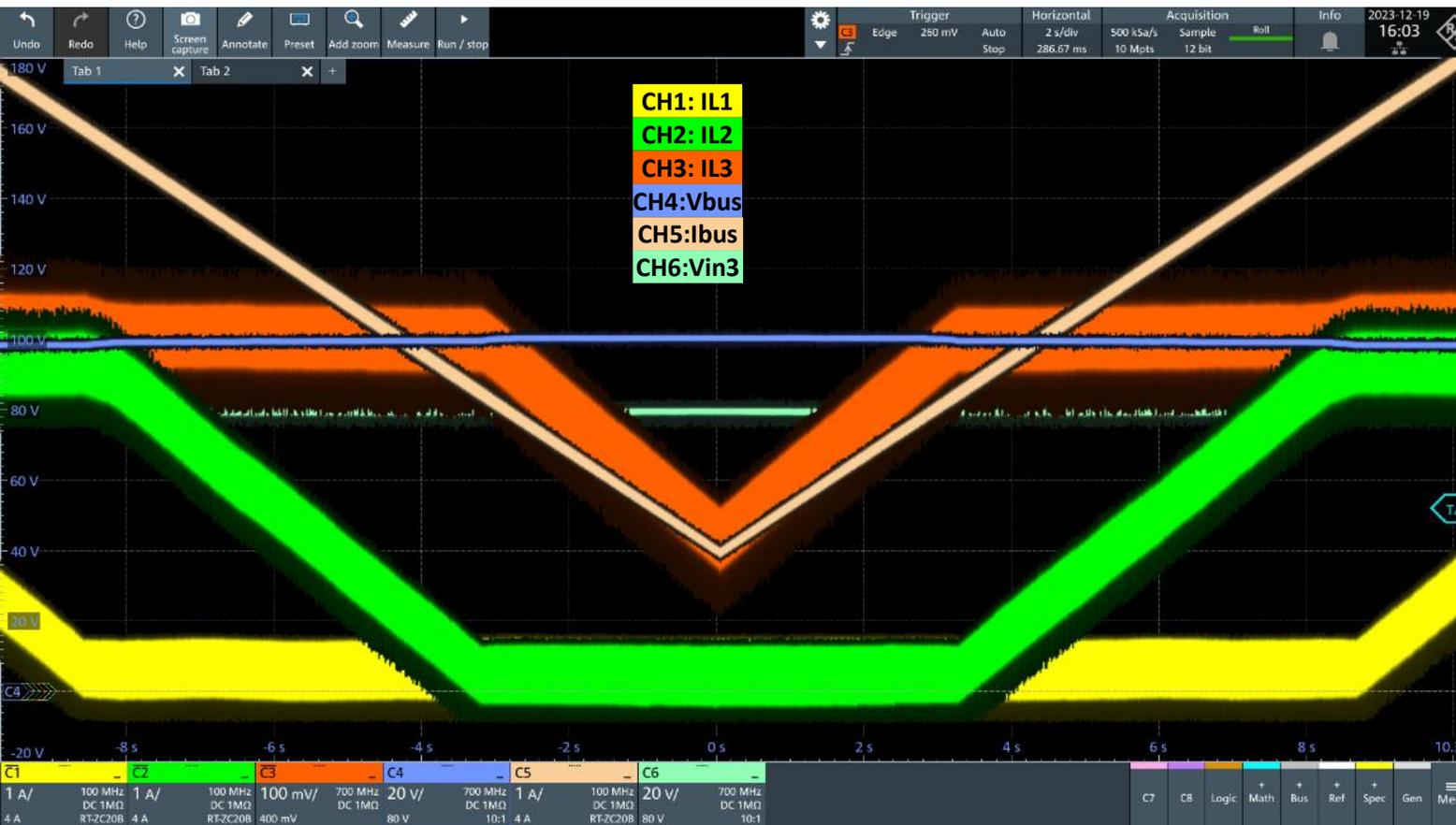


Control. Three module set-up

- Every module has the same power stage and control stage
- Minimum control configuration made by external signals (switches)
- Simplified DC/DC modules



Control. Three module: bus current sweep



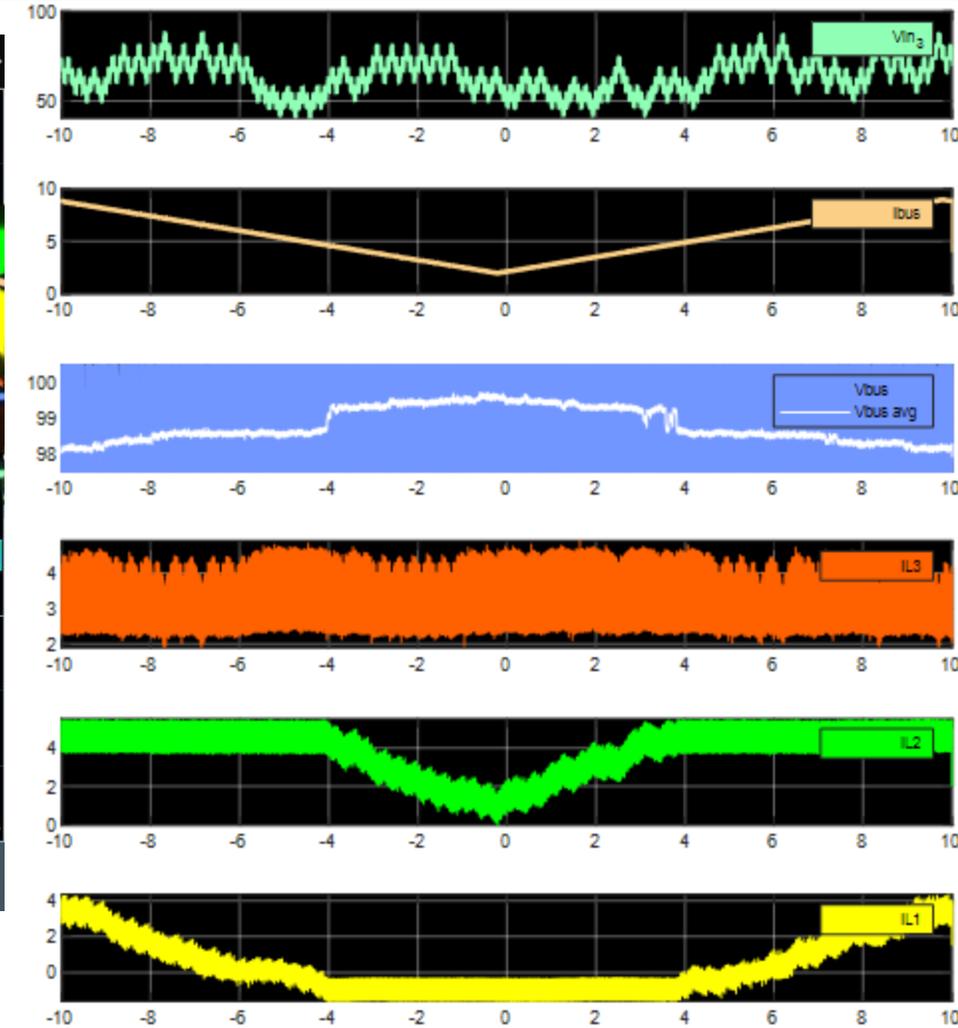
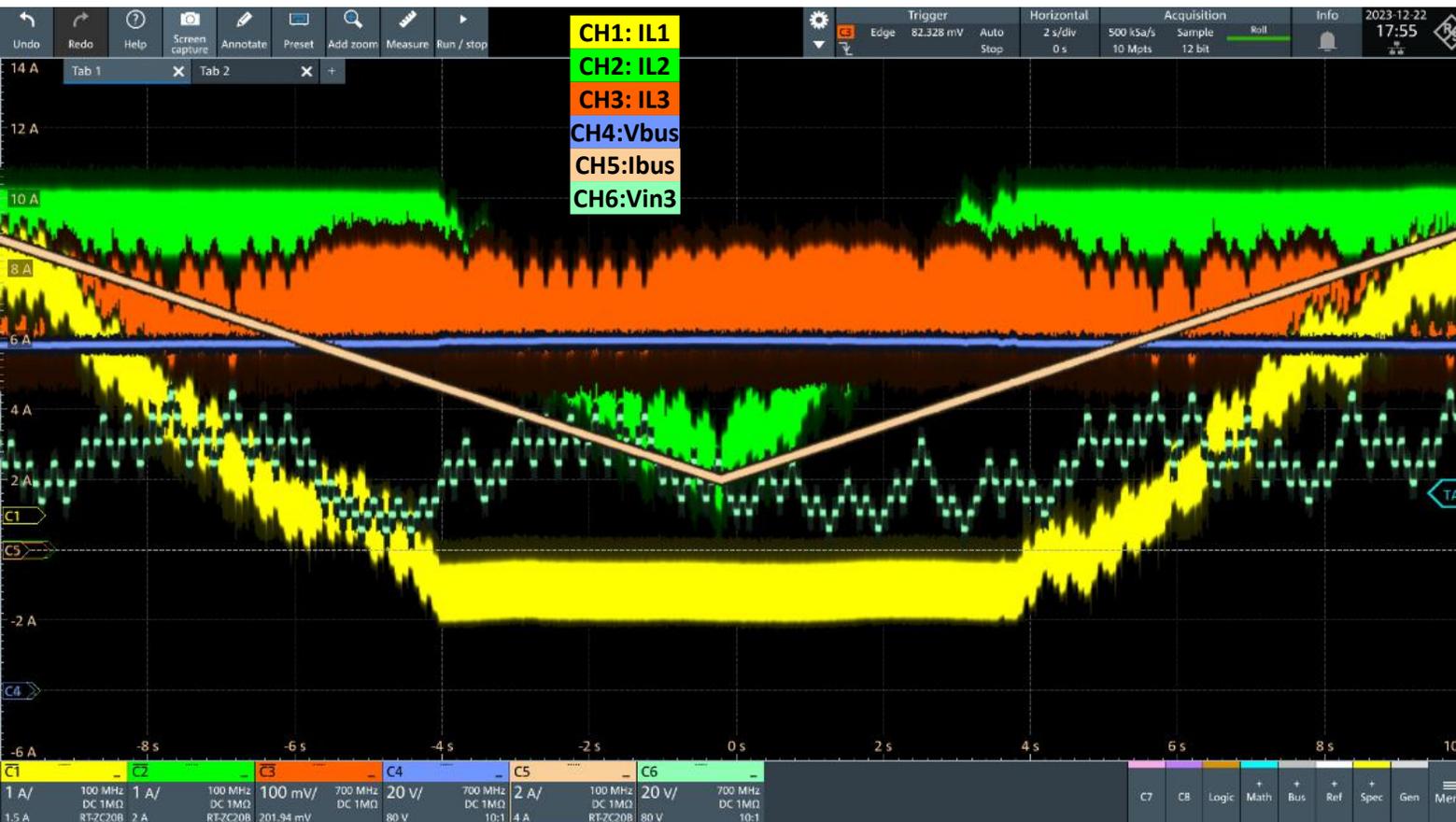
Test C3.4

$V_{in}=80\text{ V}$

$I_{bus}=2\text{-}9\text{ A}$

Module prioritization as expected using DC bus signalling

Control. Three module: full test (MPPT and battery)



Test C3.12

Vin3=PV panel emulator (MP=240W), Vin1=battery, Iload=2-9A

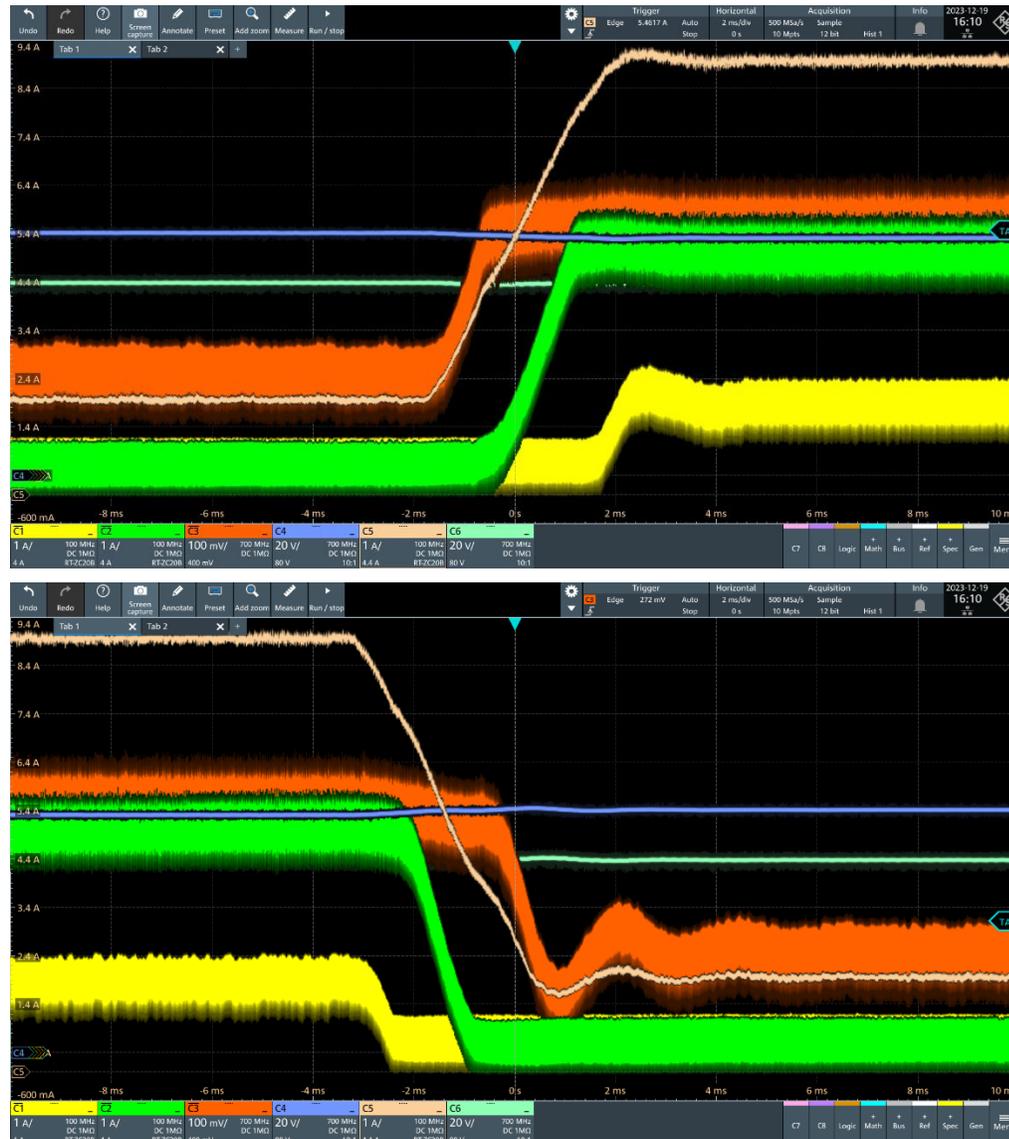
MPPT in module 1 is always operating as it has to provide the load power and the battery charge

While module 2 is not saturated, battery is being charged. When module 2 reaches its maximum output current, battery module regulates the bus

Control. Three module: load current steps

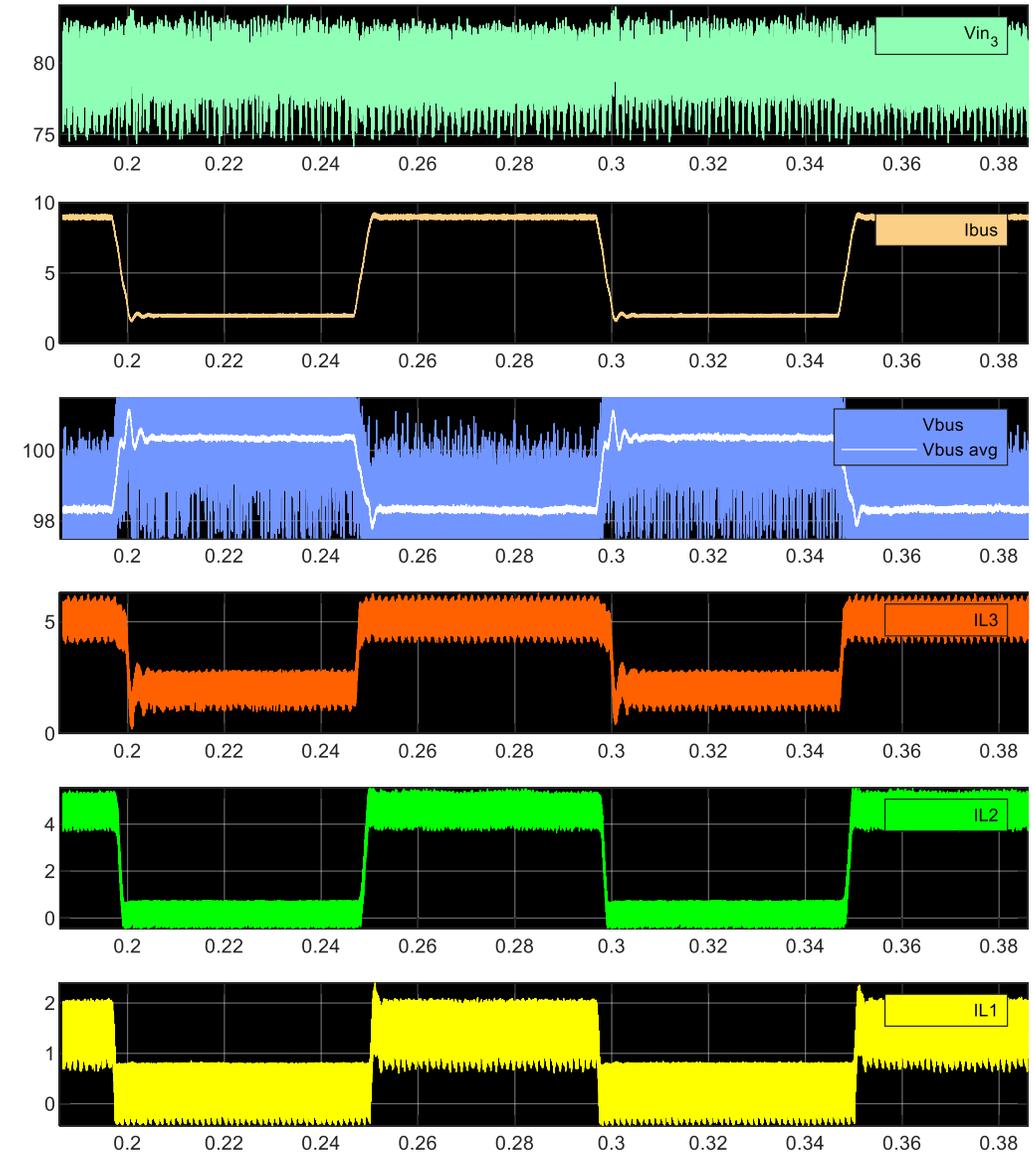


Detailed transitions

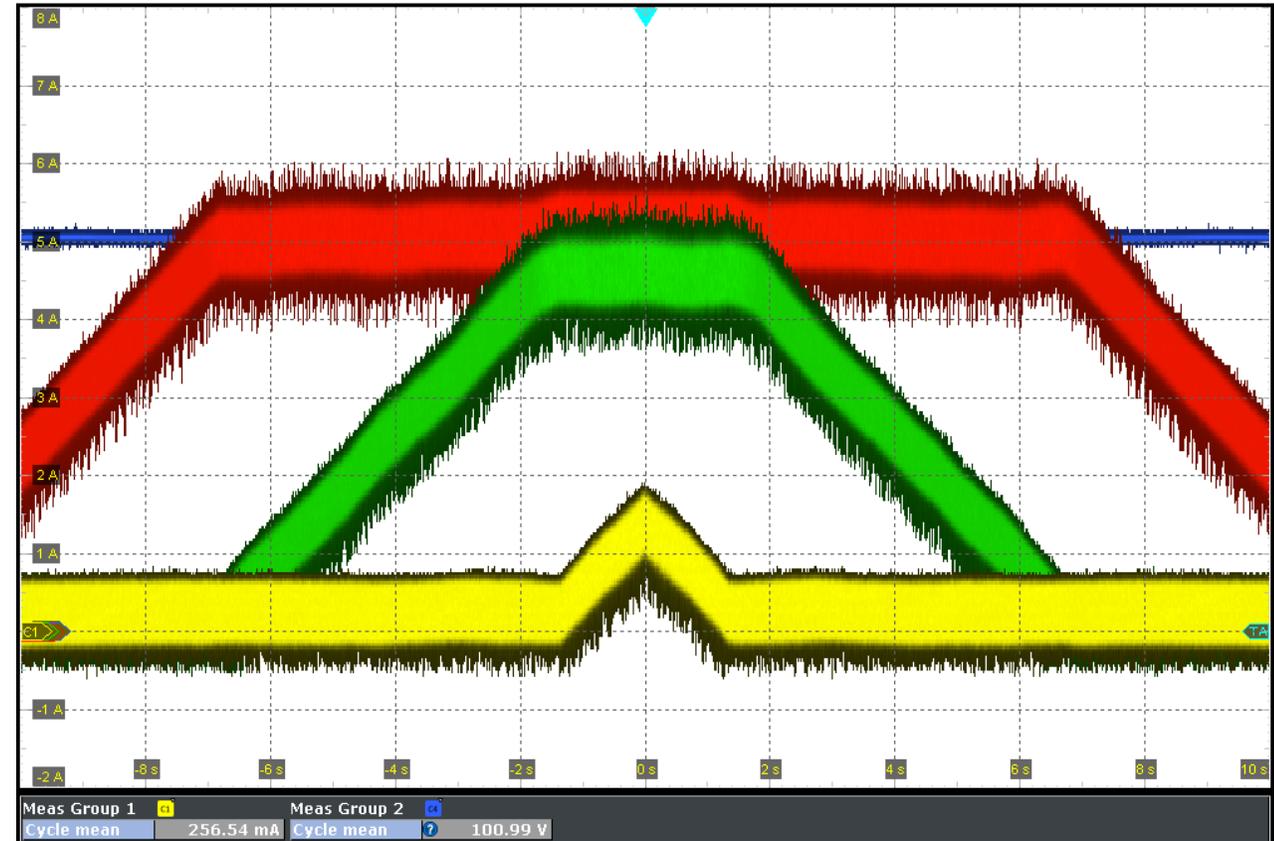
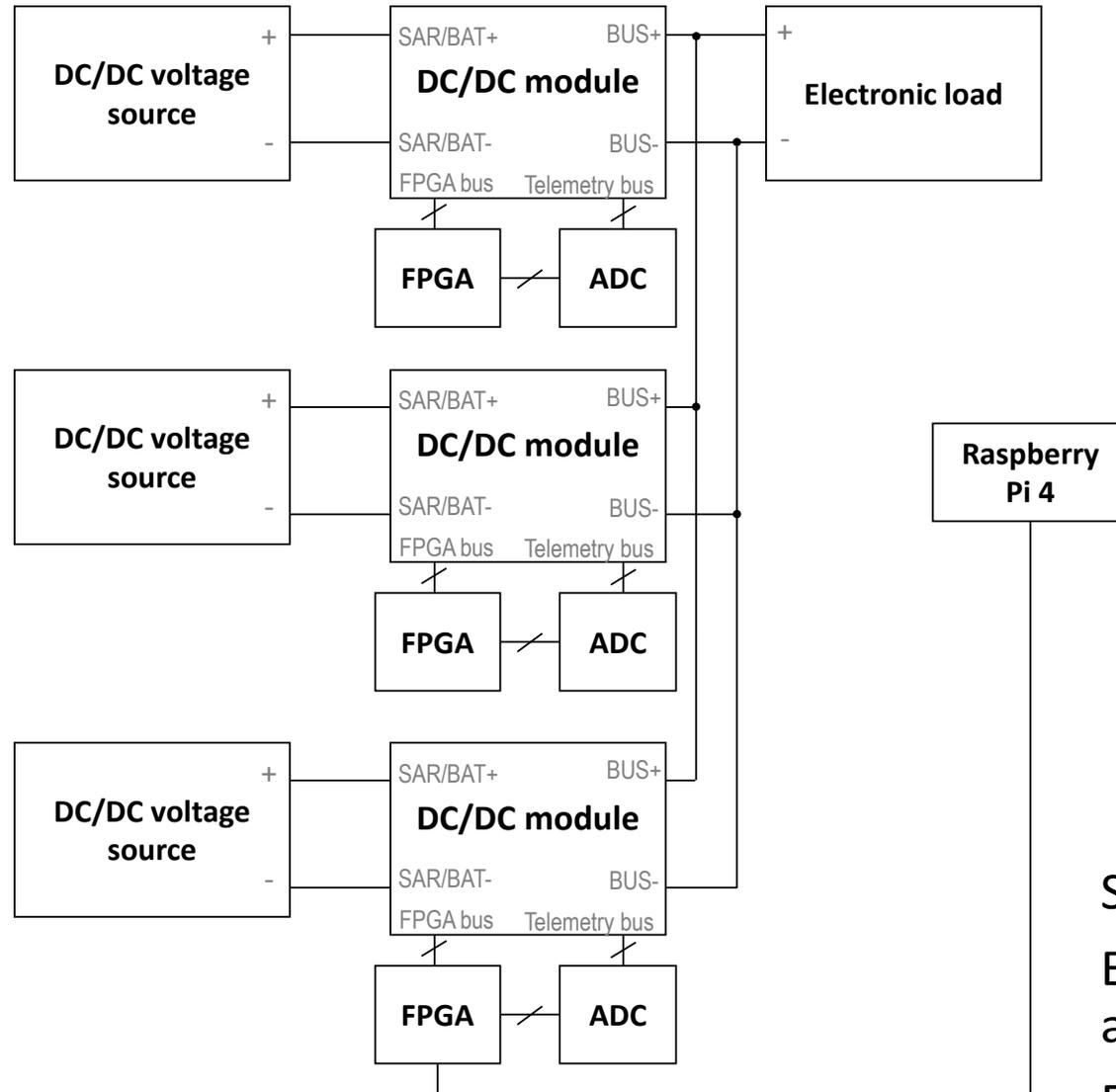


- CH1: IL1
- CH2: IL2
- CH3: IL3
- CH4: Vbus
- CH5: Ibus
- CH6: Vin3

Overall test



Control. Three module: supervisor set-up

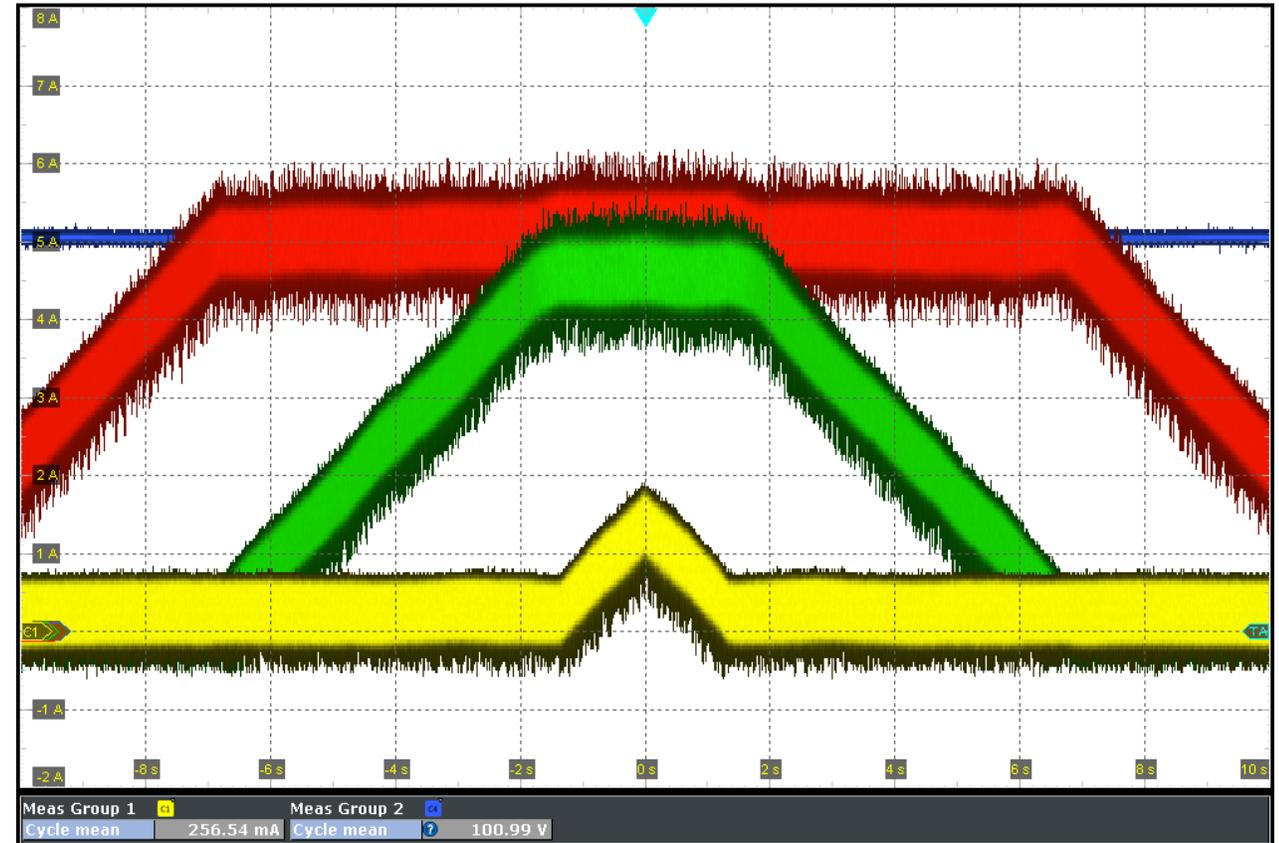
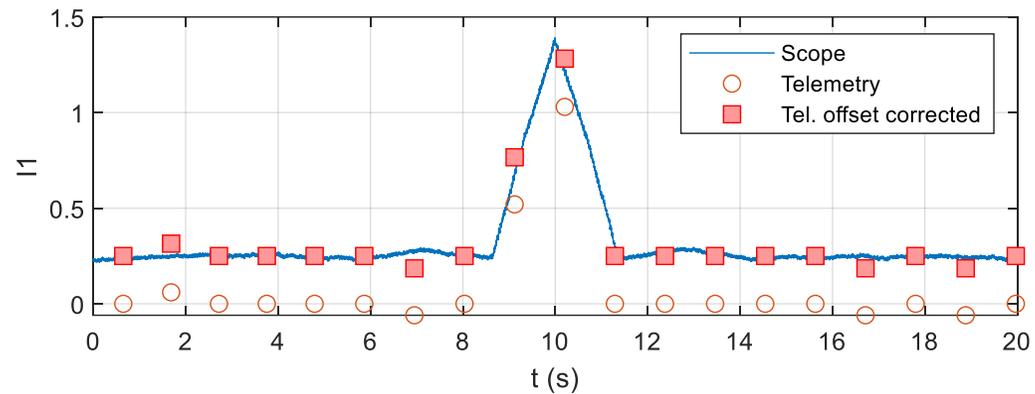
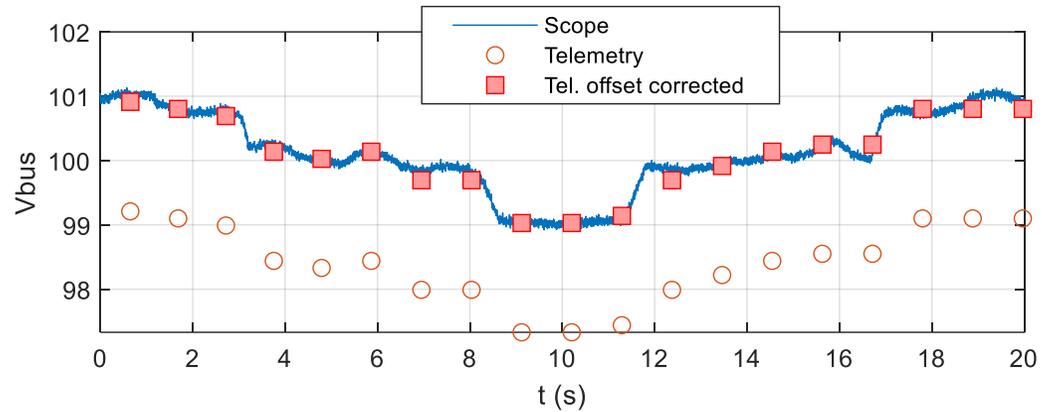


Supervisor implemented in a RaspberryPi 4

Every control module implemented in the FPGA has an SPI interface for telemetry and configuration

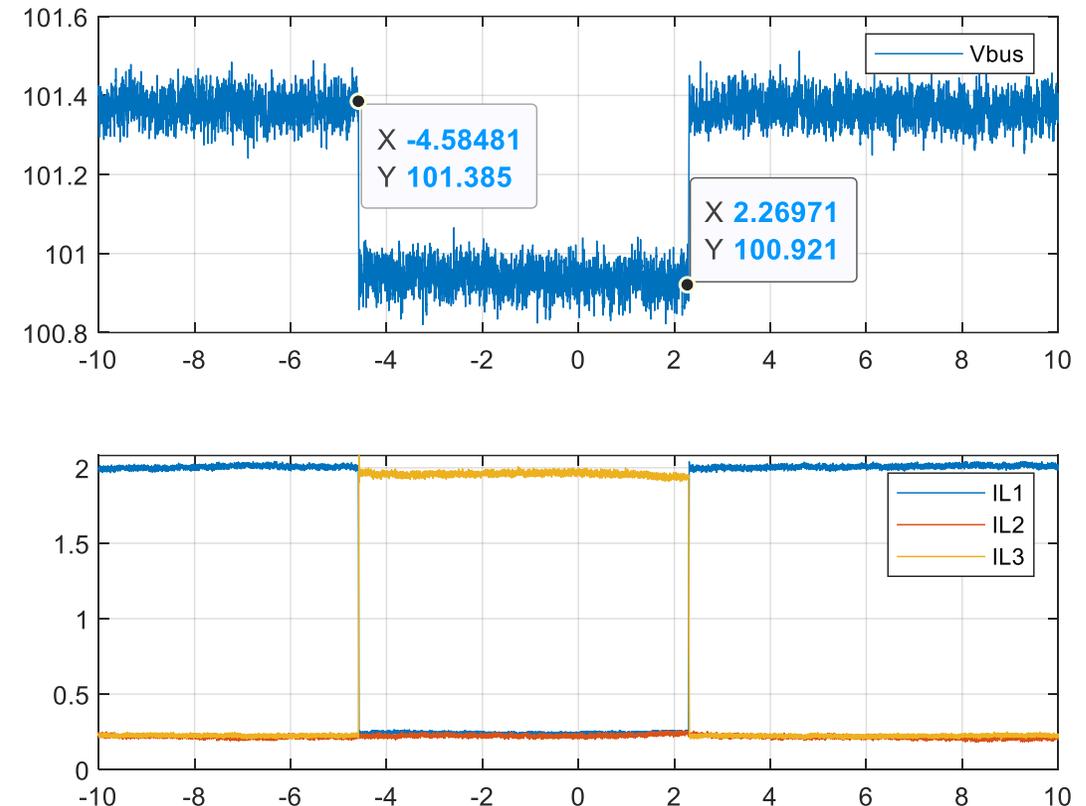
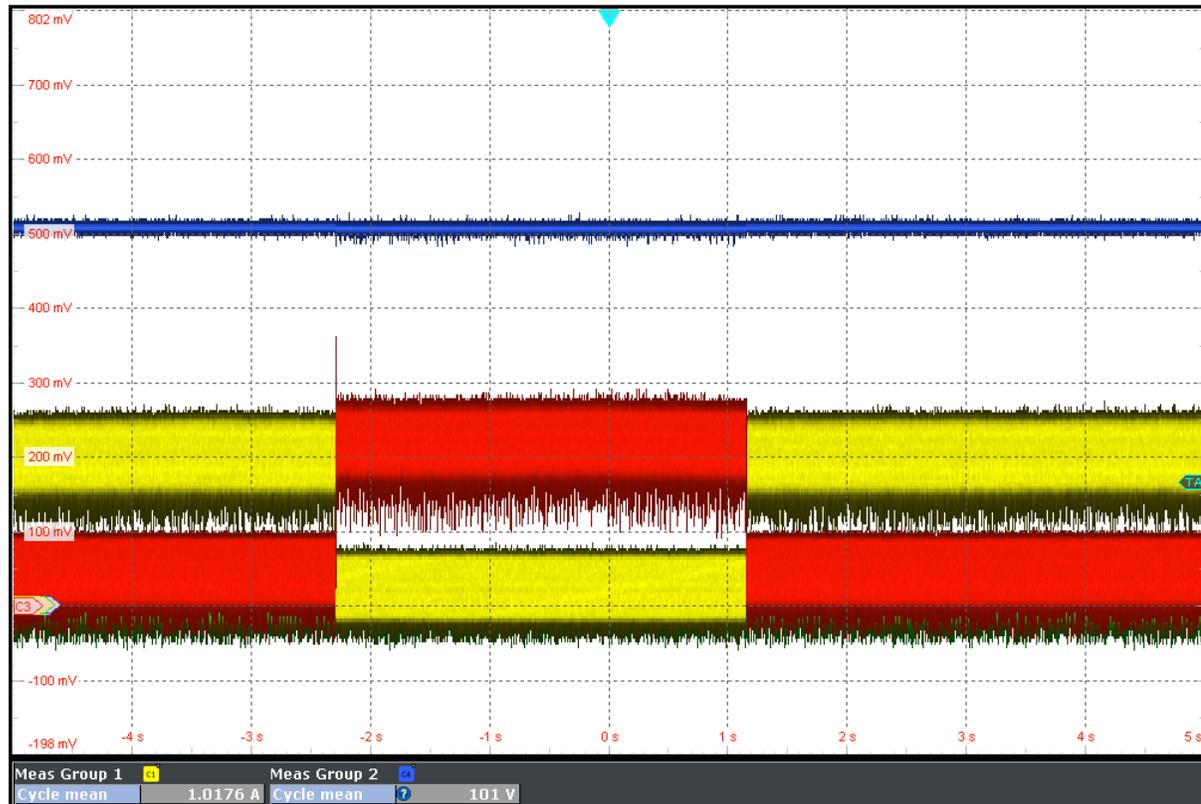
For simplicity, only connected to module 1

Control. Three module: telemetry



Supervisor gets telemetry data every second approx.
Offset in the measured data

Control. Three module: change in V-I curve

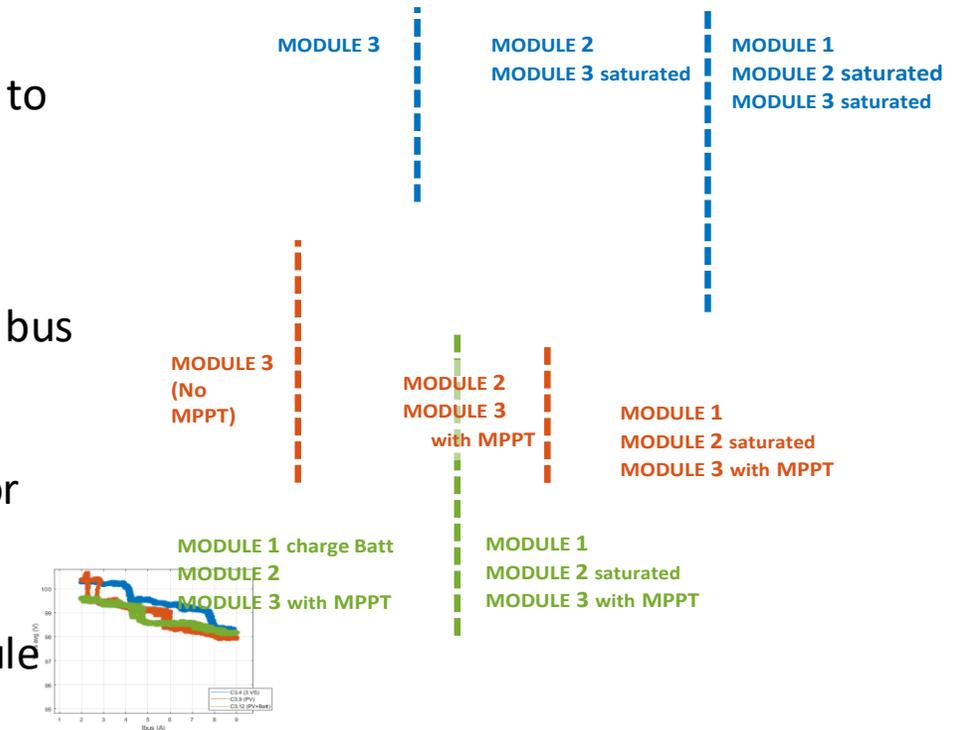


Supervisor sends a command to change V-I curve parameters in module 1

Constant current bus during test: depending on the V-I curve module 3 or module 1 regulate the bus

Bus voltage is properly regulated despite the change in V-I curve

- Feasibility of making a primary power distribution system based on equal power modules, with the same digital control and only sharing the information of the bus voltage
- DC bus signalling is used to prioritize the modules that provide the energy to the load while keeping the bus regulated: SAR modules priority vs. Battery modules to deliver power to the load
- Although the result is a non-tight regulation of the bus, the variation of the bus voltage is less than 5%.
- The priority order of the modules can be changed by the external supervisor
- MPPT algorithm is running in SAR modules. When the module is in MPPT mode, the variable injected current is compensated by the regulating module
- Battery module can be charged and is the module that ensures bus regulation despite the operation condition of the other modules
- Extensive test demonstrates the implemented control
- Co-simulation has been a useful tool for control debugging



Health Monitoring of digitally controlled flexible converters

Health monitoring

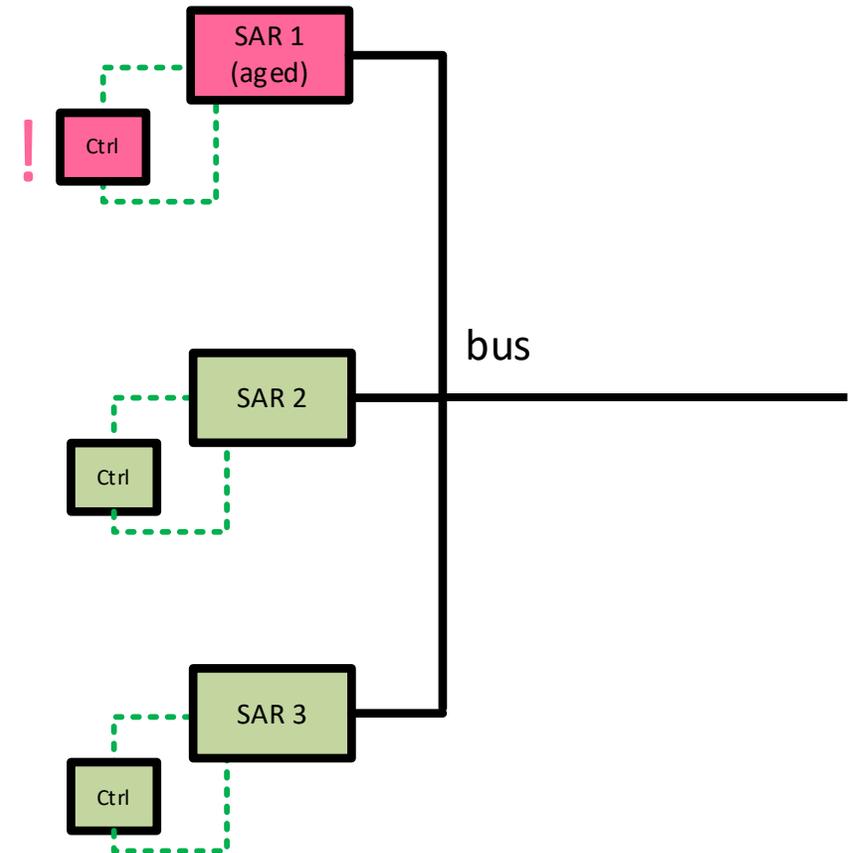


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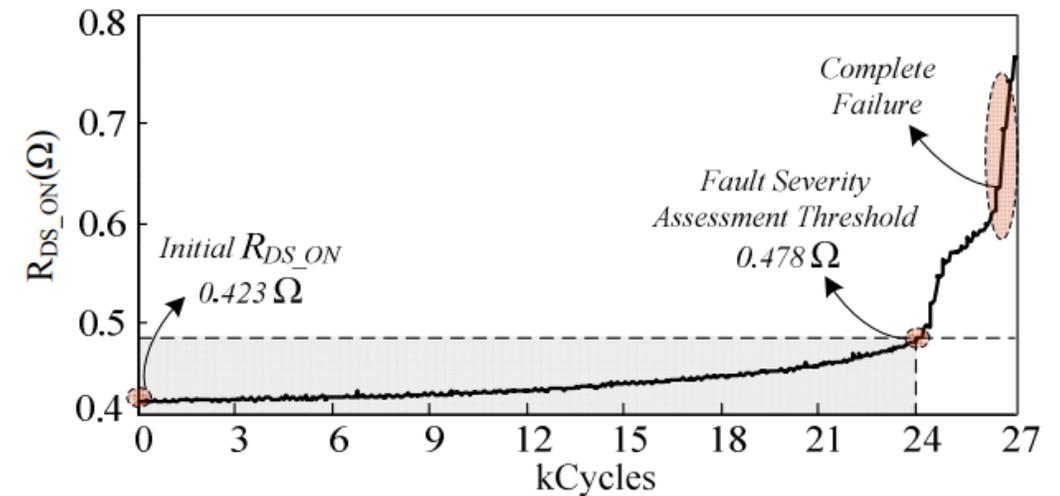
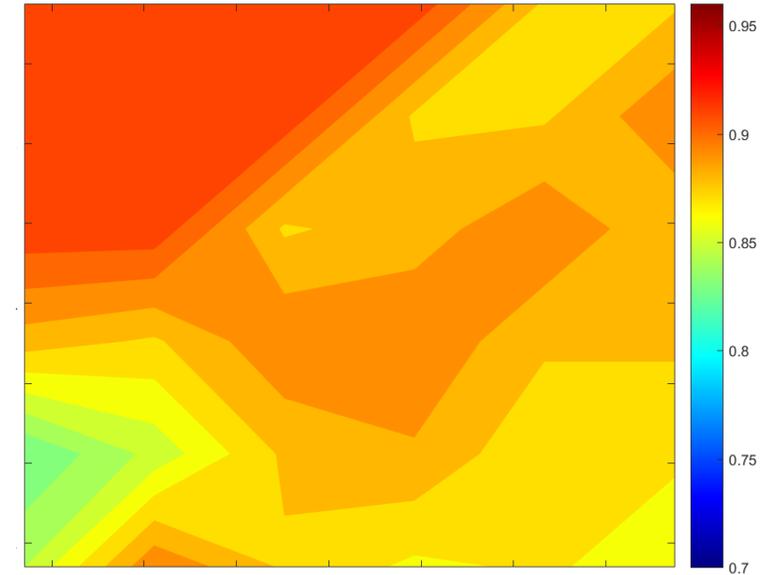
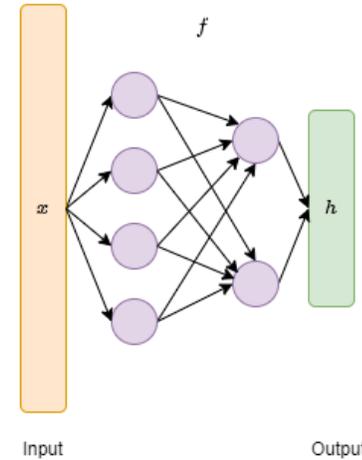
- Health monitoring methods
 - Improve reliability
 - Increase lifetime
 - Modules able to recalculate power demands



- Failure causes:
 - Magnetic elements: Almost nothing reported.
 - Capacitors:
 - One of the main causes
 - Indicators include increased ESR and reduction of capacitance
 - When modules sharing output difficult to identify which is failing.
 - Space design: Self-healing capacitors.
 - Semiconductor switches:
 - Main cause of failure
 - The ultimate root cause is in most cases mechanical and package related.
 - Multiple indicators
 - Mainly related to MOSFETs and IGBTs

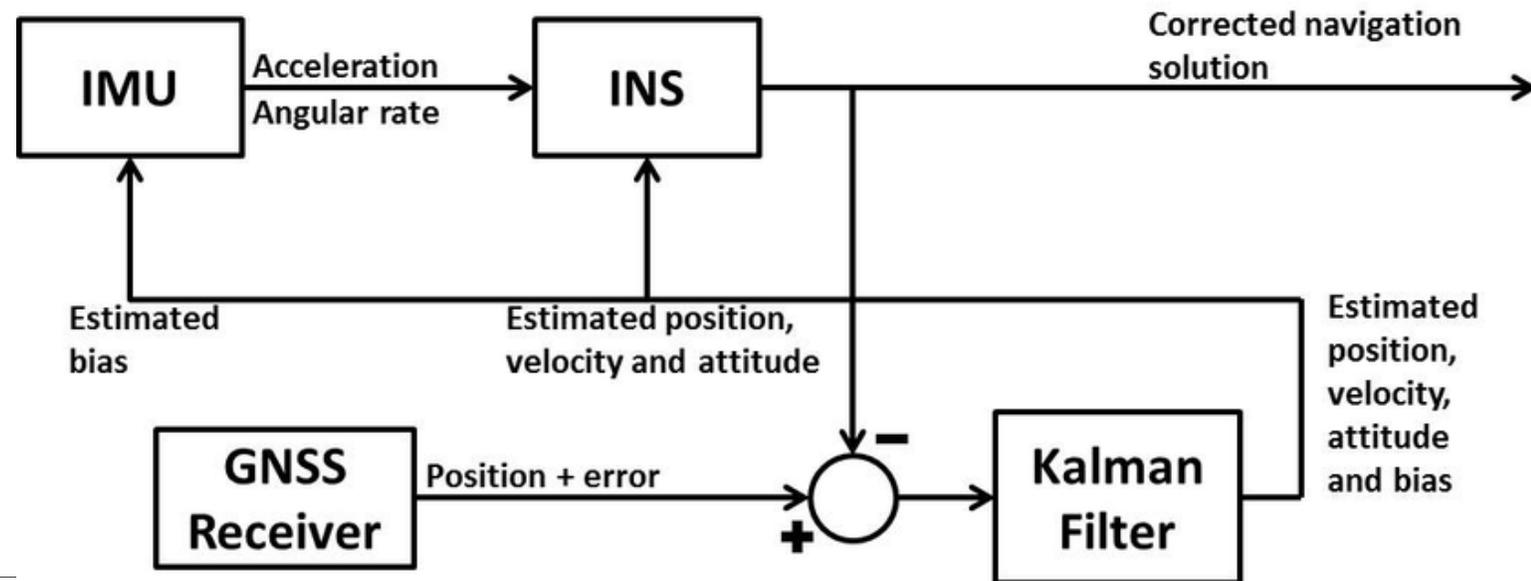
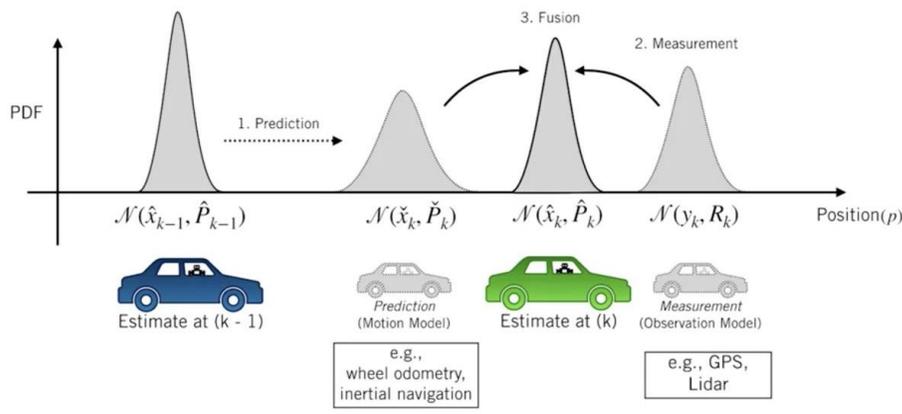
- Multiple indicators:
 - Threshold voltage
 - Difficult to measure in application.
 - Body diode forward voltage
 - Difficult to measure in application.
 - Gate charge
 - Specialized circuitry. Difficult to measure in application.
 - Parasitic capacitances
 - Specialized circuitry. Difficult to measure in application.
 - Breakdown voltage
 - Difficult to measure in application. Potentially destructive.
 - Leakage current
 - Difficult to measure in application.
 - On-state resistance:
 - Most used method.
 - Possible to measure in application.

- Detect MOSFET degradation
 - Resistance increase
 - Non-invasive
- Three alternatives
 - Kalman filter
 - Model comparison based on heatmap
 - Machine learning



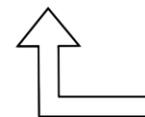
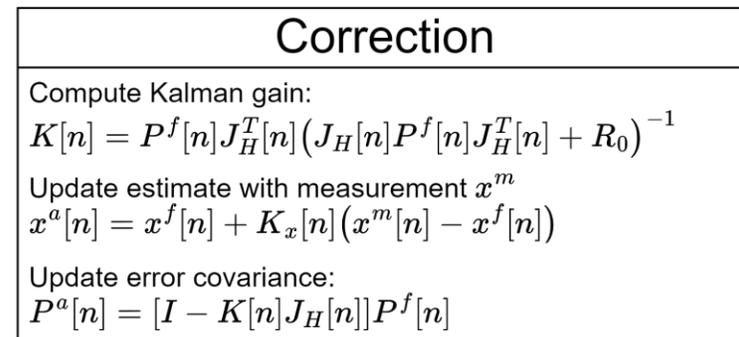
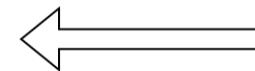
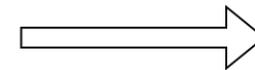
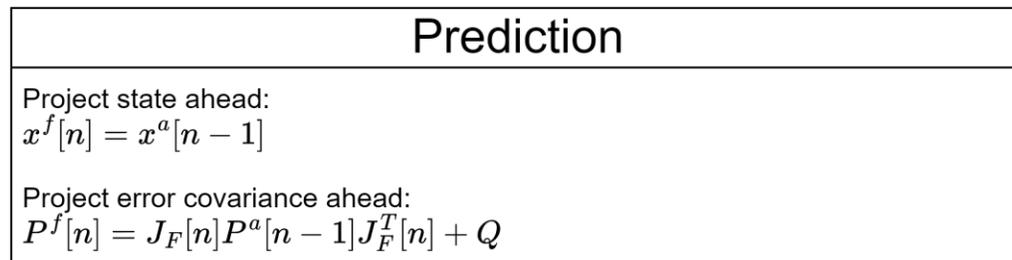
- MOSFET resistance measurement good indicator
- Direct measurement not an option
 - Added complexity. Reliability decreases
- Prediction
 - Kalman filter
 - Noisy environments, GNSS

The Kalman Filter I Prediction and Correction

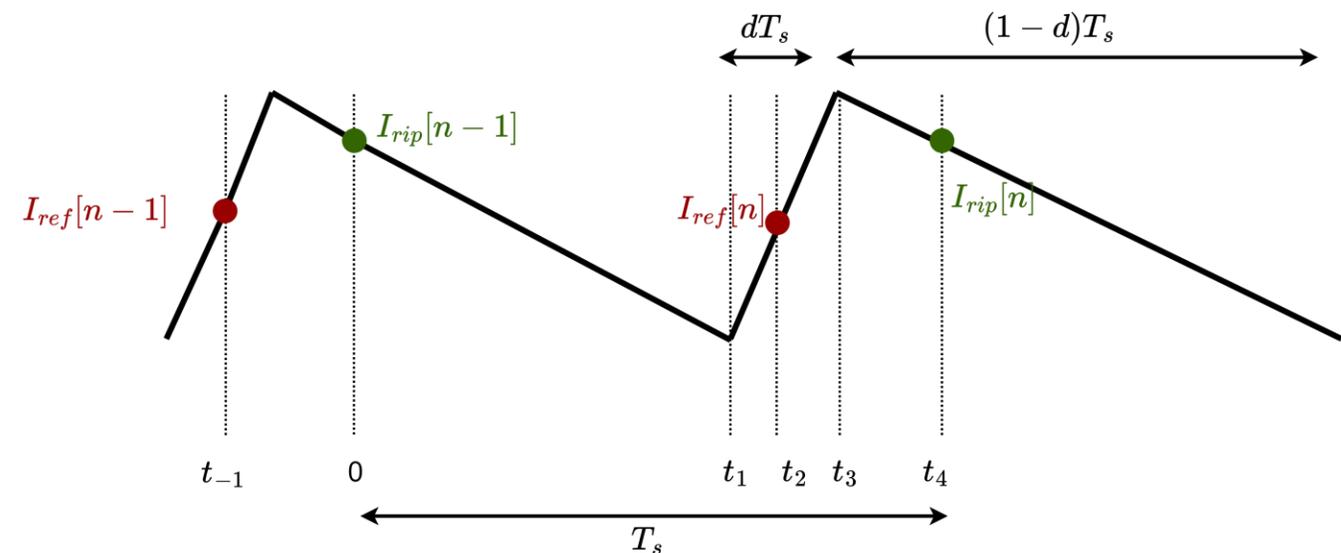
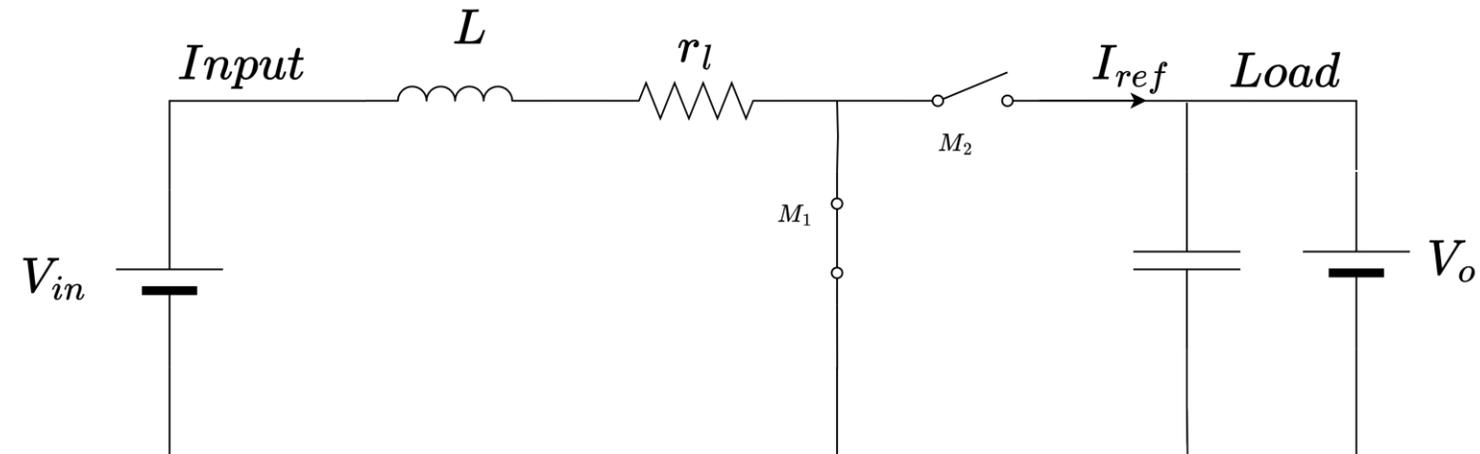


- State prediction based on previous inputs
 - State variables x_k
 - State transition matrix $x_{k+1} = f(x_k, u_k, w_k)$
 - Describes state evolution over time
 - Measurement model $z_k = h(x_k, v_k)$
 - State covariance P
 - Uncertainty in the estimated state

- Process noise covariance Q
 - Uncertainty in the process model
- Measurement noise covariance R
 - Uncertainty in sensors
- Kalman gain K
 - Weights that assign how much trust is given to measurements
- Jacobian matrices F_k and H_k



- Case of study: average current controlled boost converter
 - Adapted to Buck too
- Estimation of parasitic resistance
- Control inputs
 - V_{in} , V_{out}
 - Current reference I_{ref}
 - Additional current sample I_{rip}
 - Duty cycle d
- Output:
 - Estimated states r_l and current ripple $\Delta i = I_{RIP} - I_{REF}$



- State variables
 - Current sample difference Δi
 - Parasitic resistance r_l
- State space description

$$[\dot{\Delta i}] = A \cdot \begin{bmatrix} \Delta i \\ r_l \end{bmatrix} + B \cdot \begin{bmatrix} V_{in} \\ V_o \\ I_{ref} \end{bmatrix}$$

$$A = -\frac{r_l}{L}$$

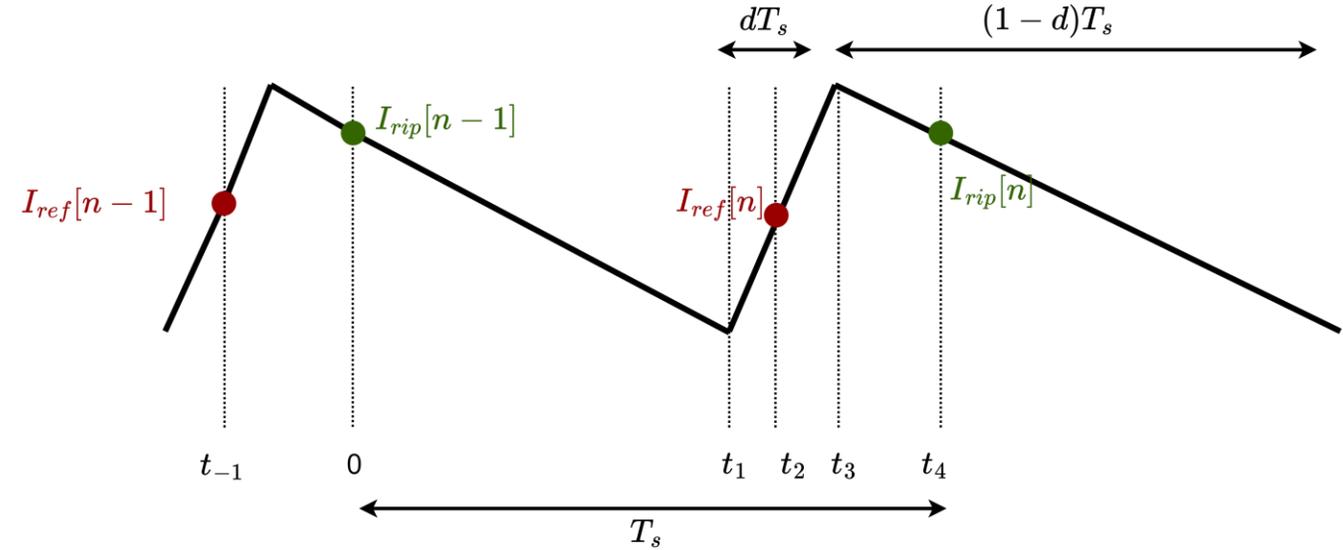
$$B = \begin{cases} \begin{bmatrix} \frac{1}{L} & 0 & -\frac{r_l}{L} \end{bmatrix} & \text{when } 0 < t < d \cdot T_s \\ \begin{bmatrix} \frac{1}{L} & -\frac{1}{L} & -\frac{r_l}{L} \end{bmatrix} & \text{when } d \cdot T_s < t < T_s \end{cases}$$

- State transition
 - One switching cycle is developed

$$\Delta i(T_s) = e^{-\frac{r_l T_s}{L}} \cdot \Delta i(0) + \int_0^{T_s} e^{-\frac{r_l (T_s - \tau)}{L}} \cdot B(\tau) \cdot \begin{bmatrix} V_{in} \\ V_o \\ I_{ref} \end{bmatrix} d\tau$$

- Next switching cycle

$$\Delta i(T_s) = \left(1 - \frac{r_l}{L} T_s\right) \Delta i(0) + \left(\frac{V}{L}\right) T_s - I_{ref} \frac{r_l}{L} T_s$$



- Boost

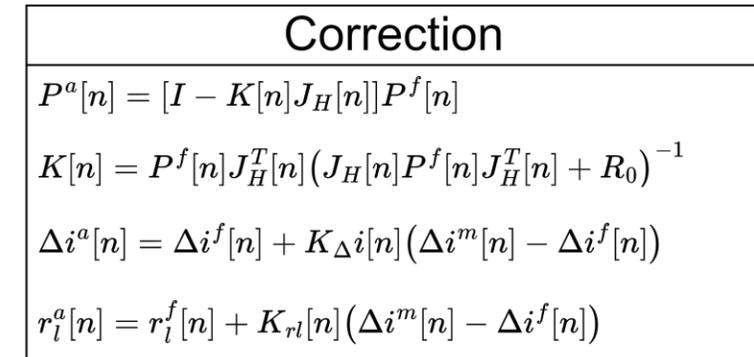
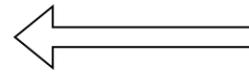
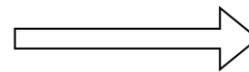
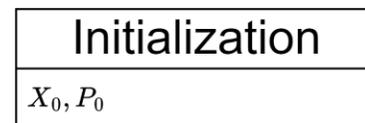
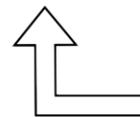
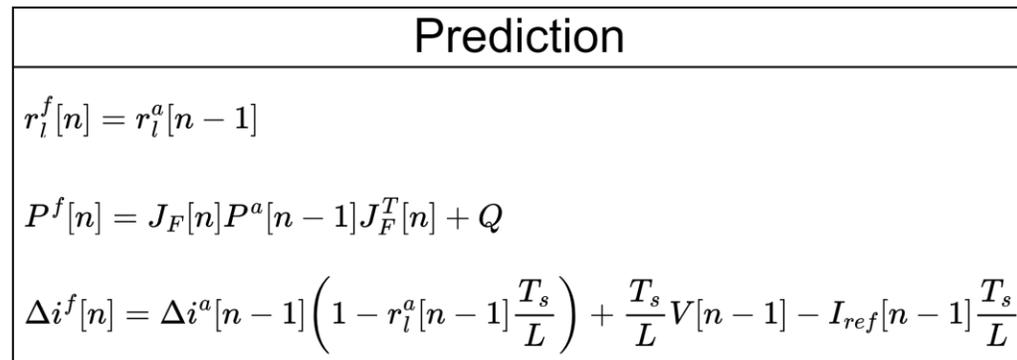
$$V[n] = V_{in}[n] - (1 - d[n]) \cdot V_o[n]$$

- Buck

$$V[n] = d[n] \cdot V_{in}[n] - V_o[n]$$

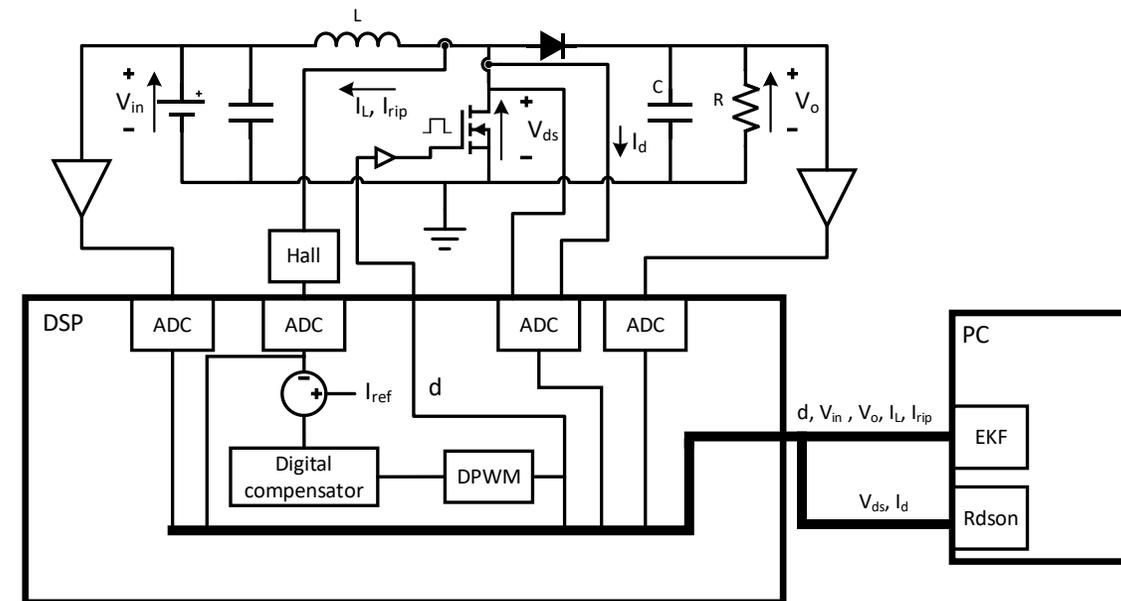
- State transition

$$F(X[n], U[n]) = \begin{bmatrix} \Delta i[n] \\ r_l[n] \end{bmatrix} = \begin{bmatrix} \Delta i[n-1] \cdot \left(1 - r_l[n-1] \cdot \frac{T_s}{L}\right) + \frac{T_s}{L} \cdot (V[n-1]) - I_{ref}[n-1] \cdot \frac{T_s}{L} \cdot r_l[n-1] \\ r_l[n-1] \end{bmatrix}$$

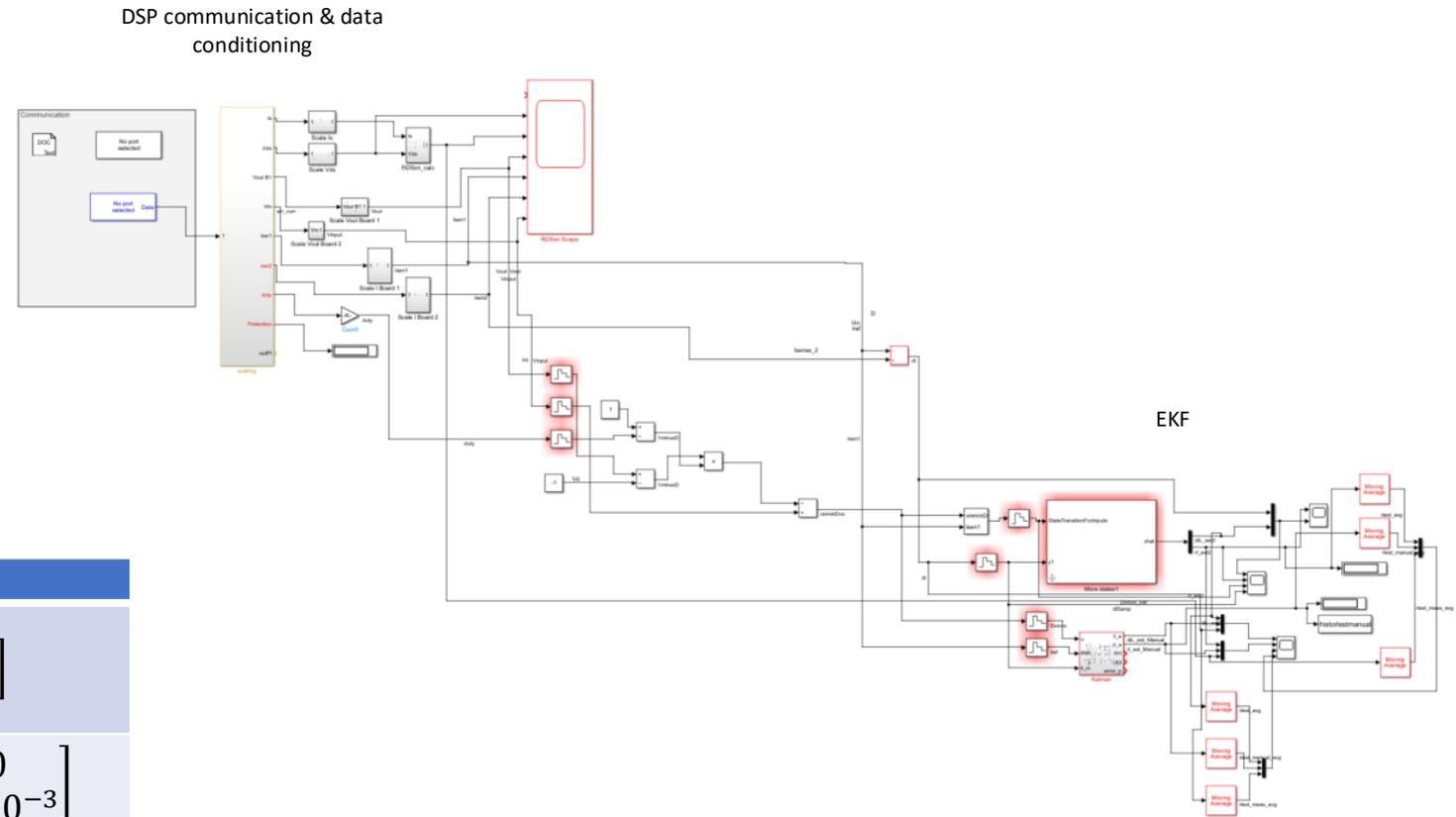


Parameter	Value
Input voltage V_{in} :	15 V
Output voltage V_o :	30 V
Inductor L :	275 μ H
Capacitor C :	570 μ F
Switching frequency f_{sw} :	10 kHz
Switching FET:	FDP26N40
Switching FET ON resistance R_{dson} :	190 m Ω
Reference current I_{ref} :	1.5 A
ADC resolution:	12 bits
ADC input range:	0-3V

- Custom boost converter
- Data acquisition
 - Texas Instruments TMS28F379
- Kalman filter execution on external PC



- EKF prediction implementations
- Simulink model
 - Wide range of toolboxes
 - DSP support

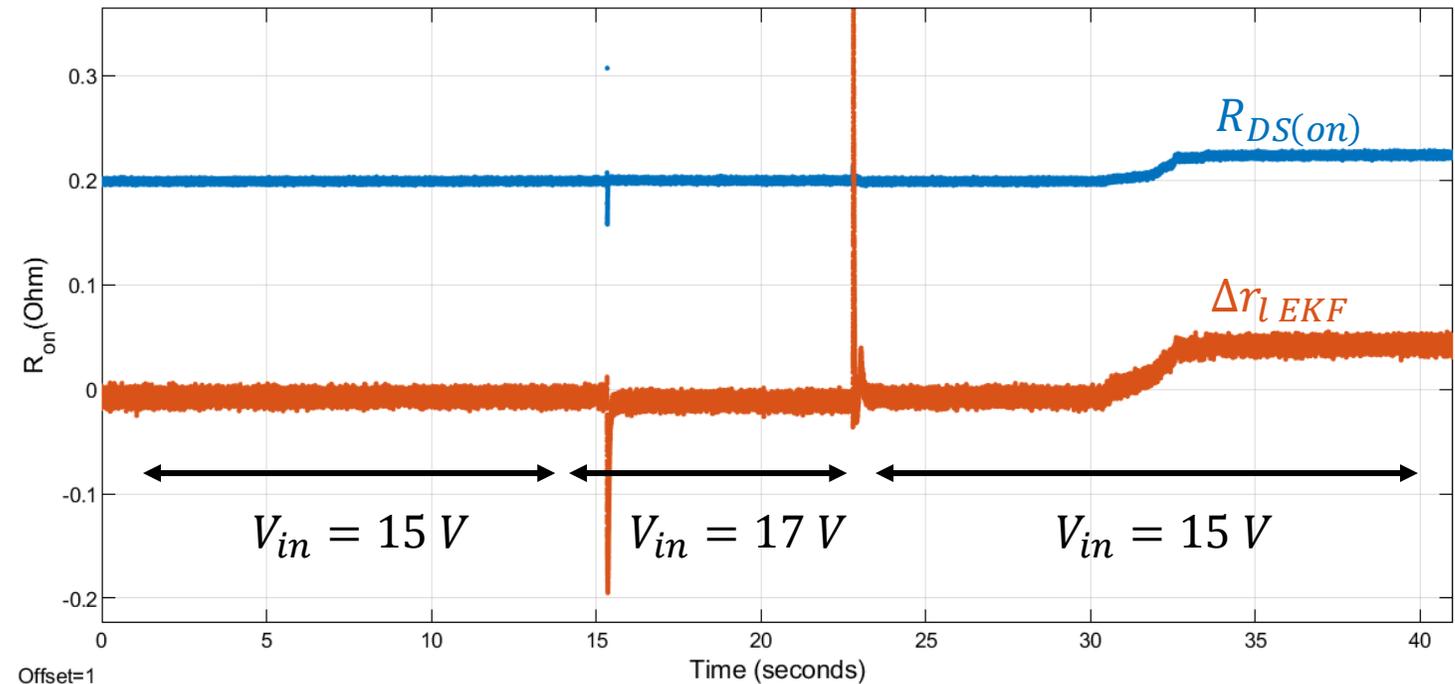


Parameter	Value
Initial states X_0	$\begin{bmatrix} 0 \\ 110 \cdot 10^{-3} \end{bmatrix}$
State error covariance matrix P_0 :	$\begin{bmatrix} 1 \cdot 10^{-3} & 0 \\ 0 & 1 \cdot 10^{-3} \end{bmatrix}$
Measurement noise R_0 :	$1 \cdot 10^{-2}$
Process noise Q :	$\begin{bmatrix} 1 \cdot 10^{-3} & 0 \\ 0 & 1 \cdot 10^{-3} \end{bmatrix}$

- Degradation simulated using MOSFET driver voltage change
 - 10% increase

- Change in conduction resistance detected

- Minor changes in input voltage cause errors in prediction.



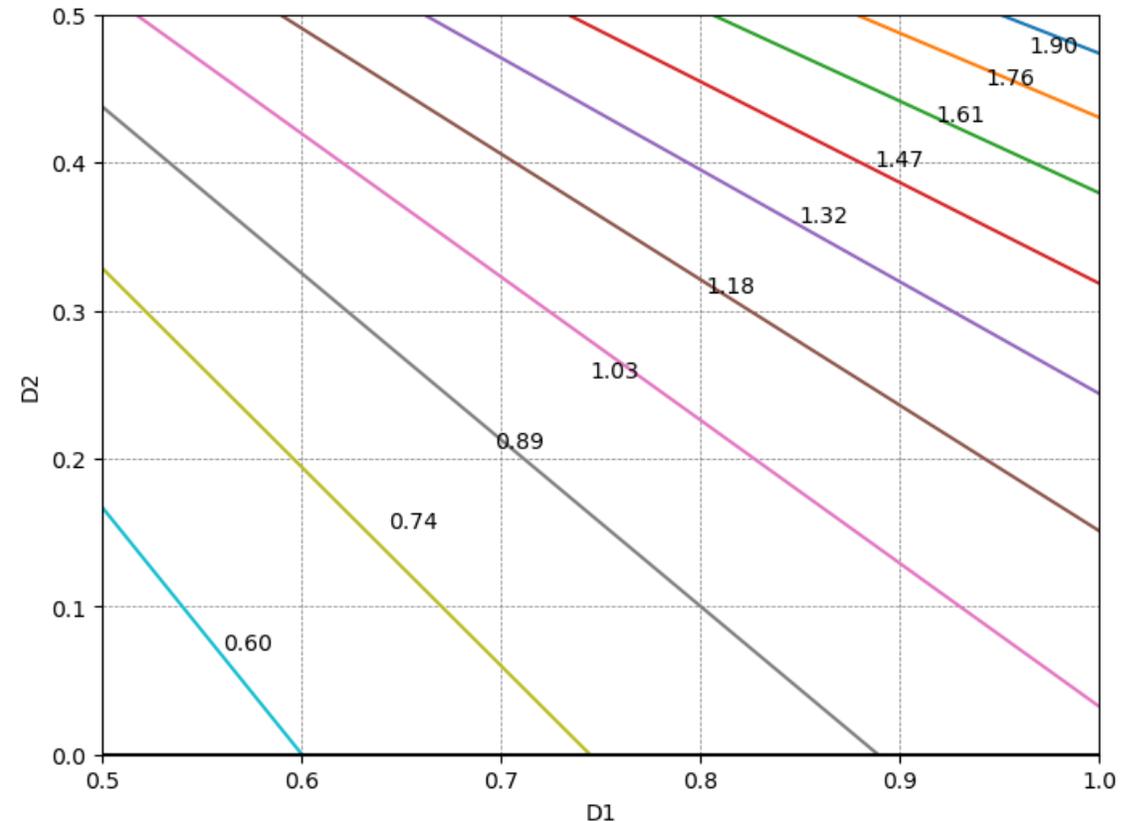
Kalman filter:

+ Detection of parasitic resistance increase

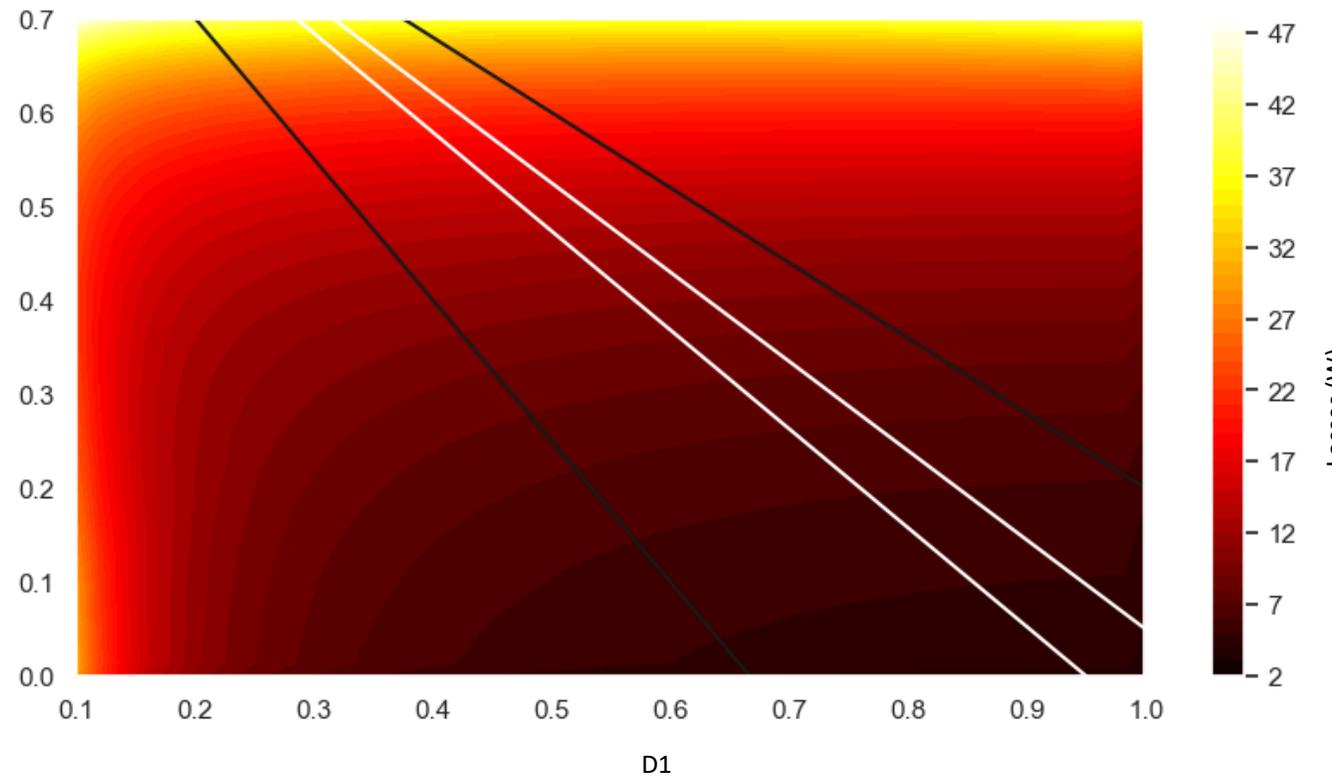
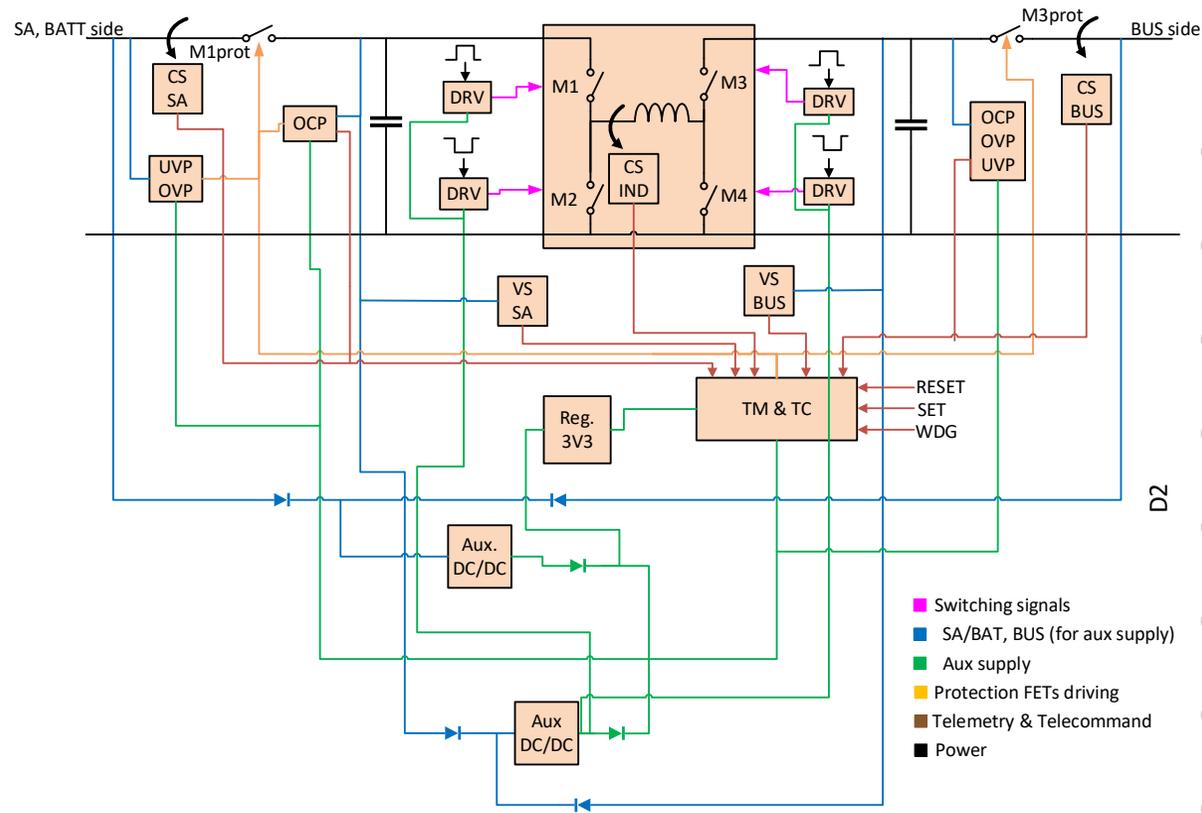
- Second current sample needed

- Temperature effects not considered

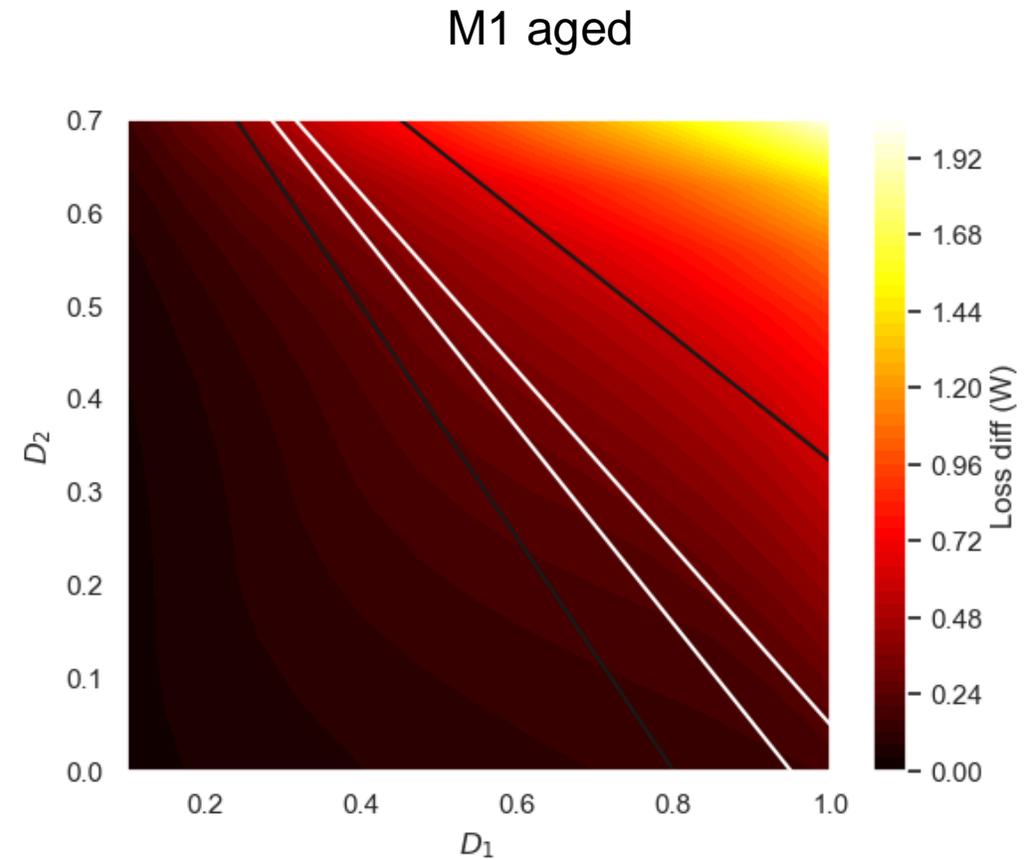
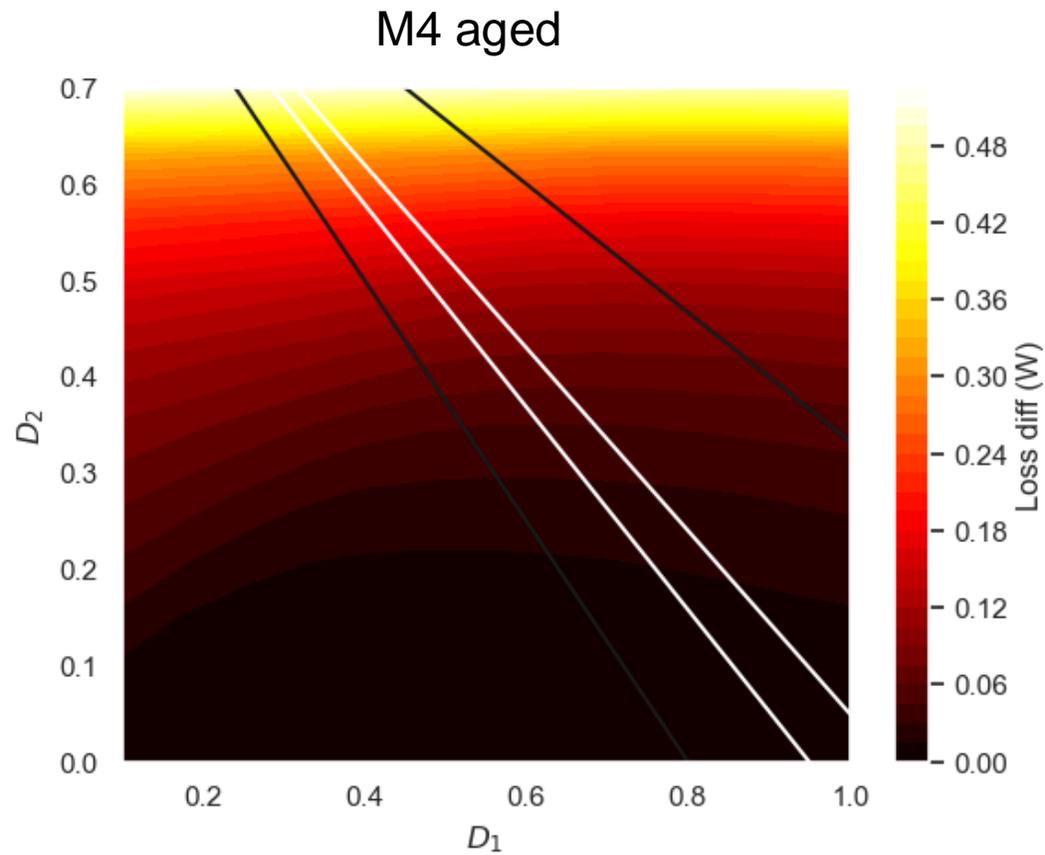
- Four-switch buck boost
 - Gain = $\frac{D_1}{1-D_2}$
- Same gain, different duty cycles
- Regions where degradation is evident
- Operating in suboptimal conditions during certain moments (e.g. out of eclipse)



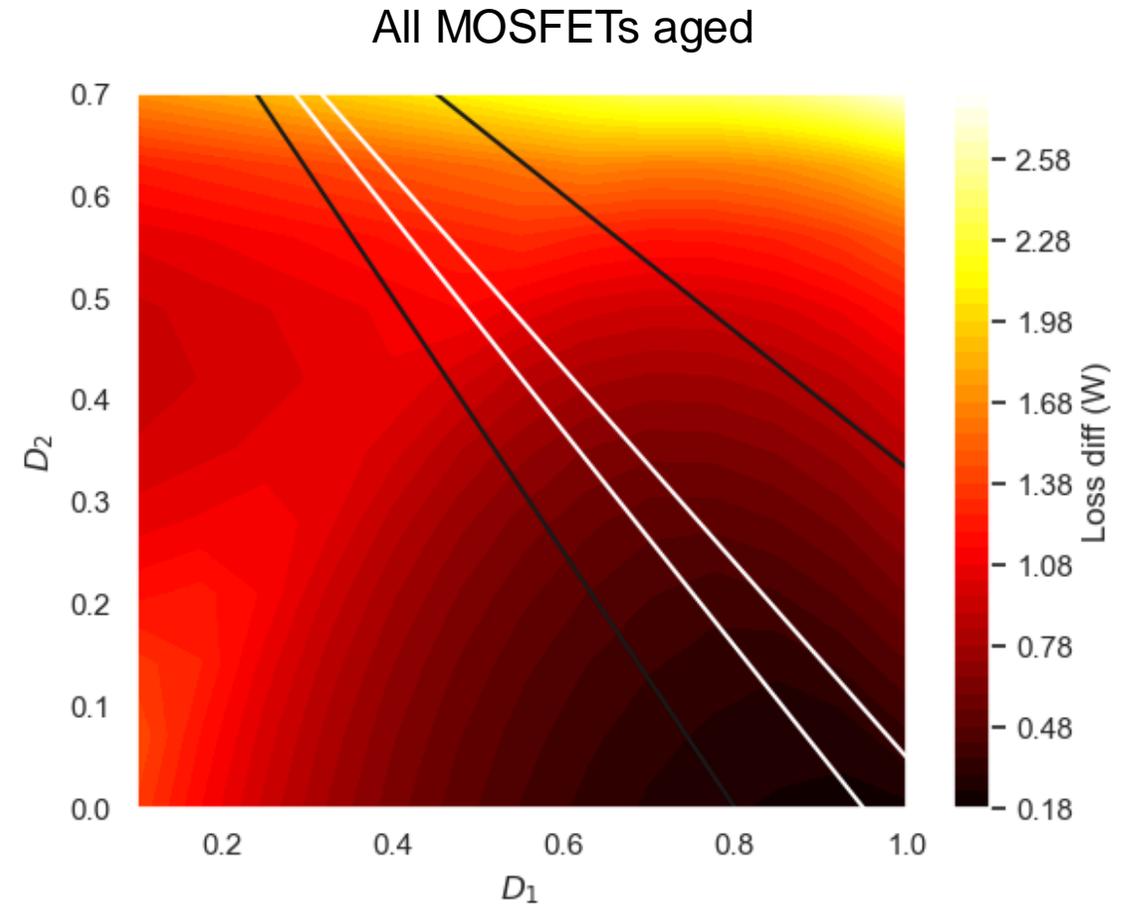
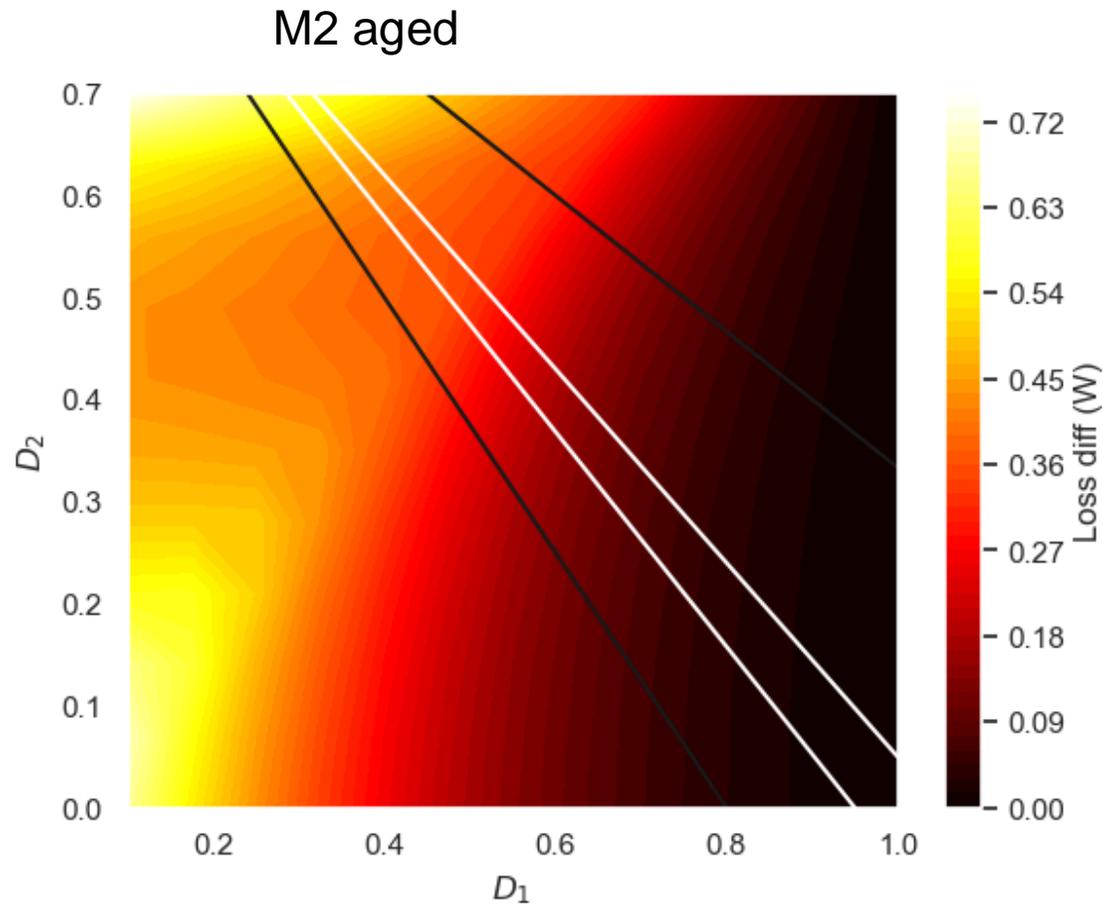
- Converter losses calculated



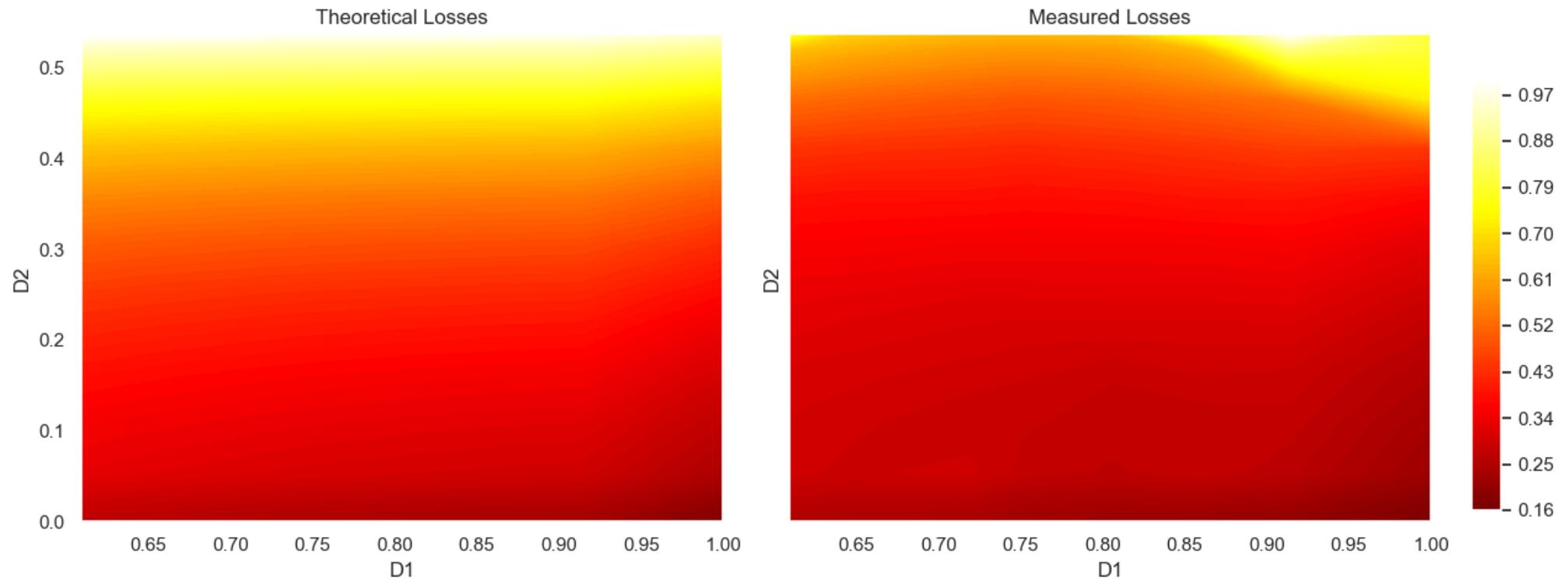
- Find zones of interest
 - Different degradations for each MOSFET



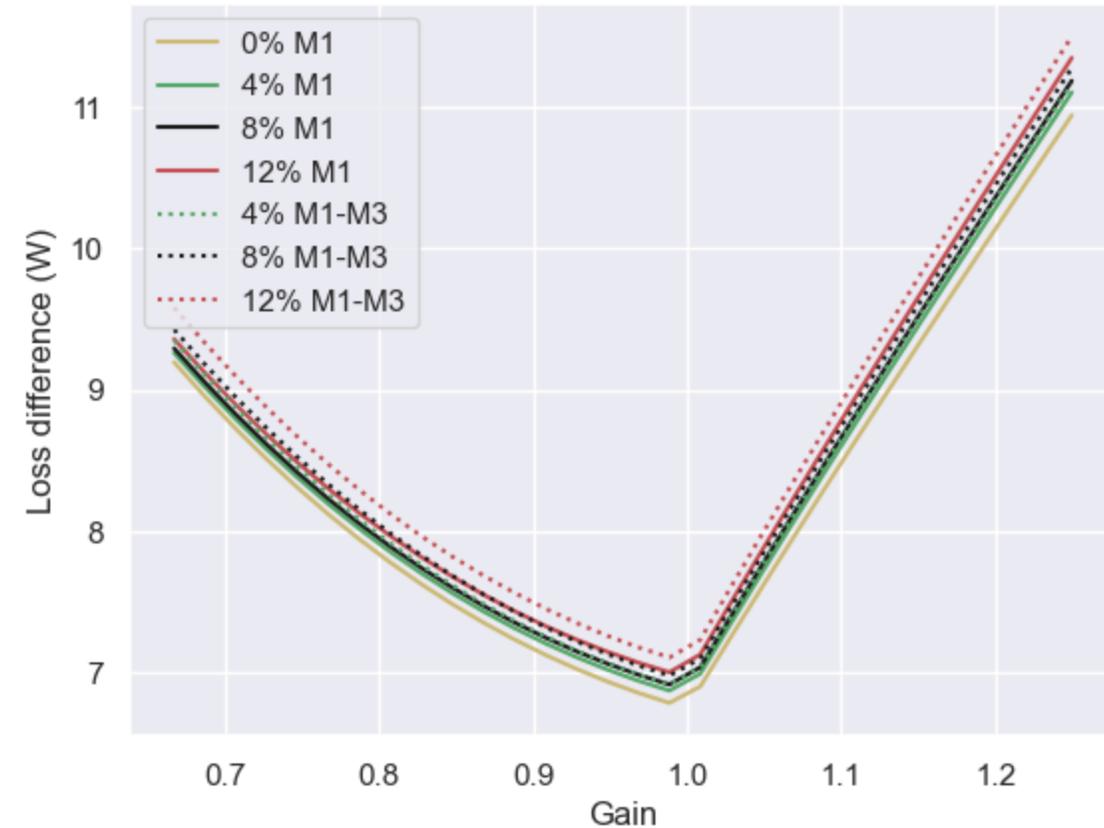
- Find zones of interest
 - Different degradations for each MOSFET



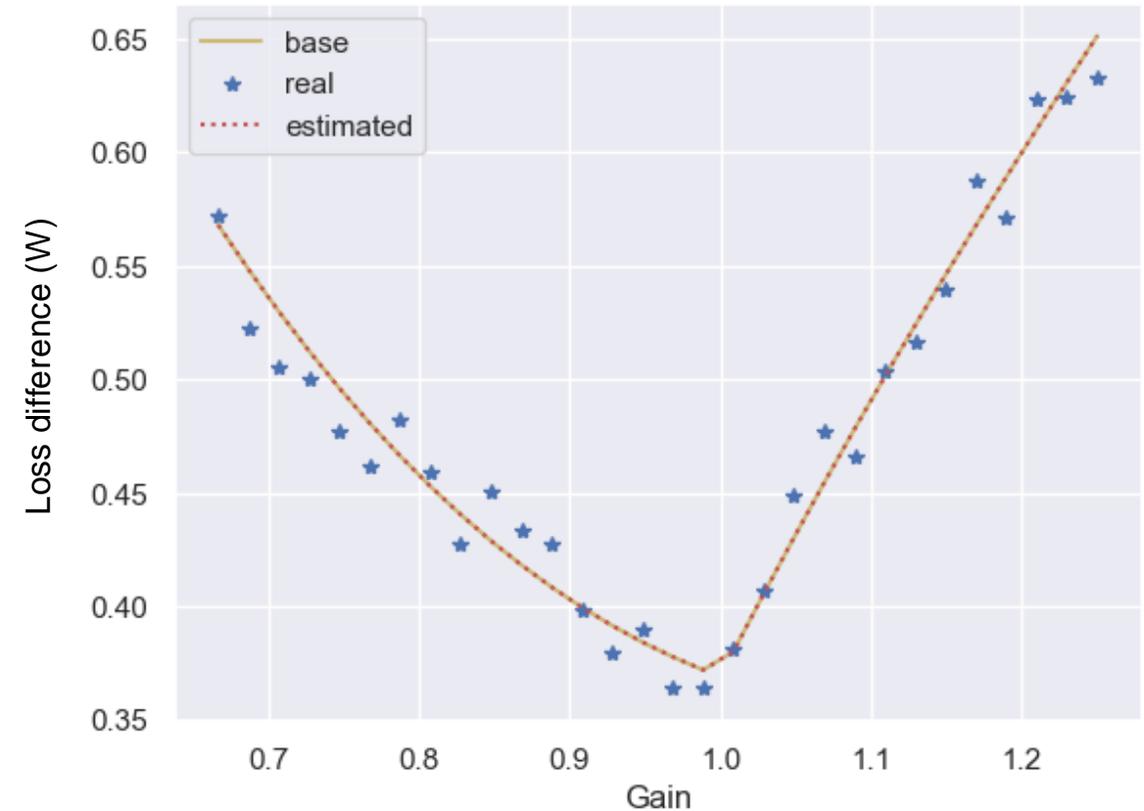
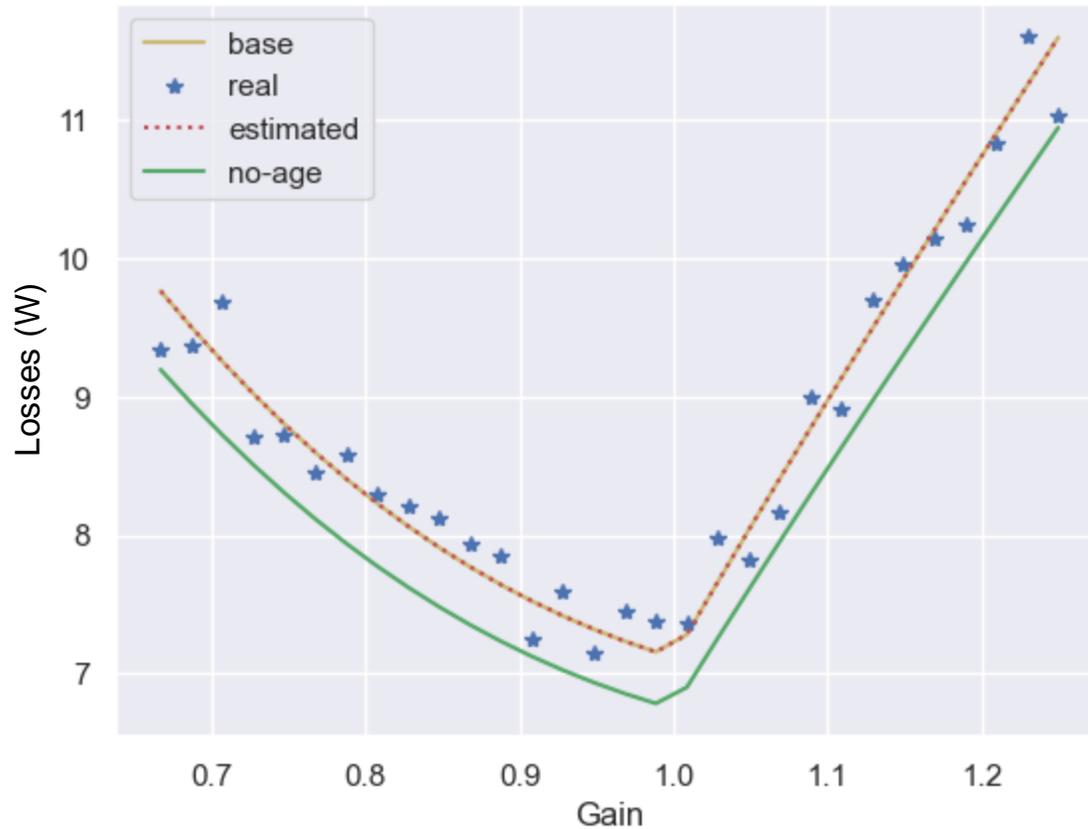
- Comparison with prototype
 - Temperature effects not considered
 - Not accurate



- Generating whole heatmap is resource consuming
- Generated database with different aging elements
- Baseline to predict behaviour



- Generated “real measurements”
 - Random noise -> 5% measurement error
- Detection

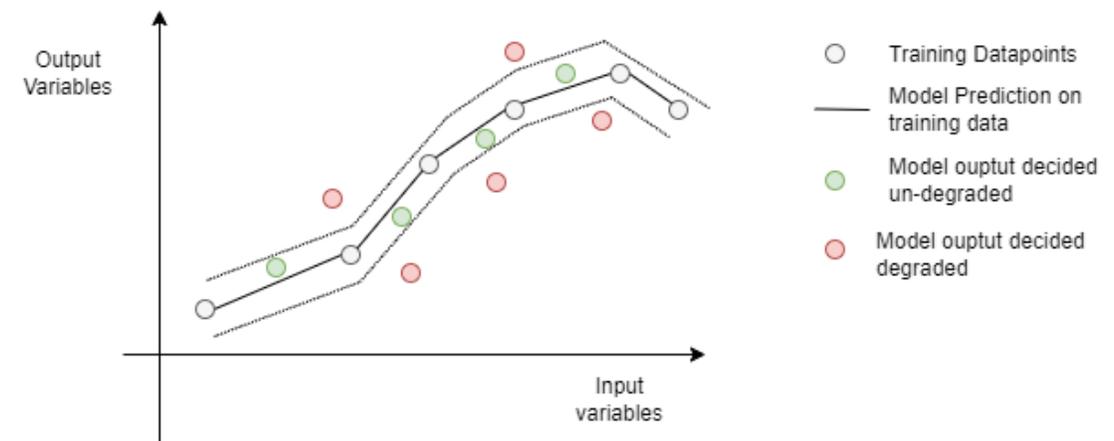
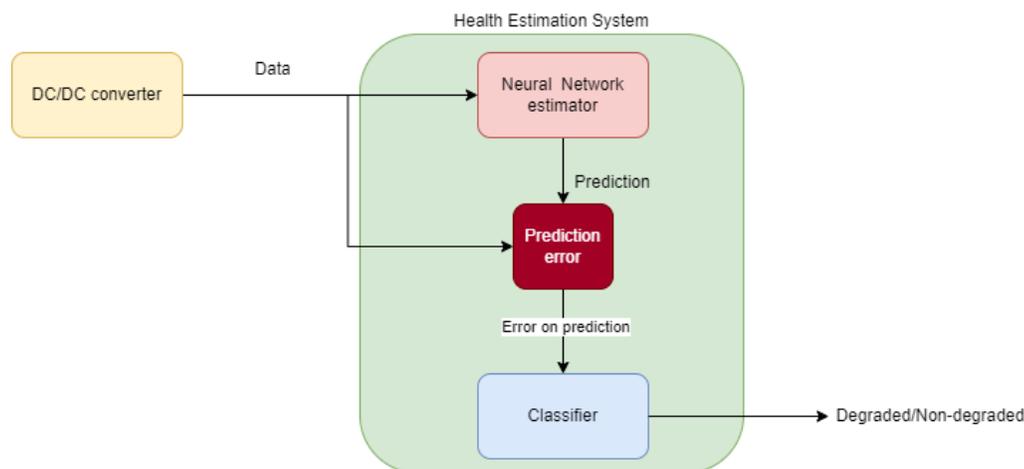


- Heatmap conclusions:
- Results inconclusive

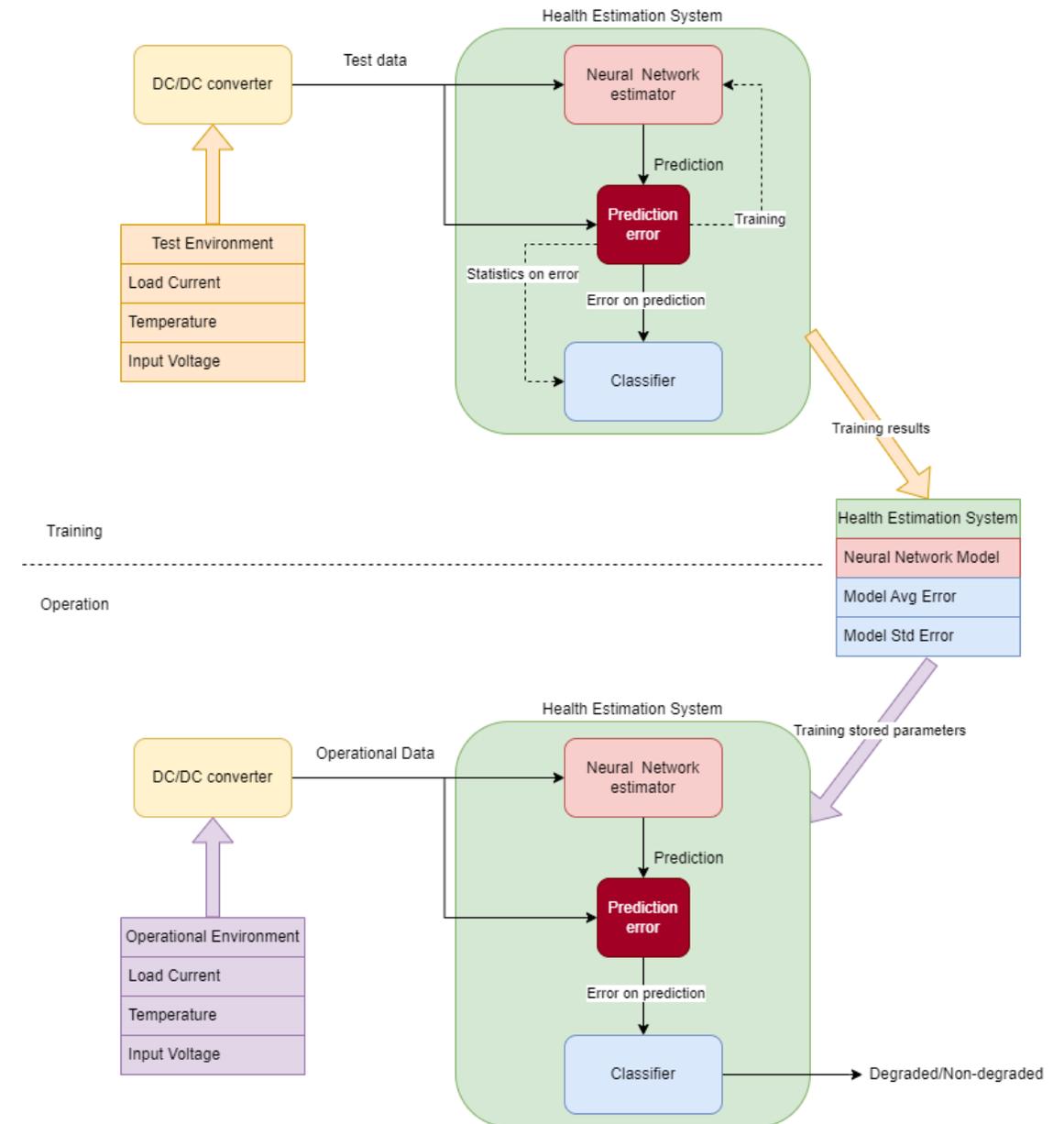
- External errors (measurement, temperature effects...) have not been considered

- No additional measurements needed
 - Input/output power

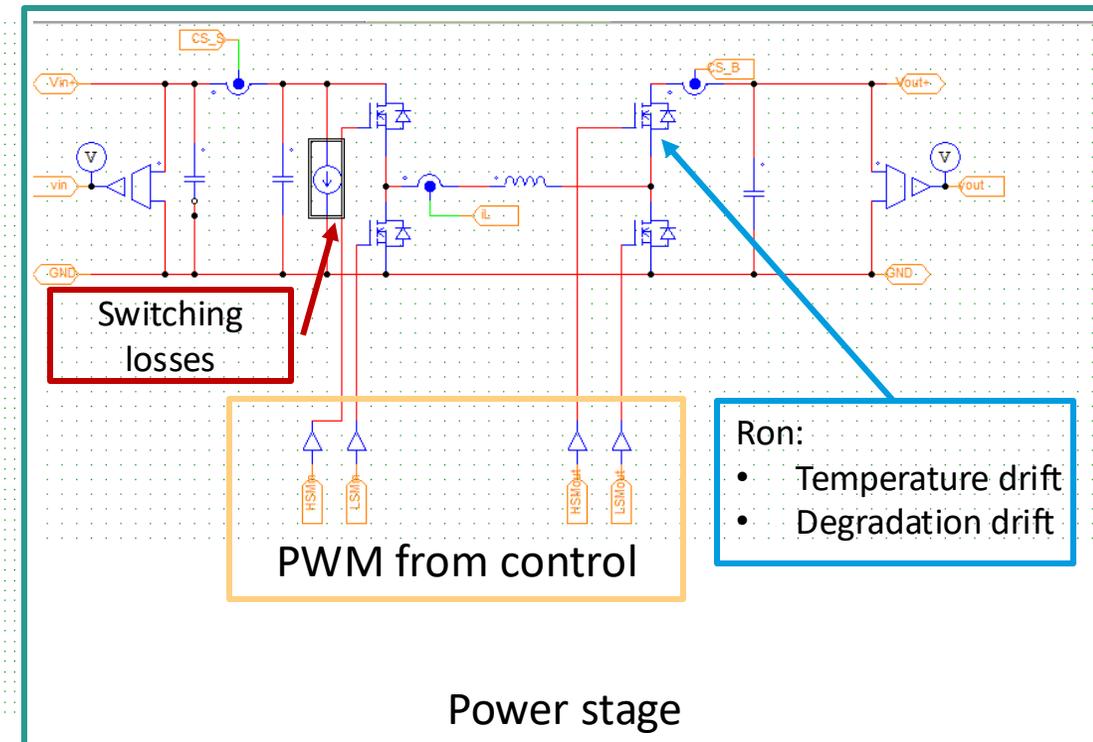
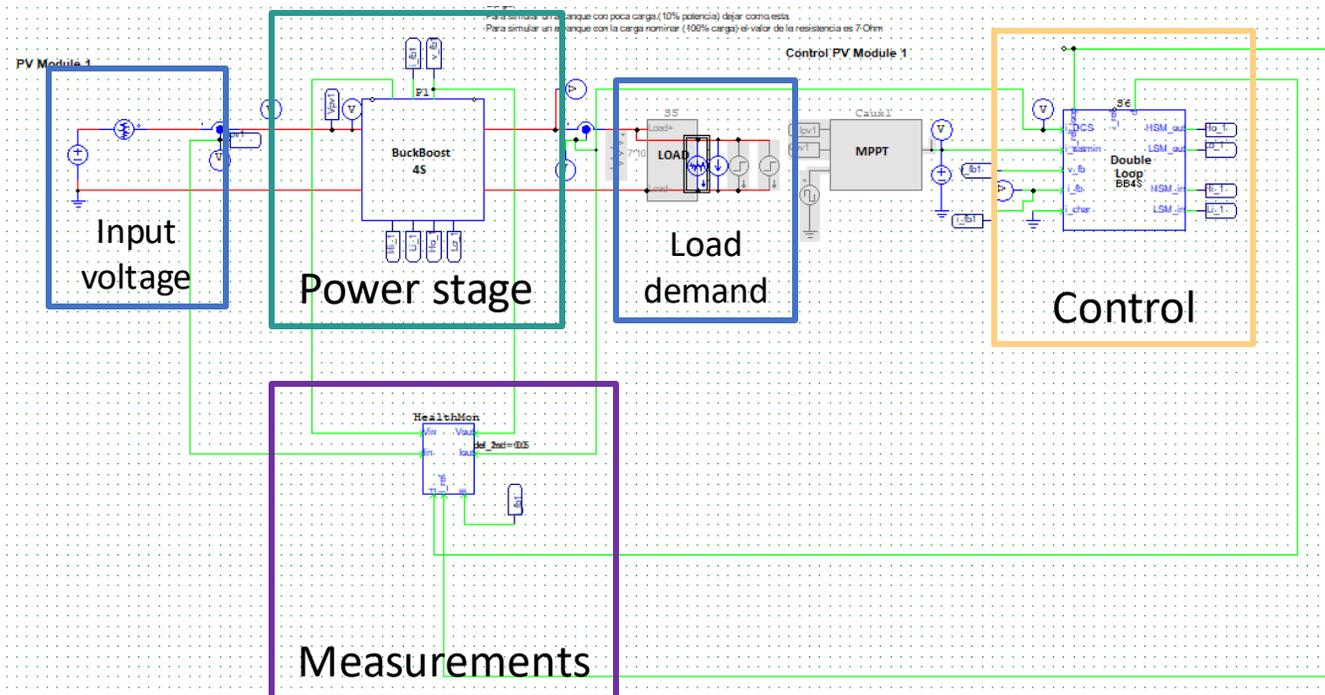
- Machine Learning Approach:
 - Forget about any prior model
 - Just use data to model a healthy converter.
 - Inputs: V_{in} , V_{out} , Temperature, I_{load} , ...
 - Outputs: Duty cycle command, inductor current ripple,
 - Neural Network fits the input data to the output. Generate a model of the converter.
 - Degradation-> Difference between model and measurements.
 - Significant difference: More than 1 standard deviation from average.



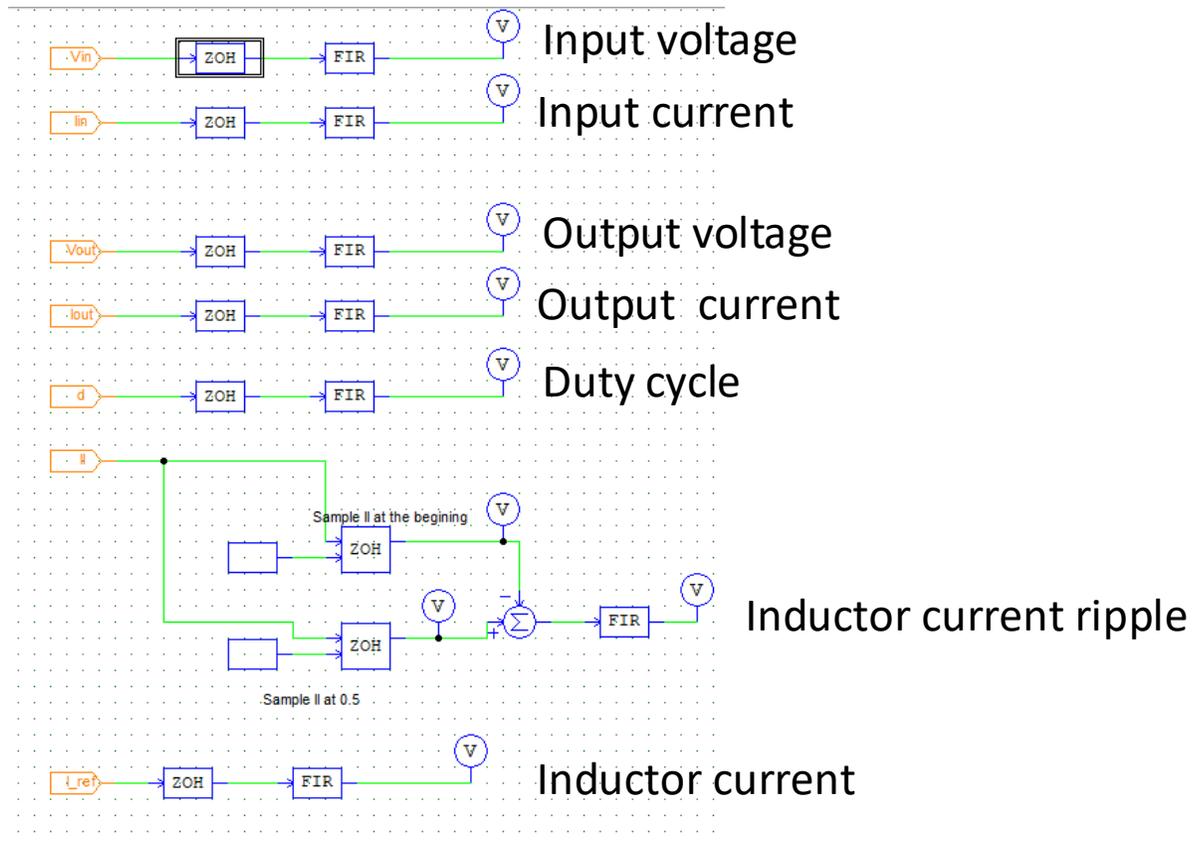
- Utilization of the approach
 - The model is specific for each unit.
 - The data could be qualification data
- Results of the activity
 - Input data identified
 - Converter indicators identified
 - Training datasets generated
 - Simulation only
 - Several estimators trained



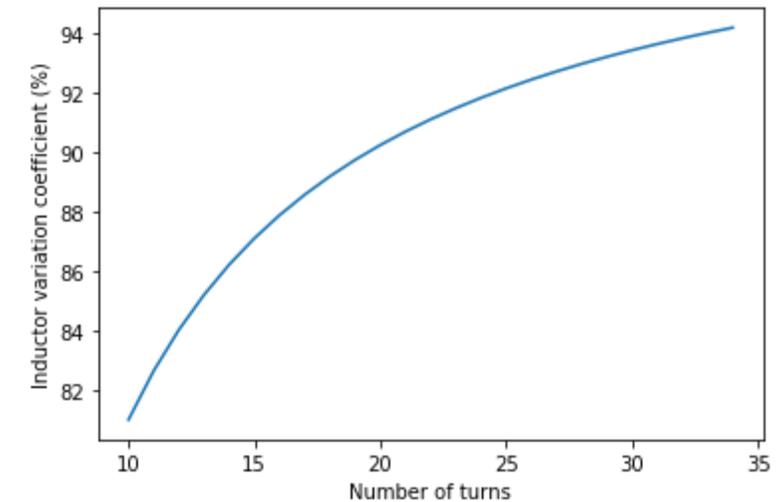
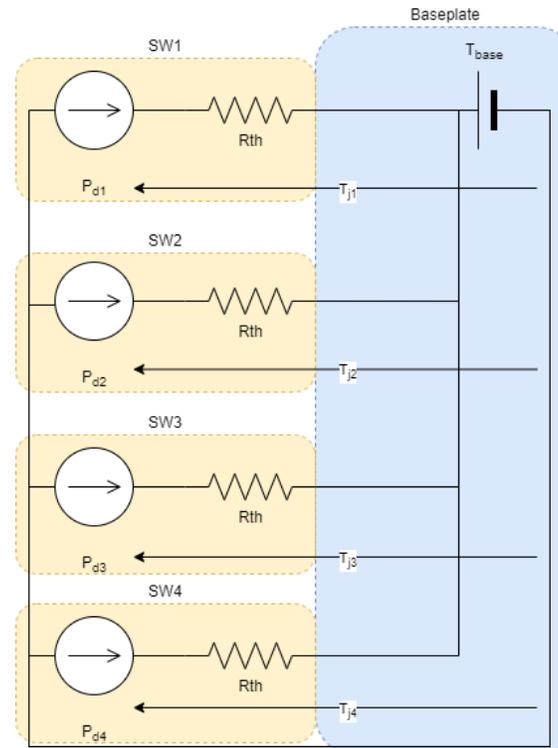
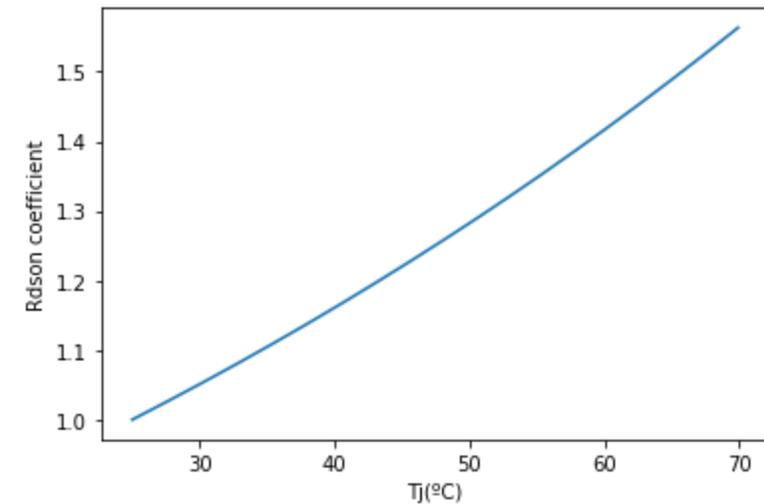
- Dataset generation
 - Module simulation in PSIM. Scripts to vary V_{in} , I_{load} and Temperature
 - Including control scheme
 - Includes temperature effect on MOSFETs
 - Includes switching and driving losses



- Dataset generation
 - Measurements
 - Sampled at the switching rate and filtered



- Dataset generation
 - r_{ds_on} varies with temperature
 - Approximation of conduction and switching losses
 - Simple thermal model for switches
 - Degradation modelled as an increase of the r_{ds_on}
 - Inductor change only for a loss of 1 turn.
- Goal of model: Provide data. The data may not reflect accurately the reality.



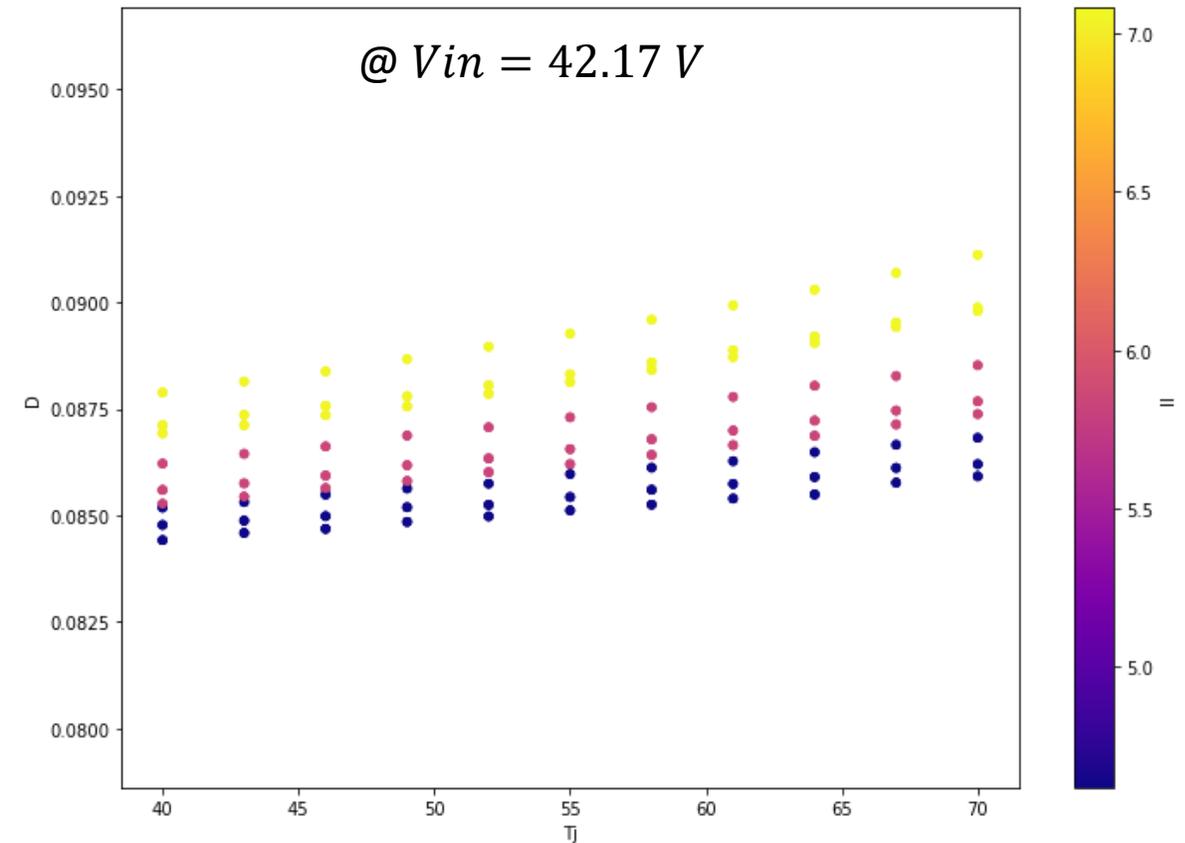
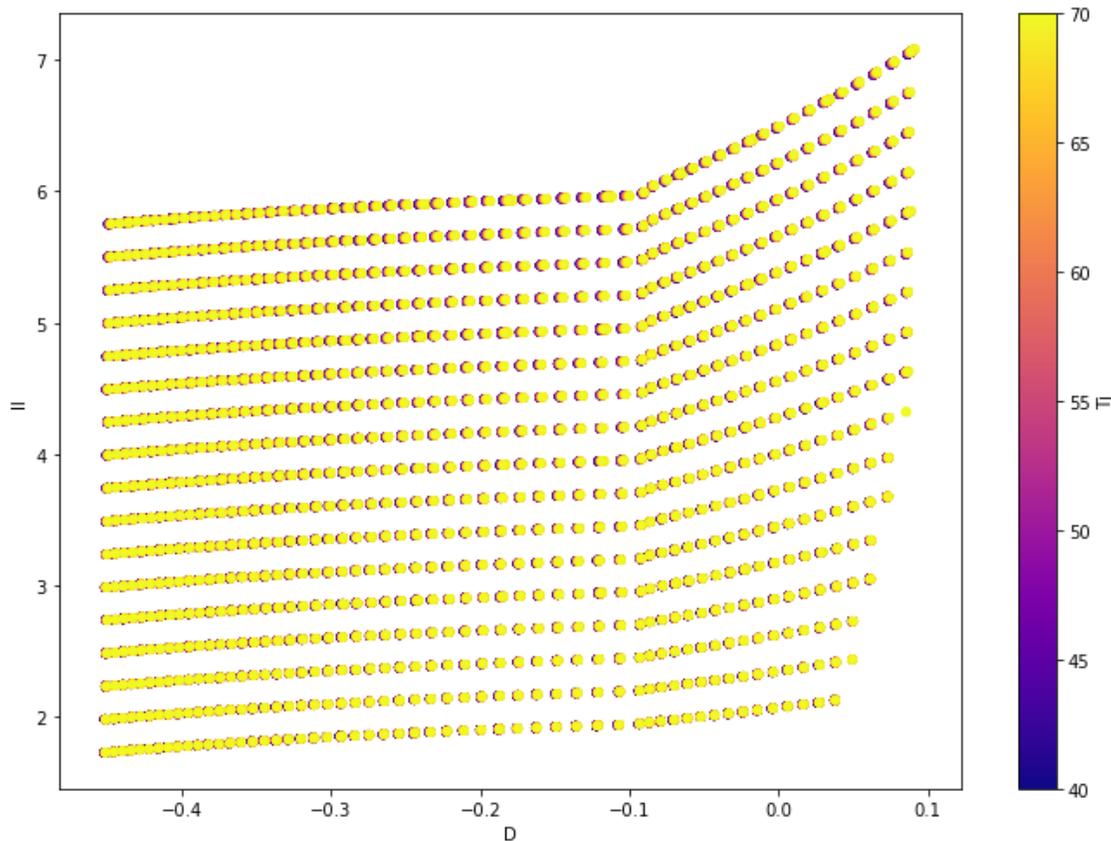
- Dataset generation
 - Change in r_{ds_on}
 - Converter labelled as degraded or non-degraded.
 - Non-degraded converters: increase in $r_{ds_on} < 25\%$.
 - Degraded converters: $1.5 \cdot r_{ds_on_nominal} \geq r_{ds_on} \geq 1.9 \cdot r_{ds_on_nominal}$.
 - Change in inductance
 - Converter labelled as degraded or non-degraded.
 - Nominal inductance: $84 \mu H$
 - Degraded converters: Inductance lower than $84 \mu H$. Minimal $67.2 \mu H$
- Training is only performed over non-degraded data.

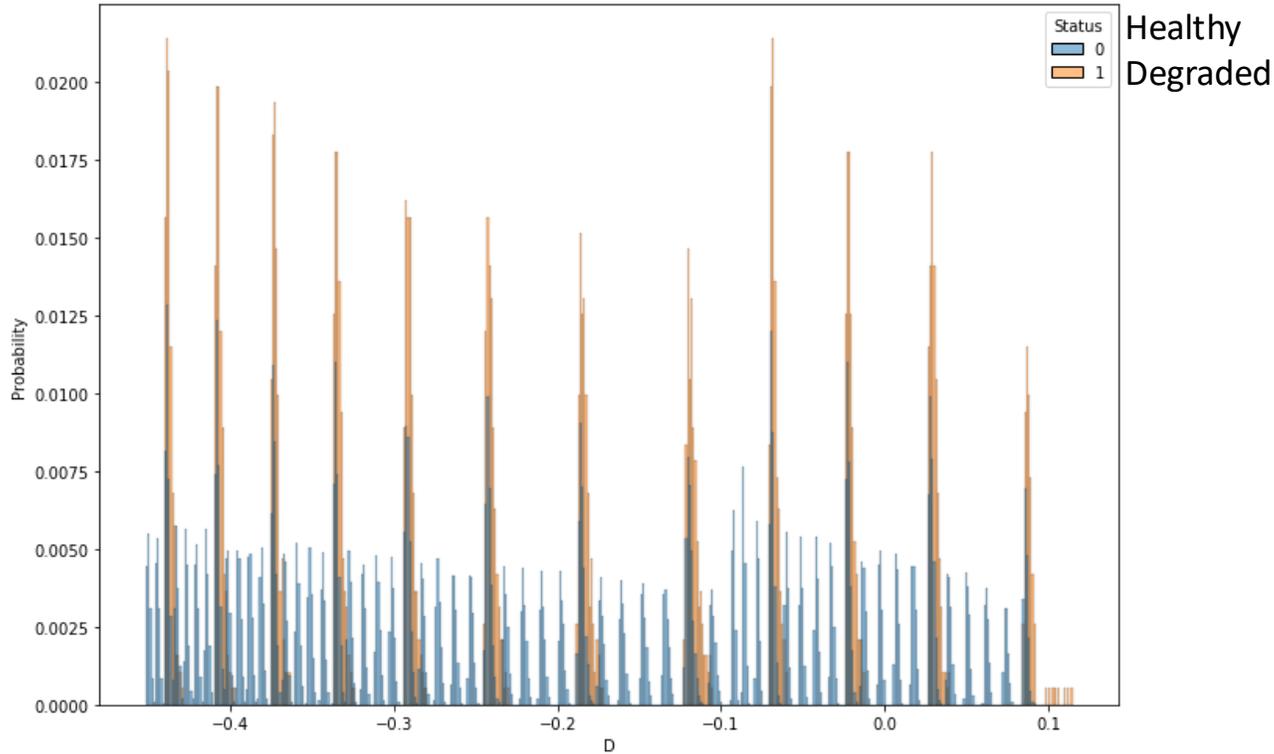
- Data for training:
 - 80% Training and Validation - 20% Test
 - Training and Validation: 80% Training 20% Validation
 - Select a data subset 80% Training and Validation - 20% Test for each of the temperatures in the test
 - Merge all the subsets
 - All the temperatures are represented in the dataset.

- Data for training:

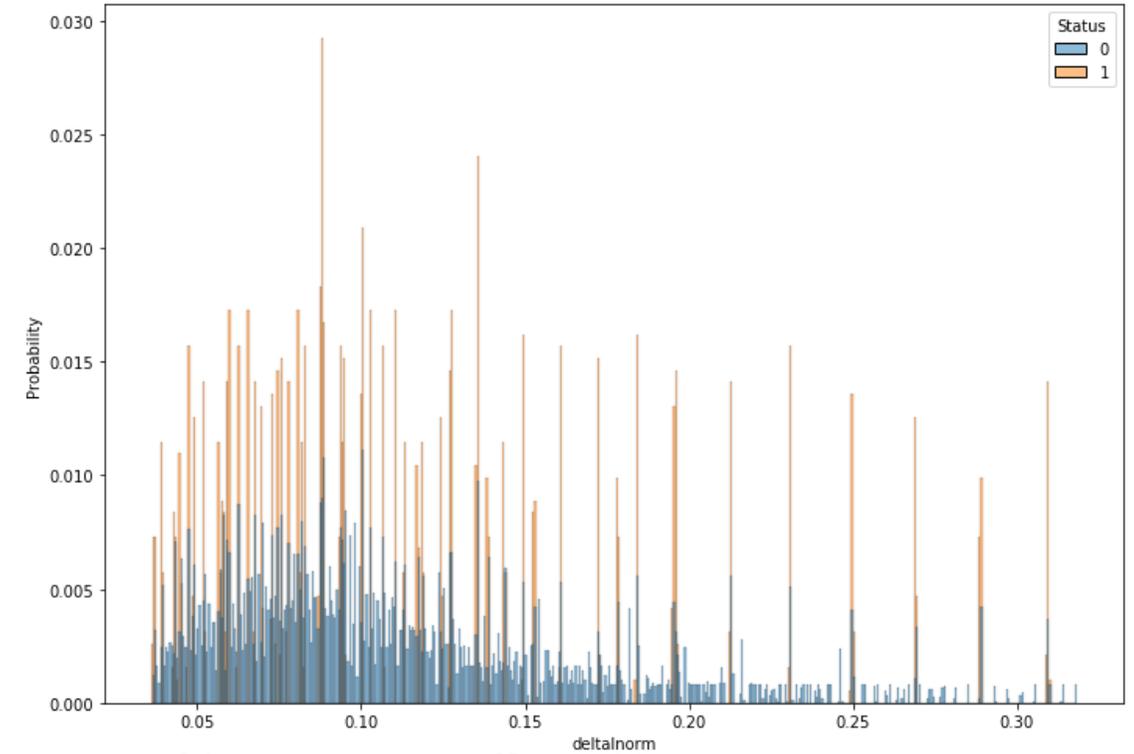
- $V_{in} = 42 V$ and $V_{in} = 100 V$. $\Delta V_{in} = 1 V$
- $I_{load} = 2 A$ and $I_{load} = 6 A$. $\Delta I_{load} = 0.25 A$.
- $T_{base} = 40 ^\circ C$ and $T_{base} = 70 ^\circ C$. $\Delta T_{base} = 1 ^\circ C$. For evaluation $\Delta T_{base} = 3 ^\circ C$
- r_{ds_on} increase between 0 and 0.25 for training.
- r_{ds_on} increase between 0 and 0.9 for evaluation.
- Inductance between $67.2 \mu H$ and $84 \mu H$. $\Delta L = 0.1 \mu H$

- Converter outputs to estimate:
 - Duty cycle
 - Normalized ripple

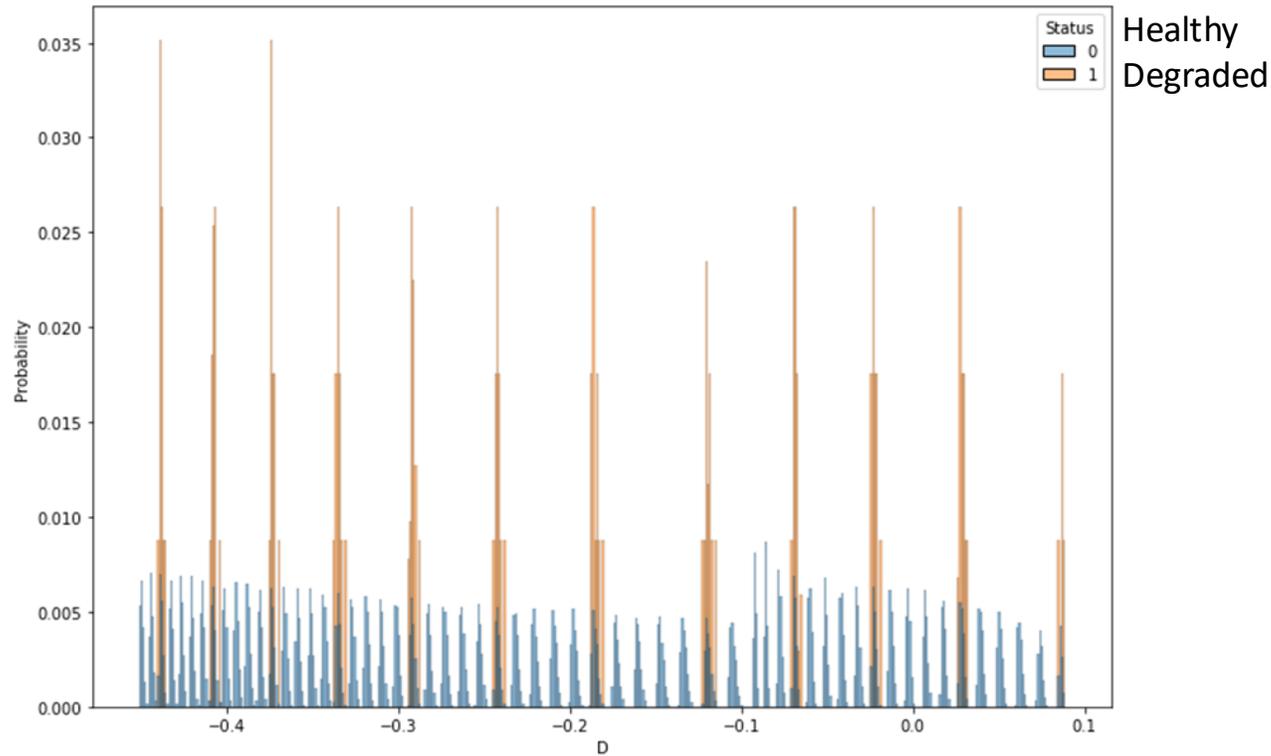




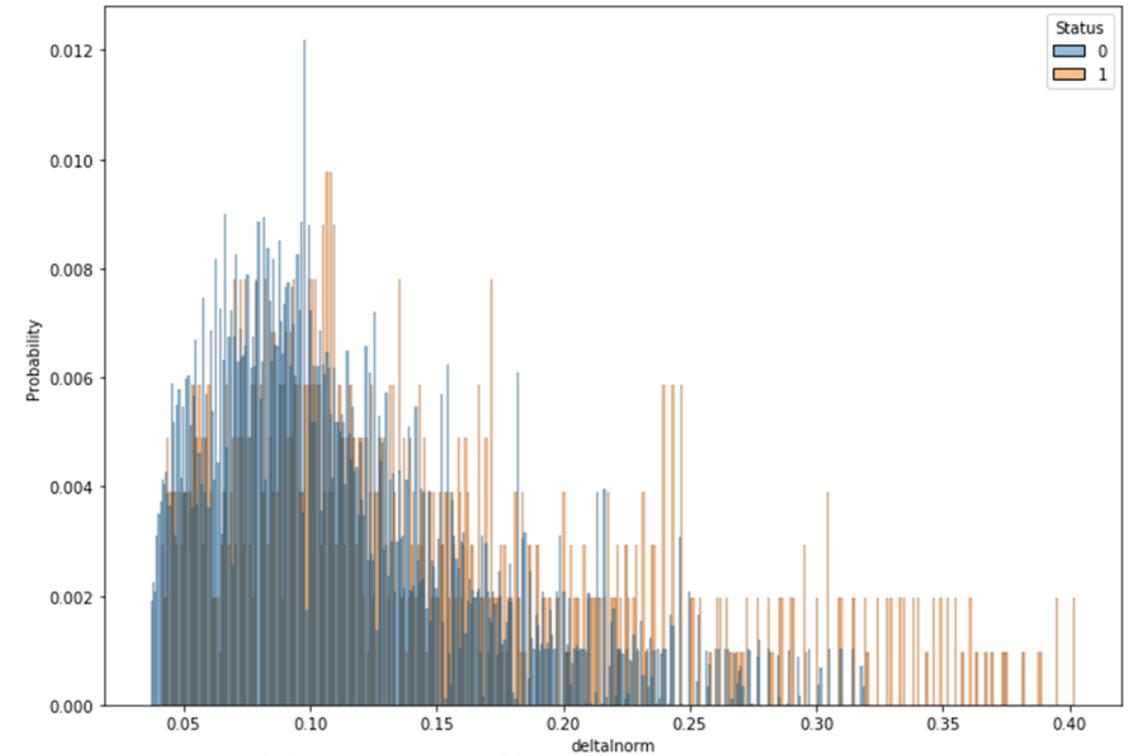
Duty cycle in degraded converters seems higher when r_{ds_on} increases



Δi_{l_norm} is not affected by increasing r_{ds_on}



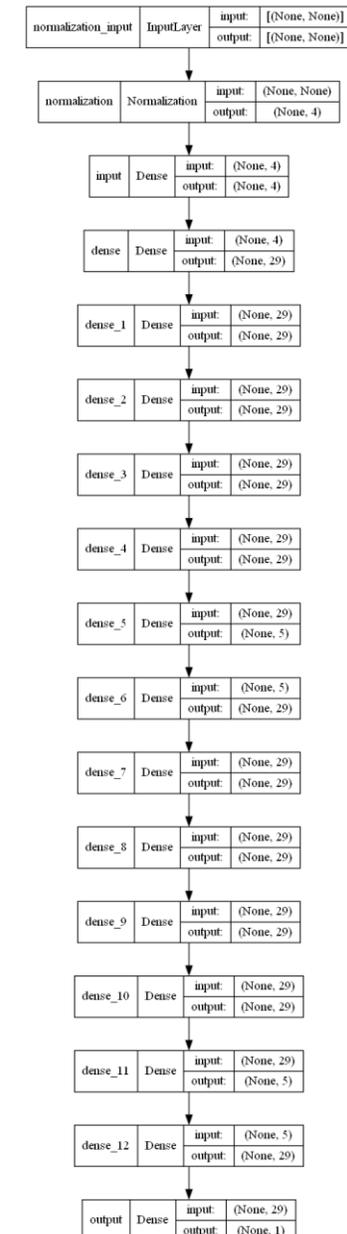
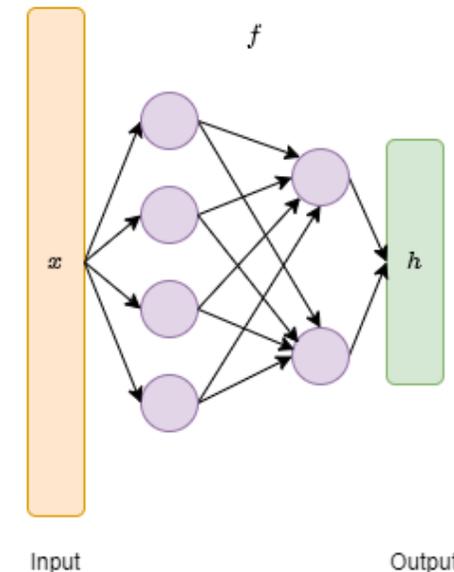
Duty cycle is almost the same when L changes



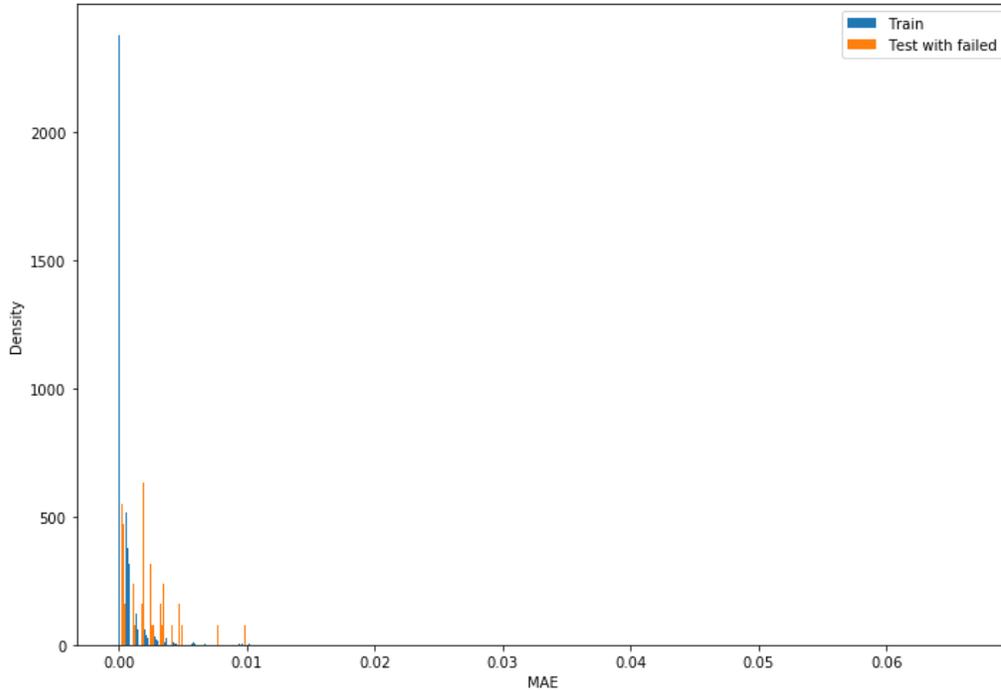
Δi_{l_norm} is affected by changes in L

• NN structure

- Tip: Every few layers constrict the width
- NN as universal function approximators.
 - A network with infinite length has a minimum width of the number inputs plus 1.
- Depth and width are free parameters
- We constrict the network each 6 layers (free parameter)
- Trial and error 13 layers, 29 neurons per layer, shrink to 5 every 6 layers)
- Activation function Rectified Linear
- Single output
 - A NN for estimating D
 - A NN for estimating Δi_{l_norm}

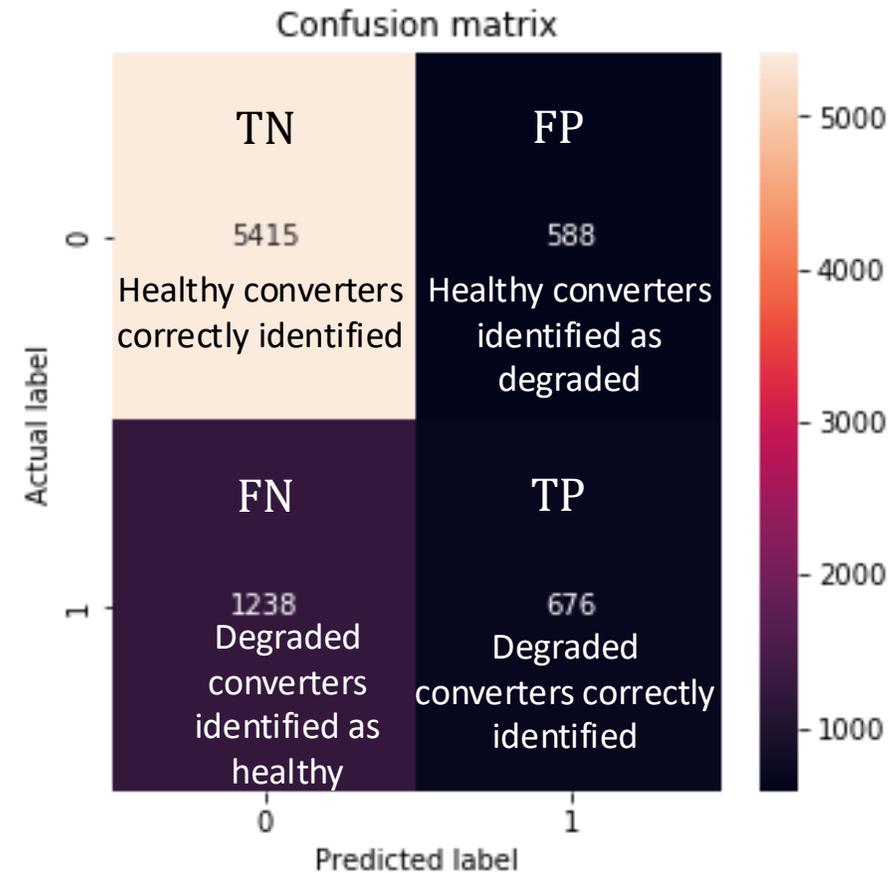


- Results:
 - Identifying r_{ds_on} degradation through D cycle estimation



Mean absolute error in training dataset

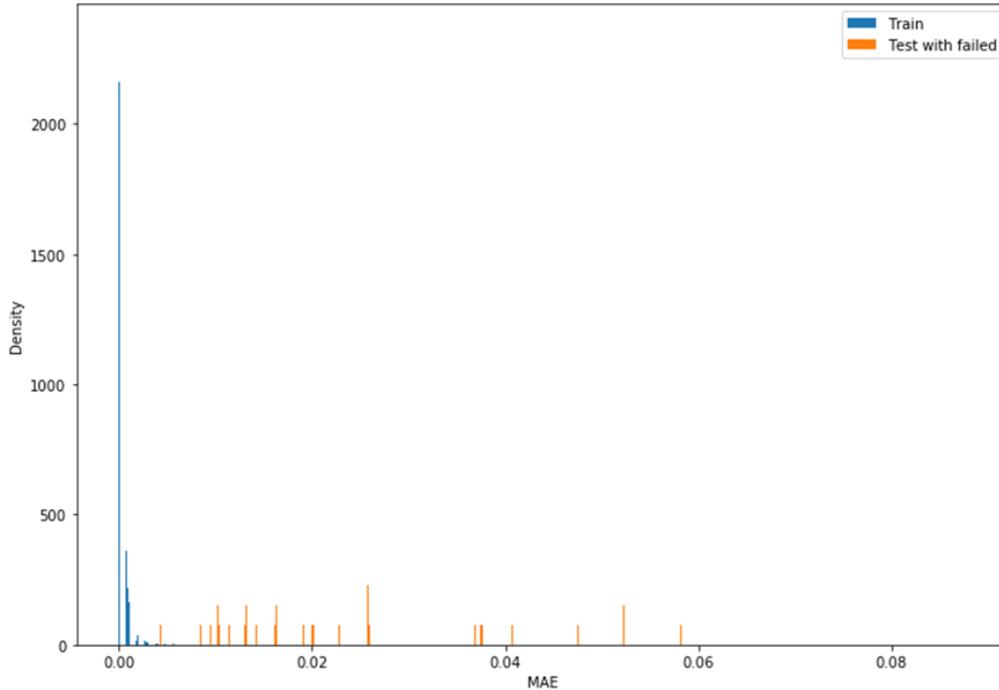
Mean absolute error in test dataset with degraded converters



$$BA = \frac{1}{2} \cdot \left(\frac{TP}{TP + FN} + \frac{TN}{TN + FP} \right) = 62\%$$

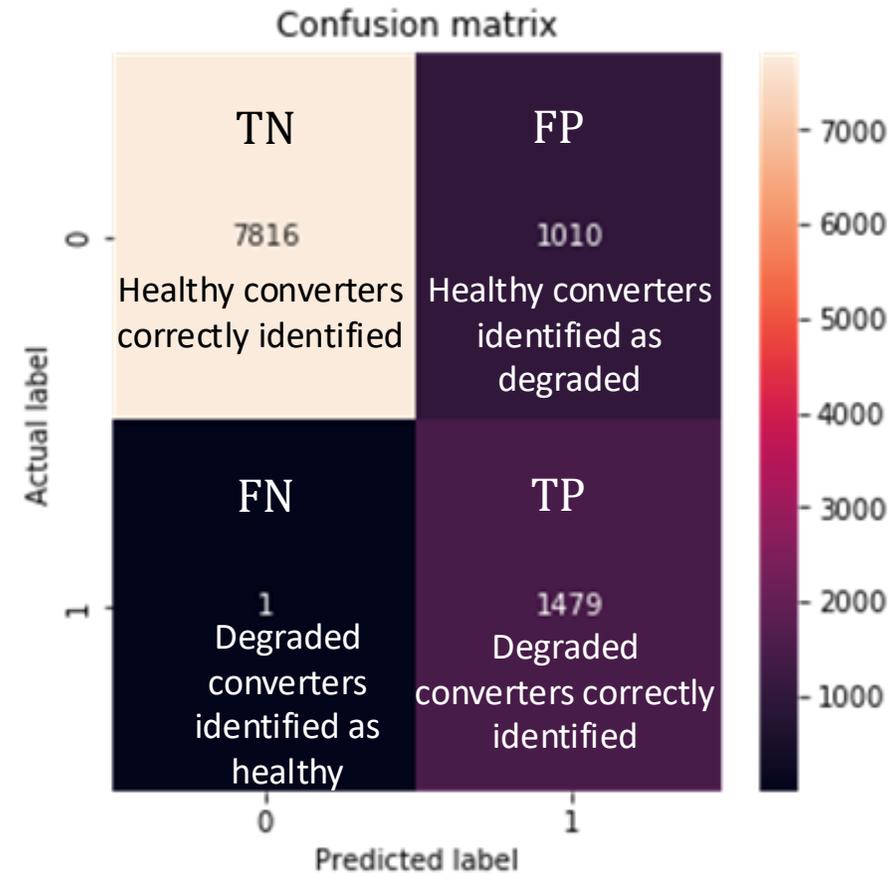
Much better results when r_{ds_on} increase duplicates.

- Results:
 - Identifying L degradation through Δi_{l_norm} estimation



Mean absolute error in training dataset

Mean absolute error in test dataset with degraded converters

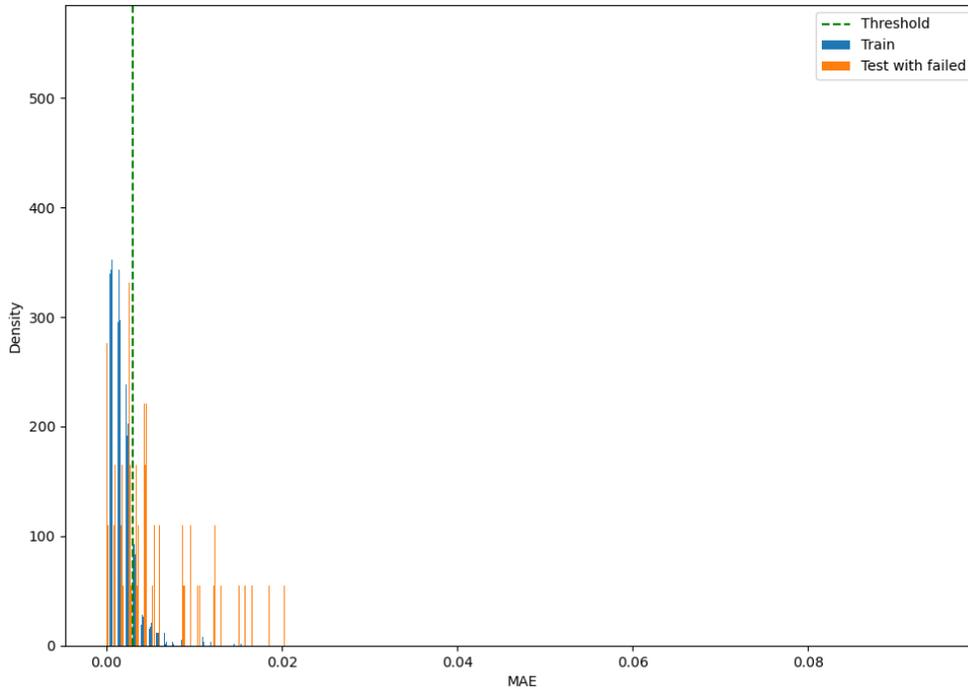


$$BA = \frac{1}{2} \cdot \left(\frac{TP}{TP + FN} + \frac{TN}{TN + FP} \right) = 98.7\%$$

- Conclusions at the time of submitting the final report:
 - Changes in r_{ds_on} imply very subtle changes in Duty cycle.
 - The approach works well with bigger changes
 - Bigger increase in r_{ds_on}
 - Changes in Δi_{l_norm} due to L changes
- Before the final presentation changes were made
 - Activation function tanh
 - Inclusion of normalization stages
 - Amplify the duty cycle changes through estimating $e^{(1+D)}$

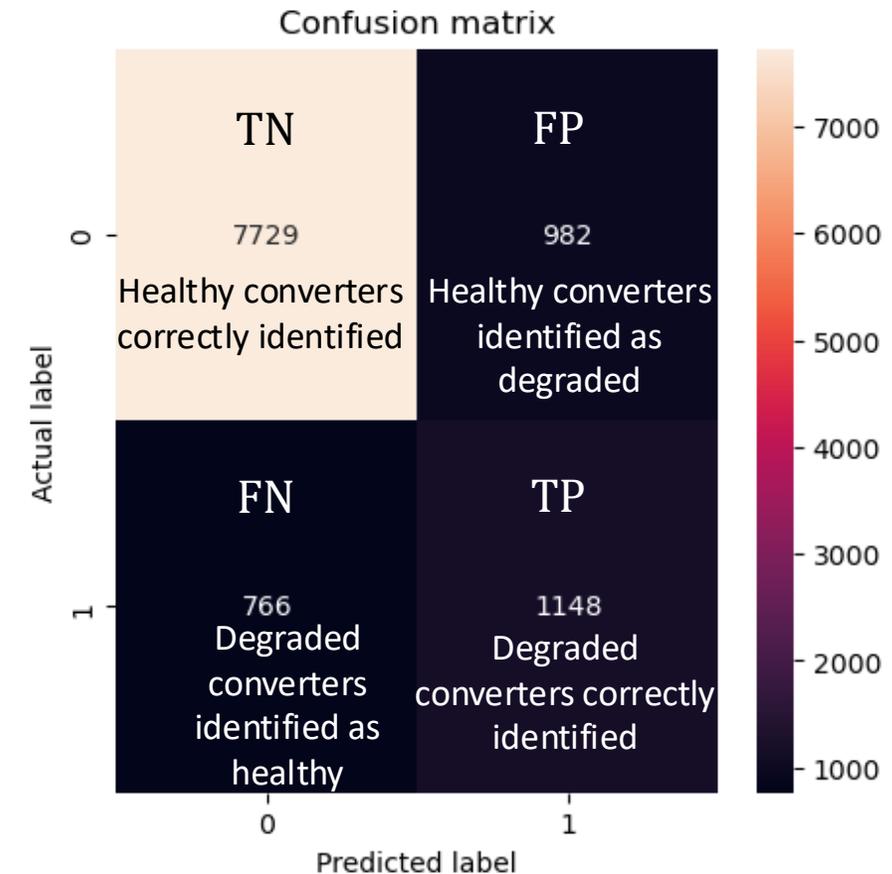
- Results:

- Identifying r_{ds_on} degradation through $e^{(1+D)}$ cycle estimation



Mean absolute error in training dataset

Mean absolute error in test dataset with degraded converters



$$BA = \frac{1}{2} \cdot \left(\frac{TP}{TP + FN} + \frac{TN}{TN + FP} \right) = 74.3\%$$

Much better result. However more False Positives

- Conclusions of Machine Learning approach
 - Interesting results (after last changes)
 - Key failure indicators found
 - Much work to be done
 - Real converter data
 - Data resolution
 - NN structure and training
 - System implementation

- Health Monitoring conclusions
 - 3 techniques researched
 - Kalman Filter most mature
 - Manage temperature changes
 - Almost ready for implementation

- Heatmaps and Machine learning promising but at a very low maturity
 - A lot of work needs to be done

- Topology
 - Single power stage
 - 4 switch Buck Boost: SAR, BDR, CDR
 - GaN Based
 - High efficiency
- Decentralized control
 - Based on DC bus signaling
 - 3 roles achieved (MPPT, battery charge,...)
 - Good bus regulation
 - Seamlessly transitions
- Health monitoring
 - 3 techniques researched
 - Premature yet interesting results

Health Monitoring of digitally controlled flexible converters

Thanks for the attention
Questions?



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