DELOS- DEveLopment Of a rad-hard repeater, multiplexer and Switch IC for high-speed communication

Contract N°4000133309/20/NL/AS

Executive Summary Report

ACRONYMS/ABBREVIATIONS

AR	Acceptance Review
ASIC	Application-Specific Integrated Circuit
ATE	Automatic Test Equipment
BER	Bit Error Rate
BS	Bit Stream
BU	Business Unit
CDR	Critical Design Review
CM	Configuration Memory
DDR	Detailed Design Review
DFF	D-type Flip Flop
DFT	Design For Test
DGA	Direction Générale de l'Armement (France)
DSM	Deep Sub-Micron
DSP	Digital Signal Processing
EKR	Evaluation Kit Review
FAE	Field Application Engineer
FTR	Final Test Review
HSSL	High Speed Serial Link
IBP	Imaging, BiCMOS ASIC & Silicon Photonics
IC	Integrated Circuit
IOB	Input Output Buffer
IOS	Input Output System
IP	Intellectual Property
KO	Kick Off
LSI	Large System Integrator
LUT	Look up Table
MPW	Multi Project Wafer
NX	NanoXplore
PCB	Printed Circuit board
PDR	Preliminary Design Review
PHB	Programmable Hardware Block
PLL	Phase Locked Loop

Table of Content

1 Objectives

Objectives of the DELOS project are based on the requirement shared during its preparation, which are: Design, develop, manufacture, and validate a radiation hardened prototype Integrated Circuit (IC). IC implements repeating, multiplexing and switching functions for high-speed link communication up to 6.25 Gbps and which is compliant to the SpaceFibre ECSS standard.

The Accepted Proposal was: Serial Link Crossbar based on NanoXplore HSSL IP on 28nm FDSOI technology.

- Architecture based on existing NX HSSL IP.
- Mixed design re-timing architecture using Digital Switch matrix (Crossbar).
- SPI interface for configuration.
- Less than 16mm2 die are -> CGA 144 or PBGA 144 packaging.

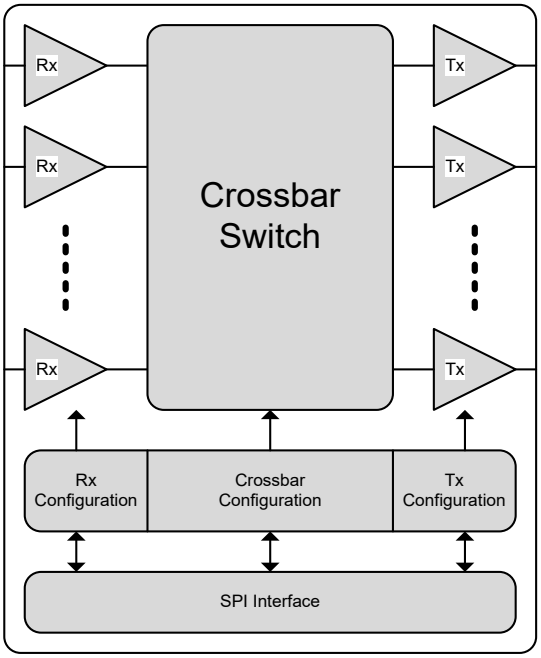

Figure 1: Functional architecture

2 Description of the work performed

2.1 Requirements Consolidation & Specification

The DELOS crossbar switch specifications and requirements included requirements for IPs, clock specifications, and radiation performance, allowing NanoXplore to develop a Cross-Bar Switch Development Plan for addressing the tasks. The Plan was structured as follows:

- ✓ **Analog Development**: To focus on designing the LDO voltage regulator using a standard analog design flow.
- ✓ **Digital Development and Integration/Validation**: To include the design of the SPI controller, an evolution of NanoXplore's existing controller, and the digital crossbar switch, which is to follow a digital design flow and be emulated on NG-ULTRA FPGA for risk mitigation.
- ✓ **Package Development**: To conduct in partnership with a subcontractor, with validation managed by NanoXplore's Manufacturing and Test Team.
- ✓ **Board Development and Bring-Up**: To involve the PCB design by NanoXplore's team.

The DELOS chip incorporated the reuse of NanoXplore's 28nm FDSOI HSSL IP, requiring only integration tasks for this component. The SPI interface utilized NanoXplore's 28nm FD28SOI LVCMOS I/Os, and the HSSL integration was conducted at the subsystem level.

On the industrialization aspects, NanoXplore has a strong partnership with STMicroelectronics (STM) to ensure a robust supply chain. This supply chain, used previously for NanoXplore's NG-LARGE and NG-ULTRA FPGAs, employed STM's space supply chain and qualification flow, combining expertise across multiple sites to meet stringent quality standards.

2.2 Architectural definition

The die design architecture is presented from a global view as block diagrams. The chip interface, functional requirements as well as environment constrains and die layout considerations are detailed. XSWITCH-16 is a configurable HSSL cross-switch Application Specific Integrated Circuit (ASIC) allowing bi-directional operation through 4 quads of 4-RX/4-TX serial link per QUAD.

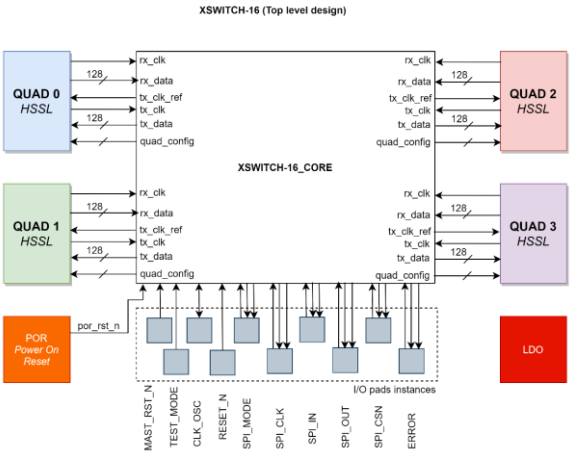

Figure 2: XSWITCH-16 Block Diagram

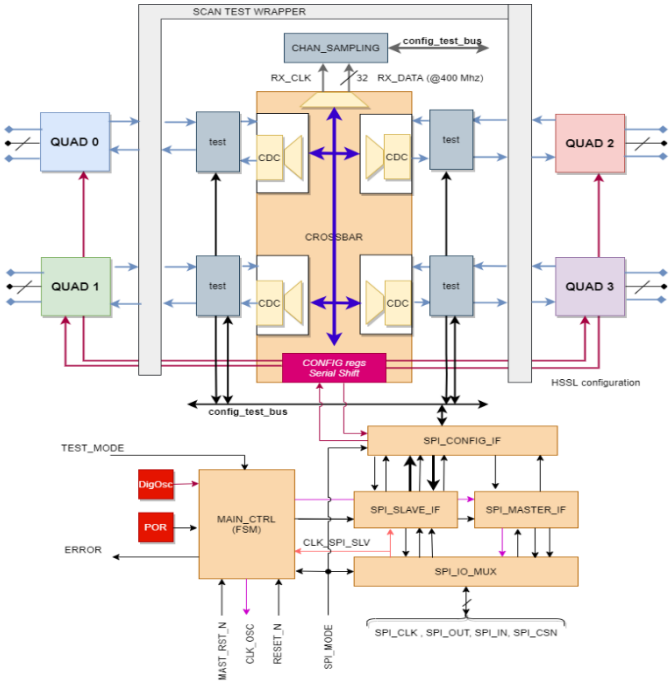

Figure 3: XSWITCH-16 digital part detailed block diagram

LDO Regulator:

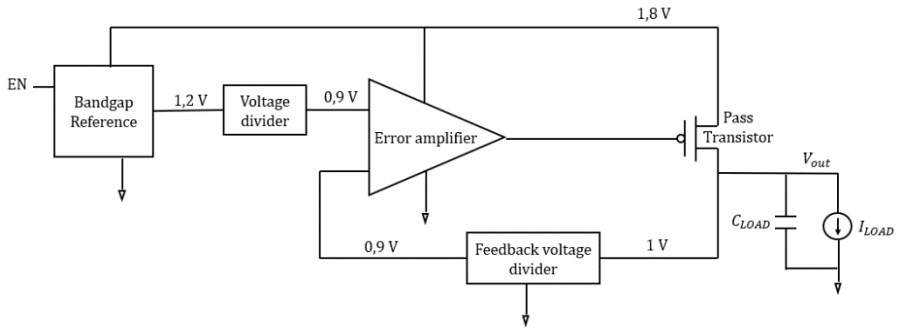

Figure 4: XSWITCH-16 LDO regulator

To offer to the end-user, the possibility to reduce external supply components on board, XSWITCH-16 uses on-die LDO. The figure above presents Capacitor-less LDO scheme allowing to generate stable 1.0V voltage from 1.8V input voltage.

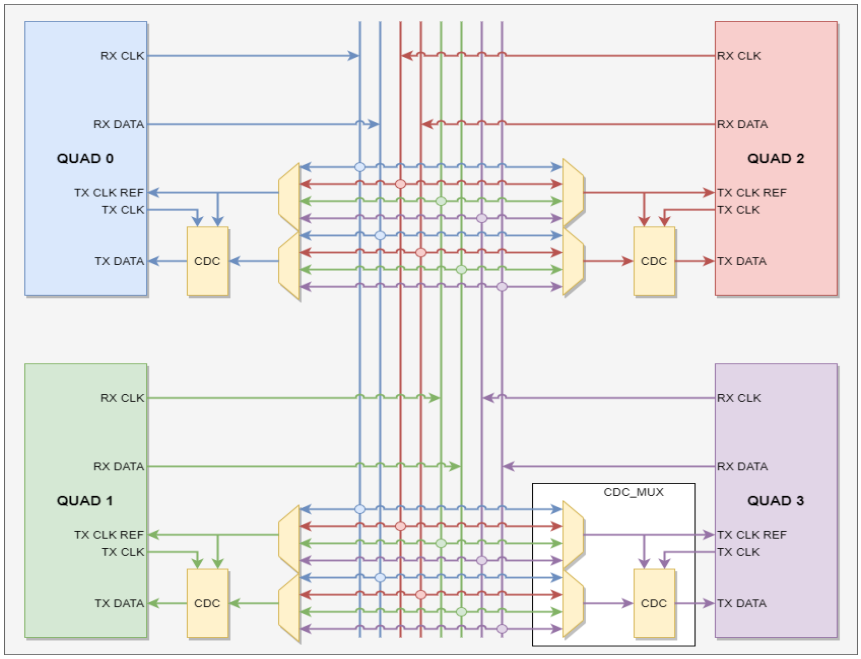

Figure 5: Digital crossbar switch bloc diagram

2.3 PCB Design

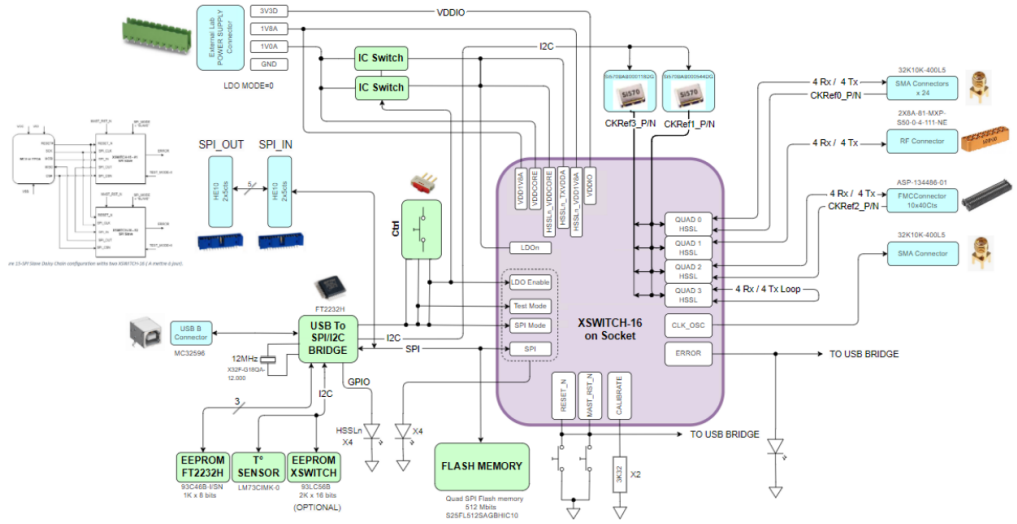

Figure 6: Devkit functional block diagram

NanoXplore's XSWITCH-16 DevKit V1.0 board offers a use case environment for our XSWITCH-16 device. Indeed, a Dual Chanel USB to SPI and I2C bridge, based on FTDI FT2232H device, allows user to communicate through an USB-B connector with our socket mounted 15x15mm FCBGA196 XSWITCH-16. FT2232H SPI channel can configure XSWITCH-16 device, while I2C channel can

activate and program 2 stable 100MHz to 200MHz (156.25MHz by default) VCXO (U2, U3) offering HSSL Differential reference clocks (HSSL01_CKREF_N/P and HSSL03_CKREF_N/P).

XSWITCH-16 DevKit V1.0 board embeds an optional (U7) EEPROM (93C46-I/SN 1K x 8 bits) configurable over the USB interface and dedicated to FTDI FT2232H device allowing an operational configuration mode and USB description strings. A second optional (U6) EEPROM (24LC256-I/SN 16K x 16 bits) with a configurable addressing (J27, J28, J29) is dedicated to XSWITCH-16 device and allows its own USB description strings such as VID, PID Serial Number or Product Description.

As described in the previous figure, each HSSL Bank is available either through SMA connectors (HSSL00), 50 GHz 2x8 Multicoax MXP50 to SK connector (HSSL01), FMC10x40cts connector (HSSL02) or simply Loop-back routed (HSSL03). Note that all HSSL Rx/ Tx are AC coupled with series Broadband capacitors.

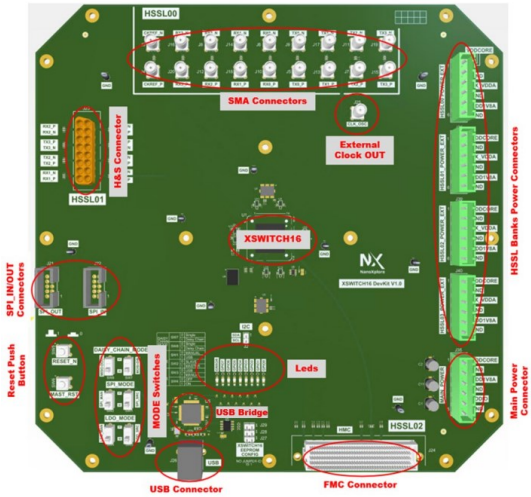

Figure 7: Devkit detailed top view

2.4 Package design

XSWITCH-16 package design was realized by NanoXplore. The design was realized in collaboration with Synergie-CAD (SCAD), Toulouse. SCAD propose package design and assembly services. In the scope of XSWICTH-16 package design, it was guaranteed to have a European package substrate manufacturer.

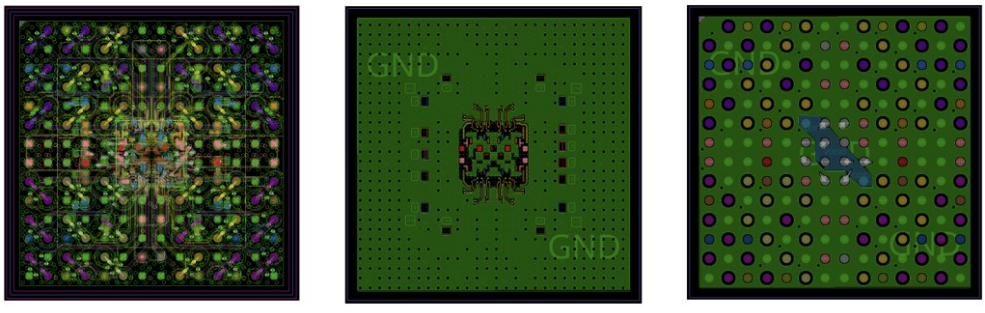

Figure 8: Package design views

XSWITCH-16 Package manufacturing was realized by SCAD and their European sub-contractor for substrate fabrication. Due to the advanced nature of substrate design, several difficulties were encountered during fabrication process. A corrective action report was shared with NanoXplore in November 2023 and details are provided in dedicated deliverables. XSWITCH-16 package die assembly was realized by Synergy-CAD, Toulouse.

Figure 9: Assembled XSWITCH-16 component at NanoXplore

3 Conclusion

The DELOS project exemplifies a thorough and methodical approach to designing a high-performance, reliable solution tailored to meet advanced requirements. It combines precise specifications with established development workflows to ensure seamless integration of complex components. By leveraging NanoXplore's proven expertise in analog and digital design, including the reuse of 28nm FDSOI technologies.

The architecture integrates innovative features such as re-timing and time-shared multiplexing.

As today, due to a design bug discovered in the HSSL IP that is used XSWITCH-16 and the delay in validation of NX FPGA HSSL IP, XSWITCH-16 validation is on-hold. First, the FPGA implementation validation will be completed (performance and radiation) before proposing a version 2 of XSWITCH-16 design.