VHDR

Very High Data Rate Breadboard Receiver for Earth to Lunar Comms

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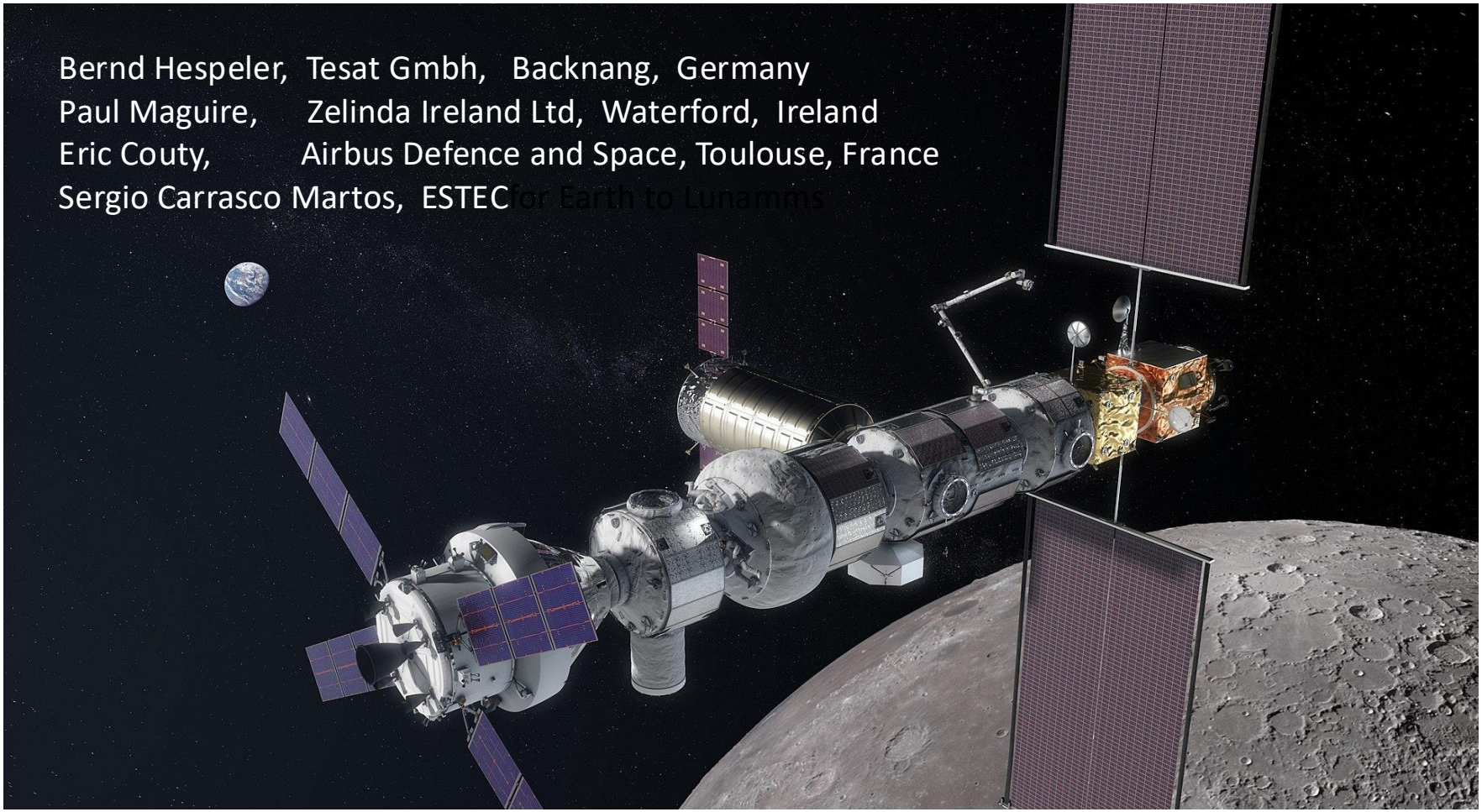


VHDR – Cislunar Space Exploration plan Overview

Lunar Orbital Platform – Gateway (LOP-G)

The next step in Human Space Exploration is a **space station in lunar orbit** intended to serve as

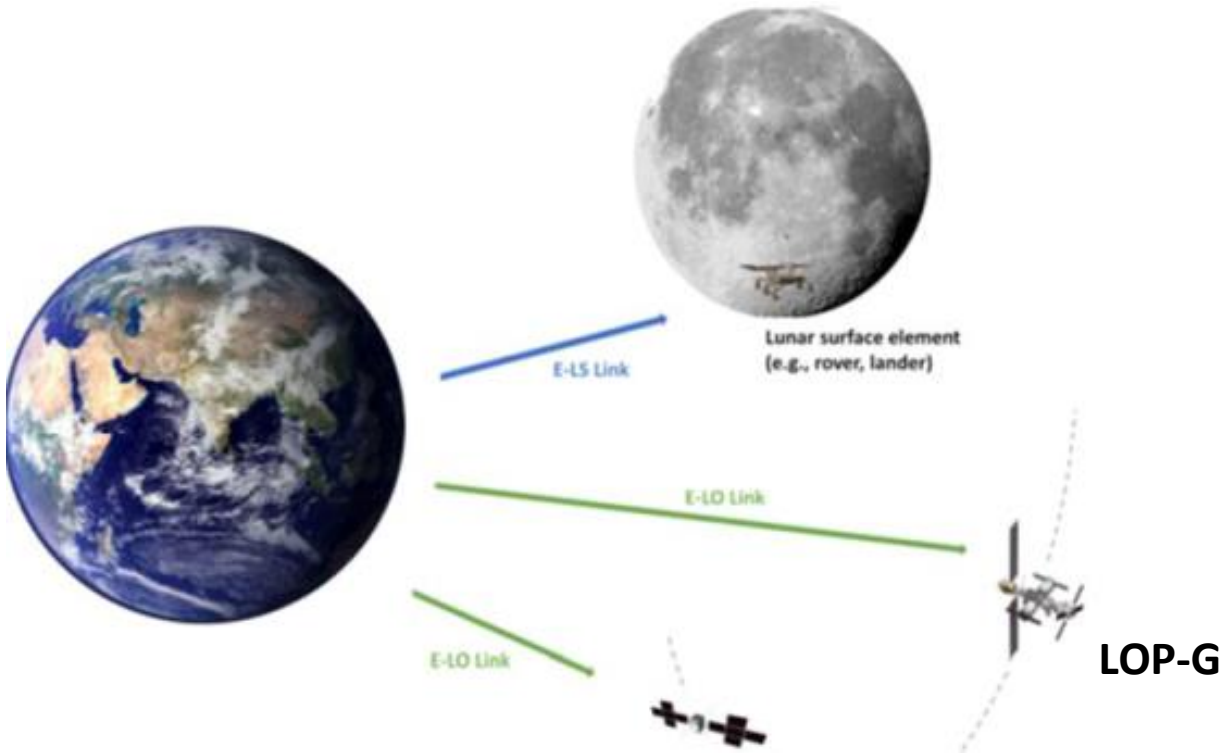
- a communication hub, between Earth, Moon (inc lander, rovers, visiting vehicles) and lunar relay satellites.
- science laboratory,
- short-term habitation module for astronauts,
- transfer station to the exploration of the Moon and Mars

Additionally a constellation of **Lunar Relay Satellites (LRS)** probably in frozen Elliptical inclined lunar orbit (stable for > 10 years without station keeping).

Generic **Lunar surface elements** communicating both direct with earth or with LOP-G or LRS.

VHDR – Comms Links

- All three links require **receivers** for comms from earth (E->LO and E->LS forward links)
- Potential comms links Orbiters to lunar surface also needs **receiver** (LO->LS link).



VHDR – Uplink Comms Requirements

ITU and SFCG recommend **K-band** for high rate Space Research comms in Lunar region, specifically 22.55 – 23.50 GHz.

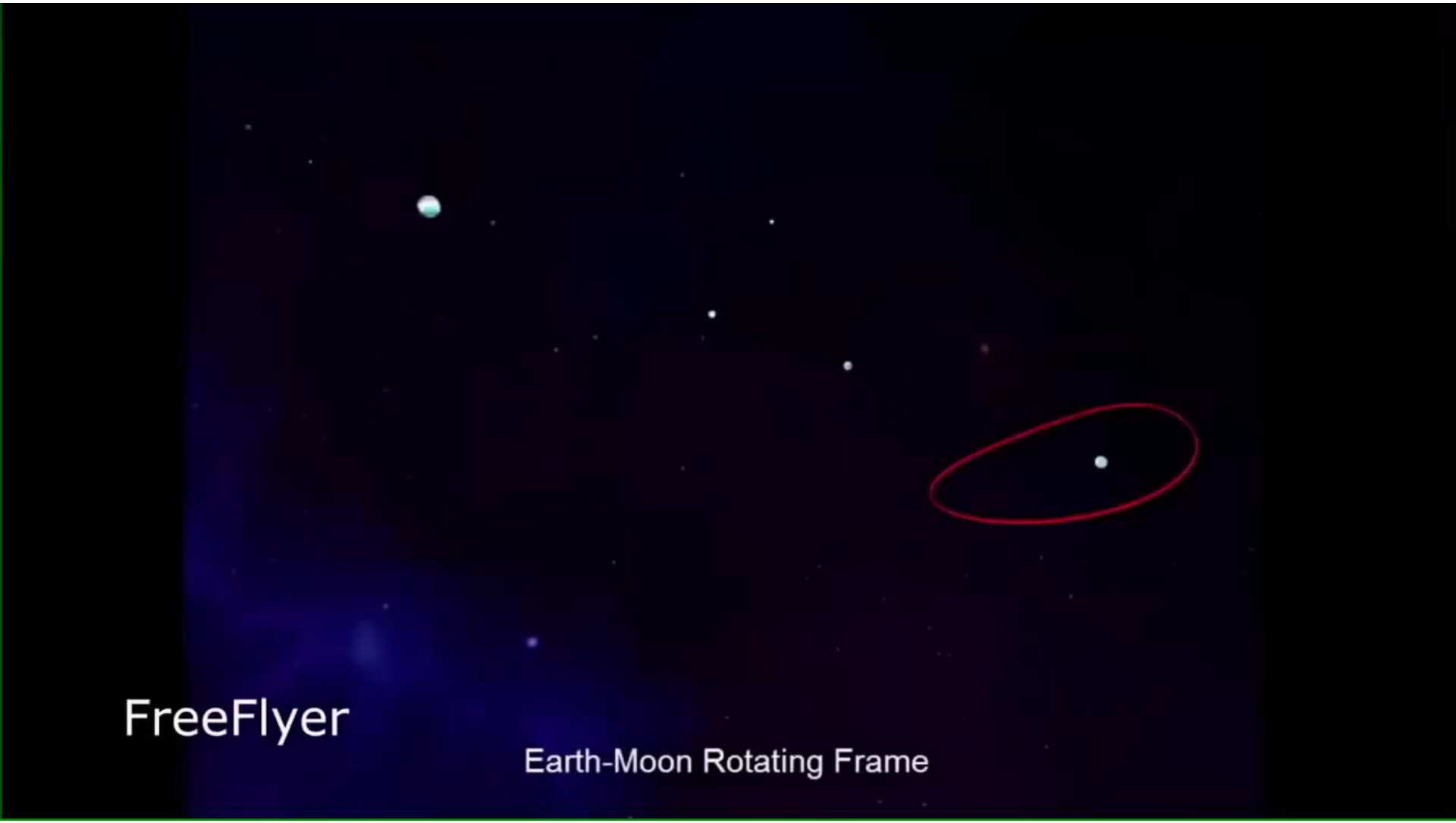
- Bandwidth limited to ~110 MHz
- For bandwidth efficiency SRRC OQPSK modulation (better than GMSK)
- AR4JA LDPC coding (as specified for TM downlink)
- 4 code rates/length combinations (1/2 16k, 2/3 16k, 4/5 16k, ½ 1K)
- Information rates up to 160 Mbps (4/5 code) with 100 Msym/S

To keep operations simple Handover from different ground station should be:

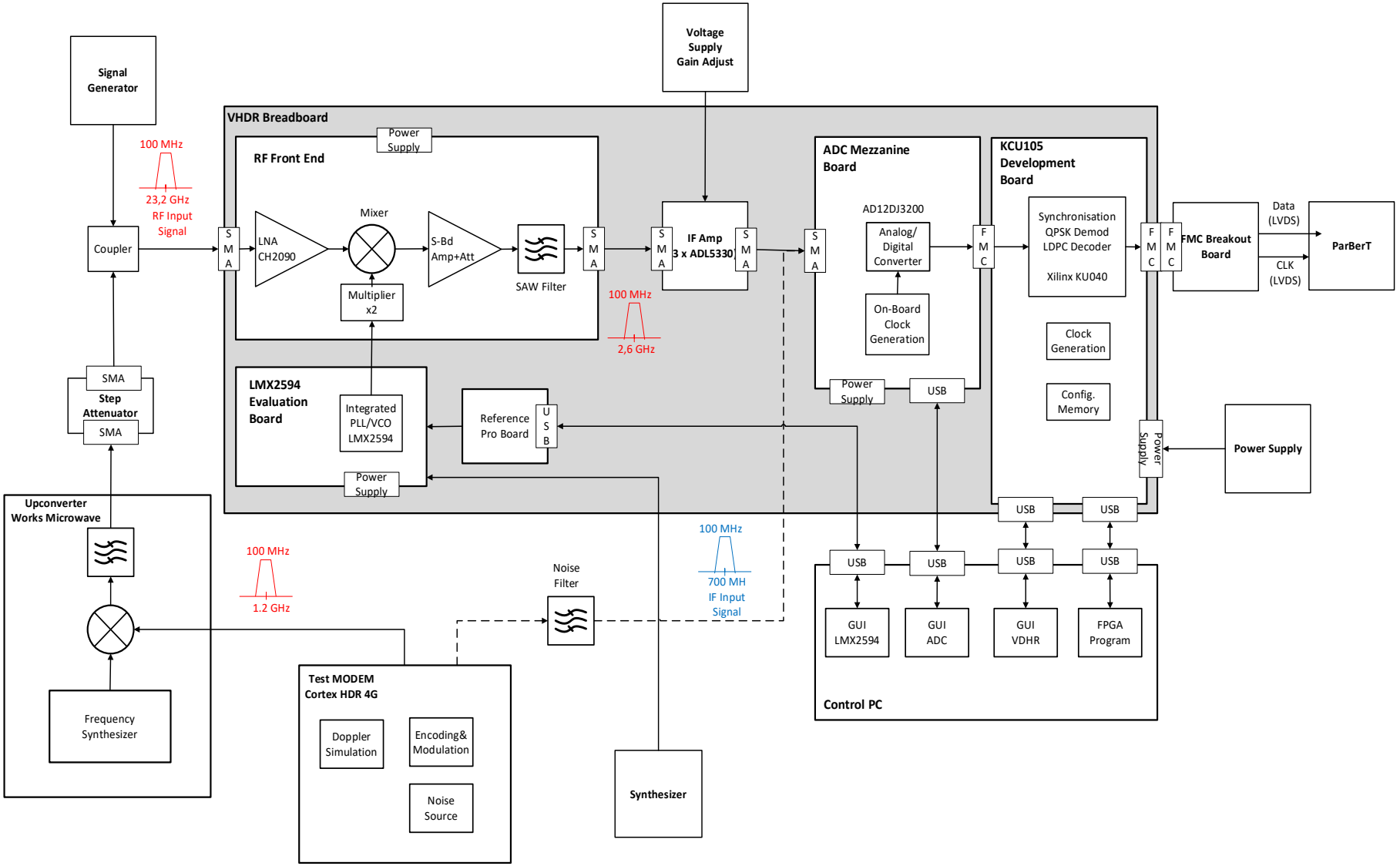
- Autonomous acquisition
- Autonomous data rate detection (from 4 preselected in range 10 -> 100 Msyms/s)
- Autonomous code rate detection
- Autonomous block length detection
- Fade mitigation

VHDR – LOP-G orbit Near Rectilinear Halo Orbit (NRHO) Animation

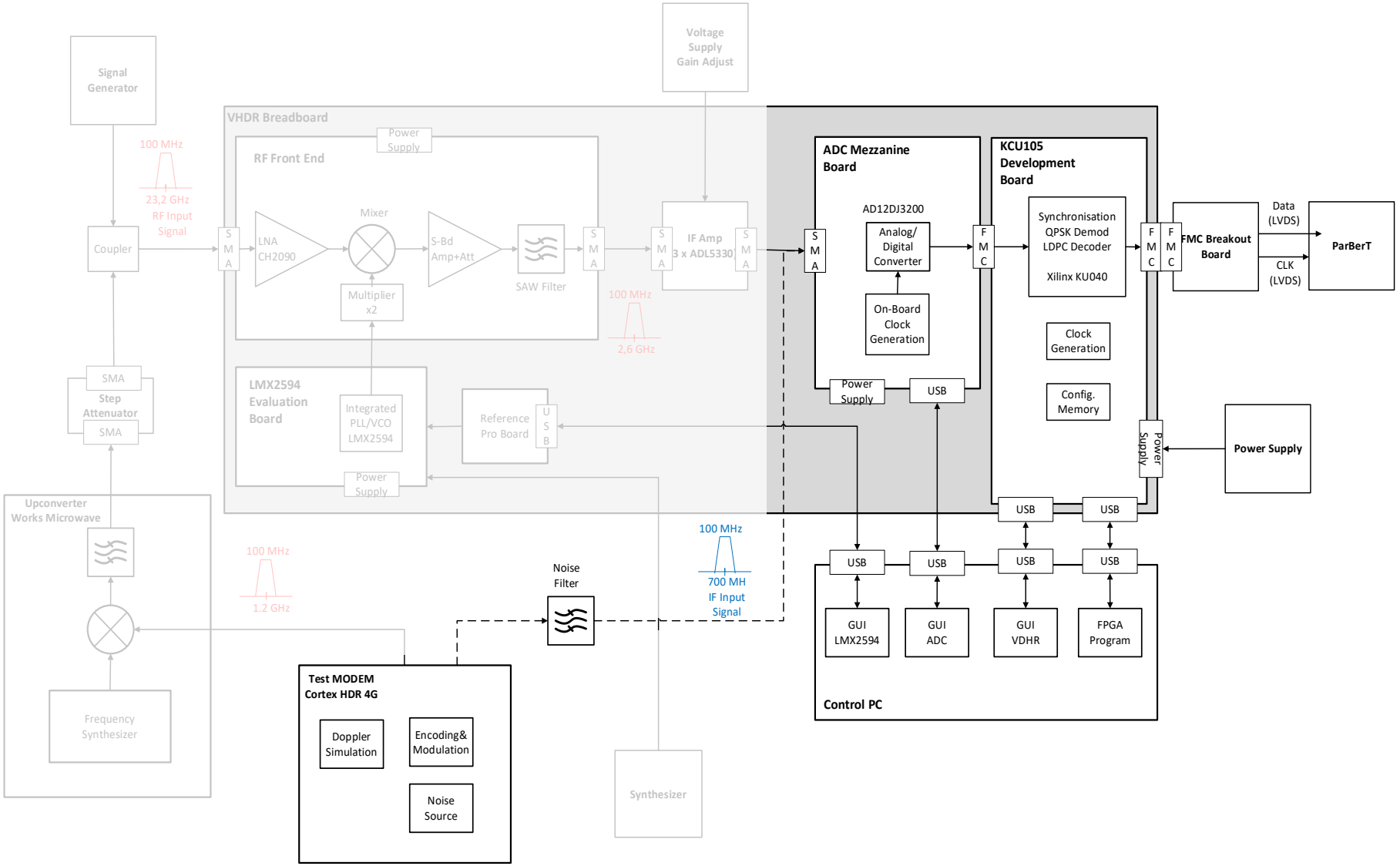
Earth L1 Moon L2



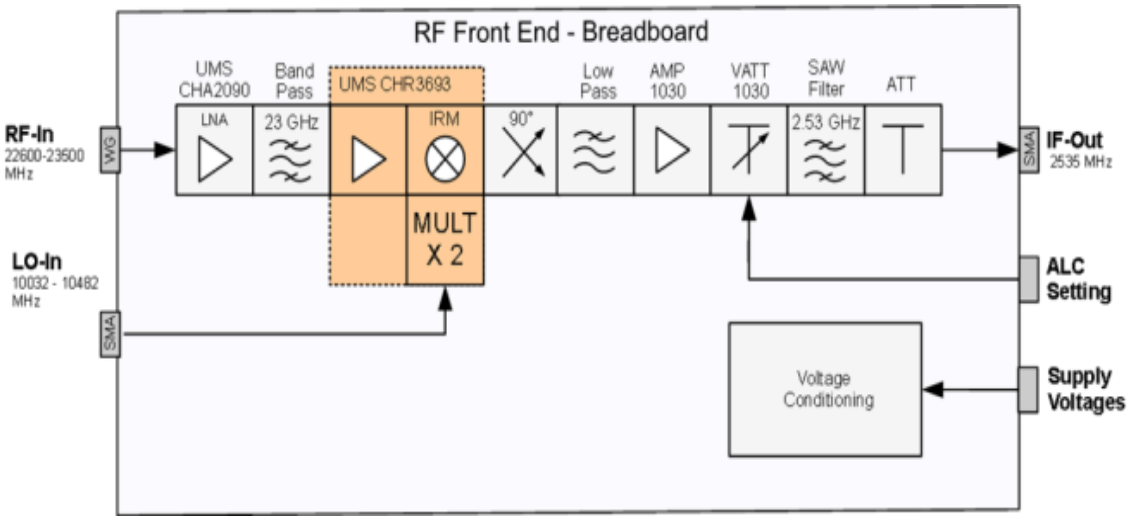
Breadboard Overview



Breadboard - IF Test @ 2.5 GHz

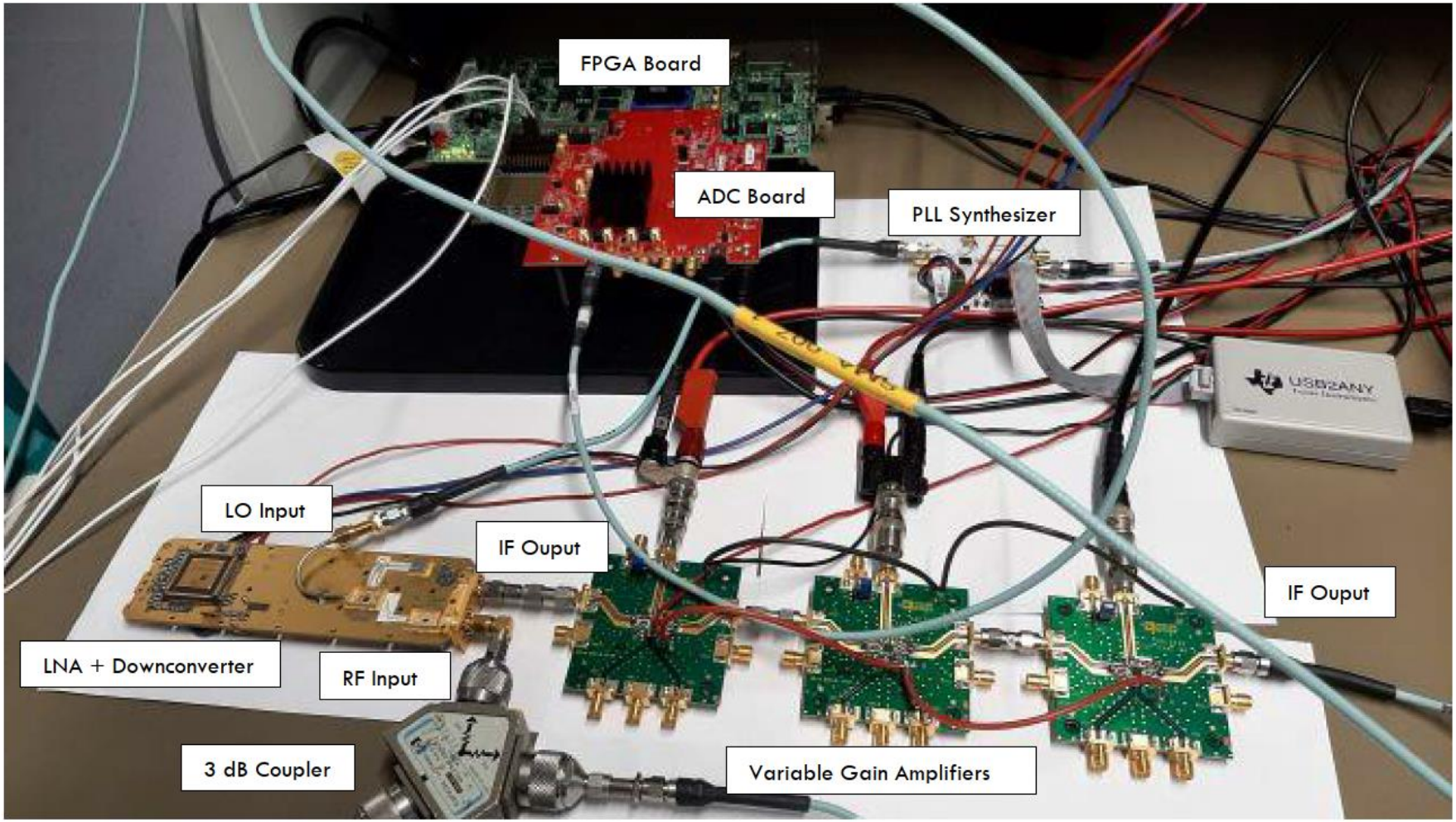


RF front end (Tesat)



- The CHA2090 LNA is a three-stage self-biased wide band monolithic low noise amplifier .
- 23 GHz Bandpasss filter of TESAT design realized as microstrip MIC filter.
- CHR3693 is a multifunction chip which integrates: a balanced cold FET mixer; a times two LO multiplier; a RF self-biased LNA.
- ~3 GHz lowpass IF filter is a TESAT design again realized as microstrip MIC filer.
- IF amplifier and attenuator MMICs are standard TESAT designs manufactured at UMS on a space qualified GaAs process.

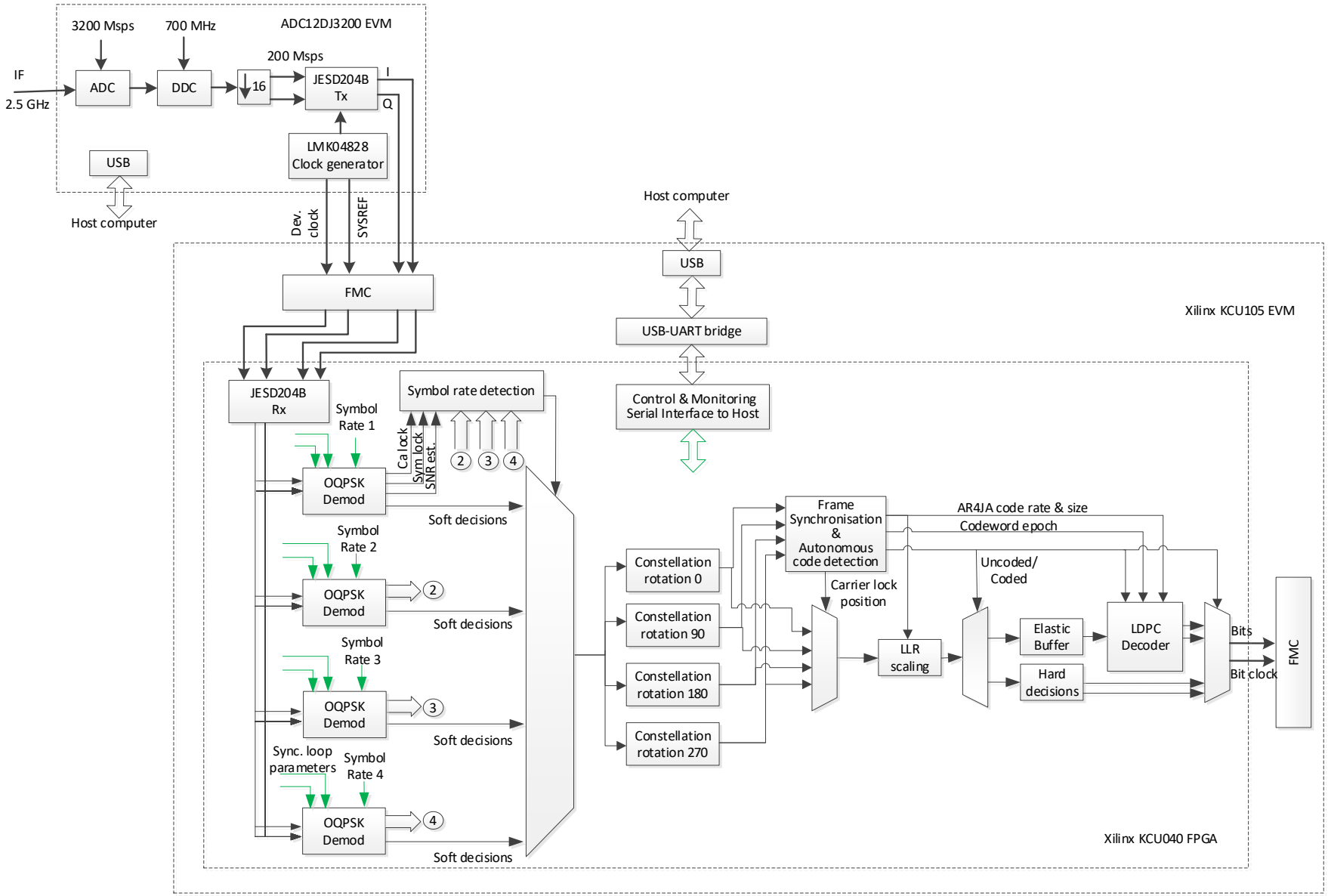
Breadboard Hardware



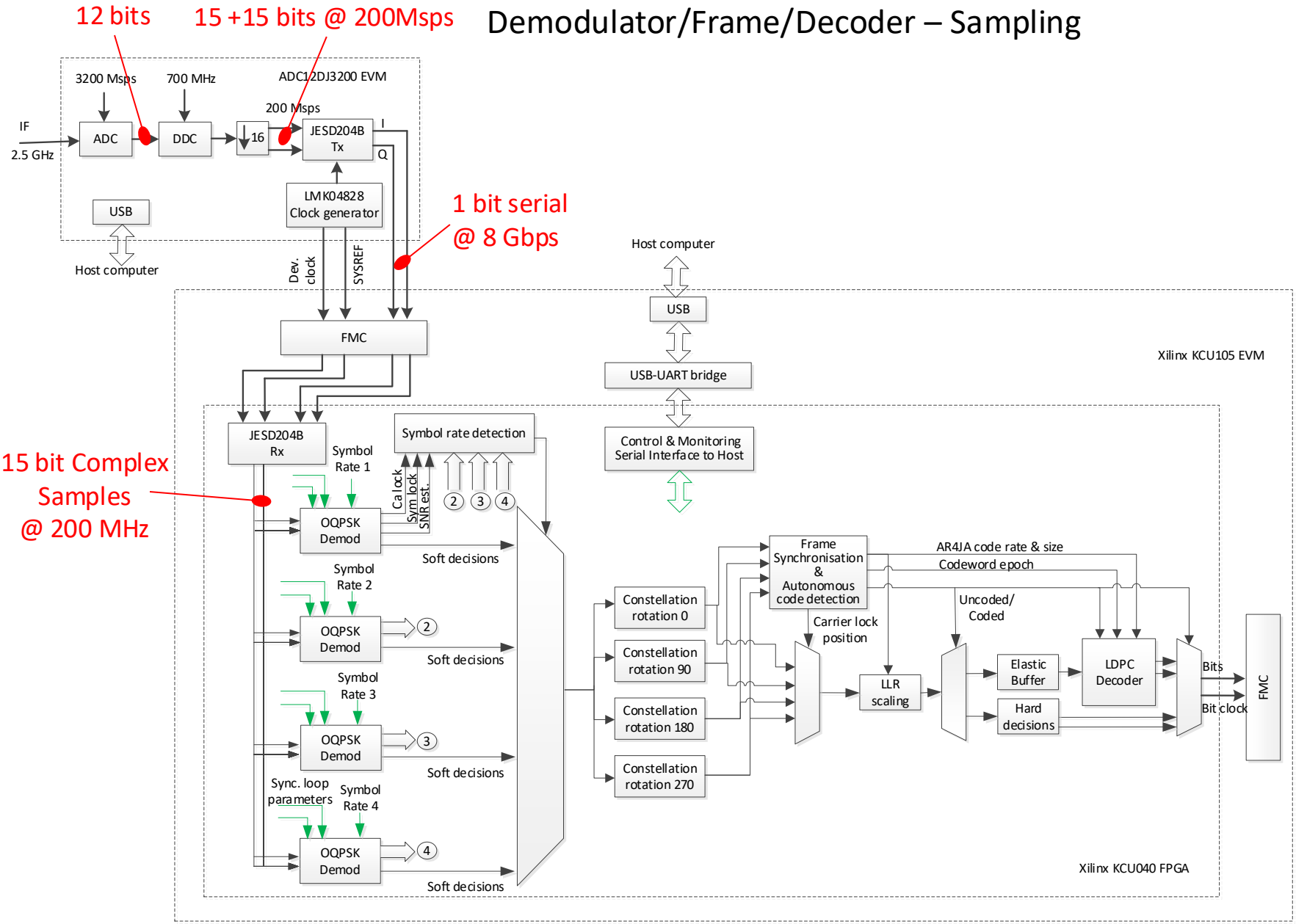
Demodulator / Decoder Requirements

- Modulation: **SRRC-OQPSK** with symbol rates between **10-100 Msym/s** (bandwidth limited)
- Channel coding: CCSDS AR4JA **LDPC codes** {1/2, 2/3, 4/5}, 16k, and ½, 1k
- **Autonomous detection of channel symbol rate** from a preconfigured list of 4 symbol rates
- **Autonomous detection of LDPC code rate** and **block length**
- Fade mitigation ("Free Wheel" through fades)
- Target Frame Error Rate (FER) of 1E-4
- **Doppler shift of up to +/-150 kHz** and **Doppler rate of up to +/-120 Hz/s**

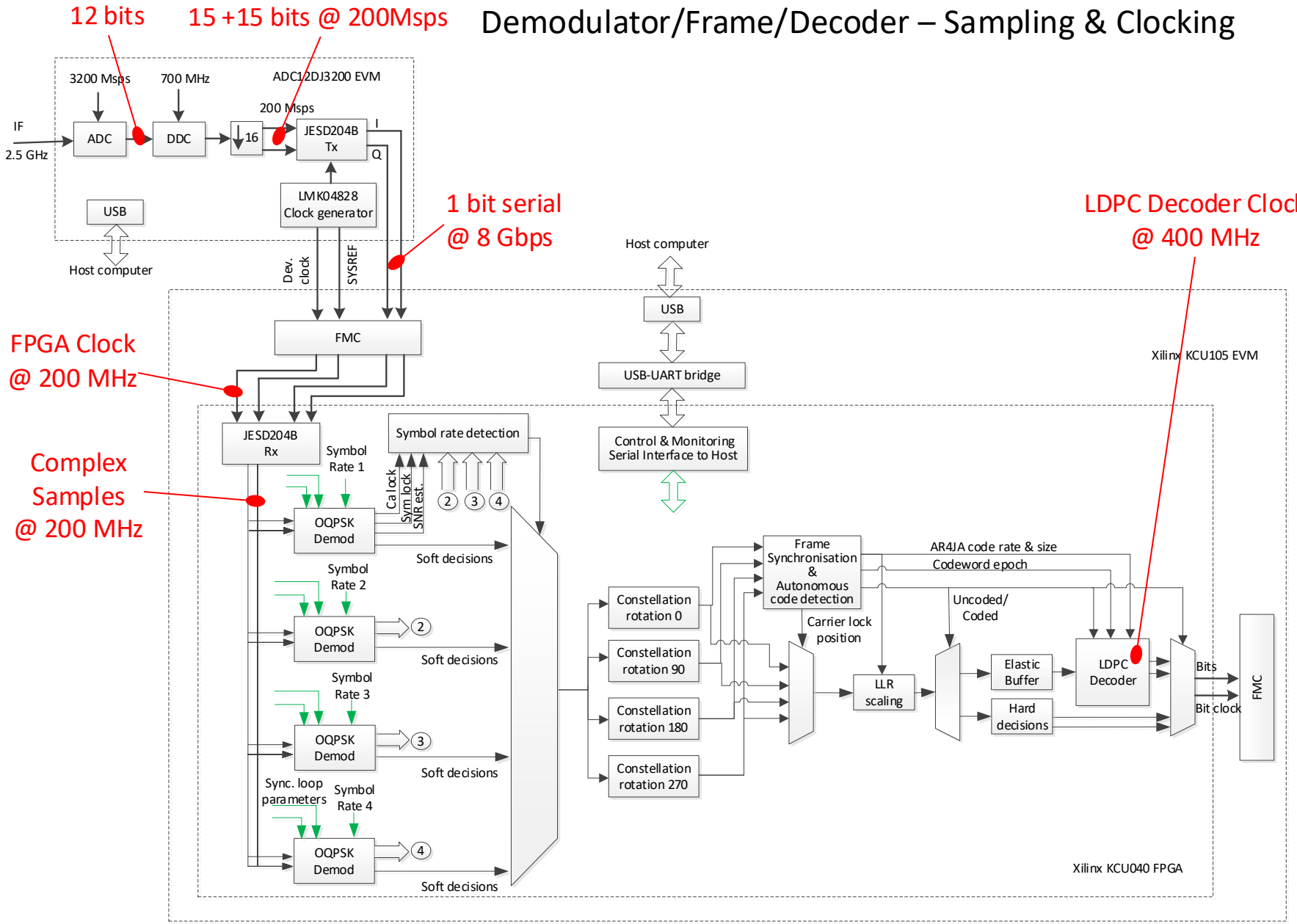
DSP : Demodulator / Codeword Sync / Decoder Overview



Demodulator/Frame/Decoder – Sampling

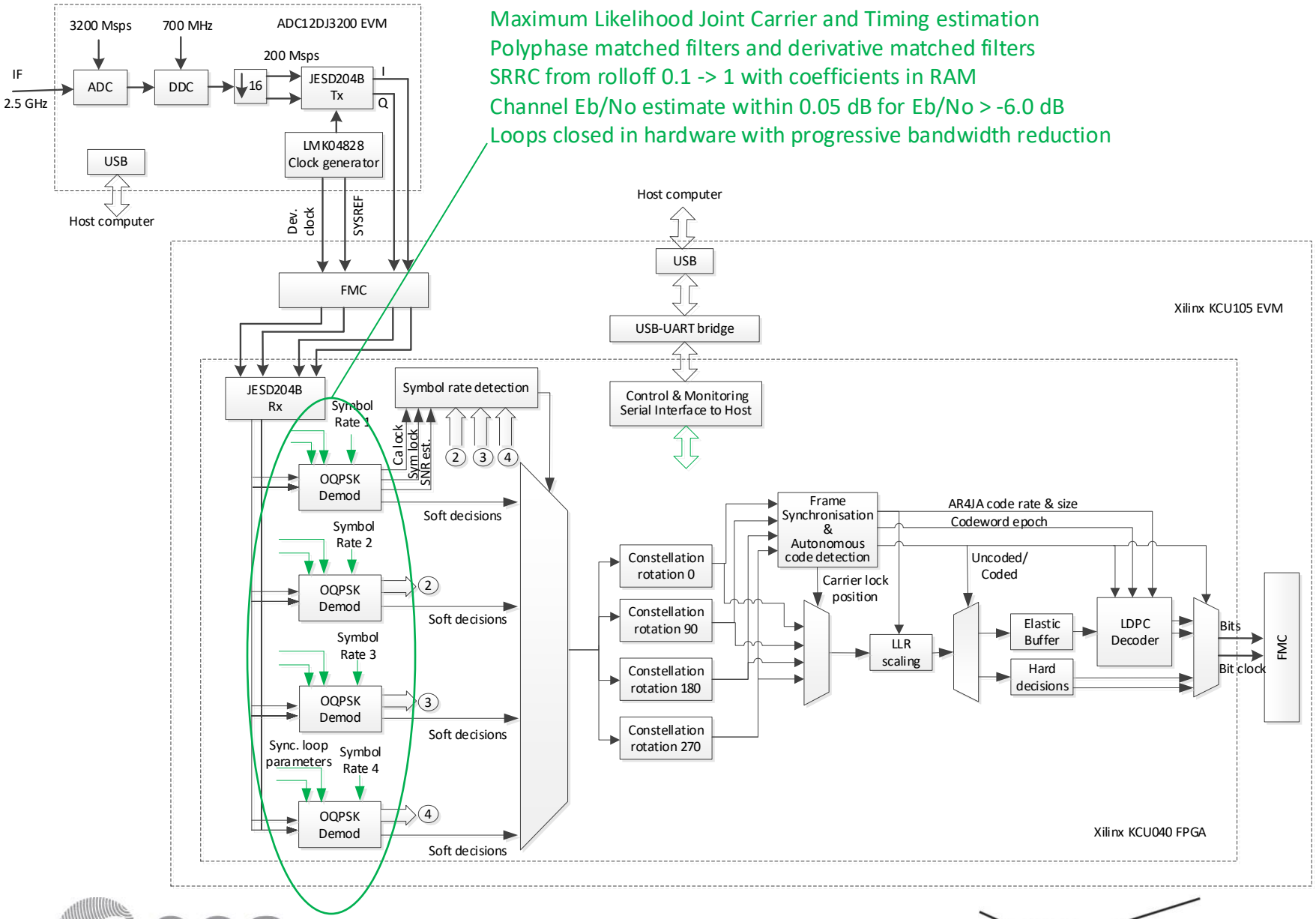


Demodulator/Frame/Decoder – Sampling & Clocking

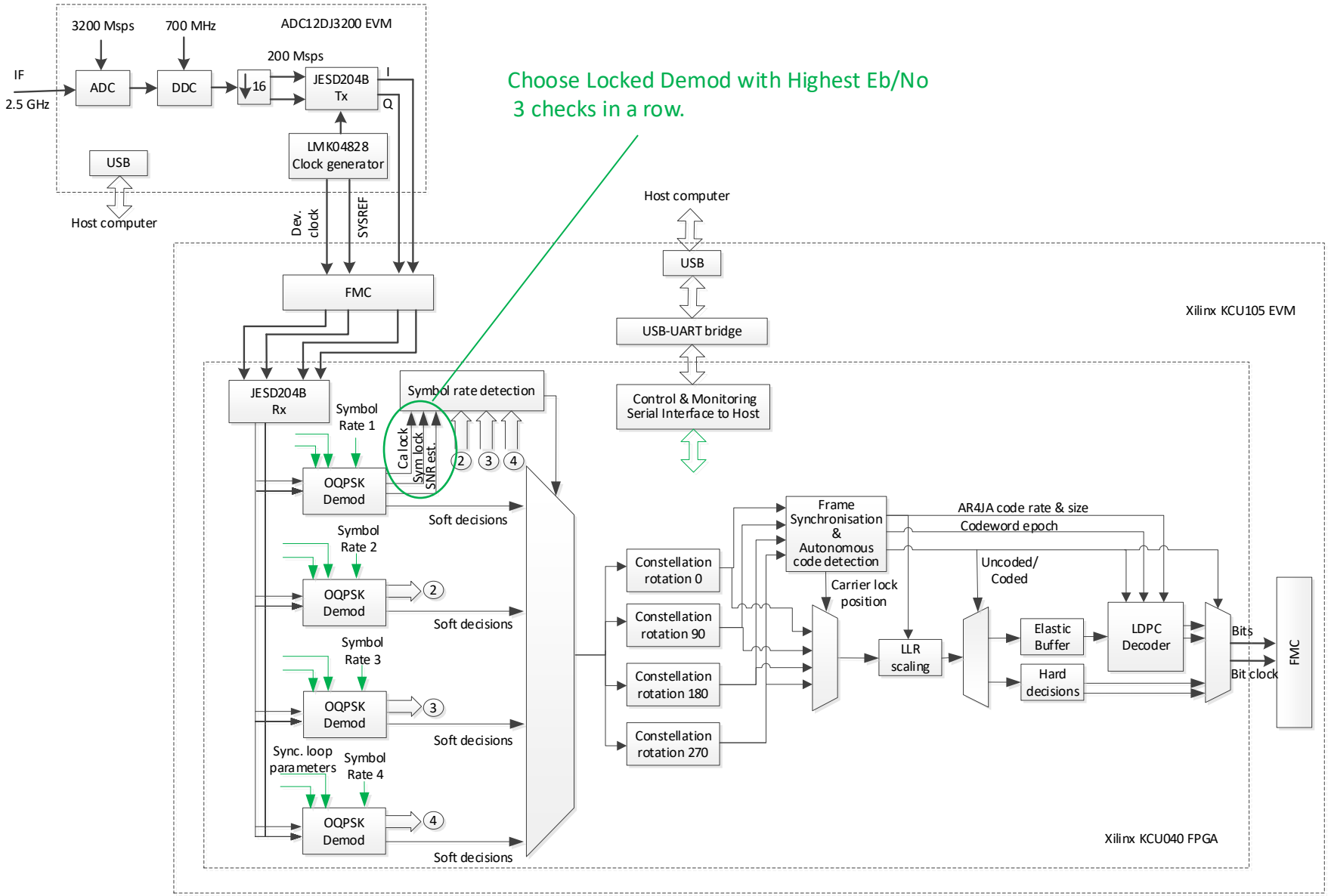


Demodulators

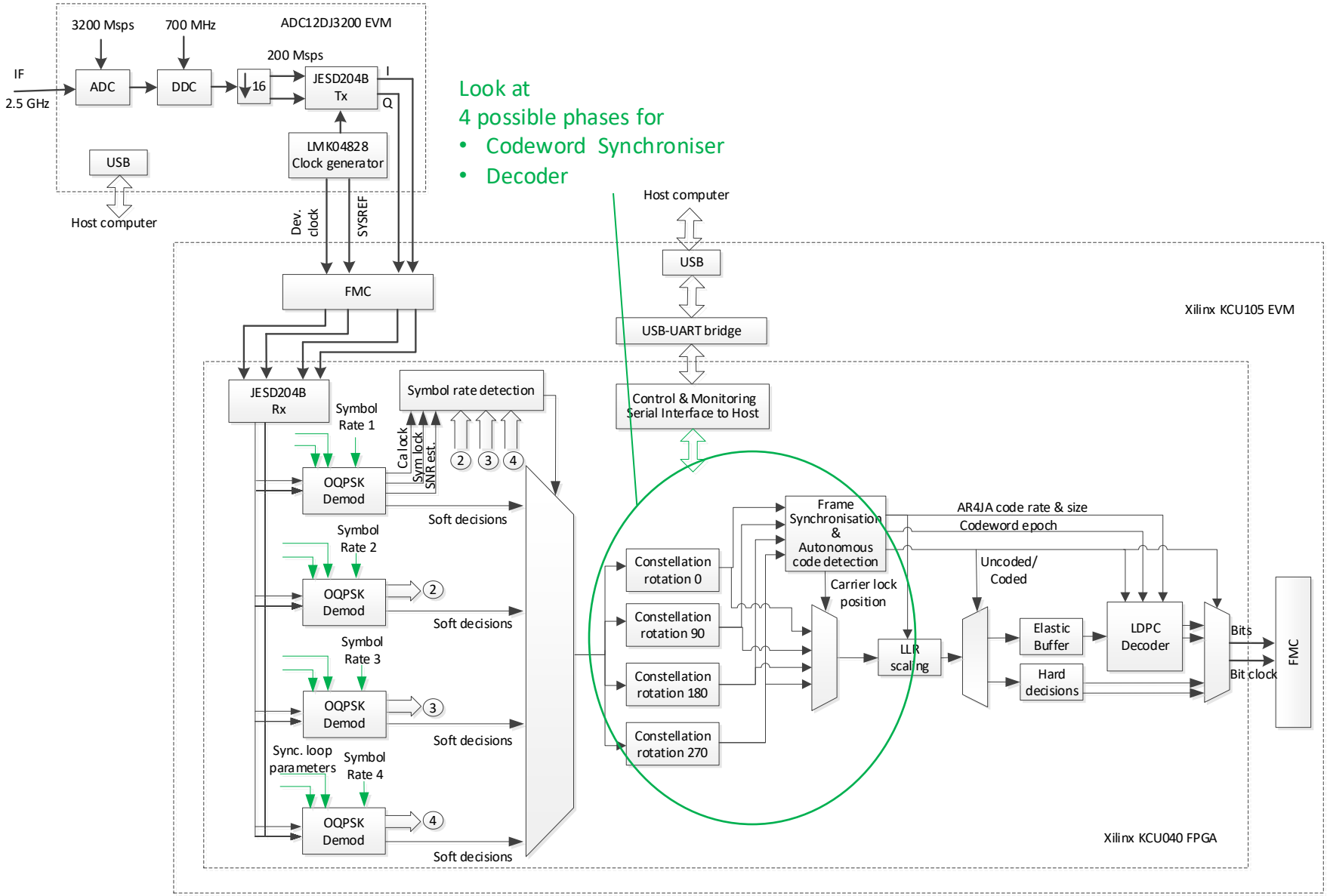
Maximum Likelihood Joint Carrier and Timing estimation
Polyphase matched filters and derivative matched filters
SRRC from rolloff 0.1 -> 1 with coefficients in RAM
Channel Eb/No estimate within 0.05 dB for Eb/No > -6.0 dB
Loops closed in hardware with progressive bandwidth reduction



Demodulator - Autonomous Symbol rate detection



Codeword Sync – Autonomous Code Rate & Length



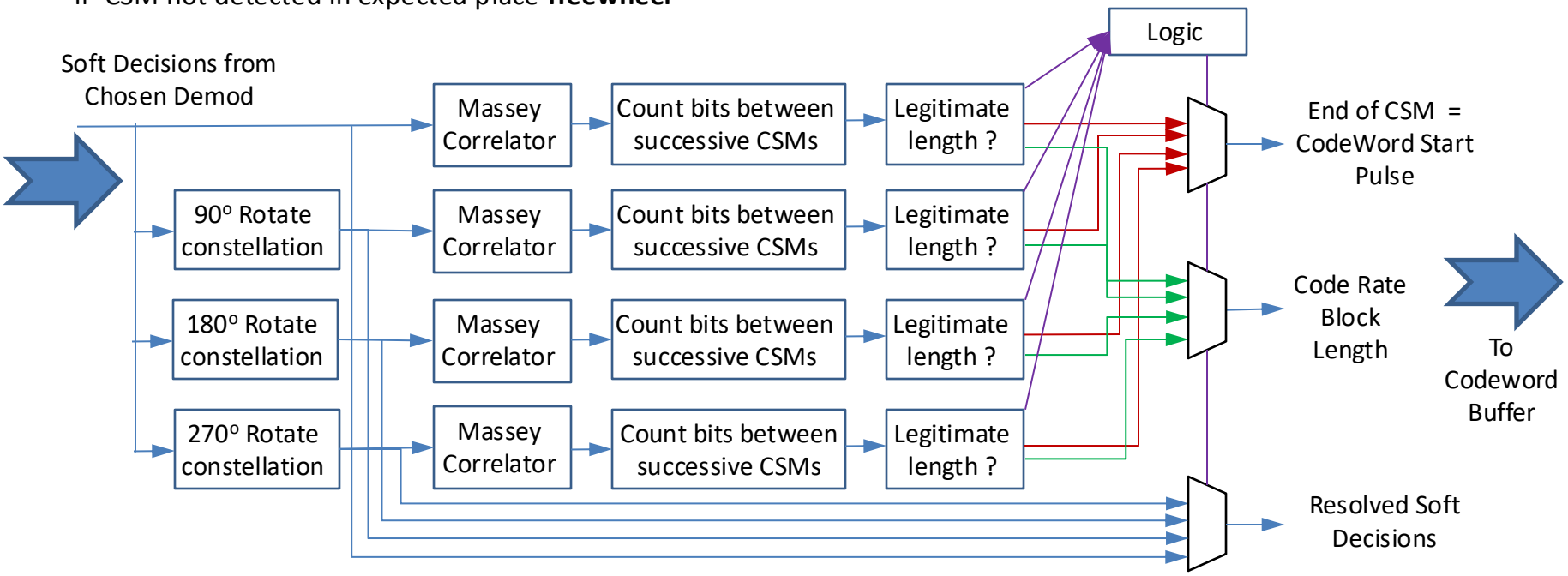
Look at
4 possible phases for
- Codeword Synchroniser
- Decoder

Codeword Sync – Autonomous Code Rate & Length Algorithm

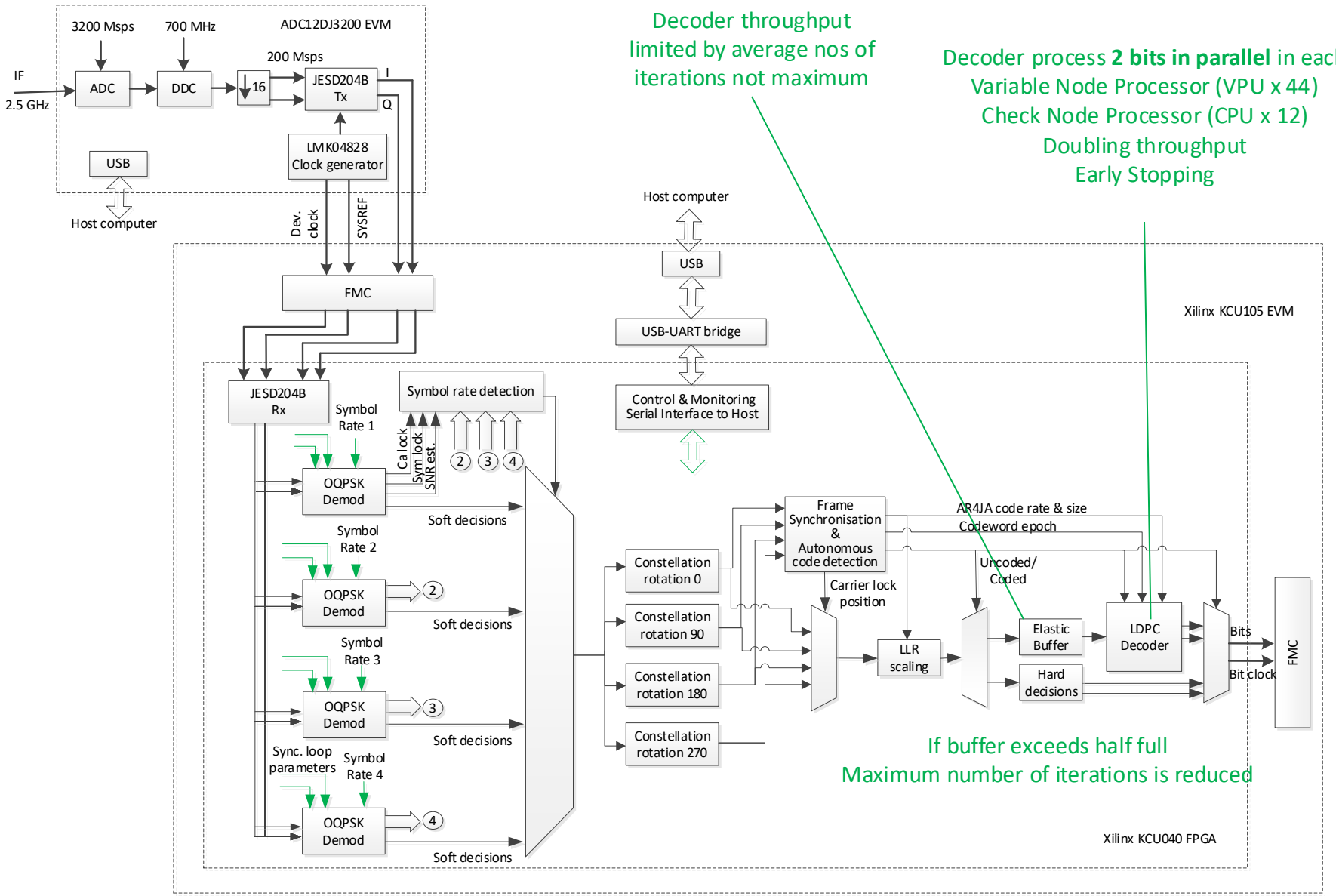
Unique Codeword Lengths

Block Size	1,024	4,096	16,384
Rate 4/5	1,280	5,120	20,480
Rate 2/3	1,536	6,144	24,576
Rate 1/2	2,048	8,192	32,768

- Maintain 4 counters counting bits between detected **Code Sync Markers** (CSMs) from Massey Correlators
- Codeword lengths are unique, confusion possible only if 2 consecutive CodeWord Sync Markers missed (3*2048=4*1536)
- If (count between detections == codeword length or twice codeword length) then declare found
- If CSM not detected in expected place **freewheel**



LDPC Decoder



Freewheeling through Fades

As depth of fade increases :

- FER approaches 1 (~0.5 dB Fade) - “immediate” recovery < 1 codeword
- Carrier phase flips => bit slips (a few dB) => Loss of Codeword synchronisation – quick recovery, < 2 codewords
- Loss of carrier lock and loss of Bit sync lock – quick recovery < 1 mS
- Loss of carrier frequency estimate & bit clock – complete re-acquisition required

Mitigation

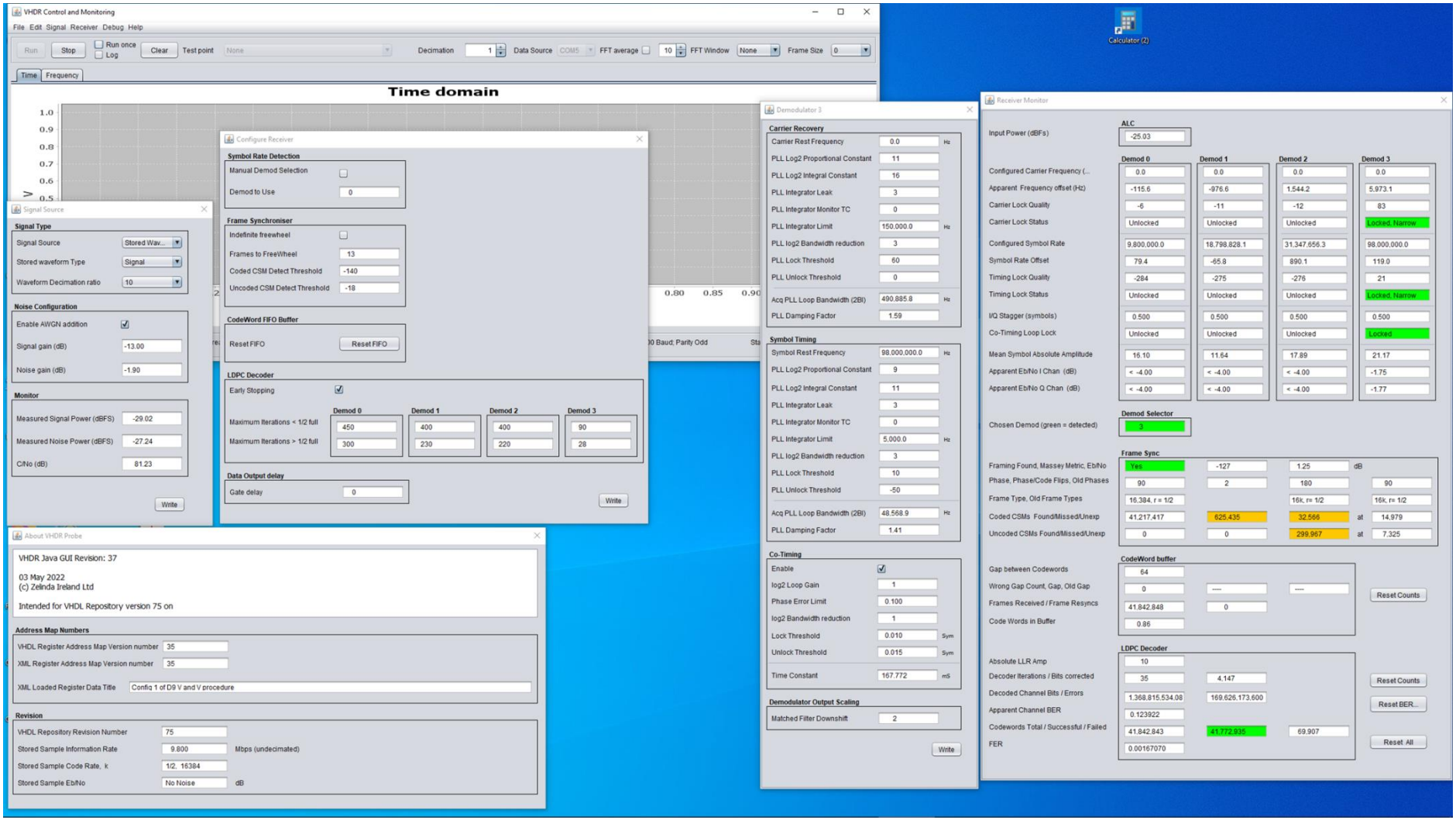
- Codeword Sync “freewheel” will generate pulses at appropriate intervals for upto 4095 missed Codewords
- Leave Carrier and Bit Sync loops in narrow band tracking mode to stay on frequency (until time out)

Testing

- Test FPGA stand alone (Demodulators, Sync detection, Code Rate & Lenth detection, LDPC Decoder)
  - Signal from wavwform sample look up (exact Eb/No setting)
  - BER from LDPC „for free“
  - FER from LDPC „for free“
  - Acquisition time from in built timers
- Test FPGA and ADC with IF input
  - Analogue signal generator,
  - BER Tester (measures errors in undecoded codewords)
- Test at RF
  - Analogue Signal generator and upconvertor, BER Tester

Testing – FPGA Standalone

98 Msyms/S, ½ rate 16384 info block, channel Ecs/No = -1.75, Eb/No = +1.25 dB



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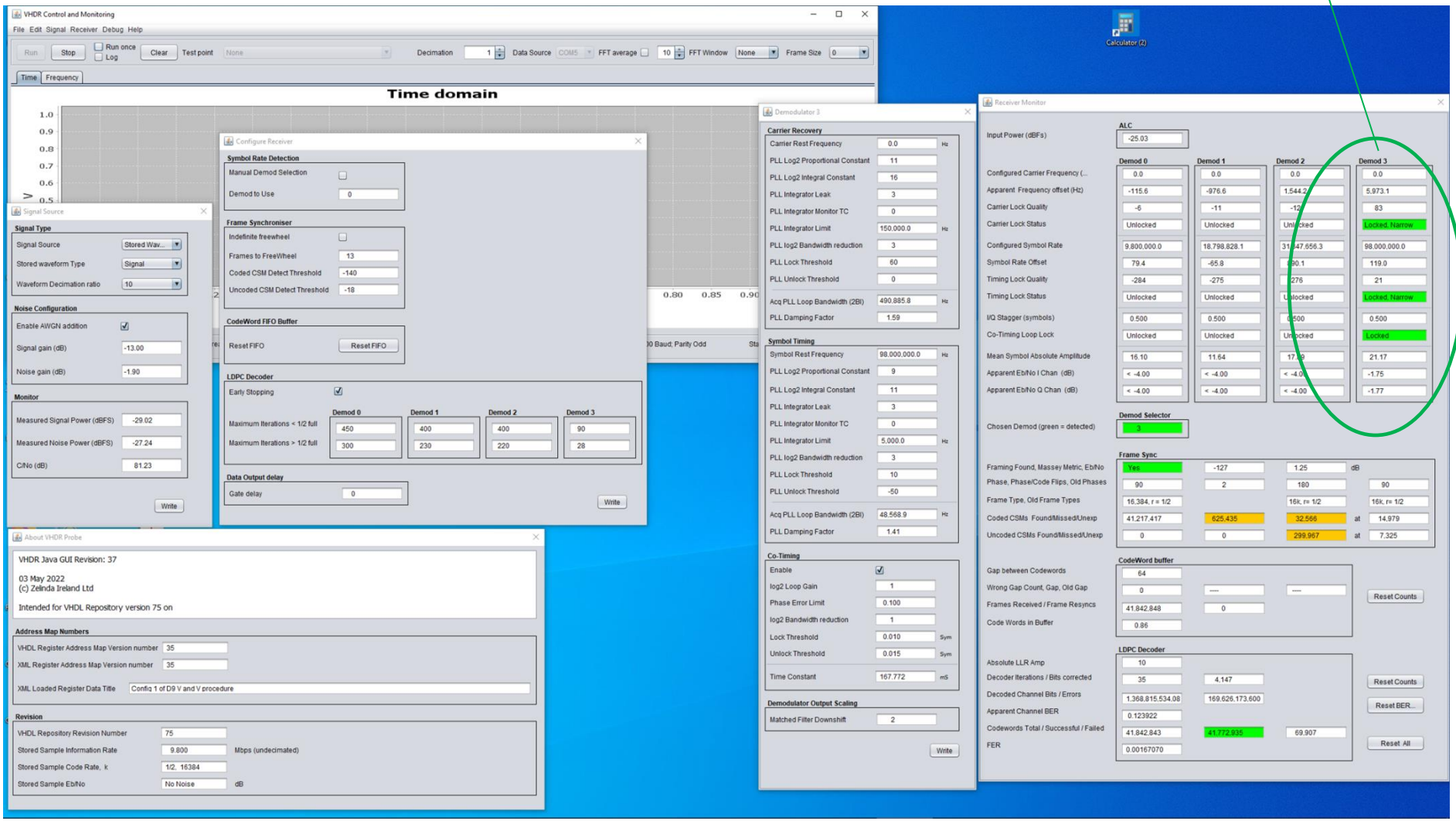

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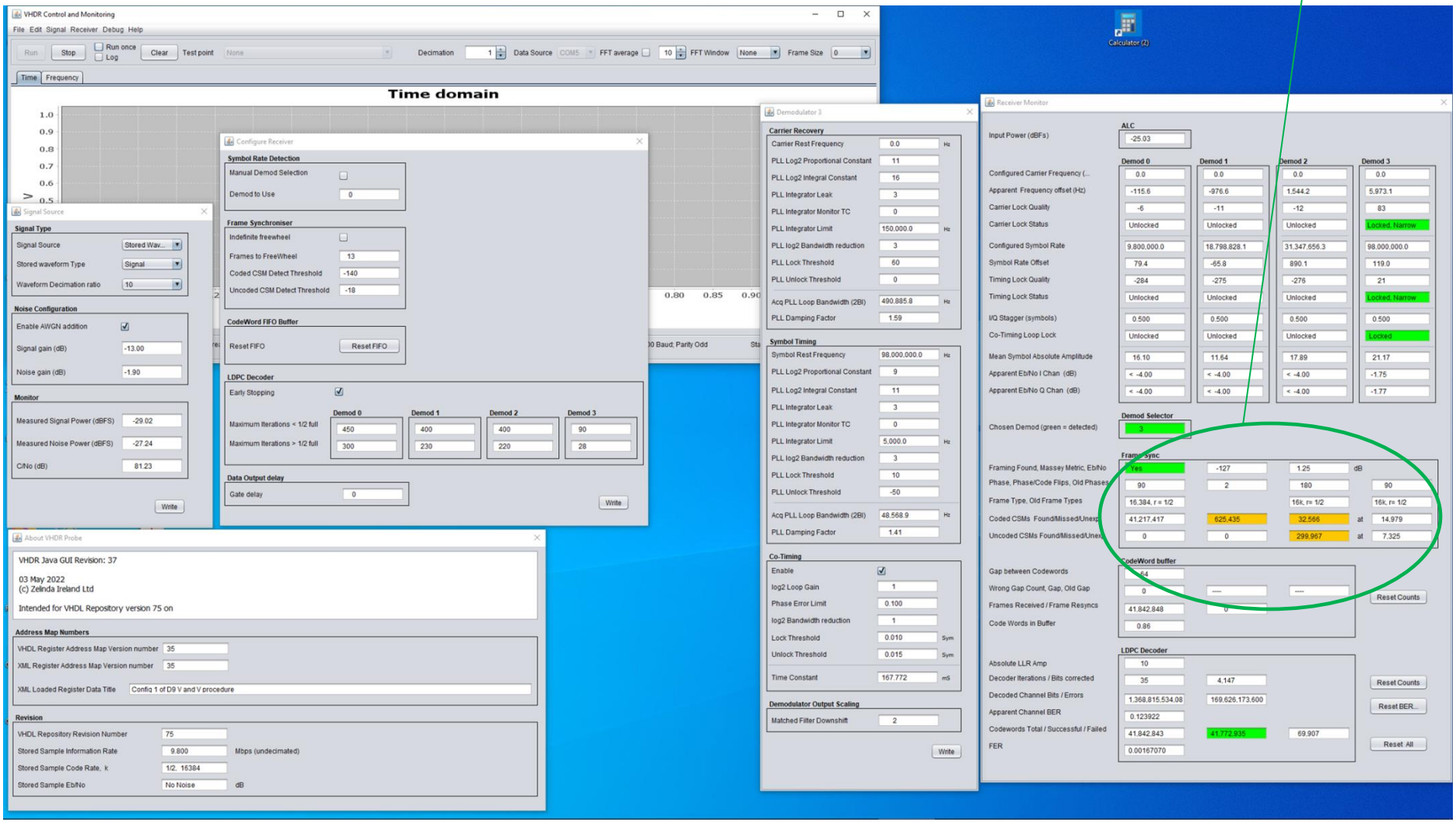
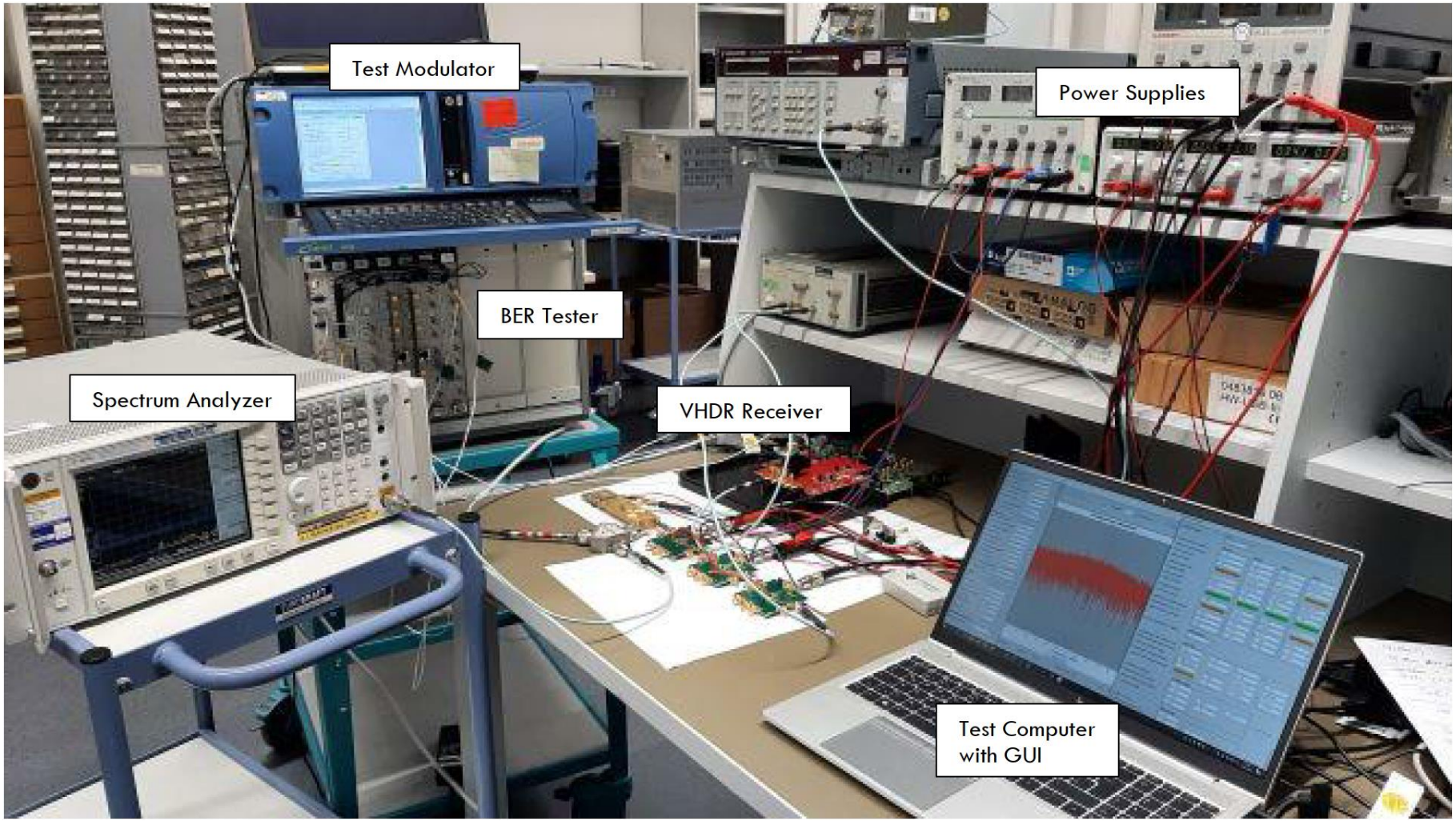
Frame Sync and Autonomous rate & Length

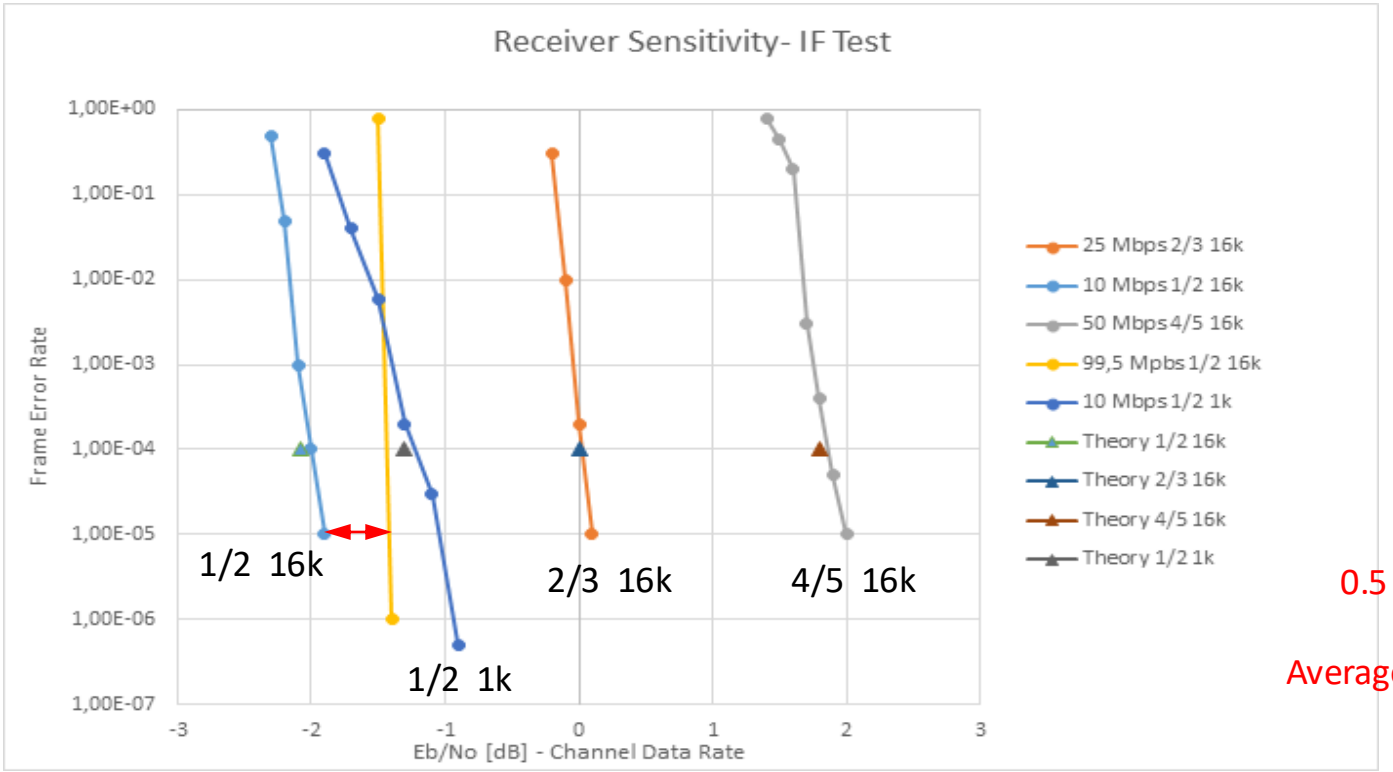


Testing – at RF and IF



Testing – Results Summary

- Noise figure : 2.5 dB
- Total Implemenentation loss (ADC, Demod, Decoder) in Digital domain : < 0.2 dB (except ½ rate > 75 Mbps)
- Acquisition time : Typically < 20 mS @ max Doppler & rate



0.5 dB additional Loss
@100 Mbps
Average iterations limit of 31

Future Qualification

- Breadboard used **Xilinx Kintex Ultrascale XCKU040** (530 k logic cells, 1930 DSP slices, ~50% logic utilisation)
- Space Qualified RT Kintex Ultrascale available **XQRKU060**, 20nm processs, 726k logic cells, 2760 DSP slices.
- SEM (Single Event Mitigation) IP core to check and correct erroneous re-configuration
- Can always use TMR (manual using VHDL functions) for critical registers (eg configuration)
- Many ADC options (in future including ADCs within the FPGA)

Conclusion

- Single stage down-conversion from 23.2 GHz
- High IF and high sampling rate, 2.5 GHz IF at 3.2 Gsamples/S
- Autonomy works reliably for modest additional hardware and no specification change.
- AR4JA codes well suited to this type of Uplink

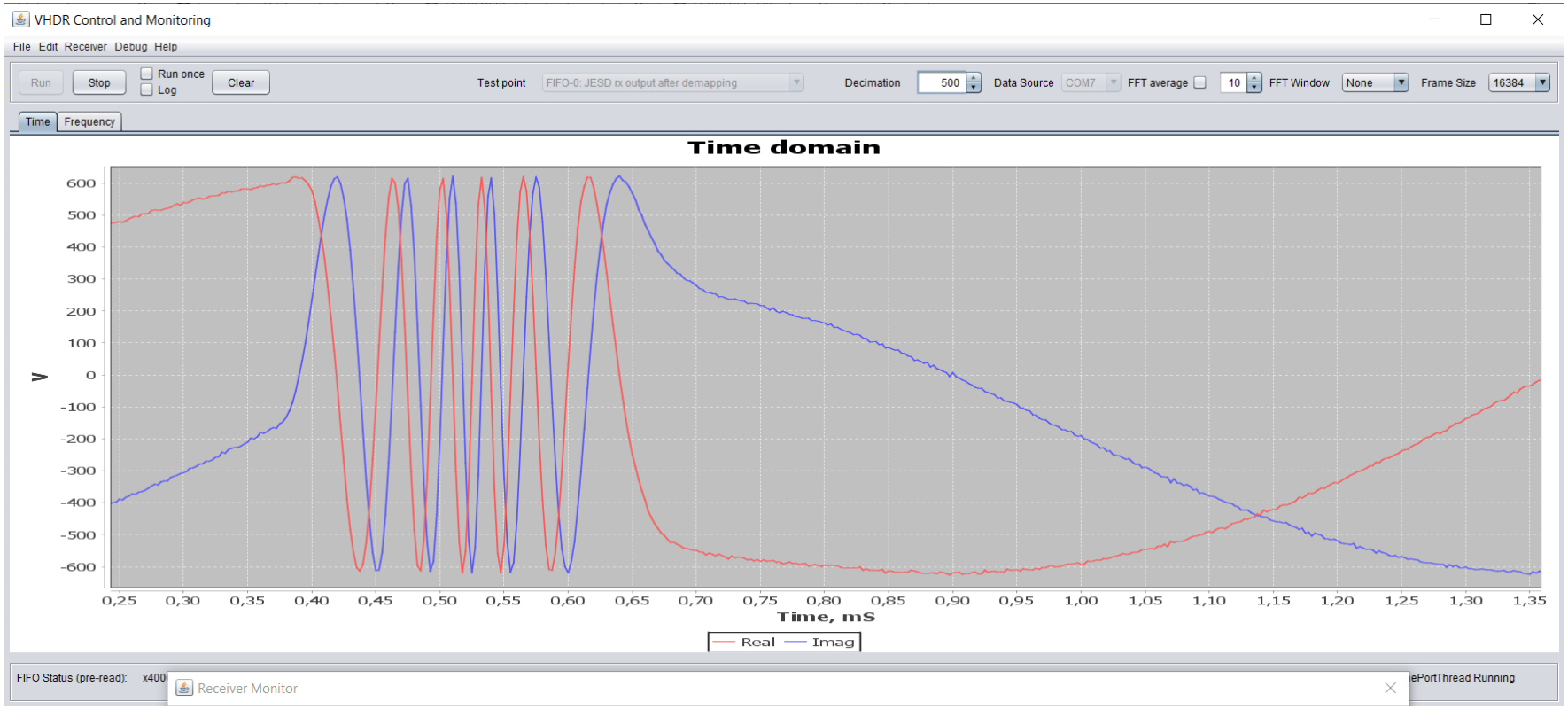
Self-Test & Self Check out – An extra Requirement ?

- Additional Self Test and Debug features can dramatically speed up development
- Stimulus
  - Noise free complex near baseband waveform samples from MATLAB (with integral number of Frames and integral number of carrier cycles) stored in FPGA
  - Choose stored samples from low symbol rate (~10 Msym/S) (one ½ rate CW of 32,768 syms => ~640k x 32 bit Mbit)
  - Use prime number of samples and Sample read back logic that decimates so 10 symbol rates can be tested
  - Added AWGN in real time within FPGA using mutiple leap forward LFSRs, with adjustable Eb/No using mutipliers
- Deep Monitoring
  - Multiple FIFOs added within FPGA to capture samples at various points
  - Timers added to FPGA to record
    - Carrier & Clock acqusitions times (for 4 demodulators),
    - Demod Selection time,
    - Frame Sync & Code rate & length detection time
- JAVA GUI over USB for control and monitoring including time and frequency domain display of FIFO waveform captures

Useful not just in development, but also in space craft integration.

A lesson Learned

- Persistent loss of Demodulator lock at low Data rates
- Tesat testing identified that at low data rates (10, 12.5 Mbps) VHDR had decoded bit errors for Eb/No < 3.3 dB (versus theory ~ 1.0 dB) and Demodulator symbol lock quality very poor.



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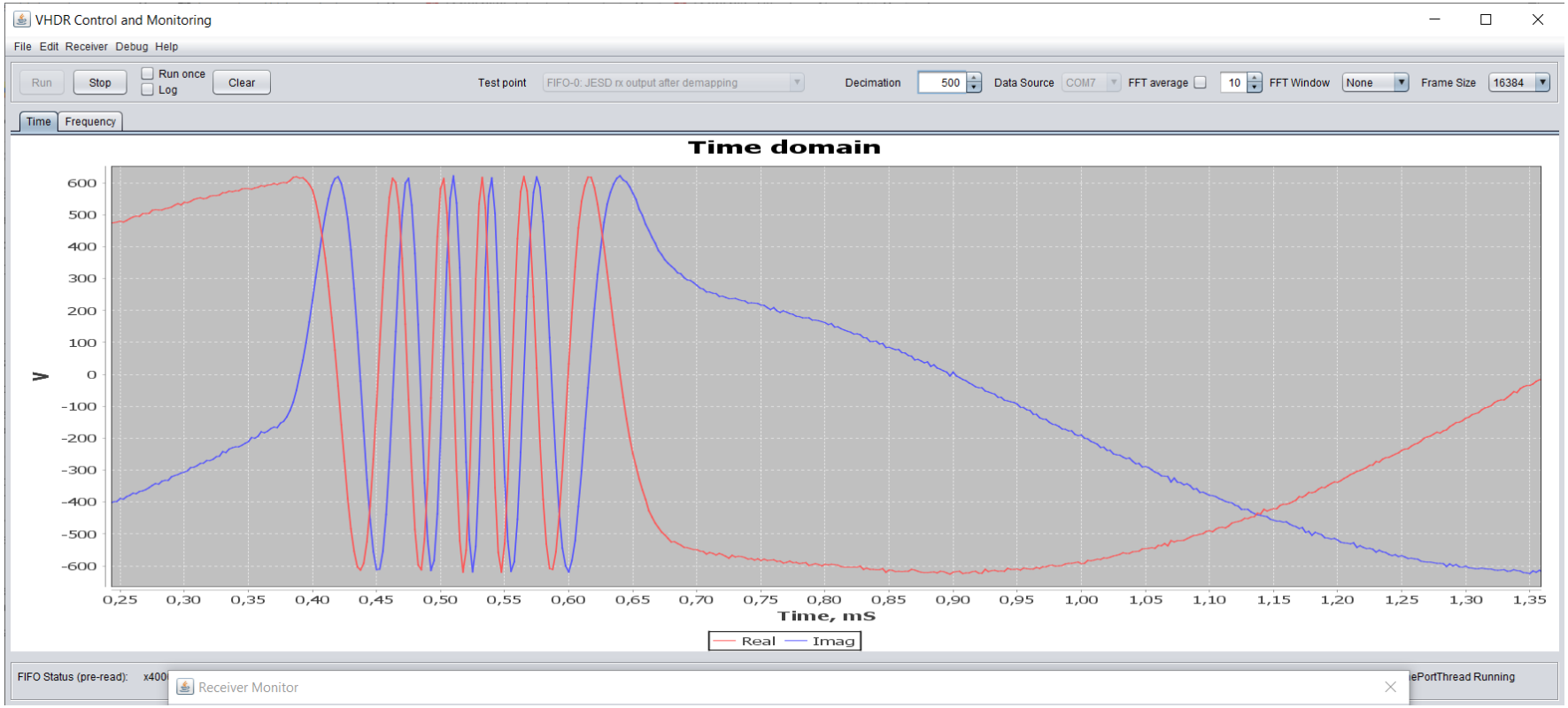


Tesat tried a Fan on ADC – problem eliminated.

VHDR – Doppler and the LOP-G orbit

Chosen LOP-G orbit is a (southern) **Near Rectilinear Halo Orbit** around L2.

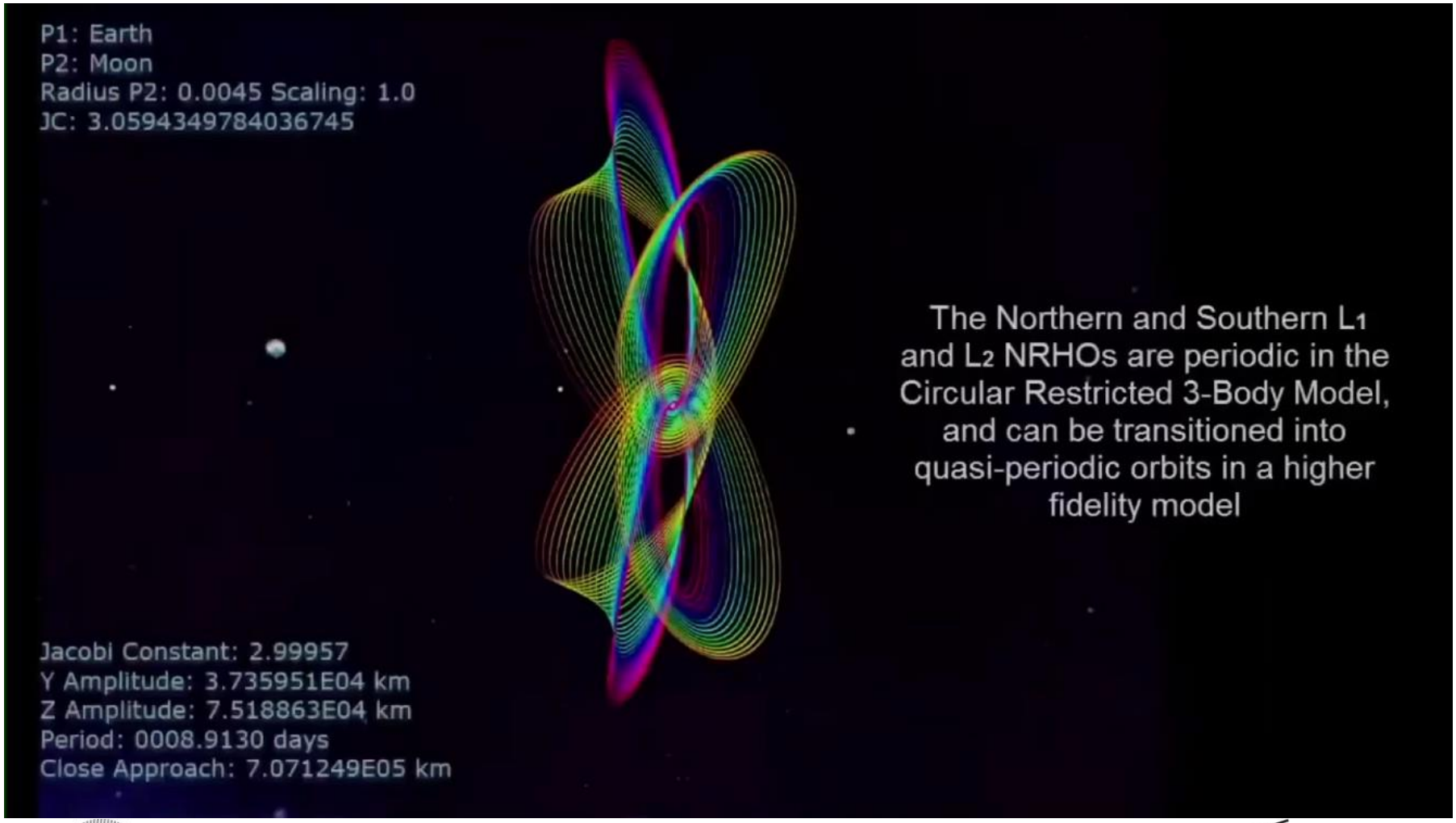
- The points Lagrange points L_1, L_2, and L_3 are positions of unstable equilibrium.
- Rectilinear - as eccentricity -> 1 so elliptical orbit tends to vertical “up and down” straight line – no use for planetary orbits as would hit the planet surface.
- near rectilinear - resembling a “flattened ellipse” with nearly parallel sides.
- A halo orbit is a periodic, three-dimensional orbit associated with one of L1, L2 and L3 .
- the NRHOs are those members of the halo family with bounded stability
- NRHP can be evolved from a “lyaponov” orbit sitting in the Moon orbital plane (5.1° to the ecliptic)

VHDR – the NRHO advantages

- Visible from far side of moon
- (almost) Always in Sunlight
- Always visible form earth (no occultation)
- Relatively Easy to get to (low energy)
- Long Period around 7 days so **low Doppler** wrt Lunar surface (LO->LS link).
- Almost perpendicular to plane of moon orbit so **low Doppler** wrt to earth (E->LO)

VHDR – other Halo orbits

- Although Halo orbits are nominally around Lagrange points they are closer to the Moon.
- Northern and Southern Halos exist around L1 as well as L2, so 4 nearly stable orbit possibilities.



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