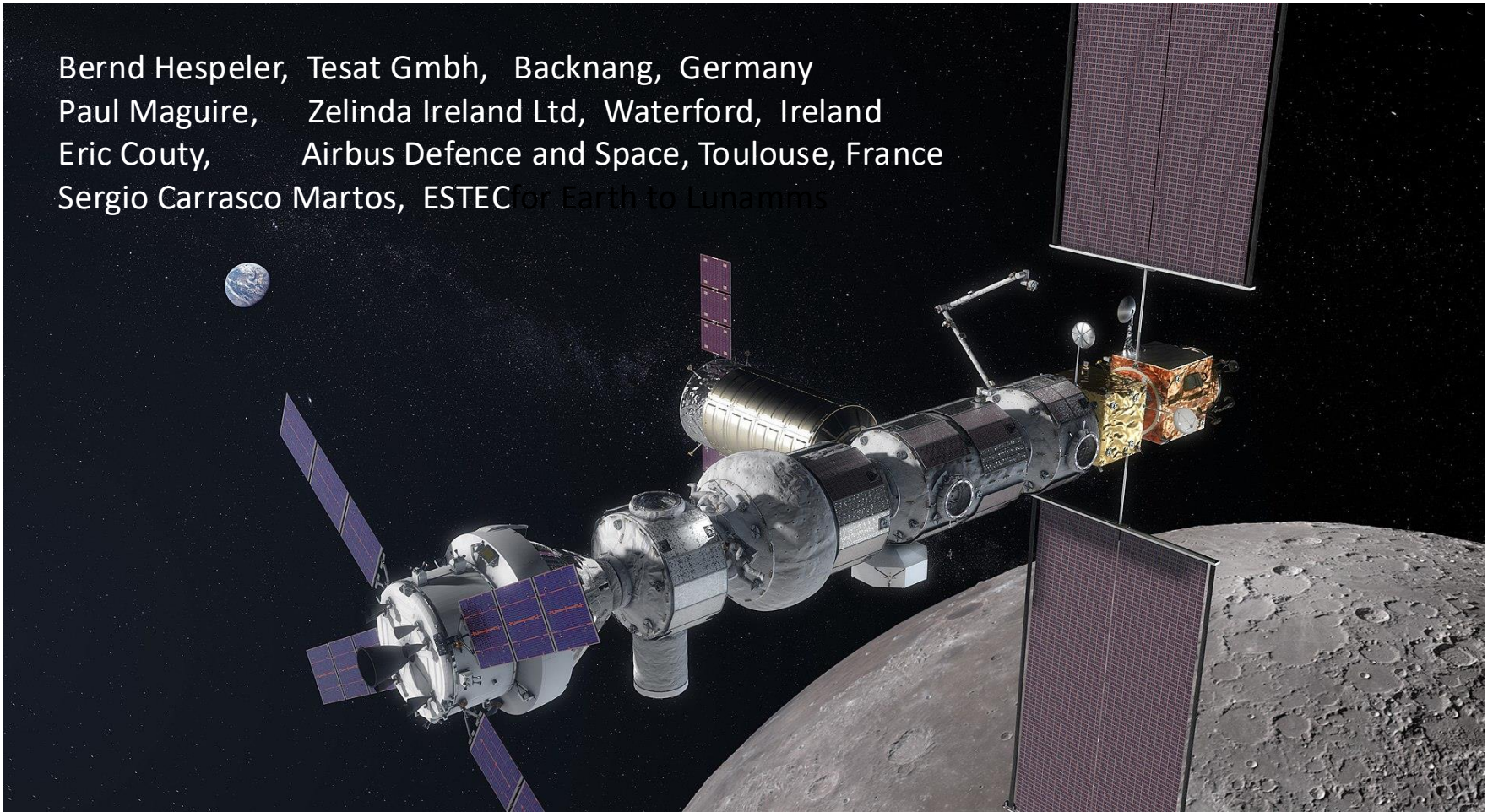


# VHDR

## Very High Data Rate Breadboard Receiver for Earth to Lunar Comms

Bernd Hespeler, Tesat Gmbh, Backnang, Germany  
Paul Maguire, Zelinda Ireland Ltd, Waterford, Ireland  
Eric Couty, Airbus Defence and Space, Toulouse, France  
Sergio Carrasco Martos, ESTEC for Earth to Lunar Comms



# VHDR – Cislunar Space Exploration plan Overview

## Lunar Orbital Platform – Gateway (LOP-G)

The next step in Human Space Exploration is a **space station in lunar orbit** intended to serve as

- a communication hub, between Earth, Moon (inc lander, rovers, visiting vehicles) and lunar relay satellites.
- science laboratory,
- short-term habitation module for astronauts,
- transfer station to the exploration of the Moon and Mars

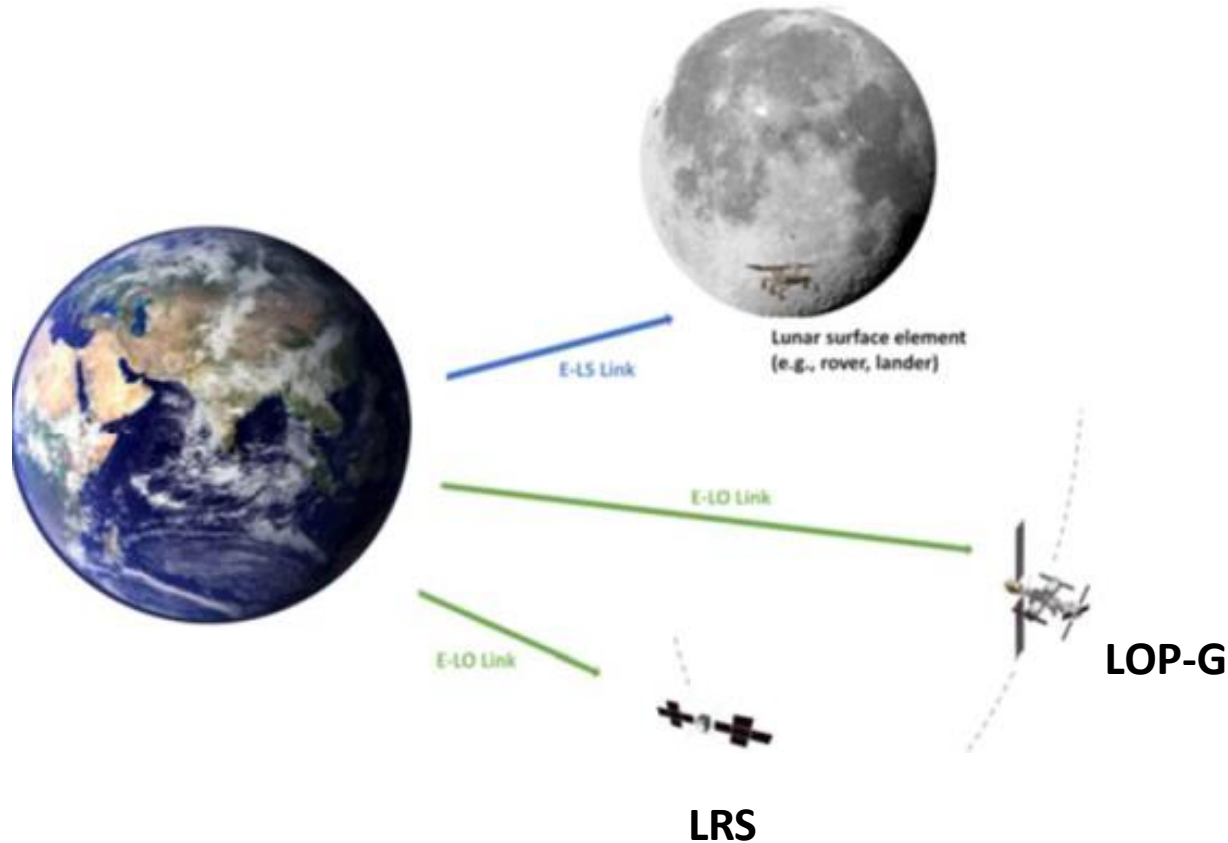
Additionally a constellation of **Lunar Relay Satellites (LRS)** probably in frozen Elliptical inclined lunar orbit (stable for > 10 years without station keeping).

Generic **Lunar surface elements** communicating both direct with earth or with LOP-G or LRS.



# VHDR – Comms Links

- All three links require **receivers** for comms from earth (E->LO and E->LS forward links)
- Potential comms links Orbiters to lunar surface also needs **receiver** (LO->LS link).



# VHDR – Uplink Comms Requirements

ITU and SFCG recommend **K-band** for high rate Space Research comms in Lunar region, specifically 22.55 – 23.50 GHz.

- Bandwidth limited to ~110 MHz
- For bandwidth efficiency SRRC OQPSK modulation (better than GMSK)
- AR4JA LDPC coding (as specified for TM downlink)
- 4 code rates/length combinations (1/2 16k, 2/3 16k, 4/5 16k, 1/2 1K)
- Information rates up to 160 Mbps (4/5 code) with 100 Msym/S

To keep operations simple Handover from different ground station should be:

- Autonomous acquisition
- Autonomous data rate detection (from 4 preselected in range 10 -> 100 Msyms/s)
- Autonomous code rate detection
- Autonomous block length detection
- Fade mitigation



# VHDR – LOP-G orbit Near Rectilinear Halo Orbit (NRHO) Animation

Earth

L1

Moon

L2



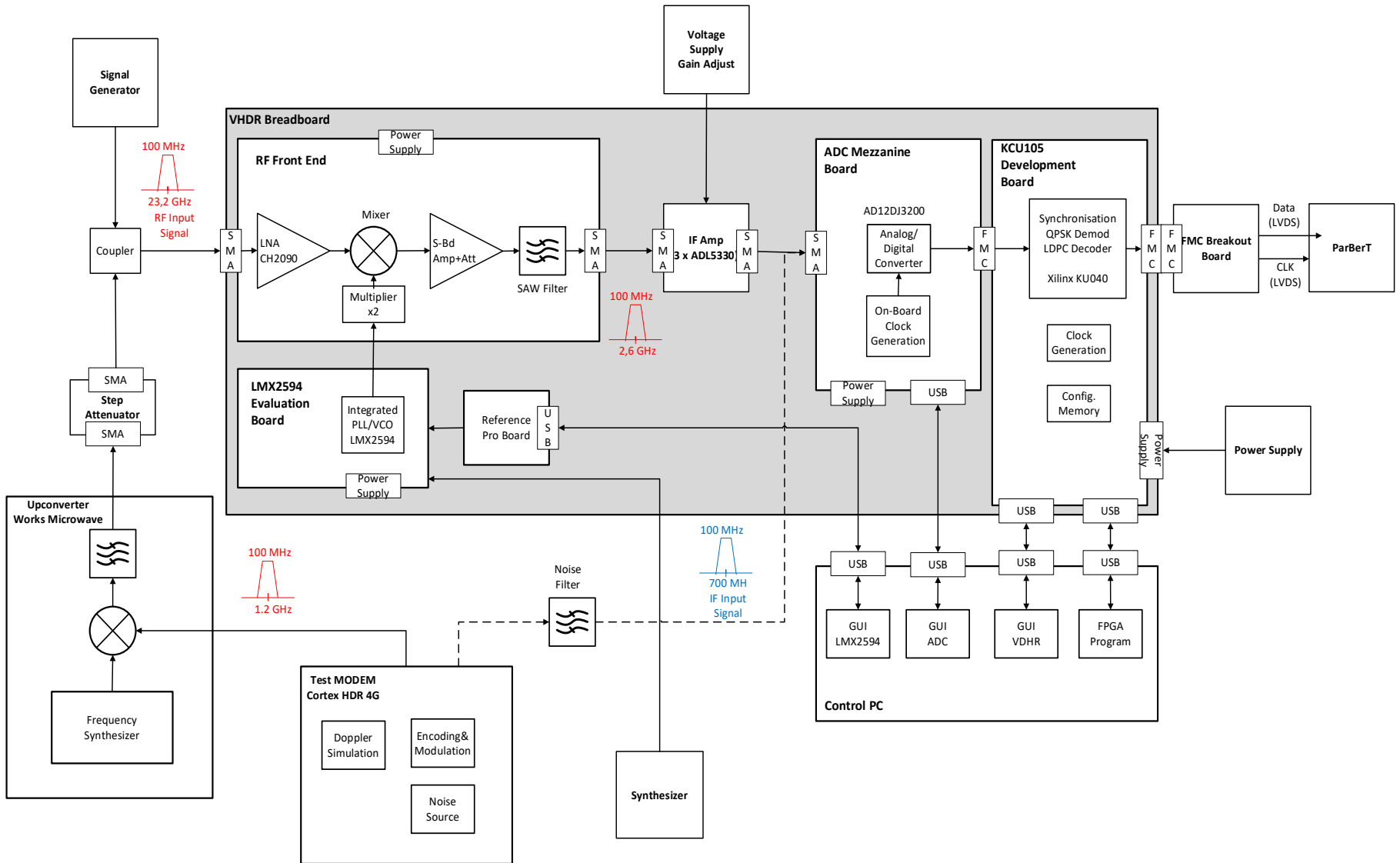
FreeFlyer

Earth-Moon Rotating Frame

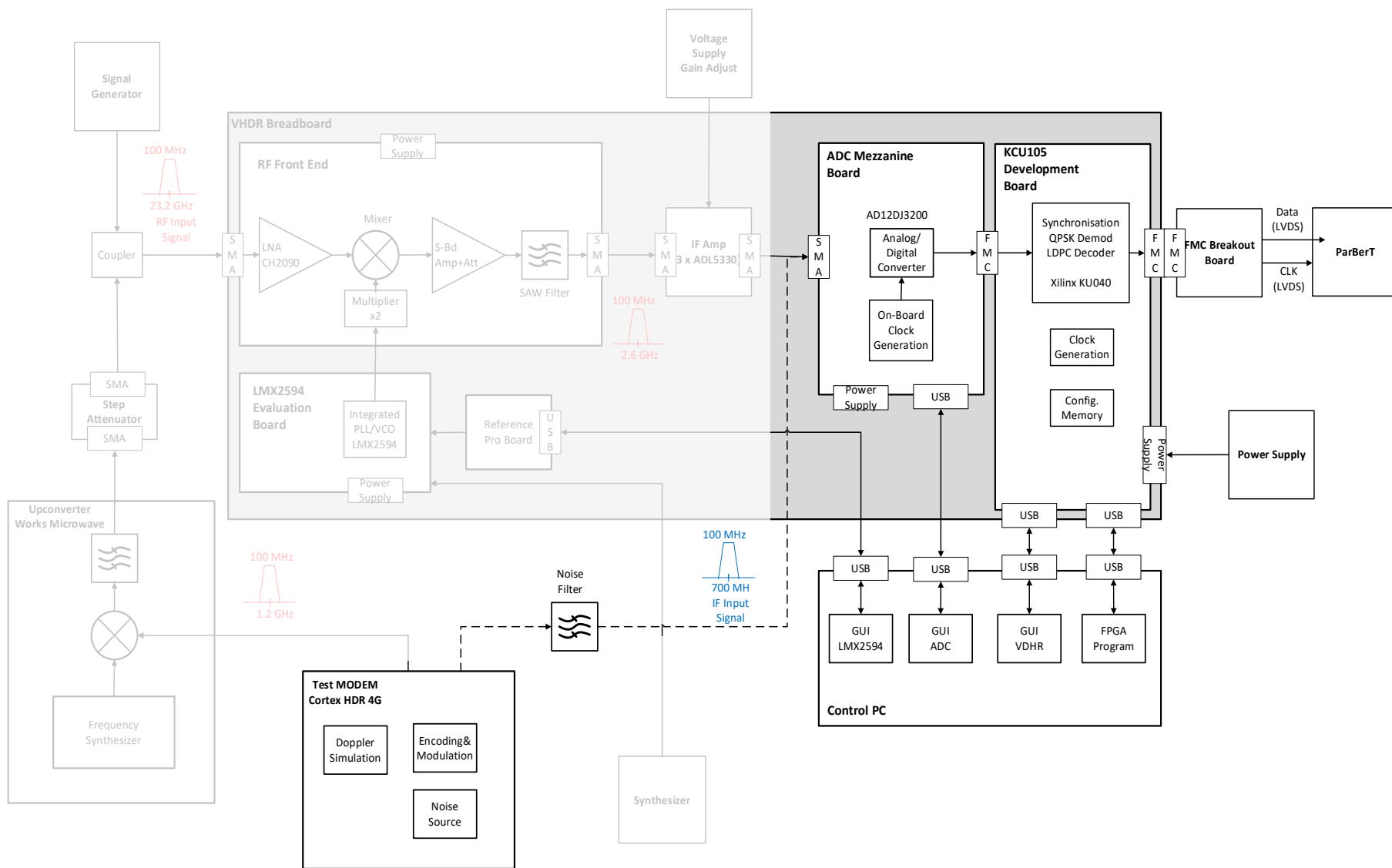




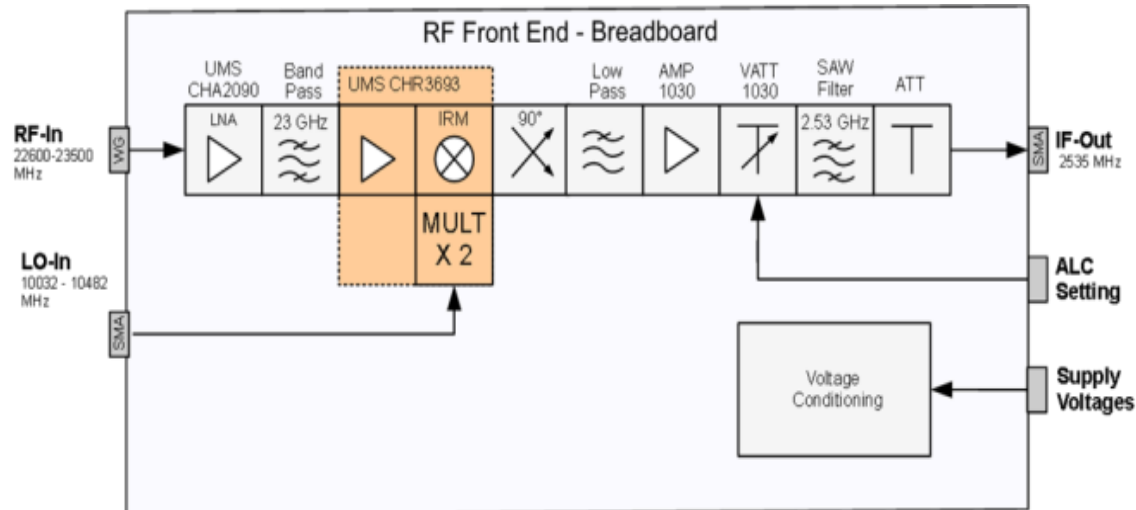
# Breadboard Overview



# Breadboard - IF Test @ 2.5 GHz



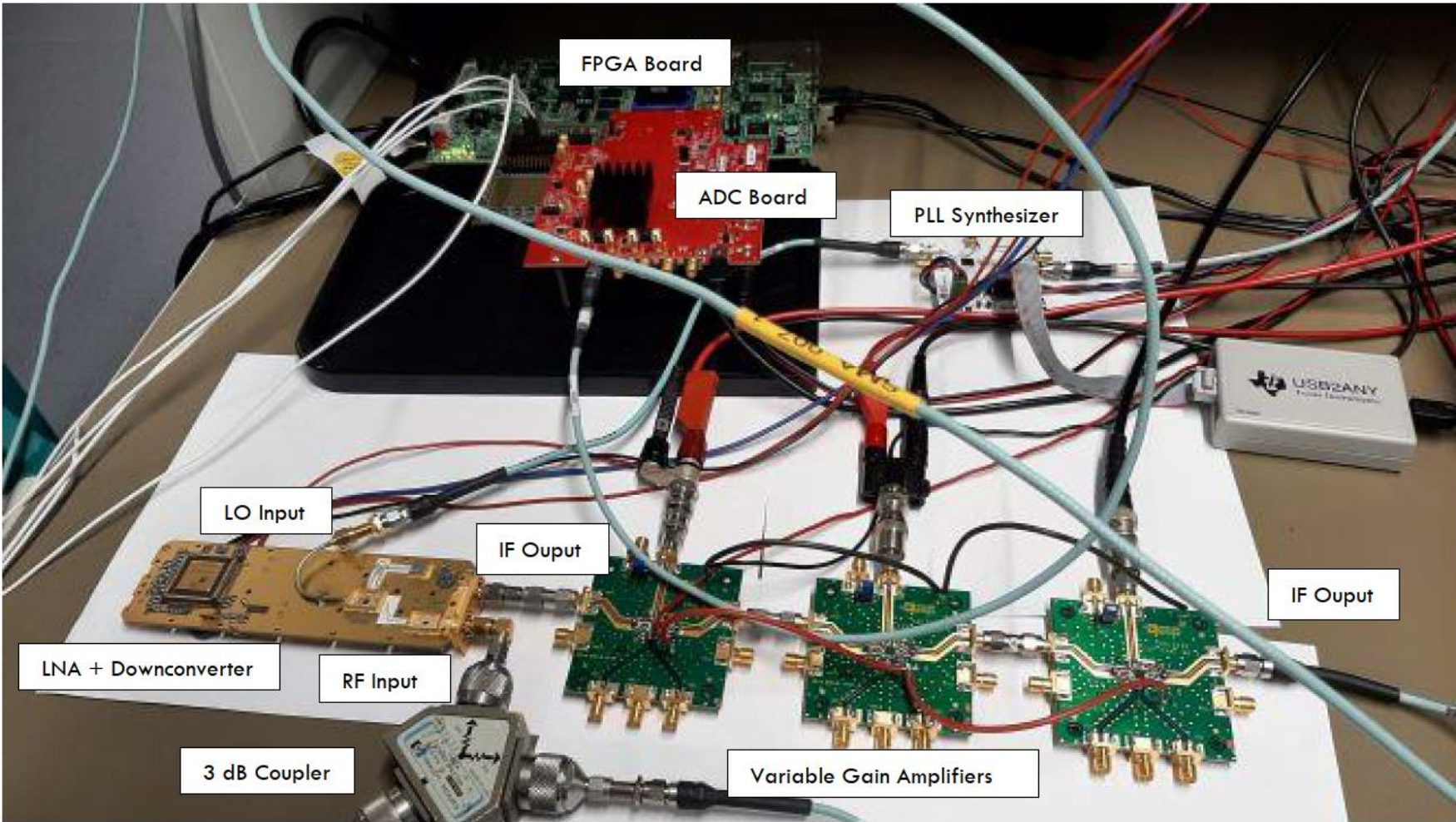
# RF front end (Tesat)



- The CHA2090 LNA is a three-stage self-biased wide band monolithic low noise amplifier .
- 23 GHz Bandpass filter of TESAT design realized as microstrip MIC filter.
- CHR3693 is a multifunction chip which integrates: a balanced cold FET mixer; a times two LO multiplier; a RF self-biased LNA.
- ~3 GHz lowpass IF filter is a TESAT design again realized as microstrip MIC filer.
- IF amplifier and attenuator MMICs are standard TESAT designs manufactured at UMS on a space qualified GaAs process.



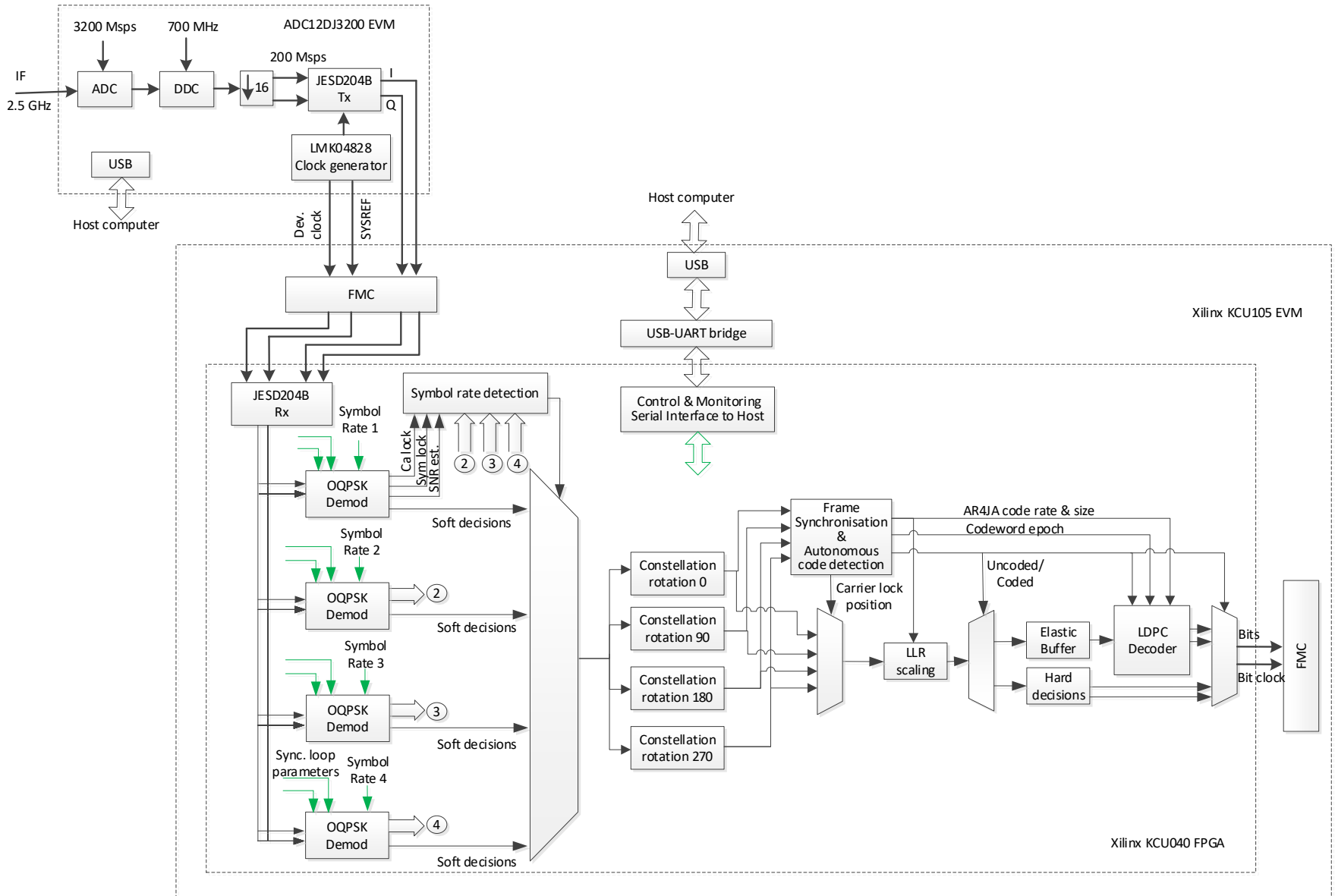
# Breadboard Hardware



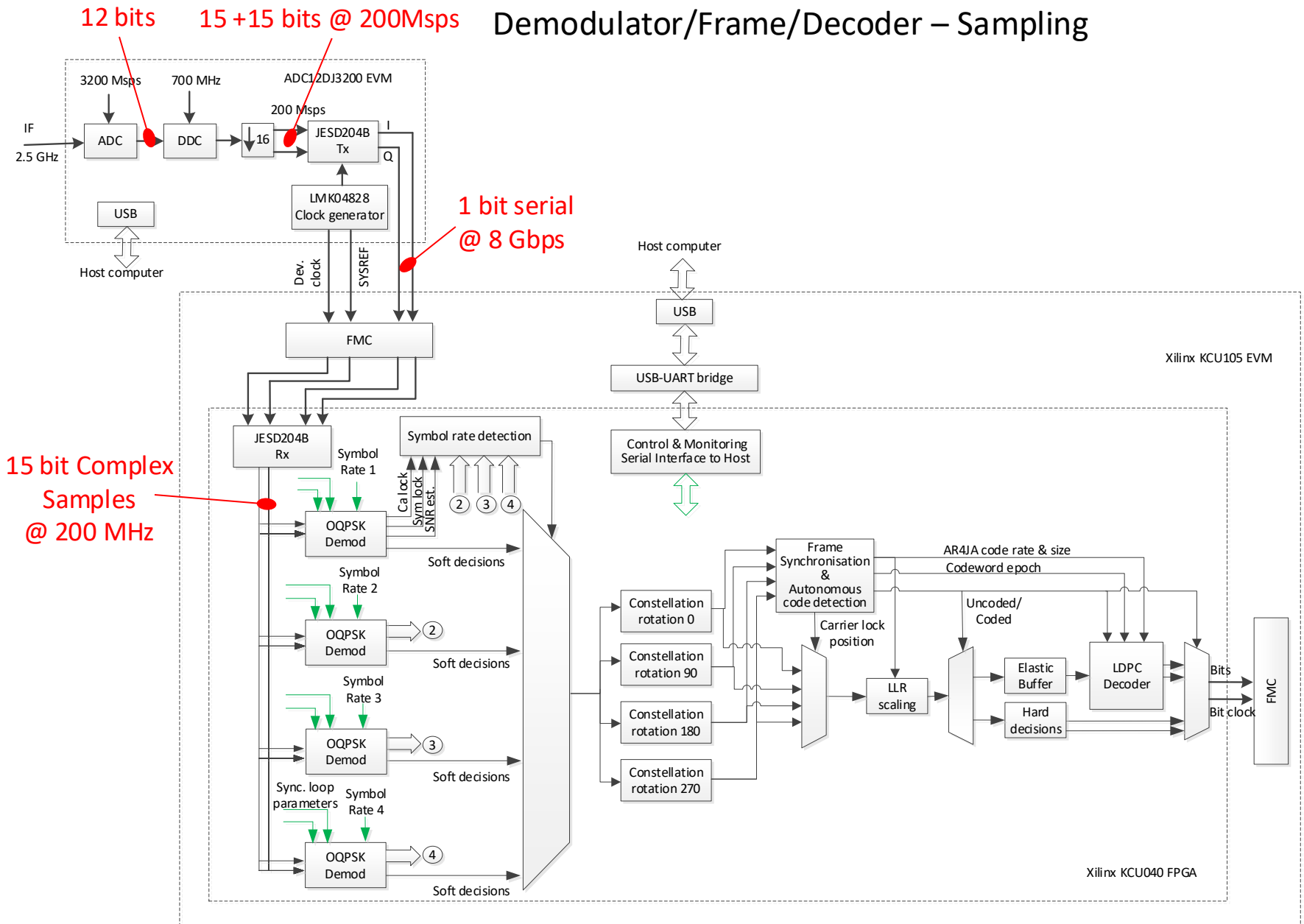
# Demodulator / Decoder Requirements

- Modulation: **SRRC-OQPSK** with symbol rates between **10-100 Msym/s** (bandwidth limited)
- Channel coding: CCSDS AR4JA **LDPC codes** {1/2, 2/3, 4/5}, 16k, and 1/2, 1k
- **Autonomous detection of channel symbol rate** from a preconfigured list of 4 symbol rates
- **Autonomous detection of LDPC code rate and block length**
- Fade mitigation (“Free Wheel” through fades)
- Target Frame Error Rate (FER) of 1E-4
- **Doppler shift of up to +/-150 kHz and Doppler rate of up to +/-120 Hz/s**

# DSP : Demodulator / Codeword Sync / Decoder Overview

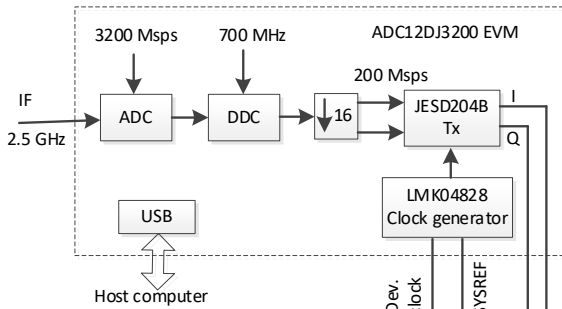


# Demodulator/Frame/Decoder – Sampling

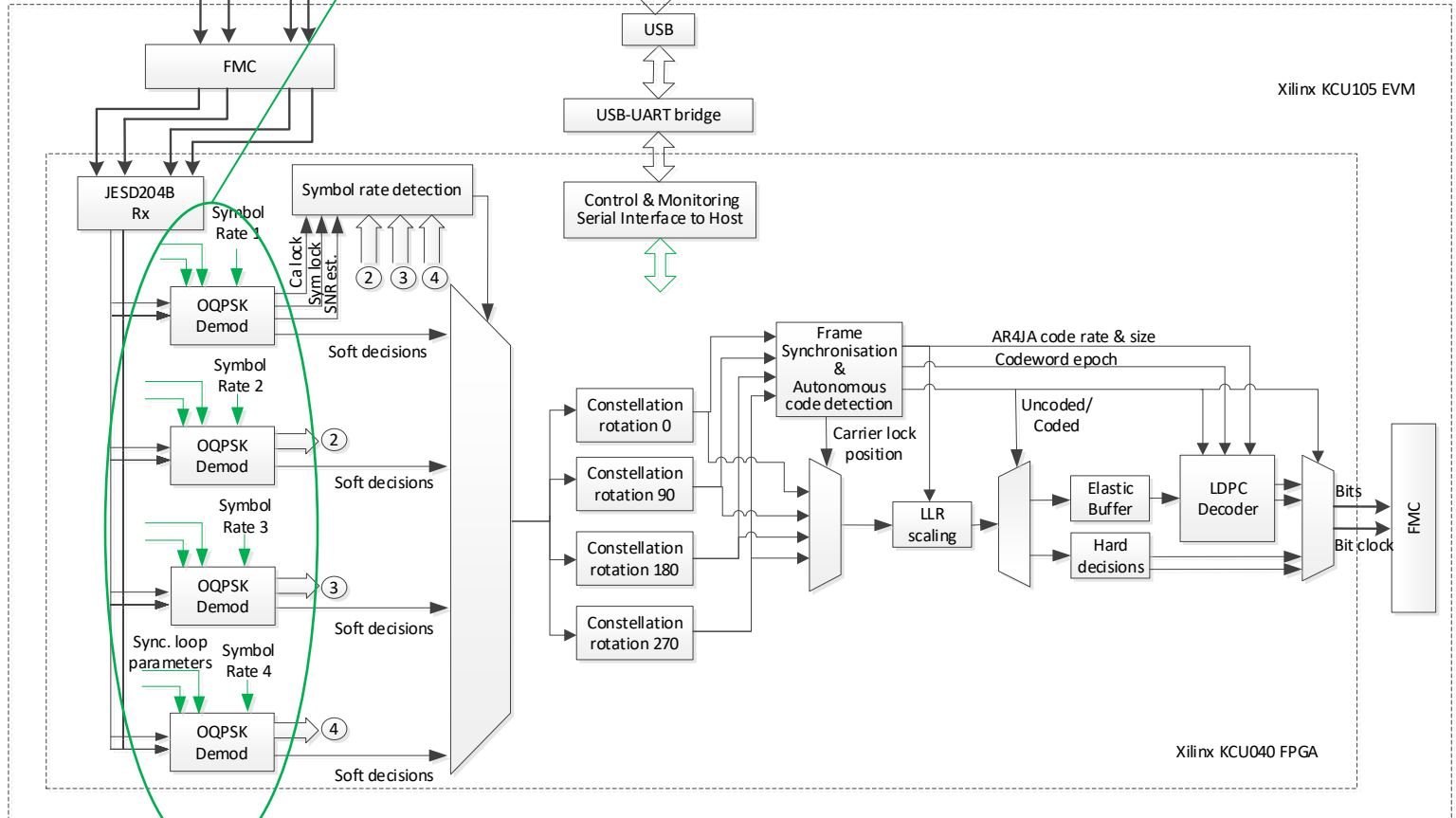




# Demodulators

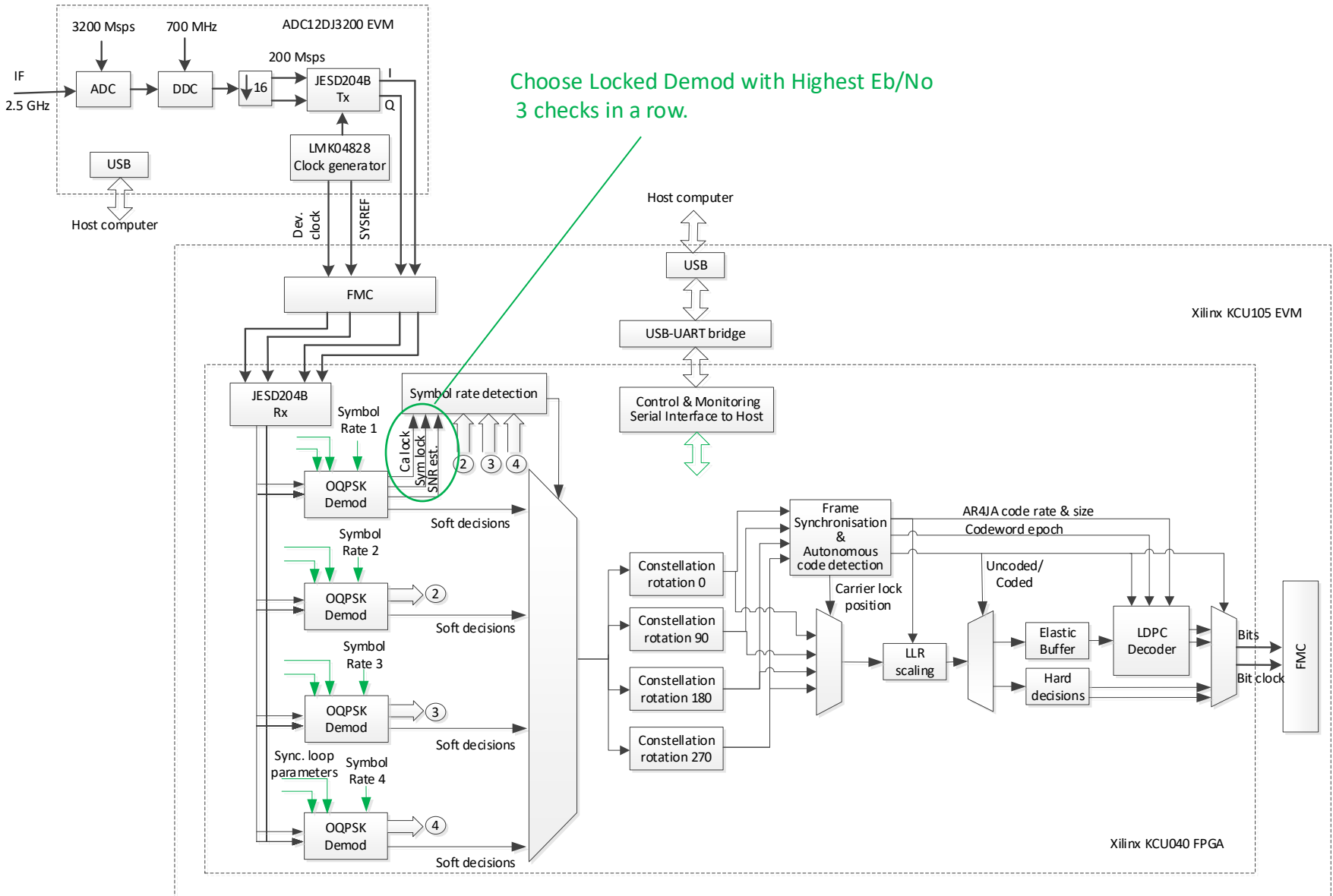


- Maximum Likelihood Joint Carrier and Timing estimation
- Polyphase matched filters and derivative matched filters
- SRRC from rolloff 0.1 -> 1 with coefficients in RAM
- Channel Eb/No estimate within 0.05 dB for Eb/No > -6.0 dB
- Loops closed in hardware with progressive bandwidth reduction

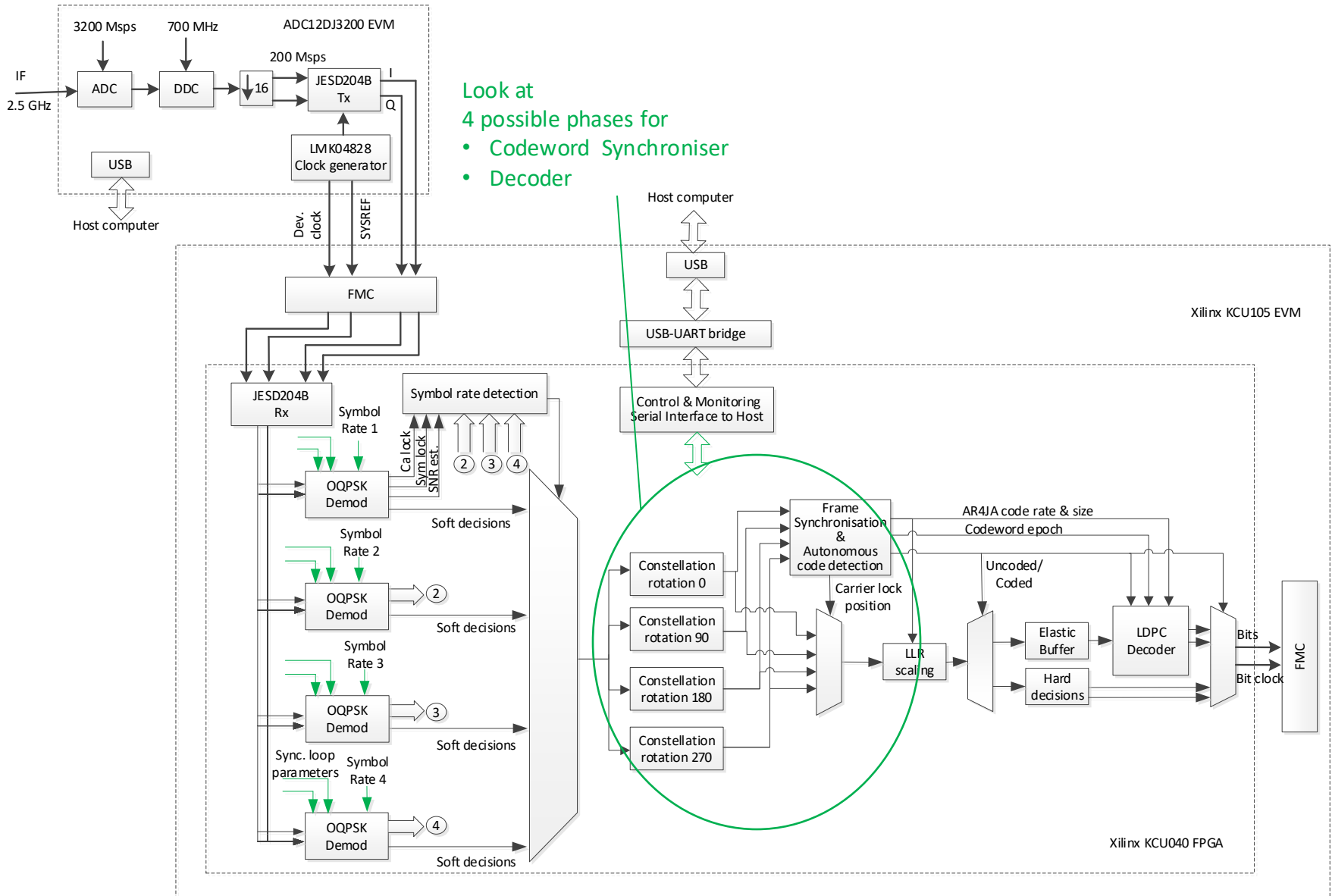




# Demodulator - Autonomous Symbol rate detection



# Codeword Sync – Autonomous Code Rate & Length



Look at  
4 possible phases for

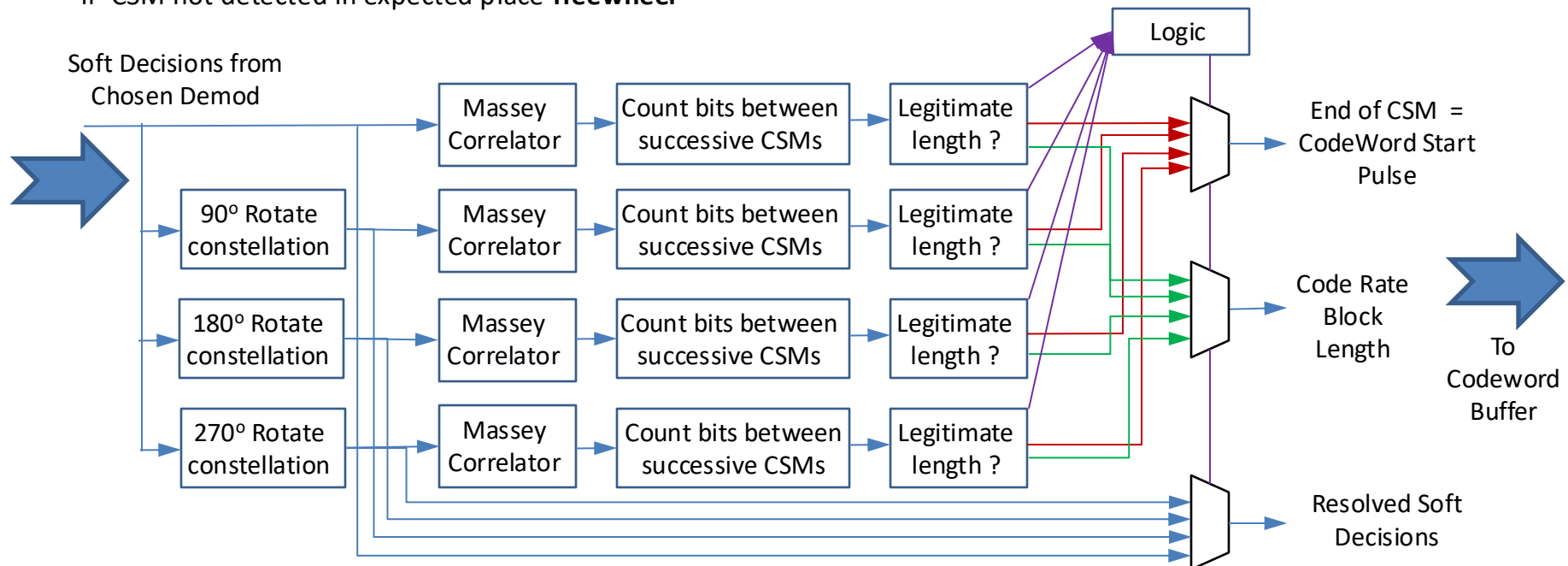
- Codeword Synchroniser
- Decoder

# Codeword Sync – Autonomous Code Rate & Length Algorithm

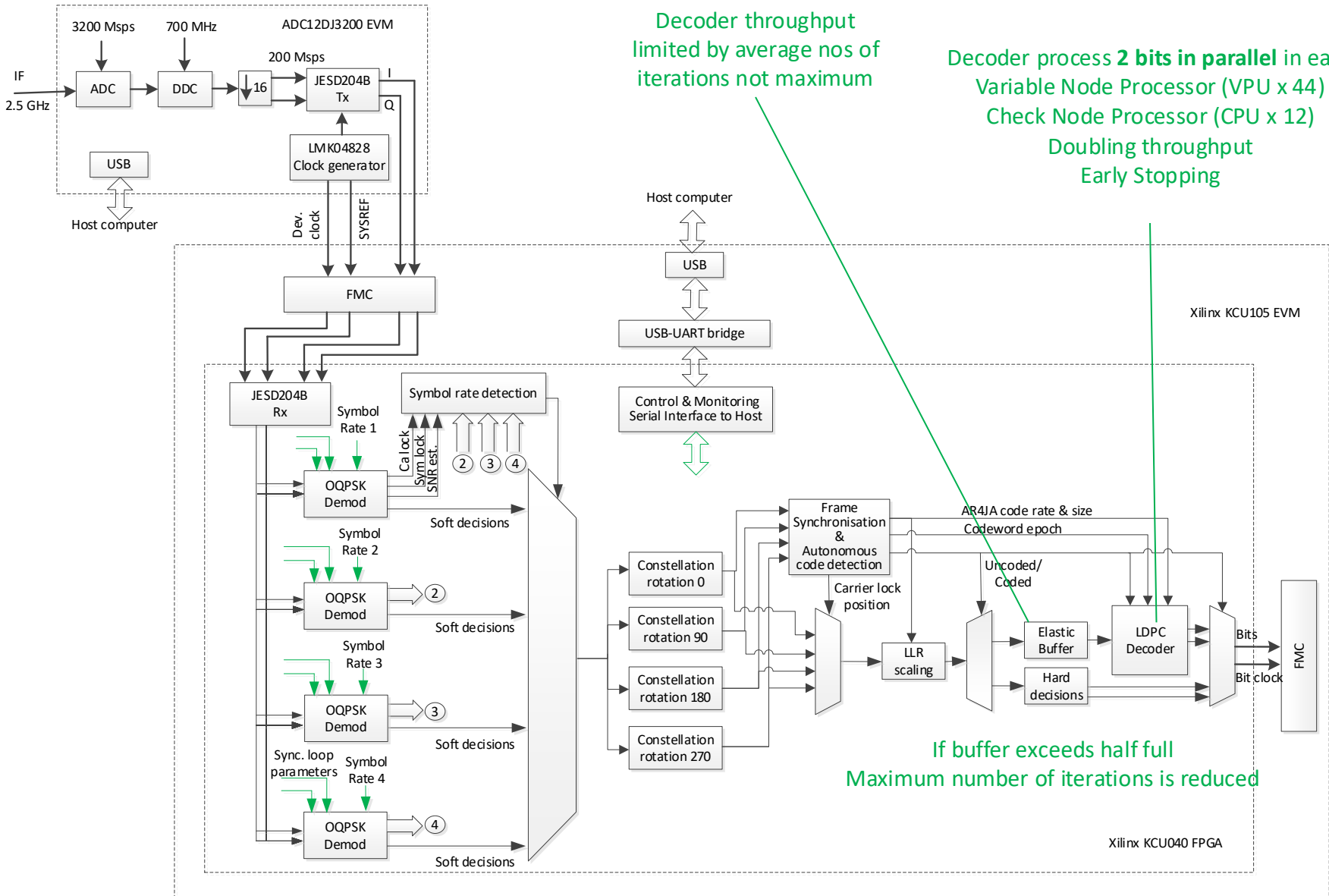
Unique  
Codeword  
Lengths

Block Size	1,024	4,096	16,384
Rate 4/5	1,280	5,120	20,480
Rate 2/3	1,536	6,144	24,576
Rate 1/2	2,048	8,192	32,768

- Maintain 4 counters counting bits between detected **Code Sync Markers** (CSMs ) from Massey Correlators
- Codeword lengths are unique, confusion possible only if 2 consecutive CodeWord Sync Markers missed ( $3 \times 2048 = 4 \times 1536$ )
- If (count between detections == codeword length or twice codeword length) then declare found
- If CSM not detected in expected place **freewheel**



# LDPC Decoder



# Freewheeling through Fades

As depth of fade increases :

- FER approaches 1 (~0.5 dB Fade) - “immediate” recovery < 1 codeword
- Carrier phase flips => bit slips (a few dB) => Loss of Codeword synchronisation – quick recovery, < 2 codewords
- Loss of carrier lock and loss of Bit sync lock – quick recovery < 1 mS
- Loss of carrier frequency estimate & bit clock – complete re-acquisition required

## Mitigation

- Codeword Sync “freewheel” will generate pulses at appropriate intervals for upto 4095 missed Codewords
- Leave Carrier and Bit Sync loops in narrow band tracking mode to stay on frequency (until time out)

# Testing

- Test FPGA stand alone (Demodulators, Sync detection, Code Rate & Length detection, LDPC Decoder)
  - Signal from waveform sample look up (exact Eb/No setting)
  - BER from LDPC „for free“
  - FER from LDPC „for free“
  - Acquisition time from in built timers
- Test FPGA and ADC with IF input
  - Analogue signal generator,
  - BER Tester (measures errors in undecoded codewords)
- Test at RF
  - Analogue Signal generator and upconverter, BER Tester



# Testing – FPGA Standalone

98 Msyms/S, 1/2 rate 16384 info block, channel Ecs/No = -1.75, Eb/No = +1.25 dB

The screenshot displays the VHDR Control and Monitoring software interface, which is used for testing an FPGA standalone. The interface is divided into several functional areas:

- Time domain plot:** Shows a signal waveform over time, with a vertical cursor at approximately 0.80.
- Configure Receiver:** A central configuration window with multiple sections:
  - Symbol Rate Detection:** Manual Demod Selection (unchecked), Demod to Use (0).
  - Frame Synchroniser:** Indefinite free-wheel (unchecked), Frames to FreeWheel (13), Coded CSM Detected Threshold (-140), Uncoded CSM Detected Threshold (-18).
  - CodeWord FIFO Buffer:** Reset FIFO button.
  - LDPC Decoder:** Early Stopping (checked), Maximum iterations < 1/2 full (450, 400, 400, 90), Maximum iterations > 1/2 full (300, 230, 220, 28).
  - Data Output delay:** Gate delay (0), Write button.
- Demodulator 3:** Configuration for Carrier Recovery and Symbol Timing.
  - Carrier Recovery:** Carrier Rest Frequency (0.0 Hz), PLL Log2 Proportional Constant (11), PLL Log2 Integral Constant (16), PLL Integrator Leak (3), PLL Integrator Monitor TC (0), PLL Integrator Limit (150,000.0 Hz), PLL log2 Bandwidth reduction (3), PLL Lock Threshold (60), PLL Unlock Threshold (0), Acq PLL Loop Bandwidth (2BI) (490,885.8 Hz), PLL Damping Factor (1.59).
  - Symbol Timing:** Symbol Rest Frequency (98,000,000.0 Hz), PLL Log2 Proportional Constant (9), PLL Log2 Integral Constant (11), PLL Integrator Leak (3), PLL Integrator Monitor TC (0), PLL Integrator Limit (5,000.0 Hz), PLL log2 Bandwidth reduction (3), PLL Lock Threshold (10), PLL Unlock Threshold (-50), Acq PLL Loop Bandwidth (2BI) (48,568.9 Hz), PLL Damping Factor (1.41).
- Receiver Monitor:** A comprehensive monitoring window showing:
  - Input Power (dBfs):** -25.03
  - Carrier Recovery Status:** Carrier Lock Quality (-5), Carrier Lock Status (Unlocked), Configured Symbol Rate (9,800,000.0), Symbol Rate Offset (79.4), Timing Lock Quality (-284), Timing Lock Status (Unlocked), IQ Stagger (symbols) (0.500), Co-Timing Loop Lock (Unlocked), Mean Symbol Absolute Amplitude (15.10), Apparent Eb/No I Chan (dB) (< -4.00), Apparent Eb/No Q Chan (dB) (< -4.00).
  - Demod Selector:** Chosen Demod (green = detected) is 3.
  - Frame Sync:** Yes (green), Frame Type (16,384, r = 1/2), Coded CSMs Found/Missed/Unexp (41,217, 417, 32,566), Uncoded CSMs Found/Missed/Unexp (0, 0, 299,967).
  - CodeWord buffer:** Gap between Codewords (0), Wrong Gap Count (41,842,848), Frames Received / Frame Resyncs (0, 0.85), Code Words in Buffer (0.85).
  - LDPC Decoder:** Absolute LLR Amp (10), Decoder Iterations / Bits corrected (35, 4,147), Decoded Channel Bits / Errors (1,368,815,534, 0.8), Apparent Channel BER (0.123922), Codewords Total / Successful / Failed (41,842,843, 41,772,936, 69,907), FER (0.00167070).
- About VHDR Probe:** Shows software version (VHDL Java GUI Revision: 37), date (03 May 2022), and intended version (75 on).
- Address Map Numbers:** VHDL Register Address Map Version number (35), XML Register Address Map Version number (35), XML Loaded Register Data Title (Config 1 of D9 V and V procedure).
- Revision:** VHDL Repository Revision Number (75), Stored Sample Information Rate (9.800 Mbps), Stored Sample Code Rate, k (1/2, 16384), Stored Sample Eb/No (No Noise dB).

# Testing – FPGA Standalone

98 Msyms/S, 1/2 rate 16384 info block, channel Ecs/No = -1.75, Eb/No = +1.25 dB

Demod #3 locked

The screenshot displays the VHDR Control and Monitoring software interface, which is used for testing an FPGA standalone. The interface is divided into several windows:

- Time domain:** Shows a plot of the signal in the time domain, with a y-axis ranging from 0.5 to 1.0 and an x-axis from 0.80 to 0.90.
- Configure Receiver:** Contains settings for Symbol Rate Detection, Frame Synchroniser, LDPC Decoder, and Data Output delay. The LDPC Decoder section shows settings for Demod 0, 1, 2, and 3.
- Demodulator 3:** Shows Carrier Recovery and Symbol Timing parameters for Demodulator 3.
- Receiver Monitor:** Displays a table of receiver performance metrics for four demodulators (Demod 0, 1, 2, and 3). Demod 3 is highlighted with a green circle and labeled "Demod #3 locked".
- Signal Source:** Shows signal type and noise configuration.
- About VHDR Probe:** Provides information about the software version and configuration.

The Receiver Monitor window contains the following data:

	Demod 0	Demod 1	Demod 2	Demod 3
Input Power (dBfs)	-25.03			
Carrier Lock Quality	-5	-11	-12	83
Carrier Lock Status	Unlocked	Unlocked	Unlocked	Locked Narrow
Configured Symbol Rate	9,800,000.0	18,798,828.1	31,47,656.3	98,000,000.0
Symbol Rate Offset	79.4	-65.8	60.1	119.0
Timing Lock Quality	-284	-275	276	21
Timing Lock Status	Unlocked	Unlocked	Unlocked	Locked Narrow
I/Q Stagger (symbols)	0.500	0.500	0.500	0.500
Co-Timing Loop Lock	Unlocked	Unlocked	Unlocked	Locked
Mean Symbol Absolute Amplitude	15.10	11.64	17.19	21.17
Apparent Eb/No I Chan (dB)	< -4.00	< -4.00	< -4.00	-1.75
Apparent Eb/No Q Chan (dB)	< -4.00	< -4.00	< -4.00	-1.77
Chosen Demod (green = detected)	0	1	2	3
Frame Sync	Yes	-127	1.25	dB
Phase, Phase/Code Flips, Old Phases	90	2	180	90
Frame Type, Old Frame Types	16,384, r = 1/2		16k, r = 1/2	16k, r = 1/2
Coded CSMs Found/Missed/Unexp	41,217,417	625,435	32,566	at 14,979
Uncoded CSMs Found/Missed/Unexp	0	0	299,967	at 7,325
CodeWord buffer	64			
LDPC Decoder	10			
Decoder Iterations / Bits corrected	35	4,147		
Decoded Channel Bits / Errors	1,368,815,534.08	169,626,173.600		
Apparent Channel BER	0.123922			
Codewords Total / Successful / Failed	41,842,843	41,772,936	69,907	
FER	0.00167070			

# Testing – FPGA Standalone

98 Msyms/S, 1/2 rate 16384 info block, channel Ecs/No = -1.75, Eb/No = +1.25 dB

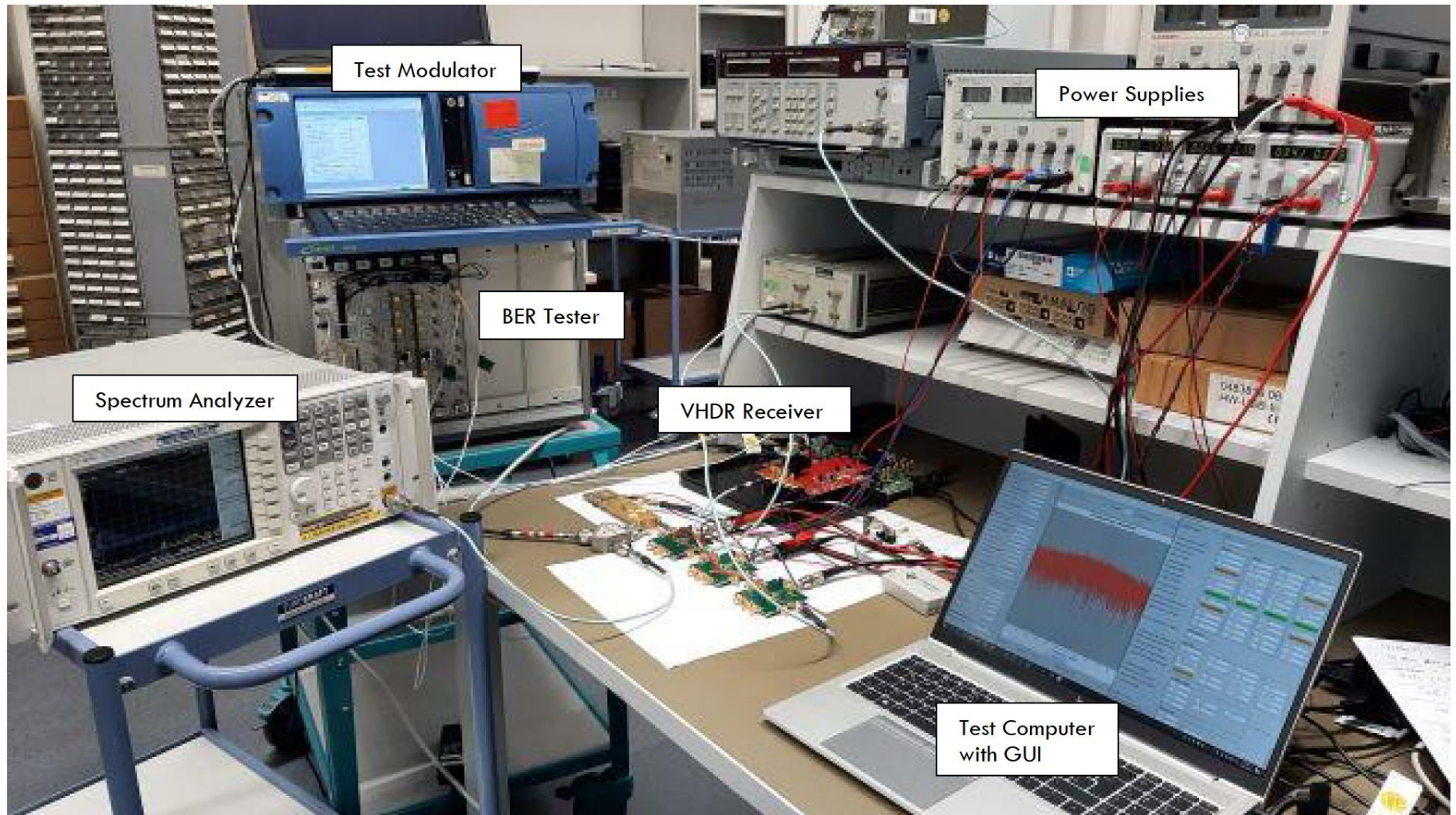
Frame Sync and Autonomous rate & Length

The screenshot displays the VHDR Control and Monitoring software interface, which is used for configuring and monitoring the FPGA standalone testing. The interface is divided into several main sections:

- Time domain:** Shows a plot of the signal waveform over time, with a 'Time' axis ranging from 0.5 to 1.0.
- Configure Receiver:** A dialog box for configuring the receiver parameters, including:
  - Symbol Rate Detection:** Manual Demod Selection, Demod to Use (0).
  - Frame Synchroniser:** Indefinite free-wheel, Frames to FreeWheel (13), Coded CSM Detected Threshold (-140), Uncoded CSM Detected Threshold (-18).
  - LDPC Decoder:** Early Stopping (checked), Maximum iterations < 1/2 full (450, 400, 400, 90), Maximum iterations > 1/2 full (300, 230, 220, 28).
  - Data Output delay:** Gate delay (0).
- Demodulator 3:** A dialog box for configuring the demodulator parameters, including:
  - Carrier Recovery:** Carrier Rest Frequency (0.0), PLL Log2 Proportional Constant (11), PLL Log2 Integral Constant (16), PLL Integrator Leak (3), PLL Integrator Monitor TC (0), PLL Integrator Limit (150,000.0), PLL Log2 Bandwidth reduction (3), PLL Lock Threshold (60), PLL Unlock Threshold (0), Acq PLL Loop Bandwidth (2BI) (490,685.8), PLL Damping Factor (1.59).
  - Symbol Timing:** Symbol Rest Frequency (98,000,000.0), PLL Log2 Proportional Constant (9), PLL Log2 Integral Constant (11), PLL Integrator Leak (3), PLL Integrator Monitor TC (0), PLL Integrator Limit (5,000.0), PLL Log2 Bandwidth reduction (3), PLL Lock Threshold (10), PLL Unlock Threshold (-50), Acq PLL Loop Bandwidth (2BI) (48,568.9), PLL Damping Factor (1.41).
  - Co-Timing:** Enable (checked), log2 Loop Gain (1), Phase Error Limit (0.100), log2 Bandwidth reduction (1), Lock Threshold (0.010), Unlock Threshold (0.015), Time Constant (167.772).
  - Demodulator Output Scaling:** Matched Filter Downshift (2).
- Receiver Monitor:** A dialog box for monitoring the receiver performance, including:
  - Input Power (dBfs):** -25.03.
  - Configured Carrier Frequency (Hz):** 0.0.
  - Apparent Frequency offset (Hz):** -115.6, -976.6, 1,544.2, 5,973.1.
  - Carrier Lock Quality:** -5, -11, -12, 83.
  - Carrier Lock Status:** Unlocked, Unlocked, Unlocked, Locked Narrow.
  - Configured Symbol Rate:** 9,800,000.0, 18,798,828.1, 31,347,656.3, 98,000,000.0.
  - Symbol Rate Offset:** 79.4, -65.8, 890.1, 119.0.
  - Timing Lock Quality:** -284, -275, -276, 21.
  - Timing Lock Status:** Unlocked, Unlocked, Unlocked, Locked Narrow.
  - I/Q Stagger (symbols):** 0.500, 0.500, 0.500, 0.500.
  - Co-Timing Loop Lock:** Unlocked, Unlocked, Unlocked, Locked.
  - Mean Symbol Absolute Amplitude:** 15.10, 11.64, 17.89, 21.17.
  - Apparent Eb/No I Chan (dB):** < -4.00, < -4.00, < -4.00, -1.75.
  - Apparent Eb/No Q Chan (dB):** < -4.00, < -4.00, < -4.00, -1.77.
  - Demod Selector:** Chosen Demod (green = detected) is 3.
  - Frame Sync:** Framing Found, Massey Metric, Eb/No (Yes, -127, 1.25, dB), Phase, Phase/Code Flips, Old Phases (90, 2, 180, 90), Frame Type, Old Frame Types (16,384, r = 1/2, 16k, r = 1/2, 16k, r = 1/2), Coded CSMs Found/Missed/Unsync (41,217,417, 625,435, 32,566, at 14,979), Uncoded CSMs Found/Missed/Unsync (0, 0, 299,967, at 7,325).
  - CodeWord buffer:** Gap between Codewords (-24), Wrong Gap Count, Gap, Old Gap (0), Frames Received / Frame Resyncs (41,842,848, 0), Code Words in Buffer (0.85).
  - LDPC Decoder:** Absolute LLR Amp (10), Decoder Iterations / Bits corrected (35, 4,147), Decoded Channel Bits / Errors (1,368,815,534.08, 169,626,173.600), Apparent Channel BER (0.123922), Codewords Total / Successful / Failed (41,842,843, 41,772,936, 69,907), FER (0.00167070).
- About VHDR Probe:** Shows the software version (VHDL Java GUI Revision: 37, 03 May 2022, (c) Zelinda Ireland Ltd) and configuration details (Intended for VHDL Repository version 75 on, Address Map Numbers, Revision).

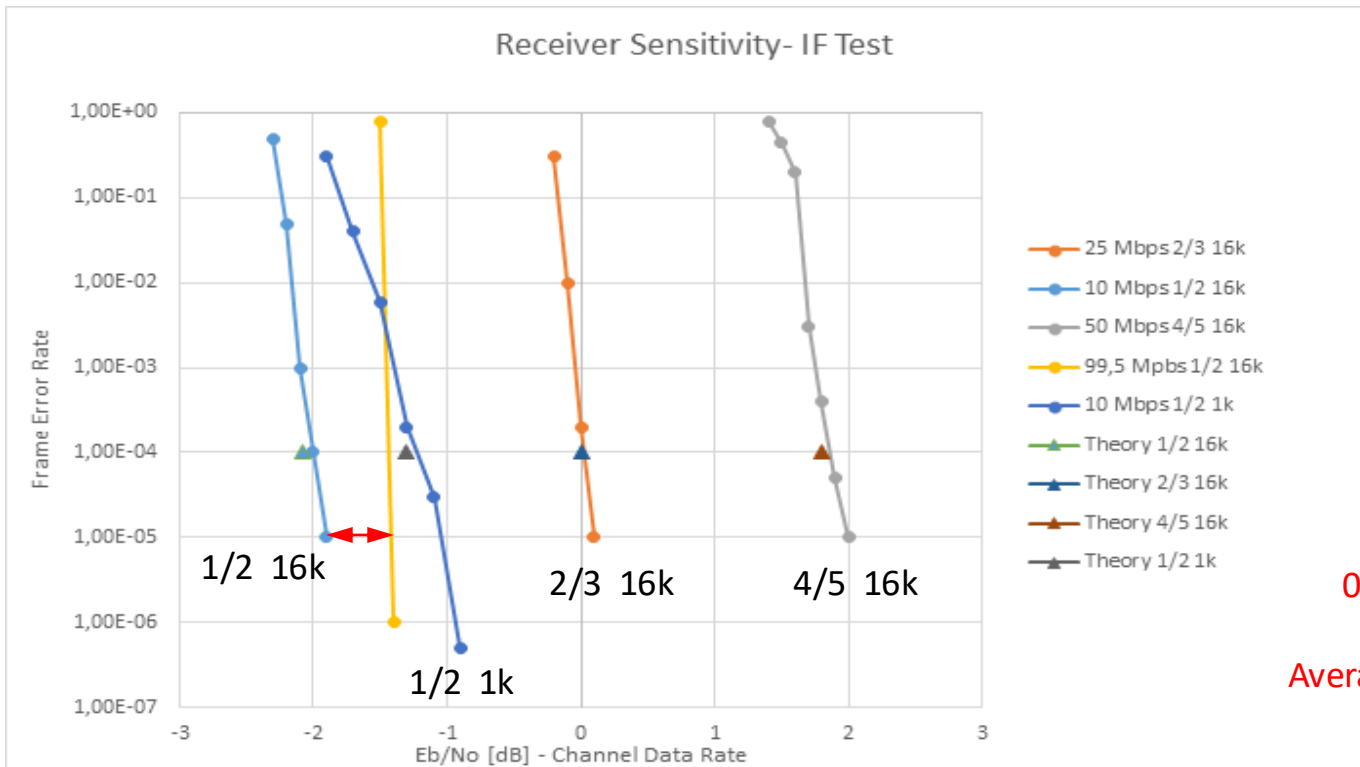


# Testing – at RF and IF



# Testing – Results Summary

- Noise figure : 2.5 dB
- Total Implementation loss (ADC, Demod, Decoder) in Digital domain : < 0.2 dB (except ½ rate > 75 Mbps)
- Acquisition time : Typically < 20 mS @ max Doppler & rate



0.5 dB additional Loss  
@100 Mbps  
Average iterations limit of 31

# Future Qualification

- Breadboard used **Xilinx Kintex Ultrascale XCKU040** (530 k logic cells, 1930 DSP slices, ~50% logic utilisation)
- Space Qualified RT Kintex Ultrascale available **XQRKU060**, 20nm process, 726k logic cells, 2760 DSP slices.
- SEM (Single Event Mitigation) IP core to check and correct erroneous re-configuration
- Can always use TMR (manual using VHDL functions) for critical registers (eg configuration)
- Many ADC options (in future including ADCs within the FPGA)



# Conclusion

- Single stage down-conversion from 23.2 GHz
- High IF and high sampling rate, 2.5 GHz IF at 3.2 Gsamples/S
- Autonomy works reliably for modest additional hardware and no specification change.
- AR4JA codes well suited to this type of Uplink





# Self-Test & Self Check out – An extra Requirement ?

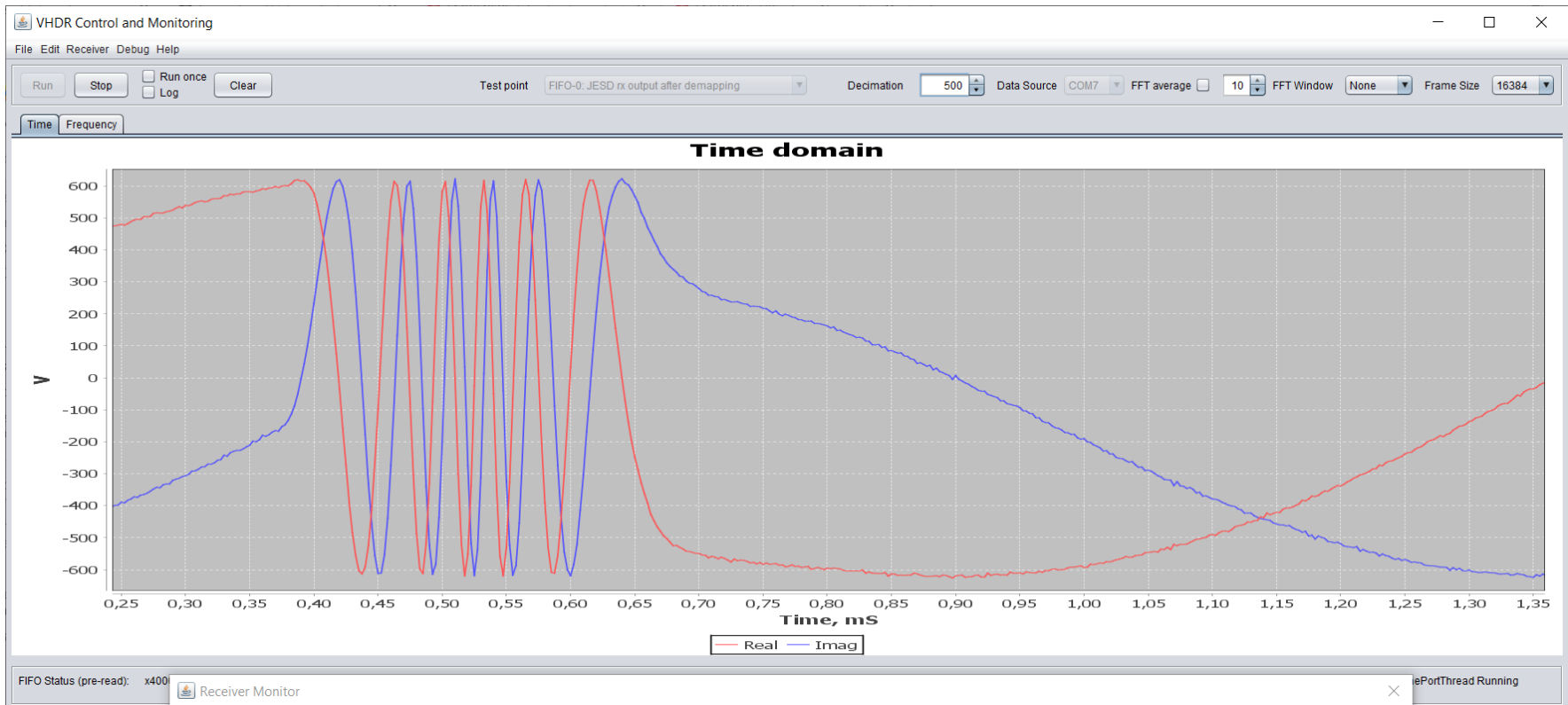
- Additional Self Test and Debug features can dramatically speed up development
- Stimulus
  - Noise free complex near baseband waveform samples from MATLAB (with integral number of Frames and integral number of carrier cycles) stored in FPGA
  - Choose stored samples from low symbol rate ( $\sim 10$  Msym/S) (one  $\frac{1}{2}$  rate CW of 32,768 syms  $\Rightarrow$   $\sim 640k \times 32$  bit Mbit)
  - Use prime number of samples and Sample read back logic that decimates so 10 symbol rates can be tested
  - Added AWGN in real time within FPGA using mutiple leap forward LFSRs, with adjustable Eb/No using mutipliers
- Deep Monitoring
  - Multiple FIFOs added within FPGA to capture samples at various points
  - Timers added to FPGA to record
    - Carrier & Clock acqusitions times (for 4 demodulators),
    - Demod Selection time,
    - Frame Sync & Code rate & length detection time
- JAVA GUI over USB for control and monitoring including time and frequency domain display of FIFO waveform captures

Useful not just in development, but also in space craft integration.



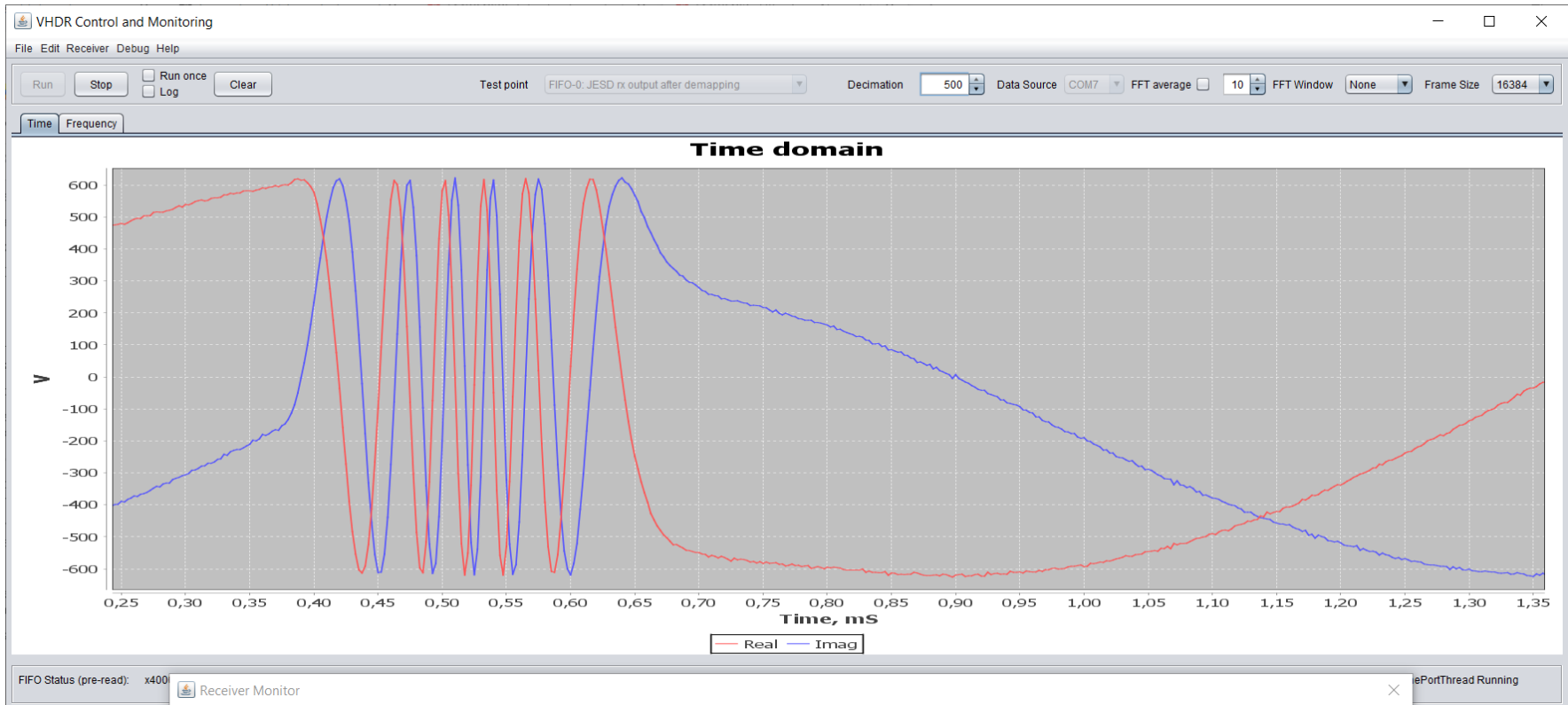
# A lesson Learned

- Persistent loss of Demodulator lock at low Data rates
- Tesat testing identified that at low data rates (10, 12.5 Mbps) VHDR had decoded bit errors for  $E_b/N_0 < 3.3$  dB (versus theory  $\sim 1.0$  dB) and Demodulator symbol lock quality very poor.



# A lesson Learned

- Persistent loss of Demodulator lock at low Data rates
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Tesat tried a Fan on ADC – problem eliminated.

# VHDR – Doppler and the LOP-G orbit

Chosen LOP-G orbit is a (southern) **Near Rectilinear Halo Orbit** around L2.

- The points Lagrange points  $L_1$ ,  $L_2$ , and  $L_3$  are positions of unstable equilibrium.
- Rectilinear - as eccentricity  $\rightarrow 1$  so elliptical orbit tends to vertical “up and down” straight line – no use for planetary orbits as would hit the planet surface.
- near rectilinear - resembling a “flattened ellipse” with nearly parallel sides.
- A halo orbit is a periodic, three-dimensional orbit associated with one of  $L_1$ ,  $L_2$  and  $L_3$  .
- the NRHOs are those members of the halo family with bounded stability
- NRHP can be evolved from a “Lyapunov” orbit sitting in the Moon orbital plane ( $5.1^\circ$  to the ecliptic)

# VHDR – the NRHO advantages

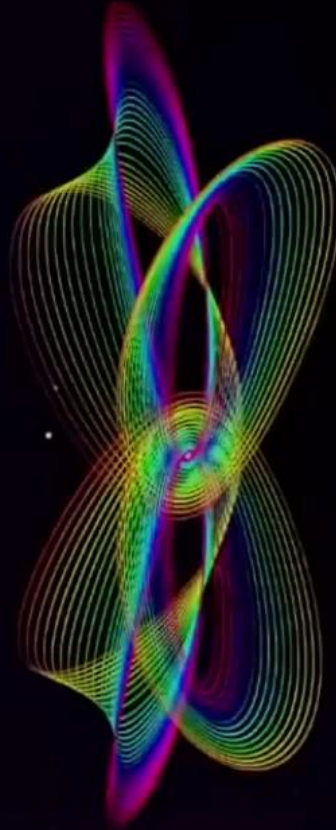
- Visible from far side of moon
- (almost) Always in Sunlight
- Always visible from earth (no occultation)
- Relatively Easy to get to (low energy)
- Long Period around 7 days so **low Doppler** wrt Lunar surface (LO->LS link).
- Almost perpendicular to plane of moon orbit so **low Doppler** wrt to earth (E->LO)



# VHDR – other Halo orbits

- Although Halo orbits are nominally around Lagrange points they are closer to the Moon.
- Northern and Southern Halos exist around L1 as well as L2, so 4 nearly stable orbit possibilities.

P1: Earth  
P2: Moon  
Radius P2: 0.0045 Scaling: 1.0  
JC: 3.0594349784036745



The Northern and Southern L<sub>1</sub> and L<sub>2</sub> NRHOs are periodic in the Circular Restricted 3-Body Model, and can be transitioned into quasi-periodic orbits in a higher fidelity model

Jacobi Constant: 2.99957  
Y Amplitude: 3.735951E04 km  
Z Amplitude: 7.518863E04 km  
Period: 0008.9130 days  
Close Approach: 7.071249E05 km

# Testing

- Test FPGA stand alone (Demodulators, Sync detection, Code Rate & Length detection, LDPC Decoder)
  - Stimulus
    - Noise free complex near baseband waveform samples from MATLAB (with integral number of Frames and integral number of carrier cycles) stored in FPGA
    - Added AWGN in real time within FPGA using multiple leap forward LFSRs, with adjustable Eb/No using multipliers
  - Deep Monitoring
    - Multiple FIFOs added within FPGA to capture samples at various points
    - Timers added to FPGA to record
      - Carrier & Clock acquisitions times (for 4 demodulators),
      - Demod Selection time,
      - Frame Sync & Code rate & length detection time
  - JAVA GUI over USB for control and monitoring including time and frequency domain display of FIFO waveform captures
- Test FPGA and ADC with IF input
  - Analogue signal generator, BER Tester
- Test at RF
  - Analogue Signal generator and upconverter, BER Tester