Highly Accelerated Life Test Pilot Supporting Agile Space Engineering

ESA contract No. 4000134569/21/NL/KM

Executive Summary Report

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1 STARTING POINT

1.1 Approach

A fast-testing methodology such as Highly Accelerated Life Testing (HALT hereinafter), already in place in other industries (mass consumer products, automotive, defense) for the past 40 years, would be of incredible interest if suitably applied to the fast-developing new space industry.

In particular, if HALT could be useful to accelerate validation processes of complete assembled boards, made up of COTS components, and identifying design key aspects more susceptible to fail during a space mission, it will be an important achievement in the new space industry.

1.2 Testing Samples & EUT description

To evaluate how the HALT testing can actually bring relevant information regarding the reliability of a COTS space board, a total of 10 samples of a printed circuit board, called TOTEM, in a relevant state of maturity, has been manufactured and subject to a specific HALT test sequence.

The TOTEM board, with a Technology Readiness Level 9, has been aboard 2 different missions in LEO orbits (LUME-I led (launched on December 2018) and AIST2U (launched also on December 2018) for more than 2 years, and it has been extensively monitored during all this time.

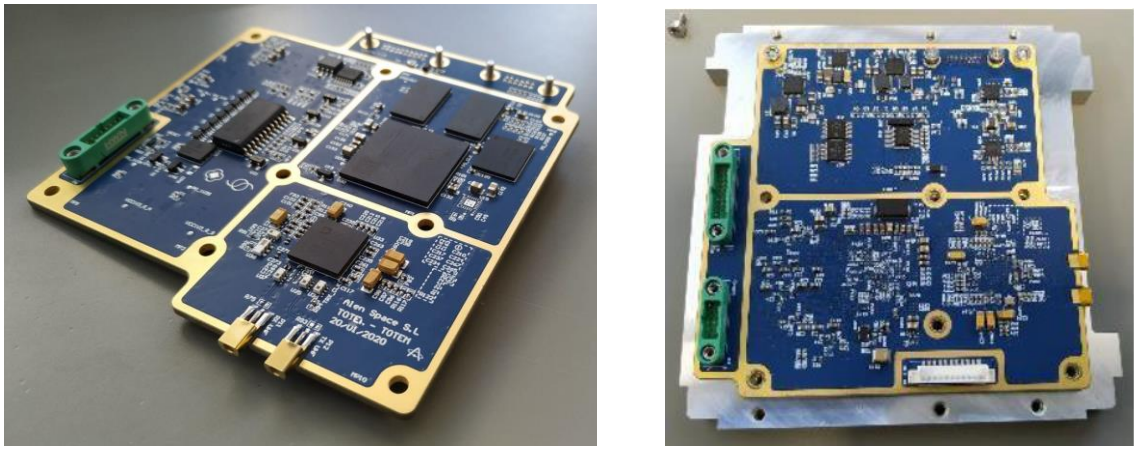


Figure 1: TOTEM board without and with enclosure, respectively.

TOTEM is a Software-Defined Radio for nanosatellites, based on a high-performance System-On-Chip (Xilinx Zynq-7000 series) and a wide frequency range RF transceiver, manufactured by Alen Space. It is a Wideband Transceiver, with Multiple Interfaces and memories (2x 4 Gb DDR3L, 8 Gb NAND Flash, 4 Mb MRAM), and a 5V power supply. Its operational temperature ranges between -40ºC and +85ºC.

The functional block diagram of the board is then displayed hereinafter:

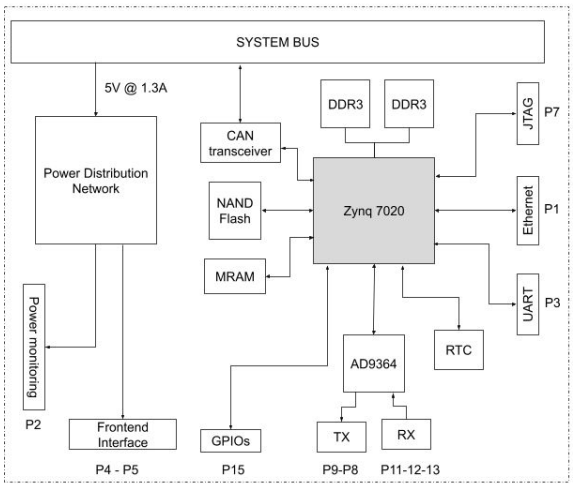


Figure 2: TOTEM block diagram

2 TEST PLAN DESCRIPTION

2.1 HALT Test plan choice

The test plan carried out during the HALT campaign was chosen in order to induce an increasing thermal and mechanical stress on each sample, with the final objective to identify latent failure modes and the environmental reliability margins of the EUT design.

It was decided to follow a serial testing routine for each TOTEM board rather than a parallel one. This choice was made considering the following technical considerations:

- A serial approach allows all the EUTs undergo equivalent testing conditions, in order to produce results more easily comparable.
- In a serial test sequence, the accumulated stress in each EUT is higher than in a parallel test flow.
- Following the previous statement, more failures can be presumably obtained in a serial approach, and successively analysed.

2.2 HALT test sequence

The initial HALT test sequence is depicted in the following figures:

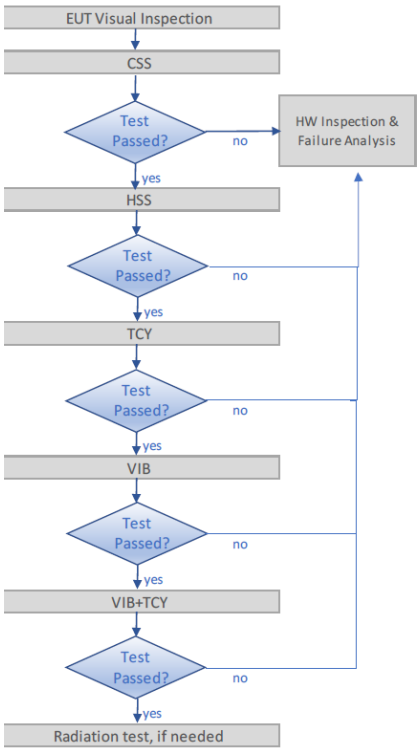


Figure 3: TOTEM HALT Test sequence

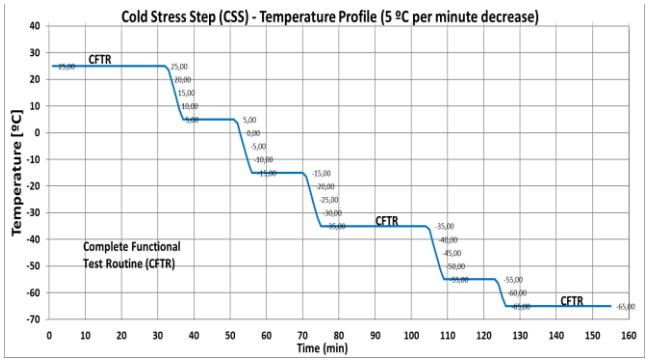


Figure 4: Cold Step Stress (CSS)

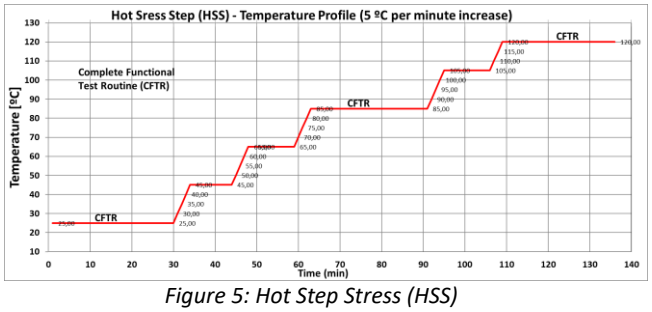


Figure 5: Hot Step Stress (HSS)

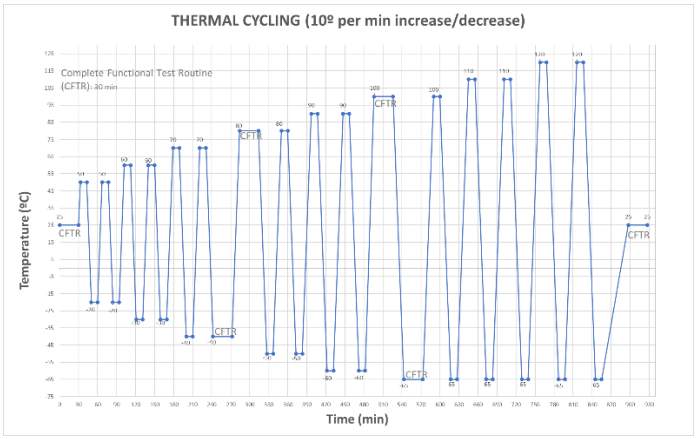


Figure 6: Rapid Thermal Cycling (TCY)

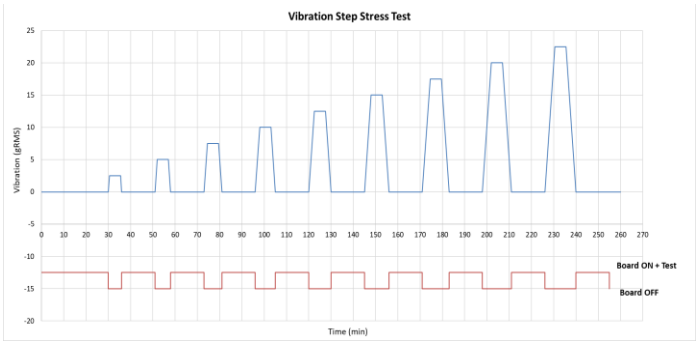


Figure 7: Vibration Step Stress (VIB)

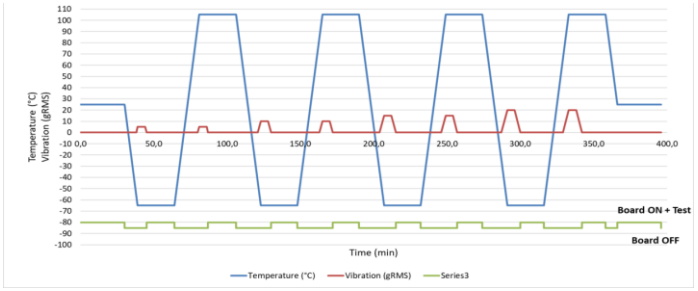


Figure 8: Vibration Step Stress + Rapid Thermal Cycling (VIB+TCY)

Component No.:		Component Designation:		Irradiation Spec. No.:	
PCB TOTEM ALÉN SPACE		PCB TOTEM ALÉN SPACE		ESCC 22900 Issue 5	
Gen. Spec.:	N/A	Functional Assignment:		Project/Programme:	
Det. Spec.:	N/A	PCB TOTEM ALÉN SPACE		A2X	
Amend.:	N/A				
Family/Group:	Technology:			Package:	
99/01	--			PCB	
Manuf. Name: Address:	N/Av	Samples Size:	3	Level of Interest:	N/Av krad(Si)
		Irradiation Devices:	3	Max. Test Level:	20 krad(Si)
		Control Devices:	0	Radiation Source:	^{60}Co

EXPERIMENTAL STEPS	1	2	3	4	5	6	7	8	9	10	11
PROCESS	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Ann
Dose [krad(Si)]	1	1	1	1	1	1	4	3	2	5	-
Cumulative Dose [krad(Si)]	1	2	3	4	5	6	10	13	15	20	-
Dose Rate [rad(Si)/h]	400	400	400	400	400	400	400	400	400	400	-
Exposure Time (Unit)	2.5 (h)	2.5 (h)	2.5 (h)	2.5 (h)	2.5 (h)	2.5 (h)	10 (h)	7.5 (h)	5 (h)	12.5 (h)	24 h
Temperature (°C)	25	25	25	25	25	25	25	25	25	25	25

Table 1: Radiations Tests

2.3 Test setup & auxiliary equipment (EGSE)

The Electrical Ground Support Equipment (EGSE, hereinafter) setup developed by ALEN Space to monitor the samples along the test routine is represented in the following scheme:

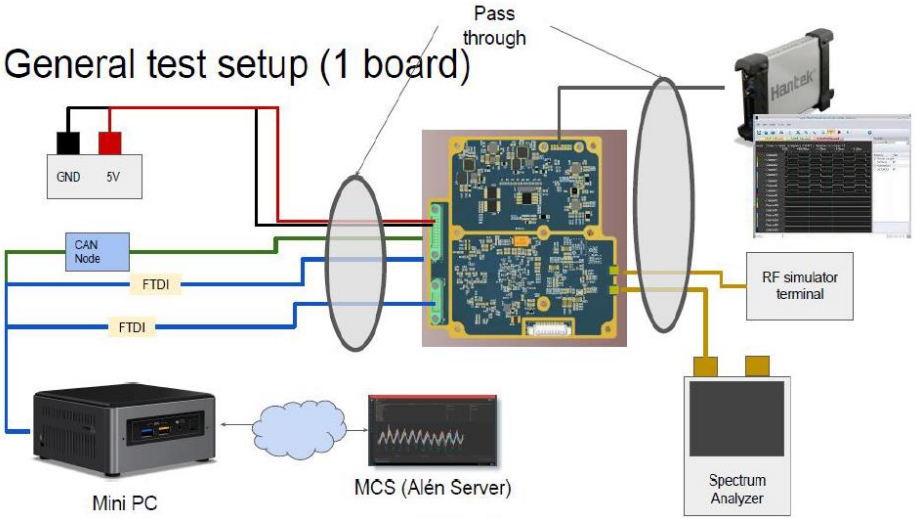


Figure 9: EGSE Setup

EGSE allows monitoring the main EUT functionalities which could be affected during the HALT tests.

2.4 Functional test routine

Two types of functional test routine, automatic and manual, are carried out during each HALT test. Once the functional test routine has been launched, all data are collected through the above-mentioned EGSE and the relevant TOTEM parameters are recorded to be later analyzed.

2.4.1 Automatic test

At the beginning and at the end of each HALT test, the complete functional test routine (CFTR) is executed to check the TOTEM board functioning. Moreover, the “rapid” functional test routine is performed during the intermediate steps of each HALT test.

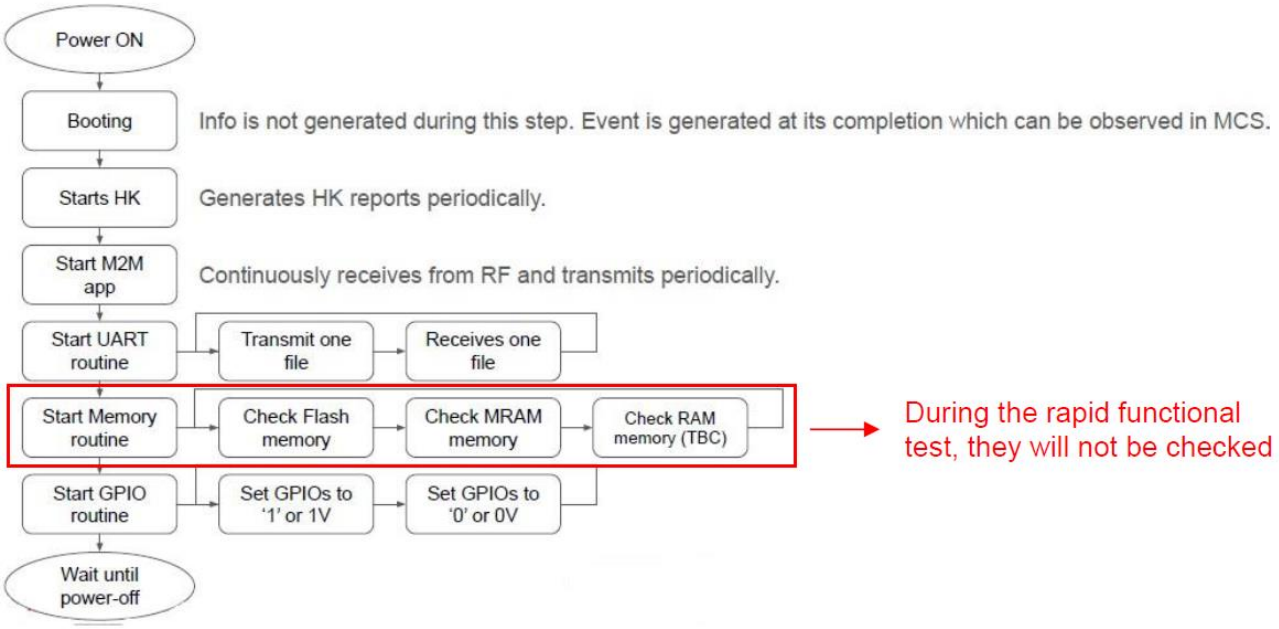


Figure 10: "Automatic" functional test

2.4.2 Manual test

Before starting every HALT test and once finished them all, a manual functional test ("Reset circuit test") is also performed to verify that TOTEM board turns on and turns off when the right supply voltage level is selected.

3 TEST PLAN ADAPTATION

3.1 Cold -Step Stress (CSS)

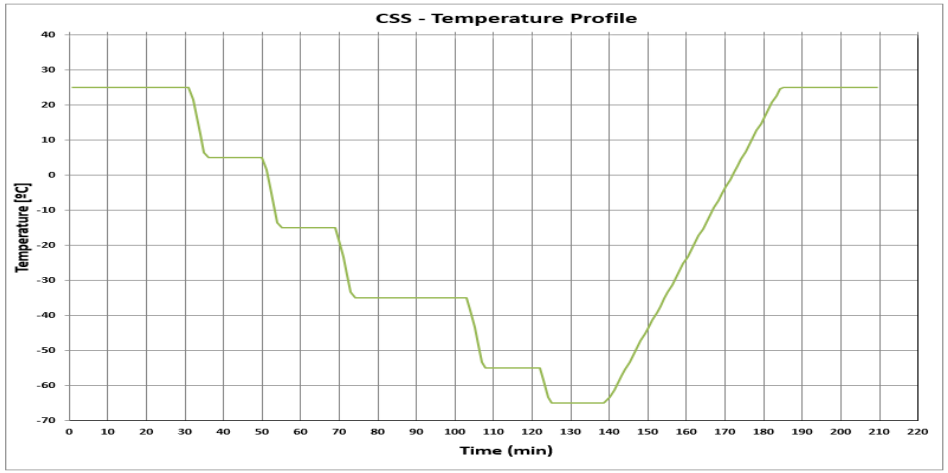


Figure 11: CSS thermal profile for all TOTEM boards

3.2 Hot -Step Stress (HSS)

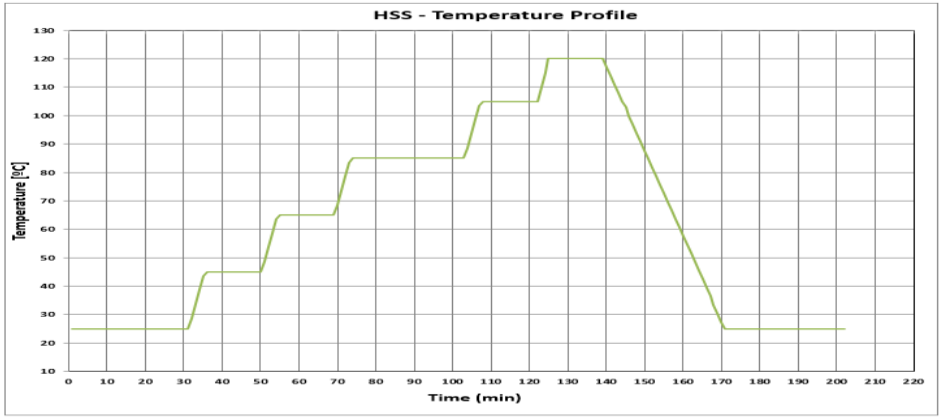


Figure 12: HSS thermal profile just for TOTEM-001 board

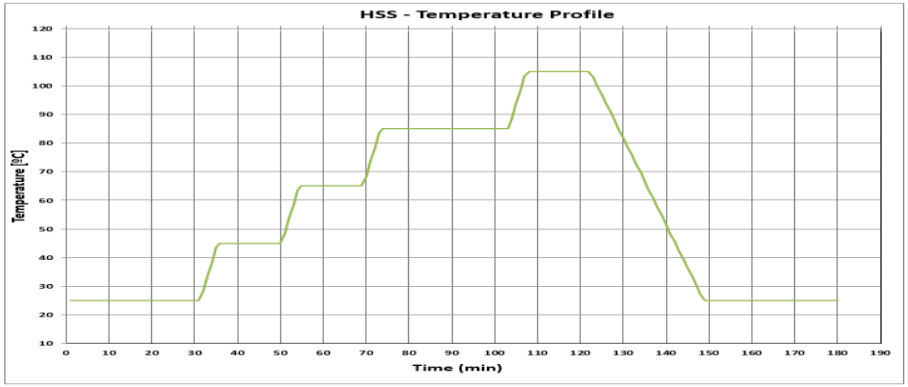


Figure 13: HSS thermal profile for all TOTEM boards, except TOTEM-001

3.3 Rapid Thermal Cycling (TCY)

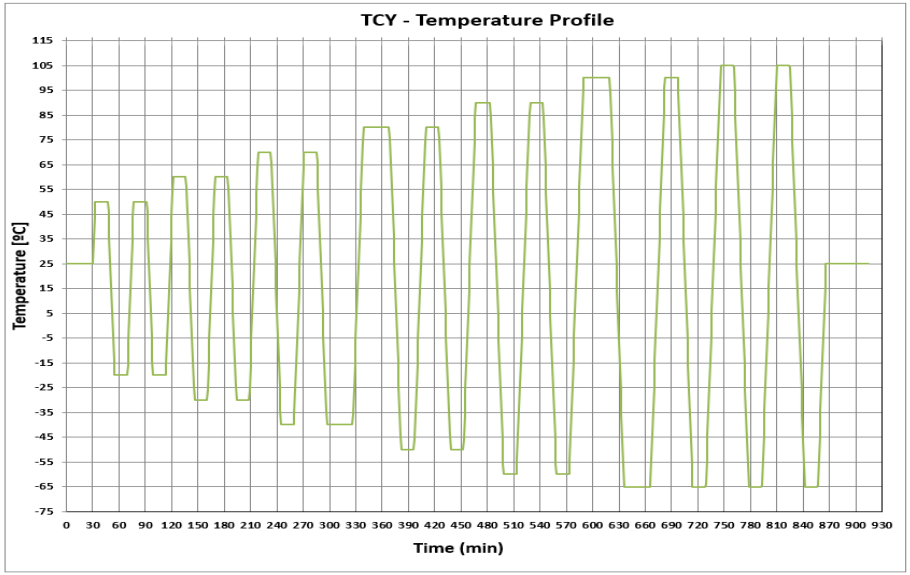


Figure 14: TCY thermal profile for TOTEM-001, 002, 003, 004, 005 and 006

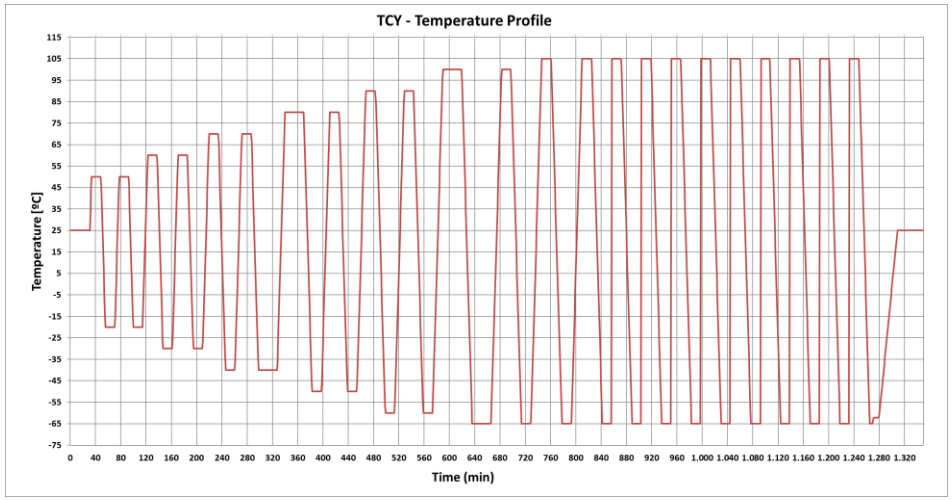


Figure 15: TCY thermal profile for TOTEM-007, 008, 009, and 010

3.4 Vibration (VIB)

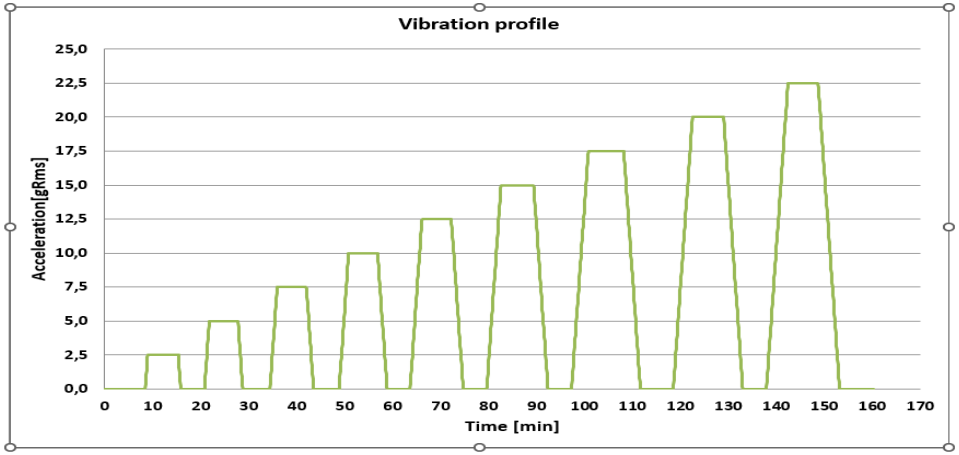


Figure 16: VIB profile for all TOTEM boards

3.5 Vibration + Rapid Thermal Cycling (VIB + TCY)

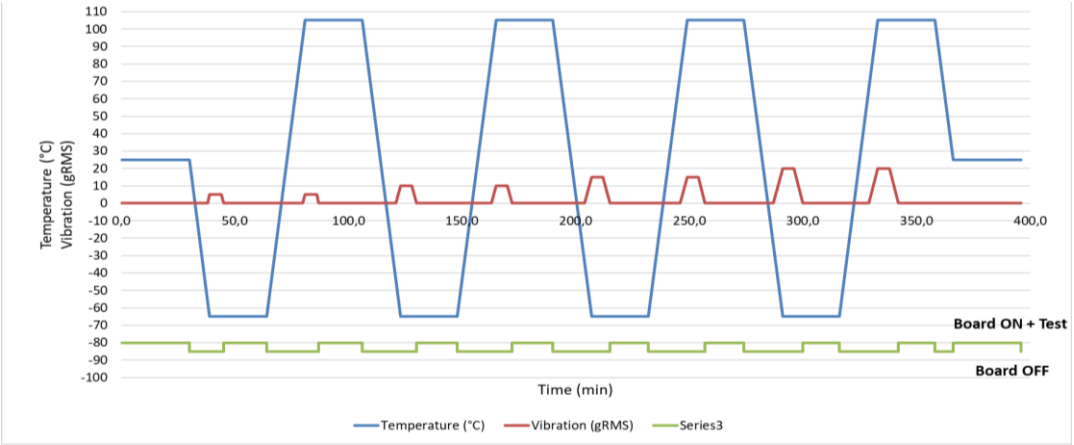


Figure 17: VIB + TCY profile for TOTEM 001, 002, 003, 004, 005 and 006 boards

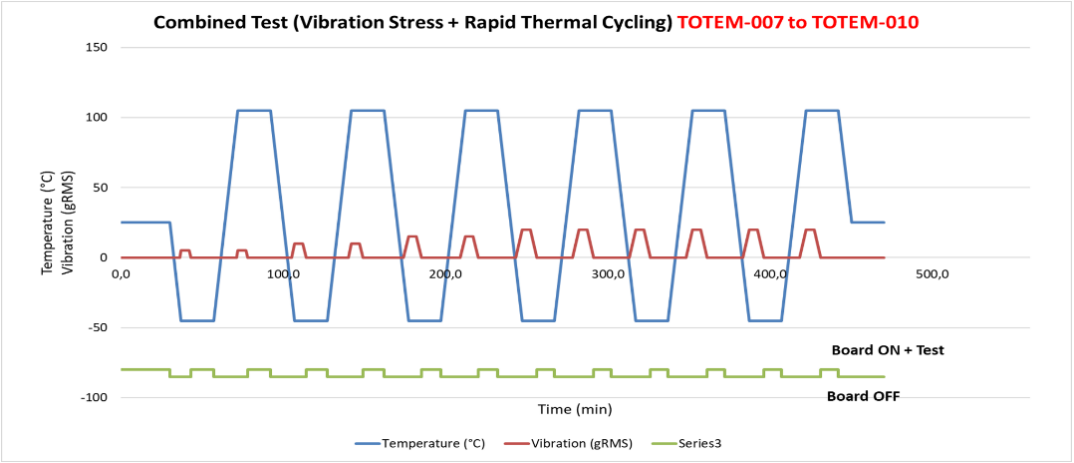


Figure 18: VIB + TCY profile for TOTEM 007, 008, 009 and 010 boards

3.6 Radiation Tests (TID)

Component No.:		Component Designation:		Irradiation Spec. No.:	
PCB TOTEM ALÉN SPACE		PCB TOTEM ALÉN SPACE		ESCC 22900 Issue 5	
Gen. Spec.:	N/A	Functional Assignment:		Project/Programme:	
Det. Spec.:	N/A	PCB TOTEM ALÉN SPACE		A2X	
Amend.:	N/A				
Family/Group:	Technology:			Package:	
99/01	--			PCB	
Manuf. Name: Address:	N/Av	Samples Size:	3	Level of Interest:	N/Av krad(Si)
		Irradiation Devices:	3	Max. Test Level:	20 krad(Si)
		Control Devices:	0	Radiation Source:	^{60}Co

EXPERIMENTAL STEPS	1	2	3	4	5	6	7	8	9	10	11
PROCESS	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Ann
Dose [krad(Si)]	1	1	1	1	1	1	4	3	2	5	-
Cumulative Dose [krad(Si)]	1	2	3	4	5	6	10	13	15	20	-
Dose Rate [rad(Si)/h]	400	400	400	400	400	400	400	400	400	400	-
Exposure Time (Unit)	2.5 (h)	2.5 (h)	2.5 (h)	2.5 (h)	2.5 (h)	2.5 (h)	10 (h)	7.5 (h)	5 (h)	12.5 (h)	24 h
Temperature (°C)	25	25	25	25	25	25	25	25	25	25	25

Table 2: RAD dose applied to TOTEM-004, 007 and 011

4 FAILURE ANALYSIS AND ROOT CAUSE INVESTIGATION PROCESS

4.1 Detected Failures modes during HALT tests

21 different failure modes related to 8 (out of 9) board functionalities have been finally recorded during the HALT test campaign, as shown in the following Table:

TOTEM Board Functionality	Detected Failure Mode at some temperature/vibration profile	Failure ID	Failure Occurrence Probability
Total & Internal Consumption	Current parameter out of range	1	Certain
	Voltage values out of range when the board is turned off and on	2	Likely
Internal Voltage Generation	Voltage Parameter (VCC_3.3 V) out of range	3	Likely
	Voltage Parameter (VCC_2.5 V) out of range	4	Likely
	Voltage Parameter (VCC_ODDR) out of range	5	Likely
	Voltage Parameter (VCC_AUX) out of range	6	Likely
	Voltage Parameter (VCC_BRAM) out of range	7	Likely
	Voltage Parameter (VCC_PAUX) out of range	8	Likely
Housekeeping collection	Motherboard (MB) temperature stopped decreasing	9	Certain
	Field Programmable Gate Arrays (FPGA) Temp. oscillates in wrong range	10	Likely
Radio Frequency (RF) Transmission	Tx (data transmission line) frequency out of range	11	Certain
	Tx (data transmission line) frequency critically out of range	12	Certain
	Tx (data transmission line) power out of range	13	Certain
	Tx (data transmission line) power critically out of range	14	Very Likely
Radio Frequency (RF) Reception	TOTEM board temporarily stopped receiving packets from RF simulator	15	Likely
	TOTEM board permanently stopped receiving packets from RF simulator	16	Likely
Memories (Flash, RAM, MRAM)	GPIOs Pins stopped working	17	Unclassifiable
General Purpose Input / Output (GPIOs) Routine	Not recurring commutation of GPIOs signal	18	Likely
	Analog reading line 0 (FE_AN_IN0) temporarily out of range	19	Certain
	Analog reading line 1 (FE_AN_IN1) out of range	20	Likely
Multiconnection System (MCS) Activity	Unavailability of telemetry data	21	Unclassifiable
Universal Asynchronous Receiver – Transmitter (UART) Bus transmission & Reception	-	-	-

Memories (Flash, RAM, MRAM)	Corruption of Flash NAND Memory	TID	Likely

Table 3: Detected Failures Modes related to TOTEM board functionalities and failure probability.

- **Certain** (Failure Probability): when the failure has occurred to each one of the 10 tested boards, during a specific test.
- **Very likely** (Failure Probability): when the failure has occurred to almost all the 10 tested boards, during a specific test.
- **Likely** (Failure Probability): when the failure has occurred at least to one tested board, during a specific test.
- **Unclassifiable** (Failure Probability): when the failure has just occurred for one board who has been the only one to reach a specific temperature/vibration profile.

4.2 Root cause analysis: findings

The following table displays the outcome obtained from the root cause investigation process performed on the failures observed during the HALT campaign:

Failure ID	Failure Mode: Recoverable/Not Recoverable	Systematic / Not Systematic	BOARDS affected	Root Cause	Failure Trigger	Solution
2	Not Recoverable (Destructive Failure)	Not Systematic	003 & 008	U28 reset chip damaged	Unknown*	U28 replacement
16	Not Recoverable (Destructive Failure)	Not Systematic	001, 002, 003 & 006	IC Transceiver damaged	Unknown*	IC transceiver replacement
17	Not Recoverable (Destructive Failure)	Not Classifiable	001	Flash Memory partially corrupted	Too extreme temperature reached: +120ºC	TOTEM-001 firmware reprogrammed
1	Recoverable	Systematic	All boards	Too high temperature	Maximum nominal operating temperature limit exceeded	To decrease temperature below 105 ºC
9	Recoverable	Systematic	All boards	Too low temperature	Minimum nominal operating temperature limit exceeded	To increase temperature above -55 ºC
3	Recoverable	Not Systematic	010	Malfunctioning of the Internal data acquisition system	Unclear (inconclusive analysis)	Unclear
4	Recoverable					
5	Recoverable					
6	Recoverable					
7	Recoverable					
8	Recoverable					
10	Recoverable					
11	Recoverable	Systematic	All boards	Frequency instability & deviation in TCXO (reference freq. of IC Transceiver)	Nominal operating temperature range exceeded	To keep boards temp. between [-55ºC & +100ºC]
12	Recoverable	Systematic	All boards	Frequency instability & deviation in TCXO (reference freq. of IC Transceiver)	Nominal operating temperature range exceeded	To keep boards temp. between [-60ºC & +105ºC]
13	Recoverable	Systematic (at specific condition)	All boards	Unclear. Not all boards affected by the same tests, temperatures, or vibration levels (except for the VIB+TCY test at +105ºC& 20gRMS)	Unclear. Connections between RF cables and RF connectors could have been affected during vibration tests, producing RF power reduction.	Unclear. Further internal analysis of the IC transceiver required
14	Recoverable	Not Systematic	All boards, except 001 & 005	Unclear. Not all boards affected by the same tests, temperatures, or vibration levels.	Unclear. Connections between RF cables and RF connectors could have been affected during vibration tests, producing RF power reduction.	
15	Recoverable	Not Systematic	001, 006, 008, 009 & 010	Unclear. Not all boards affected by the same temperatures or vibration levels.	Unclear. Connections between RF cables and RF connectors could have been affected during VIB + TCY tests, producing RF power reduction	Unclear
18	Recoverable	Not Systematic	003, 006, 008, 009 & 010	Unclear. Not all boards affected by the same temperatures or vibration levels.	Unclear. Connection between TOTEM boards and the oscilloscope could have been affected during VIB+TCY tests.	Unclear
19	Recoverable	Systematic (at specific condition)	All boards	Unclear. Not all boards affected by the same tests, temperatures, or vibration levels (except for the VIB+TCY test at +105ºC& 20gRMS)	Unclear. Root cause investigation process, based on reproducing the issue, and verifying some parameters dependences, was inconclusive.	Unclear
20	Recoverable	Not Systematic	008	Unclear. Failure could have been caused by a test setup issue	Unclear. Root cause investigation process cannot relate the detected out-of-range parameters with other housekeeping measurements.	Unclear
21	Recoverable	Not Classifiable	001	(Probably) Flash memory issue	Too extreme temperature reached: +120ºC	To decrease temperature below 105 ºC

Further investigations at the internal level of the fault component are required to find its specific weak point

TID	Not Recoverable (Destructive Failure)	Not Classifiable	004, 007 & 011	Reset circuit failure (which has affected the 3 tested boards) and Flash NAND memory corruption in boards 004 and 007	Unclear. The exact radiation dose that could have caused the failure is unknown since the boards were just turned off at the end of TID test.	To turn off and on each board in every radiation step may led to know the critical dose responsible of the issue.

Table 4: Failures Modes classification, root cause analysis results and mitigating solutions

4.3 Board Design improvements.

The detected possible improvements in TOTEM board design can be summarised, as follows:

- The development of a more complex (redundant) reset system,
- A dissipator/heater mechanism to be included in the IC transceiver,
- A scrubbing system that could eventually correct flash memory errors,
- The housekeeping circuitry made up of independent sensors and
- Better RF cables and connectors

4.4 Telemetry Data Analysis: Potential degradation parameters.

Although seven specific telemetry current parameters related to different board current consumptions have been analyzed to detect possible degradations on the boards, no conclusive results have been found able to quantify the ageing of the boards caused by HALT tests.

4.5 Key aspects to consider after completing the HALT test campaign.

- Test limits initially defined in the HALT test plan need to be adapted along the campaign to finally identify the EUT operating limits.
- FMECA analysis has shown its effectiveness to identify board critical functionalities to be monitored during the HALT test campaign.
- A total of 4 out of 21 different failure modes have been identified as destructive ones.
- IC transceiver, circuit reset, flash memory and housekeeping circuitry have been identified as potential points of failure in the board design.
- The support of the board manufacturer is critical to eventually identify board potential ageing parameters and every board failure causes, even though the root cause investigation process could be not conclusive at all.

5 HALT FEASIBILITY ASSESSMENT

5.1 Potential improvements in repeating HALT approach

Performing the whole test routine (CSS, HSS, TCY & VIB + VIB+TCY) on few samples to then adapt the testing limits better for the rest of the samples. To develop a methodology that allows an early identification of parameters that would sign the EUT's ageing along the HALT campaign. Rebooting the samples after every radiation dose applied to nail down the radiation dose affecting the functioning of the samples. To develop the project considering a "forked" approach: comparison of results obtained from an electronic board using qualified components through a "traditional" approach until completing its qualification process vs results obtained from an equivalent electronic board with COTS components using the HALT approach from its early development stages until completing its qualification process.

5.2 Rapid future assessment of complete assembled boards: recommendations

At early stages of the space development project it shall be decided whether HALT shall be part of it or not; if so, it shall be already implemented from the Pre-design Review stage of the product development. Moreover, a concise FMECA of the electronic board to be tested should be made before starting the HALT campaign. It's also important to optimize synergies between manufacturer & HALT testing lab to use HALT in the most efficient manner (i.e. To optimize hardware & software testing for clear and conclusive results obtention, to automate testing, and maximize the number of samples to be tested simultaneously).

6 HALT COST ANALYSIS

6.1 Classical approach vs HALT approach: Cost comparison

To obtain a tangible outcome regarding HALT economic feasibility for the space industry, a cost-analysis based on the following key points have been developed based on the experience acquired by the Consortium throughout the entire project:

- Manufacturing of an electronic board using the traditional space industry approach, and assessment of the Space equipment unit price using the classical qualification approach.
- Manufacturing of the same electronic board applying the HALT methodology to the product development and qualification stages, and cost assessment.
- Comparison of HALT and traditional approaches, made some reasonable assumptions.

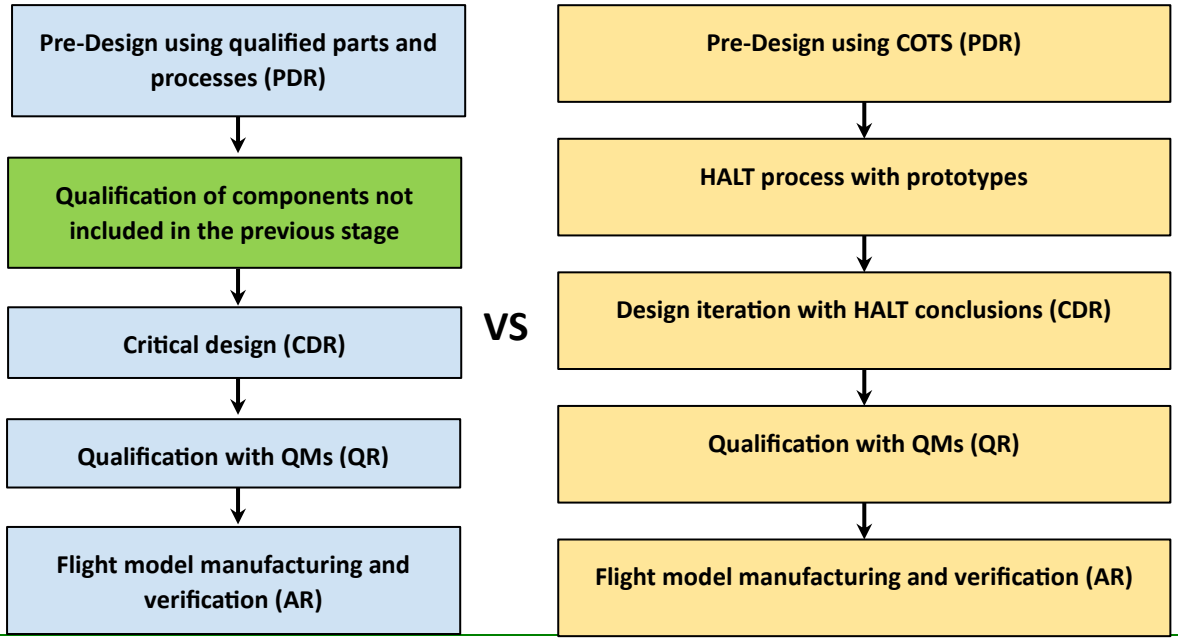


Figure 16: Space equipment traditional development scheme (Left) vs Space equipment HALT approach development scheme (Right)

The cost comparison results are below displayed:

TRADITIONAL DEVELOPMENT APPROACH BASED ON QUALIFIED COMPONENTS	
Stage	**Cost**
Pre-design (Engineering hours & prototypes manufacturing)	359.250,00€
Qualification of board non-qualified components (x5 components)	100.000,00€
QM manufacturing (x2 units)	44.500,00€
Equipment qualification	136.875,00€
FM manufacturing (per unit)	22.250,00€
TOTAL	**662.875,00€**

VS

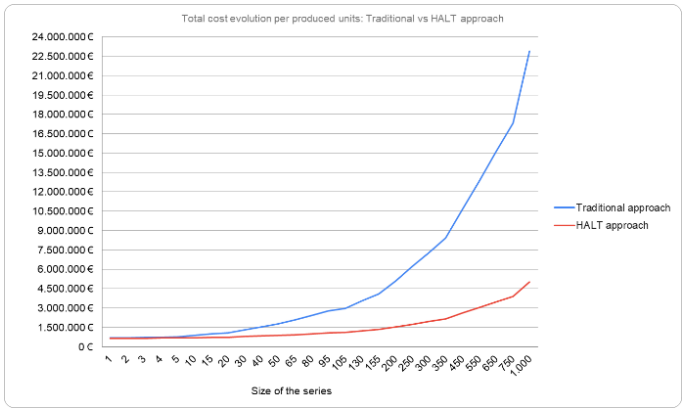
HALT DEVELOPMENT APPROACH BASED ON COTS COMPONENTS	
Stage	**Cost**
Pre-design (Engineering hours & prototypes manufacturing)	193.050,00€
HALT test samples manufacturing (x20 samples)	87.000,00€
HALT test campaign (x20 samples)	221.000,00€
QM manufacturing (x2 units)	8.700,00€
Equipment qualification	136.875,00€
FM manufacturing (per unit)	**4.350,00€**
TOTAL	**650.975,00€**

Figure 17: Cost Analysis comparison: traditional development approach VS HALT development approach

6.2 Conclusions

Assumptions made to perform the cost comparison in the previous section are highly subject to a non-controllable number of variables. Due to that, the main conclusion obtained from this analysis shall not be mistaken for which of the 2 different development approaches compared here delivers the cheaper unit produced.

Space missions where only one or a few FMs need to be manufactured would not benefit that much from the HALT development approach. However, the cost margin differences between the two approaches increases with the number of units manufactured, since the cost of each new FM unit using the HALT development approach, once the product has overcome the CDR phase, is lower than that in the traditional development approach, as it can be attested in the graphics below:



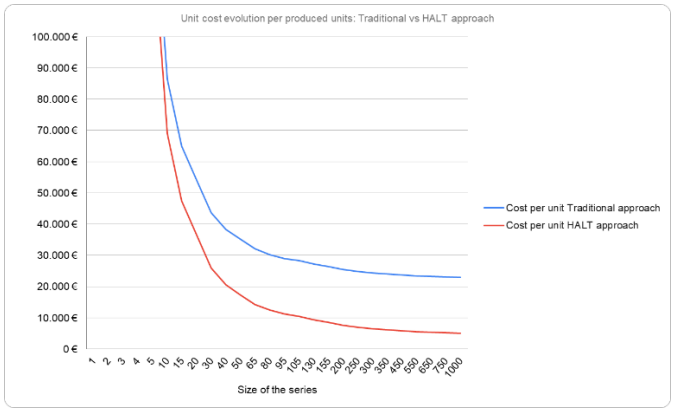


Figure 18: Total cost evolution per units manufactured by development approach (left) & Unit cost evolution per units manufactured by development approach (right).

Therefore, HALT development approach becomes more cost-effective as number of units produced increases. Its cost-effectiveness would make it advantageous for scenarios involving the use of standard products across multiple missions. Using COTS (when possible) combined with early development stages supported by HALT could lead to reduced SWaP or shorter lead times, making the product more competitive and easier to manufacture.

Finally, the conclusion above-mentioned shall be restricted to space electronics equipment, being not valid for complete systems.