SpaceNVM

Assessment of Advanced Non-Volatile Memories

ESA Contract No. **4000132931/20/NL/FE**

Title	**SpaceNVM - Executive Summary**
Reference	EMM-SNVM-REP-0010
Date	08.06.2024
Issue	i2

Abstract

The ESA project “Assessment of Advanced Non-Volatile Memories” is about the identification and evaluation of emerging non-volatile memory technology for future missions. A detailed market analysis and literature review have been conducted and Ferroelectric Hafnium-Oxid FET (FeFET) has been selected as very promising technology. Thereof, a prototype memory IC has been designed and manufactured that underwent functional, thermal and radiation testing. In summary, the goals of the de-risk activity have been achieved and the feasibility of utilizing FeFET technology in space environment has been demonstrated. NVM technology has demonstrated general suitability in this first study, but some development work would still be needed like implementation of a radiation hard addressing logic and a technology-oriented read-out scheme.

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1 Summary

The project “SpaceNVM - Assessment of Advanced Non-Volatile Memories” was about the identification and evaluation of non-volatile memory technology for future development towards utilization in space applications.

A detailed market analysis and literature review have been conducted and FeFET technology based on Hafnium-Oxid has been selected as target technology. Thereof, a test chip has been designed and manufactured that underwent functional, thermal and radiation testing.

In summary, the goals of the de-risk activity have been achieved and the feasibility of utilizing FeFET technology in space environment has been demonstrated. This NVM technology will be well suited for future applications as companion memory to processors or comparable.

2 Technology Selection

2.1 Emerging Memory Technologies

Conventional semiconductor memory technologies such as SRAM, DRAM and FLASH face scaling challenges below 22nm nodes. Several strategies aiming to overcome them have been adopted. For example, 3D-integration ensures continuous cost per bit scaling of NAND FLASH. New high-k dielectric and electrode materials and manufacturing processes guaranteeing a thickness uniformity of a few Angstroms push DRAM scaling. SRAM scales continuously with CMOS at an approximate time-lag of two generations behind the smallest feature size. Besides that, the non-charge storage-based memories such as PCM, MRAM, ReRAM and perovskite-based FeRAM although in small volume commercial production, suffer from high costs. Ferroelectricity in doped hafnia opens the opportunity to overcome these integration and scaling issues due to relative low permittivity, high coercive field EC and CMOS compatibility. Three flavours of ferroelectric (FE) devices are under consideration for memory application – the 1T1C FeRAM, 1T FeFET and the nT1R FTJ concept that are illustrated in Fig. 1.

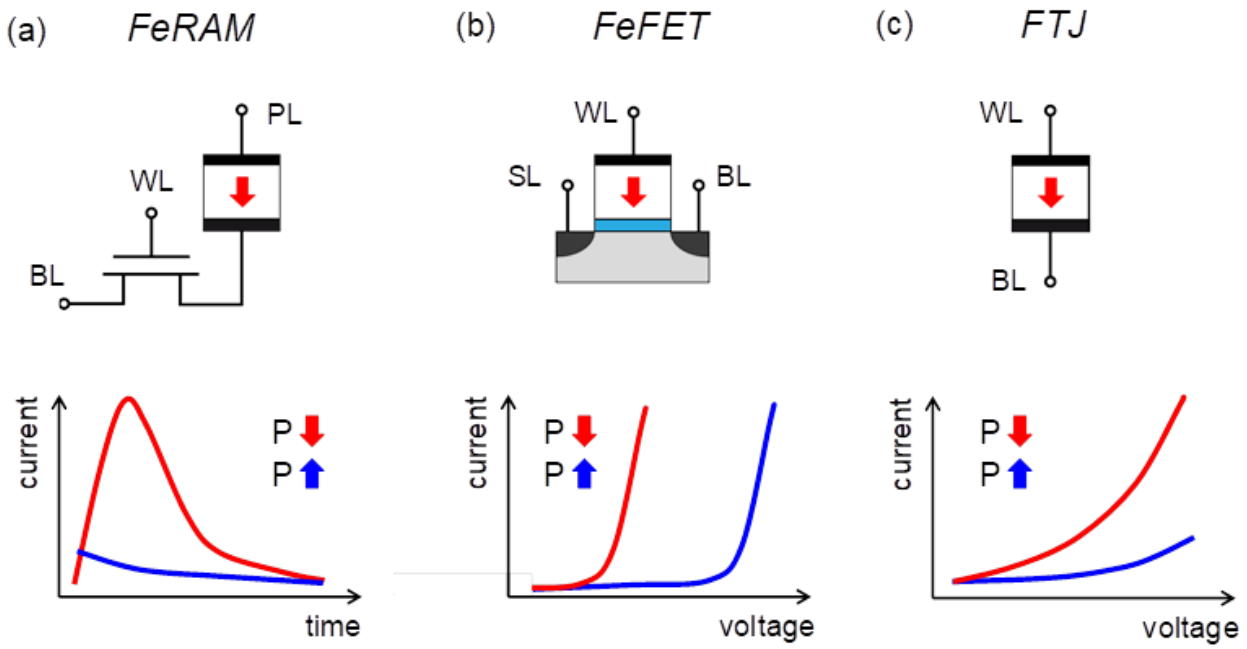

Fig. 1: Three ferroelectric memory concepts and their respective current-response as a function of time or voltage for both polarization directions: (a) FeRAM; (b) FeFET and (c) FTJ.

The FeRAM technology, when based on ferroelectric hafnium oxide, has the benefit of comparatively easy integration into CMOS manufacturing processes. From the current perspective, two realizations of hafnium oxide based ferroelectric memories are likely to enter the market in foreseeable future. For stand-alone devices a memory type storage class device based on the 1T1C concept [1], featuring close to DRAM-like performance in terms of speed and density but at reduced endurance is the most likely case. Due to low-cost implementation the 1T FeFET concept integrated into high-k metal gate technology is a very attractive candidate in terms of low-

power and cost-per-bit [2]. Additionally, reasonable cycling endurance and fast access times makes the concept very likely to find first niche applications that pave the way into eNVM market.

Ferroelectric memory is based on the physical effect of ferroelectricity, and the memory is supposedly ultimately tolerant against radiation exposure. For ferroelectric capacitors [5] [6] no noticeable change of the ferroelectric properties was observed after an irradiation with 1 Mrad (Si) γ-ray radiation and only a negligible increase in leakage current and only a decrease of the remanent polarization and the relative dielectric constant by 5 % was observed for total ionizing doses up to 10 Mrad (Si) Co-60 γ-rays. HZO-based FeFETs show a retention of 10 years after they were objected to total ionizing doses of up to 10 Mrad (Si) ^{60}Co γ-rays [7] . However, a negative impact of the radiation on the endurance of the memory cells was observed. Investigations of HYO-based FeFETs [8] showed only minor changes of the basic parameters after an irradiation with up to 10 Mrad.

Therefore, in the project SpaceNVM our focus will be on the **ferroelectric hafnium oxide-based memories** (FRAM) – namely the **FeRAM and FeFET** based memories (see Fig. 1).

3 Test Chip Design

A 64k FeFET array was designed, where each memory cell is represented by an N-FeFET transistor with dimensions of W=L=450 nm. The full 64k array is split into 2 halves, each consisting of 2 blocks and each block is constructed of 128x128 cells in and AND configuration, where parallel oriented source lines (SL) and bit lines (BL) are connected to the source/drain regions of the FeFETs, while perpendicular running word lines (WL) are connected to the gates, respectively. While single cells can be addressed for programming, an isolated p-well allows to perform a block-erase operation. The test chip was manufactured and packaged via Europractice by utilizing the 28nm SLP technology and FeFET module from GlobalFoundries Dresden. Its contact field has a single pad row of 25 pads that allows direct wafer probing and additional pad-extensions that allow packaging of the same chips into DIL24 packages (Fig. 2). The test field includes pads for a digital JTAG interface for controlling the address logic of the chip. Individual cells are routed then vial WLs, BLs and SLs to analogue pads and the array is then operated from outside utilizing pulse-measurement units (PMUs) from a Keithley 2400 parameter analyzer system.

Similar to the literature [3] [4] , also in this vehicle a certain device-to-device variability can be observed when performing switching kinetics measurements for the 64kBit FeFETs that have been manufactured in this project. In Fig. 3., program and erase behavior is depicted exemplarily for two neighboring devices. In the program case “prg” the devices are first erased to high-VT by applying a voltage of 3 V to source/drain/bulk and 0 V to the gate electrode for 10 µs and the ID-VG transfer curve is measured (blue). Then, multiple programming pulses with increasing duration and amplitude are applied to measure the switching kinetics (red). A similar approach is performed in the erase case “ers”, starting with a reference program operation with 3 V 10 µs program pulse applied to the gate, and then applying successive erase pulses to source/drain/bulk.

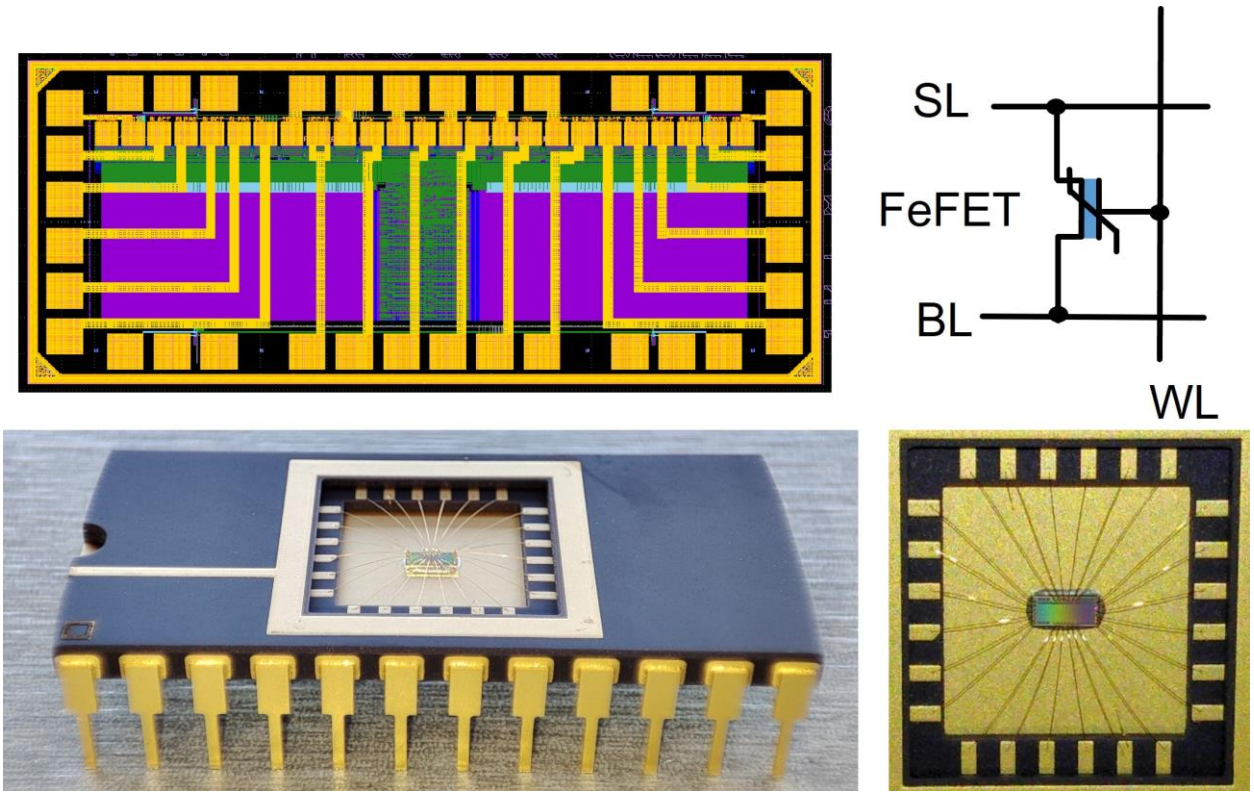

Fig. 2: (top-left) 64k FeFET chip layout. (top-right) FeFET AND array schematic. (bottom) Packaged test chip: wire-bonded and mounted into DIL24 ceramic package.

Already from the ID-VG characteristics (Fig 3) a very different behaviour can be detected. That is, for a clear opening of the memory window that is mandatory for digital readout for all devices within a larger array a program-verify algorithm would have to be implemented. However, the multiplexer-based array which was designed for statistical single device characterization is not capable for the implementation of such an algorithm for the whole array. While the measurement setup is able to apply reasonably fast programming and erase pulses down to 100 ns, read operations of single current points take approximately 0.3µs. The measurement of a full ID-VG curve for Vth extraction requires approximately 30µs. That is, the whole array can be programmed / erased or read out within half a second. However, for a full 64kBit array even when performing characterization by single-point current measurement the data transmission between measurement equipment and data acquisition unit can take up to two minutes.

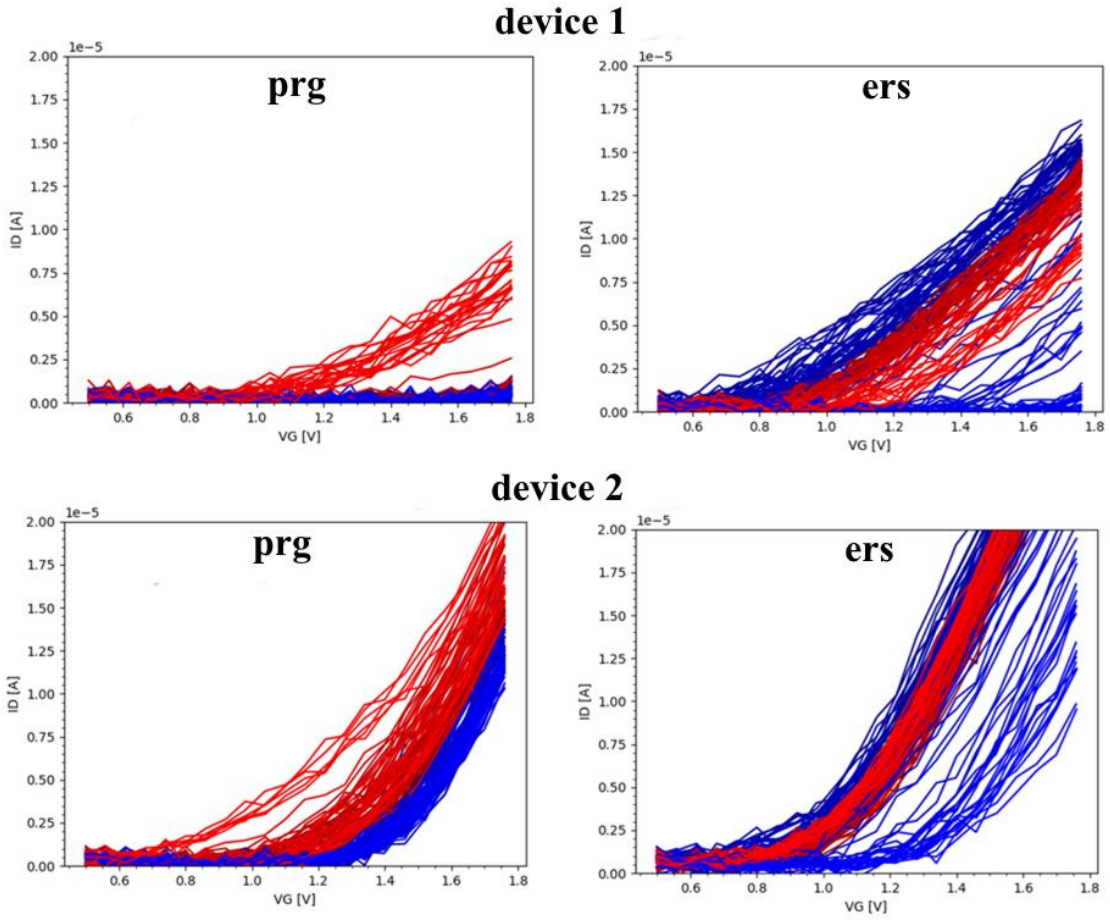

Fig. 3. Measured ID-VG characteristics of two neighboring devices within the 64kBit memory array during program (prg) and erase (ers) kinetics measurements (programmed state in red, erased state in blue)

Therefore, to attain reasonable array access times, for our investigation of the radiation effects on the memory states a fixed 'one-shot' programming with fixed voltage and time (3V, 10 µs) was chosen. This results in different Vth states that cannot be directly separated in digital low- and high-current states, but instead represents a certain distribution of intermediate memory states. More specifically, in order to investigate all the different analogue memory states in parallel in our performance test, first a block-erase was performed and subsequently an additional checkerboard pattern was programmed before starting the campaign. Then during our tests an analogue readout operation is performed for each individual memory cell and the cell-wise change in read current is monitored. Thus, our approach is to investigate the individual change in the measured analogue cell current rather than extracting digital data. A respective measured analogue bitmap of one test chip is depicted in Fig. 4 (top). As expected, the programmed checkerboard pattern is overlaid by a strong device-to-device variability and the respective cumulative probability plot for the programmed and erased cells is depicted in Fig. 4 (bottom). In this plot the quantile of a standard deviation is plotted on the y-axis with the average value at quantile 0, while the x-axis depicts the respective read current of the devices. The result indicates an average current of about 6µA and 8 µA for erased and programmed state, respectively.

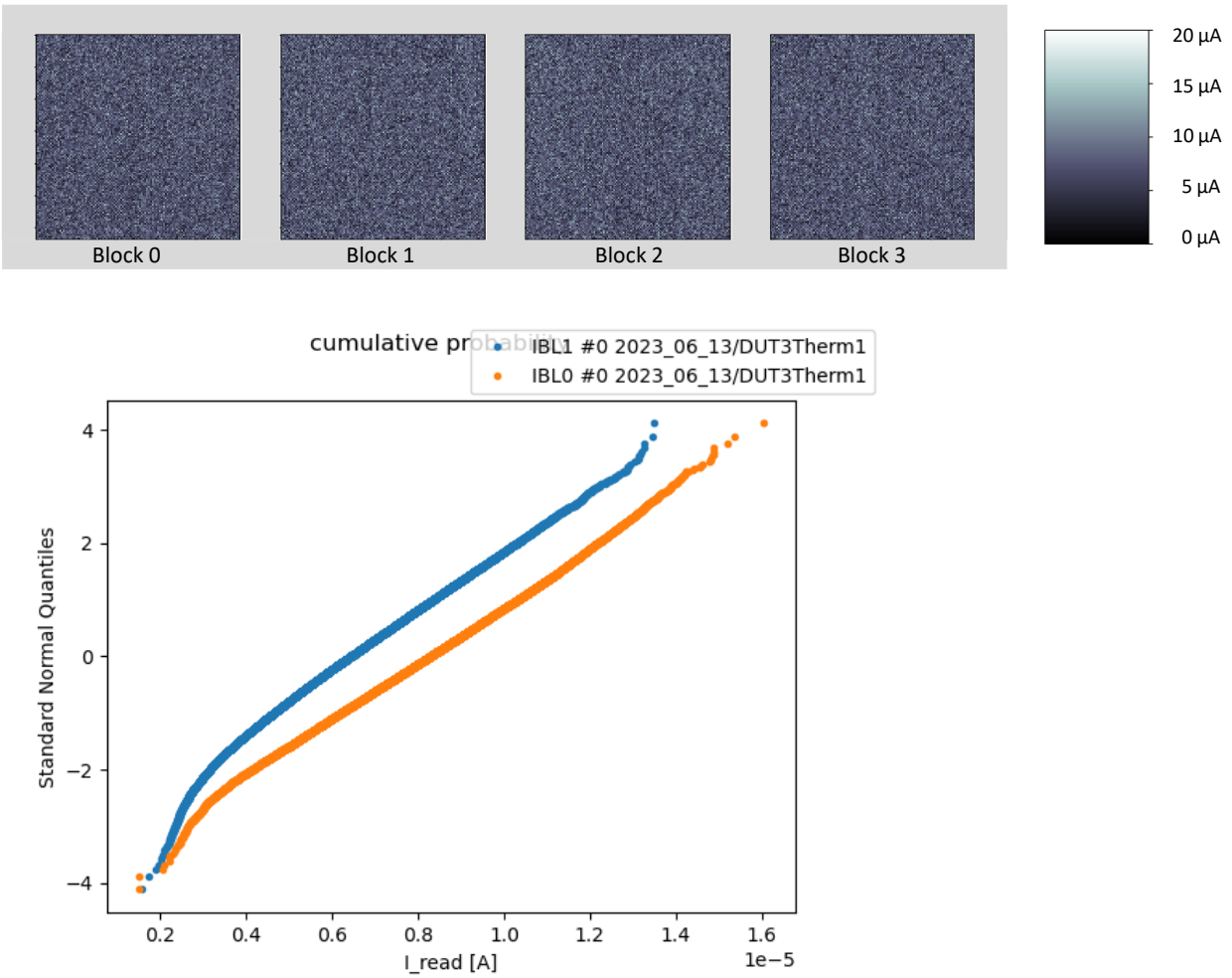

Fig. 4. (top) Measured on-current map of DUT3 (64kBit array with 4 blocks á 16kBit) after programming a checkerboard pattern with fixed program / erase conditions (+/- 3V, 10µs). Each block corresponds to one out of four 128x128 bit sub-arrays. (bottom) Cumulative probability plot of measured on-currents after one-shot checkerboard programming in logic state "0" (orange) and logic state "1" (blue). A strong overlap of the two states can be seen.

4 Functional and Environmental Testing

4.1 Test setup and Test Facilities

The architecture of the test setup is illustrated in Fig. 5.

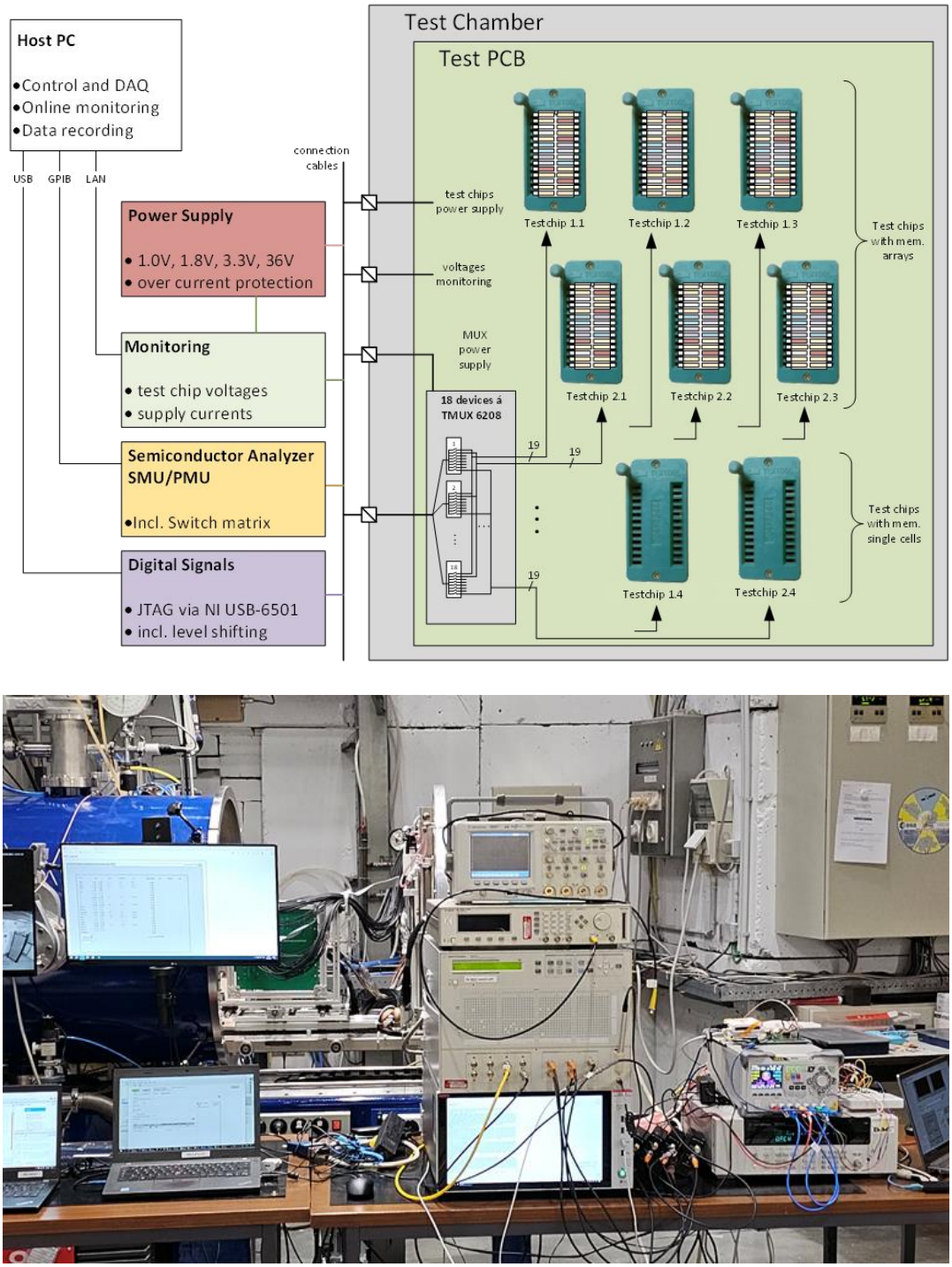

Fig. 5. (top) Architecture of test setup, (bottom) test setup at UCL

The test chips, glued and bonded into a 24-pin DIL package, are mounted at the test PCB. A test setup base on latch-up protected power supplies, Source-measure and power-measure units (SMU and PMU) data acquisition of housekeeping data (voltages and current) as well as a JTAG programmer is connected to a host PC. From there, the test chips are operated and read-out. A multiplexing multimeter type Agilent 34980A (with 34925A FET Multiplexer and 34937A Switch Matrix) is used for data acquisition of voltages and current and for distribution of supply lines to all test chips.

The HIF facility of the CYCLONE cyclotron of the Université catholique de Louvain (UCL) in Louvain-la-Neuve can provide selected heavy ion beams from Carbon to Xenon in a particle cocktail. The majority of the tests here were performed with Xenon ions, having the largest LET available with 62.5 MeV cm^2/mg. For one additional run, the ion was switched to Krypton with LET 32.4 MeV cm^2/mg.
Total ionizing tests have been performed at the TK1000B Co-60 facility at Fraunhofer INT after the SEE tests and on some devices with potentially pre-existing damage from the SEE tests.The distance between source and devices was chosen such that the dose rate was quite high to allow exposure to 100 krad(Si) and thermal tests within the same day.

Pre- and post-irradiation the devices were subjected to thermal testing with a temperature ramp from room temperature up to 125°C, down to - 40°C and back to 25°C. Several array measurements have been performed during this thermal treatment.

4.2 Single Event Effect Testing with unbiased devices

Within the chamber and already prior to irradiation, additional noise patterns appeared which resulted in positive or negative current spikes in some random cells.
During the first runs with Xenon, the FeFET arrays were left unbiased to check whether the stored data within the NVM cells is corrupted by radiation with heavy ions. As radiation effects can only occur for devices in the beam, and as the beam has a limited width, devices on neighboring test sockets were outside of the beam area and thus unaffected by radiation. Therefore, during these runs always one device could be radiated while a second device on the board was selected for electrical read out at the same time, approx. 2min per test run for pre- or post-irradiation characterization.

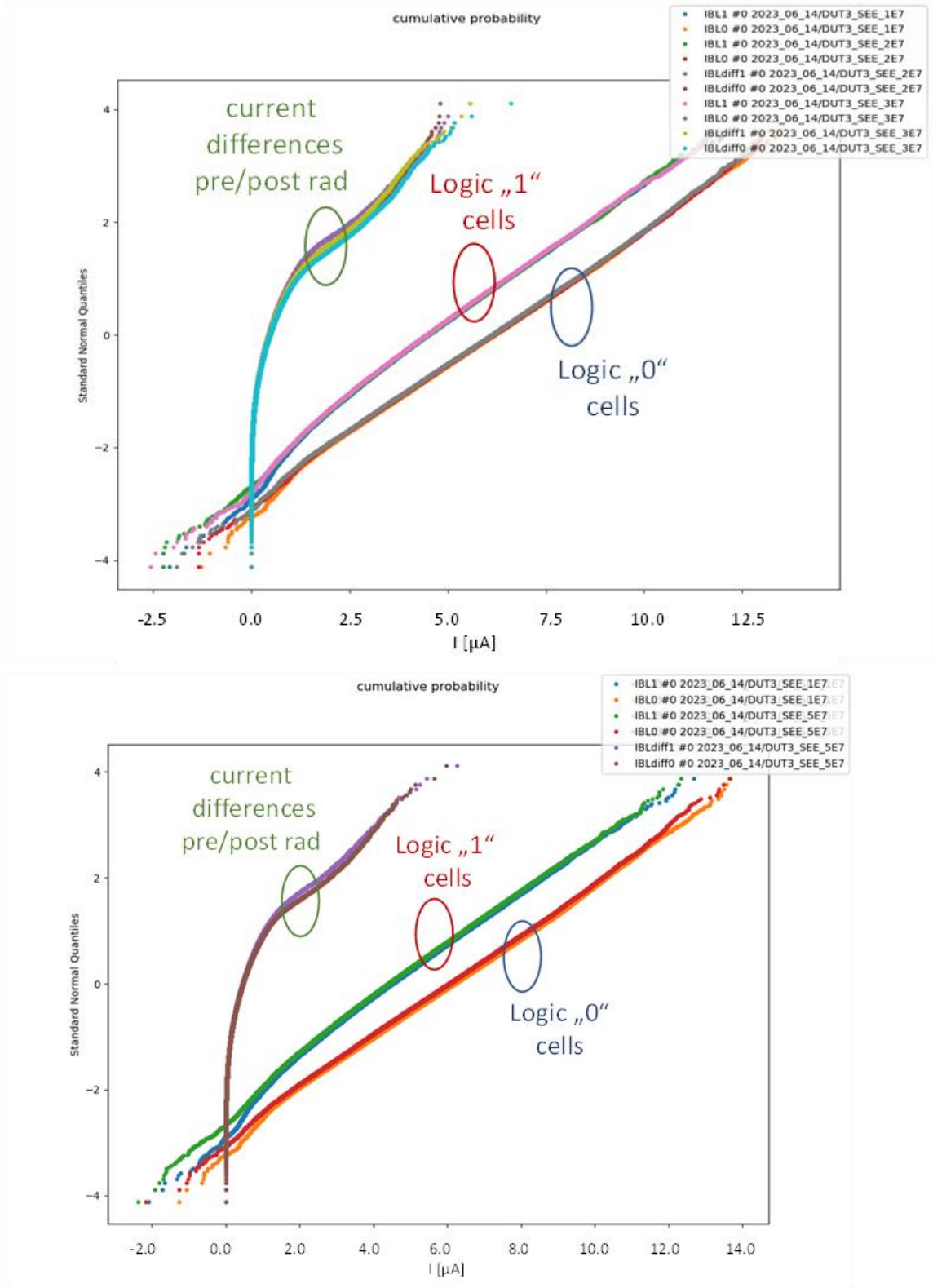

Fig. 6. Cumulative probability plot of measured cell currents and difference currents on 64kBit FeFET arrays DUT3: (top) after Xenon irradiation to fluence 1E7 ions/cm2 and 2E7 ions/cm2 and 3E7 ions/cm2, (bottom) irradiation to fluence 5E7 ions/cm2

Over the course of these tests, 3 DUTs (device under test) were irradiated to 1E7 (DUT5), 2E7 (DUT4), and 3E7 ions/cm^2 (DUT3) respectively in increments of 1E7 ions/cm^2.
Inside the HIF test chamber, a much stronger noise signal on the chips is observed than outside such that the cell-wise currents can differ randomly up to 5 µA, i.e. from step to step other cells are affected.
From the device dimensions W=L=450nm, there is an area of 2E-9 cm² per transistor and at an ion fluence of 1E7 ions/cm² the expectation value of per-cell fluence are 2E-2 ions/transistor. For the entire array, this means that 2% of the cells are expected to be hit by an ion. Therefore, it can be assumed that about 0.04% of the cells might get hit two times in two subsequent radiation runs to 1E7 ions/cm^2. Instead, from the cumulative probability plot that extends again towards negative current values which cannot originate from a memory cell itself the behavior indicates that there is again a certain impact of noise within the measurement setup with unclear origin.

4.3 Single Event Effect Testing with biased devices

During the following runs, the devices were operated during the SEE test to see the radiation effects on the memory array operation, addressing etc. Note, that the pure CMOS part of this technology is not radiation hardened. Also, the same set of devices, previously used for unbiased irradiation, were used with DUT3 irradiated to additional 2E7 ions/cm^2, so effects due to pre-existing damage, while not apparent, cannot be excluded.
First, the addressing of DUT3 was investigated by simply manually selecting addresses via the JTAG interface and reading out the respective addresses. During this test no addressing issues have been observed. In addition, the supply currents were monitored for Single Event Latch-up, none were observed.

Therefore, in the subsequent test run the device was read out automatically during irradiation with a constant Xe flux of 1.5E4 ions/(s cm²) targeting at a fluence in this run of 1E7 ions/cm^2. During this test about 1/8 of the memory array could be read out without failure, however, afterwards addressing errors occurred (Fig. 7, top). This is still observed, though less pronounced, when repeating this test with krypton ions (Fig. 7, bottom).

Since the array readout operation is performed row by row for all four blocks together in top-down direction (increasing row numbers) the addressing issues appear as horizontal blocks. A white block might indicate large currents, e.g. if one programmed cell is read again and again. A vertical stripe-pattern indicates that the row-counter did not increase properly. Due to uncertain time frame of the SEE to the readout, there is no relation between the occurrence of the first addressing error and the particle fluence up to this point, so no event rate or cross section can be estimated. However, these would characterize the non-rad-hard logic circuit and not the memory cells.
In summary it can be stated that from the SEE test results no clear indications of data manipulation within the ferroelectric memory cells due to the impact of heavy ions was observed. However, within the addressing logic which is not radiation hardened several errors during active radiation occurred. Hence, in further investigations a rad-hard CMOS library should be adopted to design the FeFET-array peripheral circuits, which was not the focus of this work.

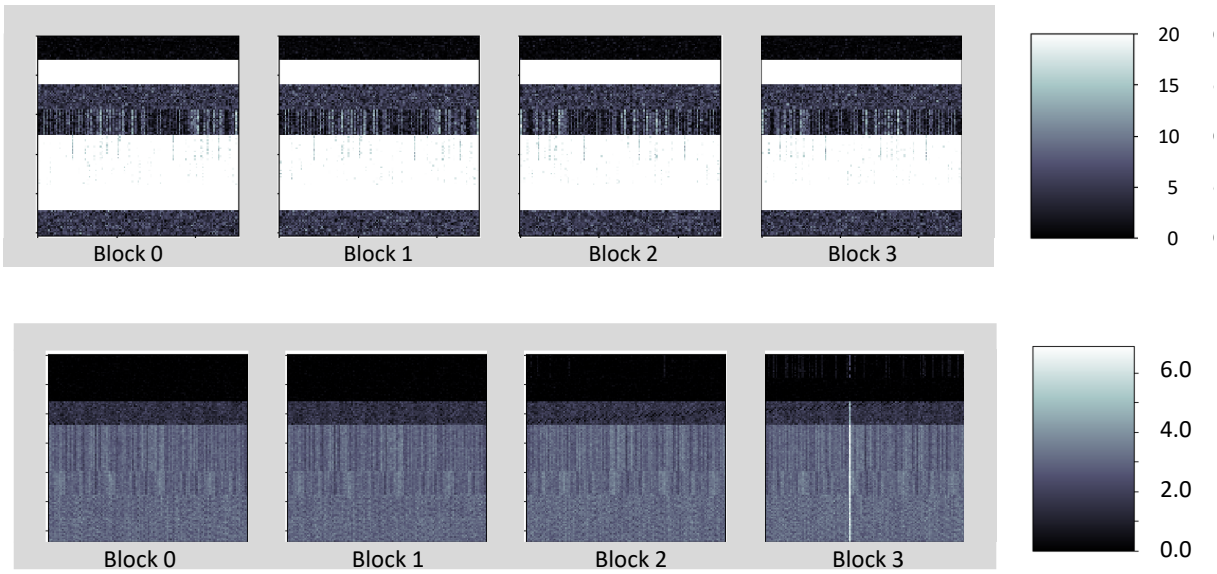

Fig. 7. DUT3 SEE test results (64kBit array with 4 blocks á 16kBit): (top) measured BL current difference between 3e7 and 4e7 Xenon ions and bottom: measured BL current difference between 3e7 and 4e7 Krypton ions , both in biased operation. After partial array readout (row-wise readout top-down) addressing issues occurred; The legend shows the difference current in µA.

4.4 Total Ionizing Dose Testing

Total ionizing tests have been performed with Co-60 after the SEE tests, and including devices with potentially pre-existing damage from the SEE tests. The measurement results of the analogue-memory state readout of DUT3 after irradiation (SEE, TID) are depicted in Fig. 8. The cell-wise map plots indicate a certain wavy noise-pattern that most probably originates from the measurement setup. Some stripe patterns are visible that indicate offset currents along the vertical bit-lines which most probably originates from leakage currents within the CMOS transfer gates that connect the respective BLs to the measurement pads of the chip. Some single cells with absolute difference currents up to 5 µA can be observed. These brighter spots indicate changes in the read currents of < 0.1% of the individual array cells that can be attributed to changes in the polarization state, charge trapping effects or junction leakages of the FeFET devices. With maximum current changes up to 5µA and for a digital operation with only two memory states and consequently a separation of the memory state distributions in the range of 10 µA it can be assumed that a small number of false bit-state attributions are possible that most probably can be corrected by the implementation of suitable ECC schemes.

Moreover, a general current offset drift of both distributions (0s and 1s) that is visible in the cumulative distribution plot in Fig. 8 (bottom) typically can be compensated for by the implementation of a suitable referencing scheme.

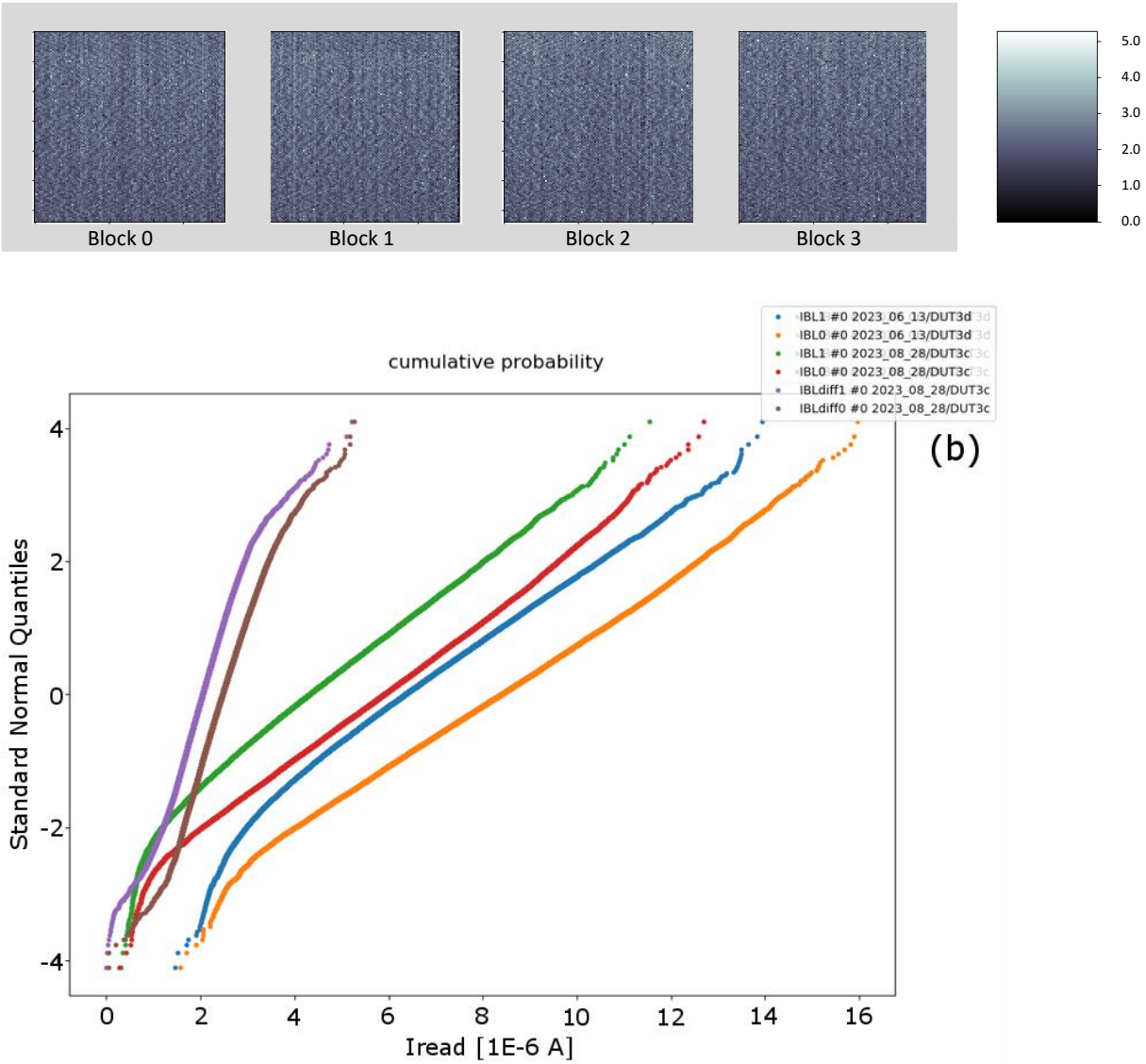

Fig. 8. (top) Analogue memory state readout on the bit lines (BL) on FeFET DUT3 (64kBit array with 4 blocks á 16kBit). Shown is the cell-wise current difference in [µA] between initial test and the final performance test after full treatment (thermal tests, SEE test, TID test to 100 krad and additional thermal test); (bottom): cumulative probability distribution of the memory states fo the same array in the initial state and final state (blue&green: cells in state '1' , orange&red: cells in state '0') and difference (brown/violet lines) between initial measured distribution and final distribution, showing only minimal shifts in the range of 2 µA in average after cumulative TID,SEE and Thermal testing In digital readout such rather uniform shift of the whole distribution might be compensated by a suitable reference current scheme utilizing a number of reference cells.

4.5 Joint effects

Two DUTs were included both in the heavy ion SEE-tests and the Co-60 TID Tests. DUT3 was exposed to in total 5E7 Xenon ions/cm^2 and DUT4 to 2E7 ions/cm^2 of Xenon and 1E7 ions/cm^2 Krypton. In the total dose approximation by UCL, which is only valid for heavy ions in pure silicon, this amounts for a pre-existing TID exposure of 50 krad(Si) for DUT3 and 25.2 krad(Si) for DUT4.

Between these SEE-tests and the TID-tests was about a month in which the devices could potentially anneal, so there is no good method except phenomenologically interpreting the measurement results, to see if this previous history of the device could have a potential effect.

4.6 Thermal Testing

The following charts show the voltages and currents of the housekeeping data measurement.

The chart shows that DUT3 has undergone all tests according to the main test sequence. The horizontal axis of the charts show time (not to scale). From left to right, the HK data are shown of the steps

- Thermal tests before radiation test
- HK before and after SEE tests
- HK during TID tests
- HK after anneal time
- Thermal tests after radiation tests

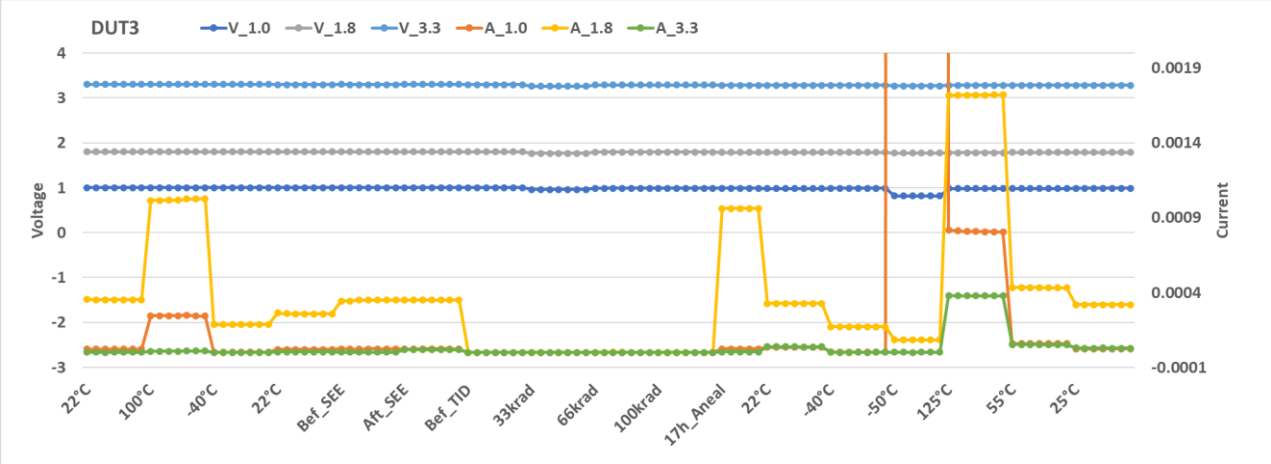

Figure 1: DUT3 Housekeeping data.

During TID testing, the current measurements did not work as expected, but current measurements after TID indicate that the currents have not changed due to total dose

At -50°C, DUT3 experienced a high current consumption of 0.108 Ampere, limited by the power supply. After warming up, this defect resolved itself.

5 Summary and Conclusion

The activity revealed, that the selected Hafnium-Oxid non-volatile memory technology can be used to achieve memory components that will be insensitive to space environmental conditions.

In the next development steps, the array logic has to be upgraded using a manufacturing technology compliant to space environment. Further, a program->verify algorithm has to be developed and implemented within the memory controller on-chip to achieve a fully reliable memory device. Not all manufactured and available devices, especially FeCAP and FeRAM test chips, have could been tested due to time and budget constraints.

Our results indicate, that the HfOx-based non-volatile FeFET memory technology is suitable for building components that will be insensitive to space environmental conditions. The test chips where able to withstand TID of 100 krad and a particle fluence of 5E7 ions/cm2. Although this was not a qualification but a technology enhancement activity, the hafnium-oxide technology has demonstrated its compatibility with representative space radiation environment. In the next development steps, the on-chip array logic has to be upgraded using a manufacturing technology compliant to space environment. Further, a program-verify algorithm has to be implemented within the memory controller on-chip to achieve a fully functional digital memory device.

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