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ELFIS

Executive Summary Report

Deliverable Document

to

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List of Abbreviations

Abbreviation or term	description
ASPI	Addressed SPI (Caeleste's flavor of register addressing over SPI)
baseline	For specifications that are under discussion and may need to be updated or refined during the project, the proposal document is based on this value.
BSI	Back Side Illumination
DS	Dark signal
DSNU	Dark signal non uniformity
ELFIS	European Low Flux Image Sensor
GS	Global shutter (-technology)
HDR	High dynamic range
PLS	Parasitic light sensitivity
PPD	Pinned Photo Diode
PR	Photo response
PRNU	Photo response non-uniformity
QE	Quantum efficiency

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1 Introduction and scope

This document contains an executive summary of the work done for ESA study contract no 4000133295/20/NL/AR: European Low Flux CMOS Image Sensor development and optimization Phase2. It provides a description of the work done during the design, fabrication and testing of the device and an overview of the results achieved.

For reference an acronym was chosen to name the project in further communications: **E**uropean **L**ow **F**lux **I**mage **S**ensor Phase**2**: ELFIS2..

The main goal of the ELFIS/ELFIS2 project was to create a European supply chain for high-performance CMOS Image Sensors. These image sensors are deemed strategic for Earth observation, and Science missions.
The main targets were to reach improvements on spectral sensitivity, signal to noise ratio and durability in a space environment.

ELFIS2 and its processor, ELFIS, were started to enhance European capabilities to design, build and qualify CMOS image sensors for space application within Europe. The concrete objectives of the activity are:

- To design a Back Side Illuminated (BSI) CMOS Image Sensor (CIS)
- To manufacture this CIS in a European wafer foundry
- To evaluate the CIS design in a European facility
- To make accessible foundry processes and CIS design to European design houses following completion of the activity

2 Project context

The ELFIS project was initiated from an initiative at ESA called : Euro CMOS Image sensor Fab Technology Development Plan" (ESA doc No EUROCIS-TDP-01032011MZ-NN).

This plan identifies a strategic need for a Europe-based CMOS image sensor for Earth observation and astronomy.

European manufacturers already offer a variety of detectors for different wavelengths and formats but they are not targeted at high-performance applications in terms of sensitivity, signal-to-noise ratio and environmental durability. In fact, worldwide there are very few CMOS foundries offering image sensors suitable for application in space.

Therefore, ESA developed a dedicated development strategy to enhance European capabilities to design, fabricate and test CMOS image sensors for space application.

In a first instance, this strategy comprised 2 paths for the development of CMOS image sensors: one targeted at Earth Observation (EO) and one targeted at astronomy and science. These targets were designated as "high flux" and "low flux" respectively.

The ELFIS project was situated in the "low flux" domain and focusses on high sensitivity, low noise and radiation tolerance.

3 Requirements

Apart from the detailed requirements for the sensor design that were listed in the project Statement Of Work (SOW), Caeleste also added additional design targets to come to a multi-purpose image sensor, usable in both astronomy (low flux conditions) and earth observation (high flux conditions).

The main design drivers can be listed as follows:

From the ESA SOW:

- Back-Side Illuminated (BSI) CIS produced in a European foundry.
- Stich-able design.
- Global shutter mode with CDS
- Parasitic Light Sensitivity(PLS) < 0.02%
- Quantum Efficiency > 75% @293K and [350 - 800 nm]
- Read noise < 5 e- rms (nominal)
- Modulation Transfer Function (MTF) > 50 % over [350 - 800 nm] range at Nyquist
- Dark Current < 20 pA/cm2
- Full Well
    - High Gain: <10 ke-, pref < 6 ke-
    - Low Gain>500, pref 700 ke-
- Radiation-hard design

4 Work Flow

As per SOW, the project execution was subdivided into several tasks that in a first approximation were to follow each other in the following way (Figure 1):

- Task 1: Detector requirements analysis (WP1000)
- Task 2: Review of detector design (WP2000)
- Task 3: Detector manufacturing (WP3000)
- Task 4: test plan and test set-up preparation (WP4000)
- Task 5: Detector full electro-optical characterization including radiation testing (WP5000)
- Task 6: Conclusions and recommendations (WP6000)

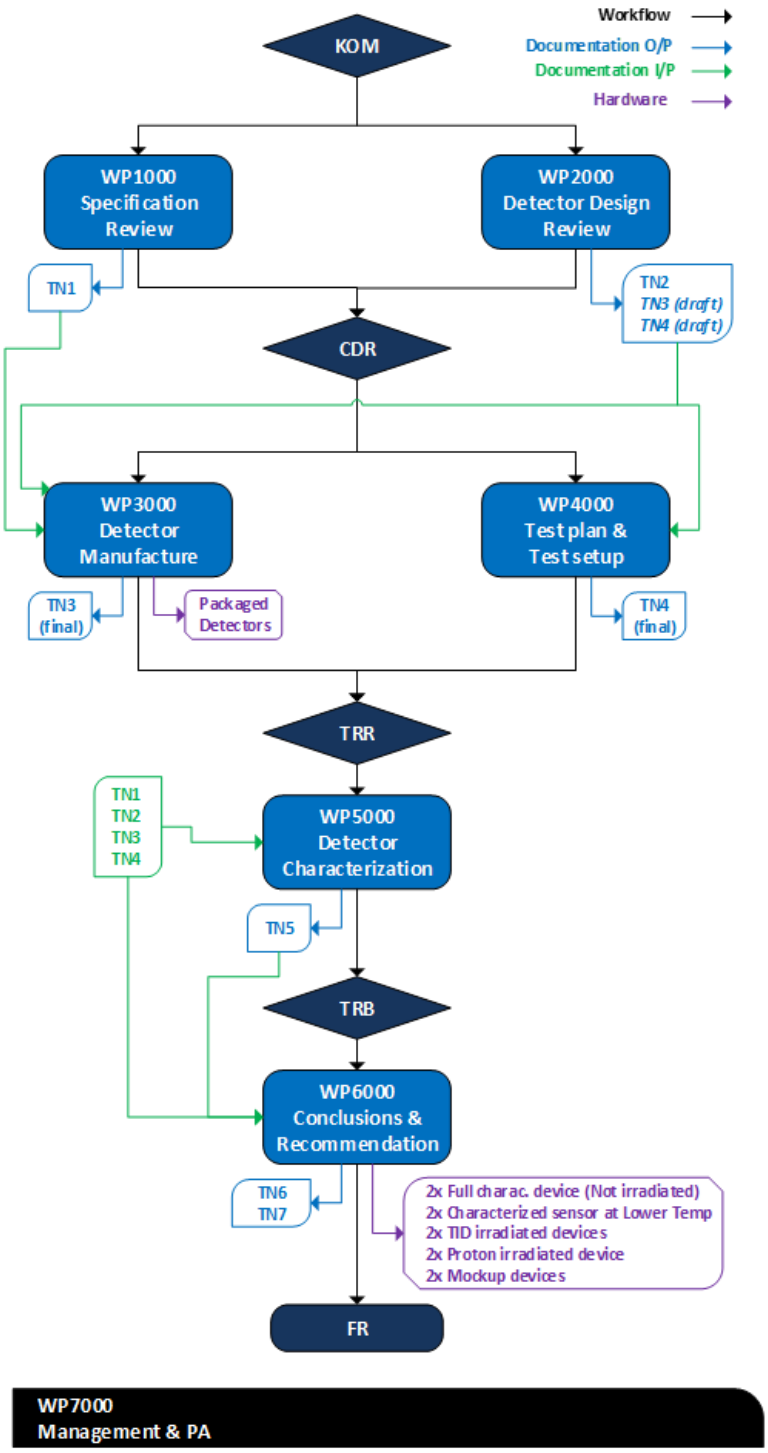

Figure 1: ELFIS2 project flow

In parallel with requirements review and first package concept, a review of the detector design as made in CCN2 of ELFIS main project was done and all preparations for manufacturing, assembly and preliminary package design were made. It was decided to split up the wafer run in 6 different splits, varying in epi thickness of the starting material (6,12 and 24um), resistivity and minor differences in the doping levels within the pixel.

The manufacturing of both silicon and package was the subject of Task3. Devices of first lots A3 and A6 were assembled. The evaluation of first lots assemblies revealed a problem with the image, stripes were found over large areas of the pixel array (NCR5). After a root cause analysis together with the silicon foundry, it was found that a yield issue at the processing was causing ill-formed or missing vias, resulting in unreadable columns. The foundry put a mitigation action in place to avoid this in the later split lots A4,5 and 2.

All splits have been characterized at room temperature and -70C at Caeleste and some devices have been measured at ADS at room temperature and 173K in thermal vacuum. Split lot A4 and A5 did not show the stripes due to this mitigation action.

5 Review of specifications and design

5.1 Image sensor architecture, floor plan

The floor plan is composed of different blocks as shown in Figure 3. It constitutes an image sensor with a focal plane area of 2048x2048 pixels.

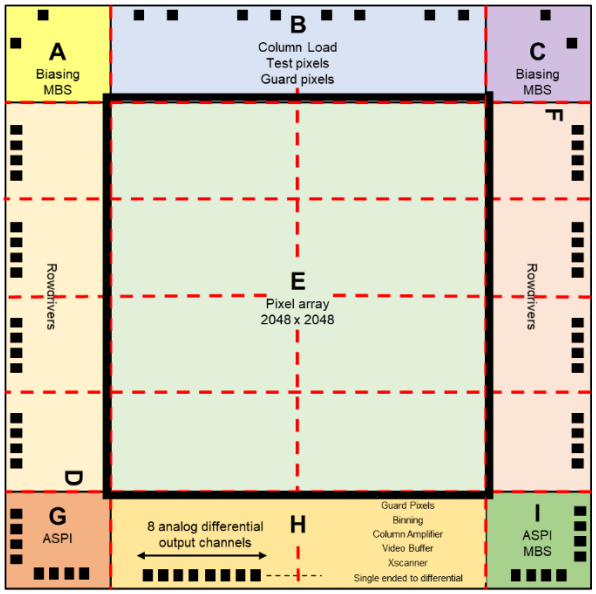

Figure 2: Elfis2 image sensor floor plan

Figure 3: Elfis2 image sensor floor plan

.

The blocks are labeled A to I (Label C missing), their respective function is listed in Table 1

Table 1: ELFIS functional block description.

Block label	Function
A	biasing electronics and digital control structures
B	column loading of the pixel array
D / F	This block contains the row drivers
E	pixel focal plane area.
G	This block contains the aSPI digital control circuits
H	X-scan logic , the single-ended to differential output converters and the output drivers.
I	logic for the addressed SPI interface.

5.2 Detailed design, Layout

During detailed design the schematics that were developed in the previous phase of the project are converted into real layouts combined into a full image sensor.

The layout work was split into different parts that were combined into a final layout:

- Pixel layout: different variations of the basic pixel
- Periphery blocks: Supporting blocks for the pixel array
- Test blocks: Additional test structures for direct measurement of QE and evaluation of variant designs

6 Fabrication

The processing of the 12 ELFIS2 wafers was split into 6 splits with different starting material (epi thickness) and slightly modified doping profiles in the pixel.

Group	#wfrs	Stitch config	BSI/FSI	DEEPNWELL	p+ implant on backside	starting material	Final Thickness
A1	2	2k*2k	FSI	no	no	EPI 6um LowRES	4um
A2	2	2k*2k	BSI	no	no	EPI 6um LowRES	4um
A3	2	2k*2k	BSI	no	no	EPI 14um HiRES	12um
A4	2	2k*2k	BSI	YES	YES	EPI 14um HiRES	12um
A5	2	2k*2k	BSI	YES	YES	EPI 14um HiRES	12um
A6	2	2k*2k	BSI	YES	YES	EPI 24um HiRES	22um

To reduce risks and save material, it was decided to start the manufacturing of the Lots in several stages:

1. BSI_A3 and A6

Processing started on ELFIS2 tape-out and ran until BSI completed. Then a few samples were assembled and functionally tested by Caeleste. Devices from both splits had only limited area where the device was sensitive to light, this was due to a yield issue at the foundry. After the root cause investigation, a mitigation program was set up by the foundry.

2. BSI-A2,A4,A5

also started on ELFIS2 tape-out and stopped before contact as to wait for the results of split A3 and A6. Due to the root cause investigation on the A3 and A6 split lots, A2, 4 and 5 were kept longer on hold as initially planned.

7 Characterization

For the characterization of the ELFIS2 image sensor a dedicated test system was developed that was used both Caeleste and at ADS.

At Caeleste a complete electro-optical characterization was don at room temperature, at ADS the main electro-optical parameters were evaluated at room temperature and at 173K in thermal vacuum.

7.1 Test system

The ELFIS2 test system is a set of tools that allows to obtain images using Elfis2 device and grab the data to the PC. It consists of the test board and the actual the Elfis chip-on-board (COB). Figure 4shows test system schematic diagram. Figure 5 shows pictures of the Elfis2 COB (a) and test board (b) respectively.

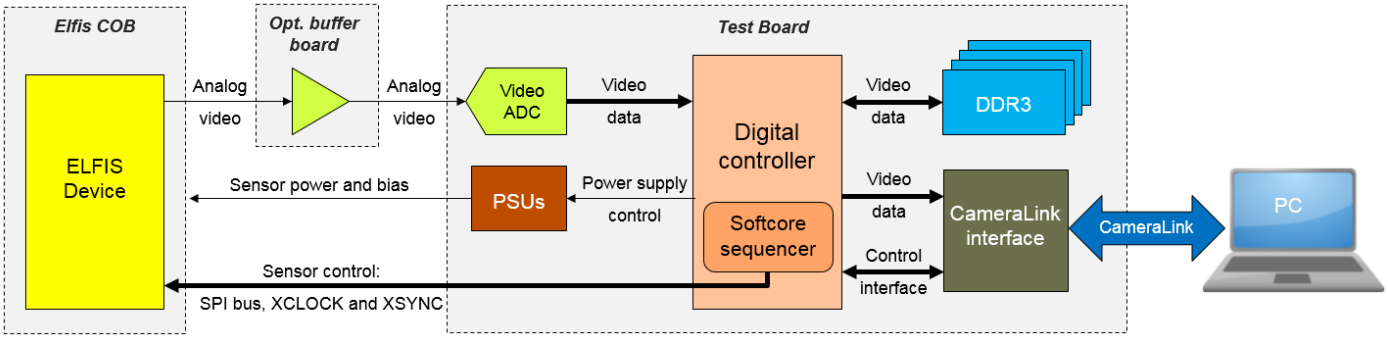

Figure 4. Test system functional diagram

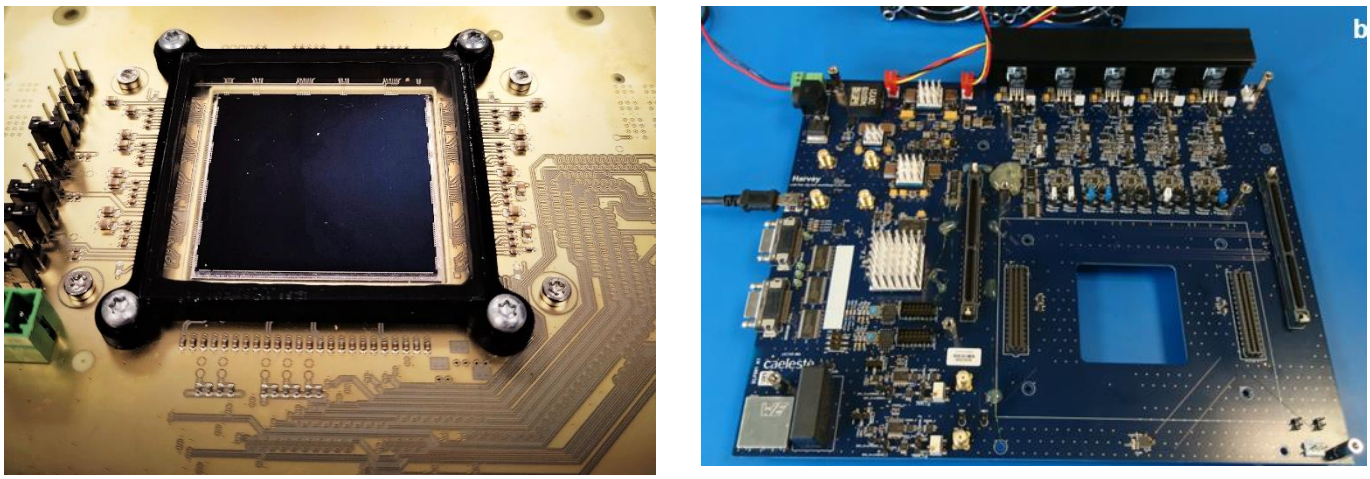

Figure 5. Photographs of Elfis COB on the left and test system board on the right.

A typical test procedure is as follows:

- Elfis2 software running on personal computer initializes communication with the test system, configures and enables DUT power supplies according to the desired settings.
- For image acquisition Elfi2s software compiles and downloads selected sequence to test board's
- Digital controller executes the sequence and places sampled analog data into test board's memory blocks
- Elfis2 software sends a request to digital controller to upload acquired image data via CameraLink interface to the PC
- Raw image data is remapped and processed on the PC.

7.2 Characterization

A full electro-optical characterization was conducted at Caeleste at room temperature and a sub-set of the most important parameters was measured at ADS, both at room temperature and at 173 K in thermal vacuum.

The room temperature measurement results, obtained at ADS are in good agreement with the results seen at Caeleste. However, at low temperature some discrepancies were seen: low QE, increased dark noise, decrease full well capacity and non-linearity in the photo response curve near dark.

However, these anomalies can be explained by non-optimal tuning of the device for low-temperature operation and by incorrect threshold voltage from processing.

8 Conclusions and Recommendations

8.1 Conclusions

Under ESA Contract No. 4000133295/20/NL/AR : European low-flux cis development and optimization - Phase 2 (ELFIS2) a BSI image sensor was designed, fabricated, and characterized in Europe-based facilities:

- Caeleste, Belgium: CMOS Image Sensor Design and test system design and full electro-optical characterization
- LFoundry, Italy: Silicon process development and wafer production
- Airbus Defense and Space, France: Electro-optical characterization at 173 K in thermal vacuum
- AIM Micro Systems, Germany: Device assembly.

The ELFIS2 image sensor demonstrates a unique combination of high sensitivity, high dynamic range true global shutter operation and radiation hardness. This combination of properties makes it applicable not only in low-flux operations as astronomy but also in high-flux ,high dynamic range operations as earth observation.

The high sensitivity is realized by applying Back-Side Illumination processing where the full area of the focal plane can be used for charge collection.

High dynamic range was obtained via a multi-gain pixel design allowing to read out the pixel charge using multiple gain factors for the same integration period.

Global shutter operation is realized by developing the technology for an embedded storage node in the pixel.

Radiation hardness was obtained by standard Caeleste radiation-hard design techniques.

An operational sensor was demonstrated with the following characteristics:

- Stitched compatible sensor with possible sizes of 2048 x 2048 pixels (baseline) and 4096 x4096 pixels (bigger stitched config variant):
  - Possible stitch block in X-direction corresponding to 1024 columns
  - Possible stitch block in Y-direction corresponding to 512 rows
- Pixel size: 15 x 15 µm
- Operation mode: RWI (Read While Integrate), ITR (Integrate Then Read) and Rolling Shutter
- Radiation hard device
- Global shutter pixel with HDR and BSI feature
- Pixel has two gain settings corresponding to full well values
- Additional analog gain in the readout (x2, x4, x8)
- Frame rate: 131 Hz
- Noise level: <5 e-
- Dynamic range: 95 dB

A full electro-optical characterization was done at Caeleste, and the most important parameters were also characterized at ADS both at room temperature and at 173 K in thermal vacuum. The test results, obtained at Caeleste and at ADS show good agreement (awaiting report ADS).

Six different process splits were processed and tested

The required specifications from the SOW were largely met apart from the following specifications:

- the DSNU (due to the low dark currents measured BOL)
- the full well capacity which is at 13.8 ke^- and 189ke^- for HG and LG respectively. 390ke^- achieved with ultra-low gain mode
- The PLS which is >0.02% at 830nm and roughly at 0.024% at 630nm for A4 and A5 lot.

8.2 Lessons learnt and recommendations

8.2.1 Design

By design the following things are improved with respect to ELFIS1

- Lower Read noise below 5e- is reached. In certain cases, 1.7e- could be reached.
- In split A6 a thick HiRES EPI wafer (24µm) was used for split lot A6.
- Back biasing to improve MTF for thick EPI was implemented. But in practice the effect of it was only present at the border of the pixel array. Toward the middle of the array, the effect decays fast.

8.2.2 Processing

However, it was observed across multiple devices of split A3 and A6 that a vast portion of the image shows many black columns. This is due to process variability. SEM photos from the foundry showed that the video wires of channel 0 are interrupted and thus floating over a long distance. Detailed photos show that VIA5 is missing over a wide narrow area and explain the defects at the input of the video buffers, as the controls of these switches also need VIA5. This issue has been recorded in detail as NCR-05. Due to instability in the process at this foundry, it is recommended to port the design to another silicon foundry.

8.2.3 Characterization

8.2.3.1 Low T

At low T a non-linearity is observed near saturation. This is due to the use of CMOS caps instead of MiM caps, necessary to be able to implement the backbias.

8.2.3.2 Noise measurements

During the test campaign, it was shown that the read noise was below the spec of 5e-. However, the target of 2e- was not met. Test showed that the main contribution to the read noise is the 1/f noise of the source follower.

The noise of SF is higher than expected. The root cause is not yet known but should be investigated at the time of a design port.

8.2.4 Project management, Planning

The ELFIS2 project faced considerable delay when compared to the original planning. This was due to the delayed processing of the different splits caused by the root cause analysis of NCR5 in split lots A3 and A6 and also by the increased processing time for the last splits due to the mitigation actions that were in place in the foundry for NCR5

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