Cost effective Tandem Space Solar Cells

Project: **4000134993/21/NL/FE**

Code: **CoffeTaSS**

Type: **Executive Summary Report (ESR) - public**

Doc.-Ident.: **D10**

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		Name *name*	Datum *Date*	Signatur *signature*
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Freigabe / *Released*	B	V. Khorenko	27.06.24	V. Khorenko

PGR 00010797-01-00

Dateiname / File 00010763-RIX_CoffeTass_4000134993_FR.docx; UA: TR; UVST: RPV

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Introduction

Over the past years an emerging trend in the space industry is observed aiming for the use of many small to medium size satellites (<500 kg) working and communicating together to serve different purposes such as earth observation, IT services and other. In particular, constellation programmes like OneWeb, Iridium Next, Telesat LEO, Starlink, etc. aim to deploy numerous (>10 … >1000) small satellites to provide

worldwide IT services with high data rates and signal latencies even better than today's ground-based technologies. Due to a high number of satellites and their constantly same built-up within a program, standardized manufacturing technologies with high throughput are urgently needed to satisfy the demand of these programs in low-cost components with high production volumes and short delivery times. To fulfil these requirements, the state-of-the-art technology requires further development to satisfy the industries need for lower costs.

1 Activity Description

To improve cost effectiveness for the state-of-the-art technology, numerous process adaptions with different cost saving potentials but also risks were studied. As the first step an in-depth elaboration of the cost structure for the established 3G30 cell technology was performed in combination with risk assessment for each process step. In the following, the selected processes were developed and tested . Subsequently, these processes were implemented and cell prototypes were manufactured and subjected to engineering tests to evaluate the cell performance after processes adaptions in comparison to the standard 3G30 cell. Finally, the overall potential cost savings were evaluated.

In parallel, a development aiming for a novel cell concept with a long-term but much higher cost-saving potential was started. The key element of the development was complete release of device layers from the growth substrate enabling the substrate reuse.

2 Study on cost structure and cost saving potentials

In order to identify approaches to reduce the cost of advanced multi-junction solar cells starting with Ge wafer level through solar cell epitaxy and up to solar cell processing a technology specific cost-of-ownership (COO) model was elaborated. The developed parametrized COO model takes into account footprint, consumption of process materials or process/labour times while 8 cost categories were defined (see Figure 11). Cost of yield loss (CYL) results from mechanical, optical and/or electrical scrap and

depends on statistical loss as well as the value of the workpiece during this process step. Waste disposal and process consumables are similar to each other. One describes the consumed materials for the process, the other describes the cost of waste disposal. These costs are usually specified per workpiece/batch or per time (hour/year/…). Labour cost include cost of operators, engineers and service personnel. Maintenance/service cost consist of material cost for maintenances, e.g. parts exchange or cleaning. Utility costs include base material/media cost (i.e. standby electricity) as well as facility wide process media such as nitrogen, cooling or compressed dry air. Facility costs included rent, cleanroom operating cost (footprint) and/or depreciation of building cost. Depreciation (invest) cost of tools are allocated to equipment cost.

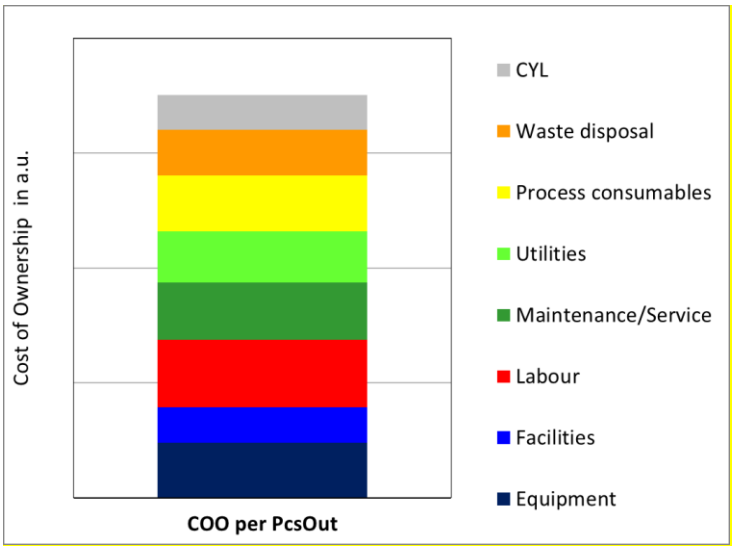

Figure 1: Cost Of Ownership (COO) calculation example. From top to bottom, these cost aspects are: Cost of Yield Loss (CYL), cost of waste disposal, cost of process consumables, utility cost, maintenance/service cost, labour cost, facility cost and equipment cost.

3 Development and test of process changes

3.1 Epitaxy Process Study

AZUR SPACE Solar Power GmbH produces lattice matched triple junction structure 3G30-Advanced space solar cells based on 150 mm wafers. The process is well established on the state-of-the-art epitaxy production equipment. When using the new tool generation, the production efficiency isn't comparable to the heritage tools yet. In

order to improve this, a detailed simulation of the key parameters of the epitaxy process (e.g. temperature distribution inside the epitaxy reactor, geometrical and process recipe variations) was established and several modifications and their impact were simulated.
Finally, the best results were experimentally validated, while the growth increase for a selected solar cell material of up to 11% was confirmed.

3.2 Low-cost metal contacts

One approach to reduce the cost share of the front and rear side metallization is to omit the gold layers on top. Correspondingly, cell samples without the gold layer on the front side only and without the gold layers on the front and rear side of the metallization were manufactured. The result was comparable with the performance average of standard cells. We performed our standard acceptance tests procedure on the cells:

- Visual inspection was passed.
- Weld and pull tests with Ag interconnectors and tape peel tests after 24 h humidity exposure were also passed for the front side contacts.
- Weld and pull tests with Kovar interconnectors were also passed after minor adaptions of welding parameters.

In summary, principal process feasibility could be confirmed.

Activities on using electroplating metallization approach for III-V solar cells were performed at Fraunhofer ISE. For this, we selected metals already qualified for use in space solar cells. The resulting wafers showed the desired metallization properties, a complete metallization in all resist-free regions and sufficient adhesion.
In a second iteration we processed 3G30 epitaxial structures. In order to reach sufficient homogeneity of the metal height over the wafers optimization was still necessary but not addressed in the project.

3.3 Low-cost AR coating

At AZUR, physical vapour deposition (PVD) is used as standard deposition process for double layer anti reflection coating (ARC) consisting of titanium oxide (TiOx) and aluminium oxide (AlOx). However, the necessary large ultra-high-vacuum chamber and the complex handling procedure represent a significant cost share of the solar cells. We concluded that high speed atomic layer deposition (SALD) process is able to produce reproducible homogeneous TiOx and AlOx layers, which can be processed within our standard production chain. Welding tests and tape peel tests were passed after process adaptations. To date, the layer properties such as refractive index do not completely fit the optimum optical stack design, so further iterations for optimization and understanding of how the optical parameters can be adjusted by SALD process parameters are necessary.

However, SALD is a completely new technology. Therefore, after achieving required layer properties, a credible justification based on extensive engineering tests will be needed before the SALD process can be implemented. Cost calculations indicate the cost reduction potential of the SALD process.

3.4 Cost-efficient laser processing

The anti-reflection coating (ARC) is applied over the complete wafer including the metal contact pads. To interconnect the cells, it is necessary to remove these layers on the contact pad areas. Currently, this removal (“pad opening”) is done by a wet chemical process. For the preparation, a photo-litho-process with resist coating, photomask UV-exposure, wet resist developing, rinse and dry and control steps are needed. After wet etching of the ARC, the resist is stripped in organic solvents, followed by a rinse and dry step.

Laser ablation of the ARC-Layers is expected to enable shorter processing time per wafer due to the relatively small surface area of the pads. For different coating variation a complete removal of the layer was demonstrated and the results of weld/pull tests met AZUR’s standard acceptance criteria.

Laser based process has been also tested for dicing of III/V cells. In general, the Thermal-Laser-Separation (TLS-process) is well established for dicing silicon solar

cells. Thereby at first, a small scribe is ablated with a laser. In the cleaving process, the laser just heats up the substrate in the cutting street followed by a water jet, which cools the workpiece. This thermal tension induces a precise separation without micro cracks. This process is kerfless meaning there is no material loss along the cutting street, and it is typically faster than mechanical dicing.

The transfer on III-V-solar cells is however difficult due to the very different scribing behaviour of the Germanium wafer. After adaptions of the tool, fundamental investigations showed the possibility of separation with the TLS process. But in contrast to silicon, it is necessary to ablate at least 50% of the Ge wafer from the rear side within the scribing process. In case of further implementation of the TLS process to Ge-wafers, a laser machine should be equipped with another laser source, to test and generate smoother edges in germanium.

3.5 Direct printing instead of photolithography

The goal of this work package was to evaluate inkjet printing for masking of dielectric layers and mesa structuring. This also includes removal of the ink and an assessment of the quality of the process. A prerequisite for successful printing is a printing system that allows the ink to be applied as precisely, reliably and reproducible as possible. This process is a complex interaction of ink, print head and substrate. In order assure this, an industrial inkjet tool from a well-established machine supplier in the semiconductor industry was utilized in this work.

The suitability of the process for etch dielectric layers in an acidic etch was demonstrated. Only a very small undercut of approximately 5 µm per side could be measured. The ink shows overall very good adhesion and can be removed in acetone and isopropyl alcohol.

Finally, a whole mesa structuring sequence (dielectric – GaAs – Ge) was successfully conducted.

4 Evaluation and manufacturing of prototypes

The intense investigation performed in the project enabled many processing routes. For evaluation we decided to combine the technologies with the highest expected manufacturing readiness with one production step with a higher risk.

Epitaxy Process Study: Based on intensive simulation work done during the first part of the project, modification of the epitaxy reactor was done and the potential of this reactor modification in combination with process parameter adaption could be validated. Nonetheless, there are still further elements to improve before implementation in order to maximize the effect for costs reduction.

Cost optimized metal stack: For the cost optimised metal stack mainly the removing of the Au-flash has a relevant cost saving potential without reduction in performance. The historic reason for the Au-flash is corrosion prevention if the cells are stored in humid atmosphere before launch- mainly before welding to strings and panels. Nowadays the storage conditions are much better controlled during the complete life cycle from cell to SCA, shipping, string and module generation and launch. The savings are however limited to the real usage of gold whereas a large amount of gold not remaining on the wafers but in the tooling, can be effectively recycled.

Metallization process: The plating experiments at the subcontractor FhG-ISE showed a significant influence of the preparation process before plating onto the adhesion of the metal fingers. An optimized process enabled a small and precise finger grid with sufficient adhesion. This could further improve the costs for the metallic layers but needs further investigations, in particular, regarding the layer thickness homogeneity and process reproducibility.

Low-cost AR coating: SALD promises combination of benefits of the high deposition rate of a PVD process with a high layer quality of a classic ALD process. The experiments showed an uniform deposition nearby the defined optical characteristics. But there is still some variation in the available process. In particular, the tool was

installed in a clean room environment leading to reduced adhesion due to some contamination during the shipping process. Also no stable process is available yet. But, there is still a high potential for this technology, especially due to the significant lower investment cost compared to a PVD-tool and the expectation of a higher yield due to better handling conditions. Furthermore, the layers seem to have a better uniformity over complete wafer.

Laser processing: The pad opening with laser was developed and examined with different coating technologies (PVD, SALD and PVD without Au-flash). For all manufacturing routes, the cell samples produced with the laser process successfully passed humidity and welding tests. Laser process can omit an entire photolithography and etching-step sequence. In addition to cost savings, this process is more environmentally friendly due to less chemicals needed, less wafer handling has the potential to increase the yield in production.

Novel laser dicing process for III/V cells on Ge: The transfer of the method to III-V-solar cells is difficult due to the scribing behaviour of the Germanium wafer. Nevertheless, for the long edges satisfying results are achieved. For the shorter edges, especially for the cropped corners failures in maintaining geometrical dimensions were exhibited and mechanical robustness is considered critical due to the rough cell edges.

Direct printing instead of photolithography: With the direct printing process the photo-litho-steps coating, mask-alignment, illumination and development can be replaced. The simplification of the process route combined with a lower resist consumption is quite cost attractive. It was possible to select a resist with good adhesion and develop printing parameters for a fast and homogeneous coating. Etching experiments showed that the process generates a layer that withstands the etching fluid. The application of the process to real cells was established at a laboratory printing tool.

Table 1 summarizes the results achieved. In general, none of the individual processes is evaluated as having “no potential for cost saving”. However, for two processes there

is much more research work needed to have a realistic chance for being used for manufacturing solar cells with a sufficient quality. Therefore, these ones were excluded from the final prototype manufacturing. For three other processes, there is a higher chance but still with a non-negligible risk of failure. Finally, we decided to evaluate these processes individually. Two process steps showed a good potential and could already be tested within the process development phase. These steps could be included in the manufacturing.

topic	samples	
EPI-process	dummy	Simulation and proof of principle -> not applicable
Low-Cost-Metal-Contact	cells	No Au-flash tested i.O. -> applicable
Metal Plating (ISE)	dummy / 4“-cells	Tests still running -> partly applicable
Low-Cost AR	cells	In principle OK, but still large variation -> not applicable
Cost-efficient Laser Process	cells	Opening ARC i.O. -> applicable
TLS-Dicing (ISE)	cells	Tests still running -> partly applicable
Direct Printing	Dummy / 6“-cells	Tests still running -> partly applicable

Table 1: Summary of the results.

Resulting manufacturing of the cell prototypes was split into four routes to reduce the risk of outage and delays. In total, 82 pcs. wafers produced on ø150mm-wafers was used resulting in up to 164 cells, divided in a low risk route and more challenging and, thus, more risky routes but with higher cost reduction potential. For two process route wafers needed to be shipped to partners with correspondingly higher risk of breakage and time delay.

5 Engineering Tests

The manufacturing process for the 4 different routes took over a period of 6 months for capacity and availability reasons. Produced cells were subjected to the engineering tests carried out in 4 subgroups based on ECSS-E-ST-20-08C, Rev.1, whereby the available cells of the variants were evenly distributed among the groups.

In the engineering tests, the manufactured cell samples mostly fulfil the norm requirements except some devices within the subgroup A and O.
For Subgroup A, the pull test on the front side interconnector is below the requirements for a number of cells. The lack of a gold flash on top of the silver surface of the devices was identified as an issue in environments with high humidity. This could be expected as gold is known to protect silver contacts from oxidation. However, there might be some parameter in the processes to be further improved. The adhesion was better in the variants with gold flash and without gold flash but with shorter storage periods due to later production finish, which gives cause for optimism here. The storage including the duration and humidity as well as the parameters used in the interconnector welding process should be optimized.
In Subgroup B “Begin of Life Performance” and Subgroup C “Electron Irradiation” the cells showed the expected behaviour. Only the cells with the front side metal done by plating process showed deficiency in the overall performance that most probably is related to the thickness of the metallisation, which has to be improved within further development work.
In Subgroup O grid detachments could be observed for the samples with front side metal plating. This was expected and has still to be improved. For the cells separated by TLS dicing, the rough edge geometry tends to crack during thermal cycling and in the welding process of the front side interconnectors.

6 Evaluation on cost saving potentials

AZUR SPACE’s standard process as well as alternative production processes have been analysed regarding their COO in a five-step process as follows: Step 1 (cost model basic acquisition) and step 2 (simplified comparative technology and cost study

for current and cost reduced 3G30) have be performed. Afterwards the multiple parameter cost model has been fully established, upgraded and adjusted to our technological features and needs (step 3). Based on this, the technological model of the state of the at 3G30 process and its innovative adaptations have been designed and completed (step 4) for a realistic COO and TCO calculation. Finally, a comparison study of different process routes has been perfomed.

The alternative processes have been continuously updated in terms of content and running costs based on the experience made in the course of the project. An addition of cost calculation for a low-cost metal contact has been included. For the subsequent cost comparison study, three manufacturing route scenarios have been formed – 6” 3G30 standard and 6” 3G30 CR in two variations. The updated cost calculations resulted in a best cost reduction potential for Scenario 1 - compared to 3G30 standard. The cost reduction potential of Scenario 2 was calculated to be moderate. Including the other cost reduction approaches considered in this project (epitaxy, low-cost-metal-contact), the cost reduction potentials additionally increases for both, Scenario 1 and Scenario 2.

The overall cost reduction potential of many technological alternatives was found smaller than expected at the start of the project. However, some technologies also showed larger cost reduction potential than initially expected (especially, laser ablation technology).

Perspectively, AZUR will expand the cost model and create a COO for every process to facilitate a parametrized total cost of ownership calculation. Total cost of ownership calculations (TCO) enables throughput harmonization and correct cost of yield loss calculations.

For further cost reduction, more process technologies should be evaluated. Further process technologies of interest include screen printing, spray pyrolysis, electroplating for rear side, other spatial ALD concepts and epitaxial liftoff.

7 Low-cost processing route for future cell concepts

Another part of the project was dedicated to radically new cell concepts based on inverted epitaxy and epitaxial lift-off process (ELO) to reuse the cost intensive substrate. The work has been mainly performed by ISE with the main objective to demonstrate release of a double heterostructure (DHS) layer made of relevant materials from Ge substrate by epitaxial lift-off process. The work specially addressed achieving sufficiently high process speed and direct characterization of ELOed layer. DHS has as advantage that photoluminescence (PL) measurements can be performed on fresh epitaxy wafers and on ELOed film after ELO process as well.

In order to reduce the ELO time, the wafers were designed to maximize the longitudinal and vertical diffusion of etchant happen during ELO process. For this, chemical structuring and laser perforation of ELO trenches approaches were used.

Prior to wet trench etching, the wafers were metallized and annealed. After wet chemical structuring, the wafer was laminated. The handling tape was applied in such a way that the opening in the tape were aligned with the ELO trenches on/in the wafer. Tape perforation was carried out by a laser process. The lamination was carried out manually and was difficult to control, which could have slowed down the vertical etchant diffusion during ELO process.

Another approach used the perforation by laser irradiation. The laser process has the advantage to be less time consuming with respect to chemical structuring process. This results in just two steps: 1) lamination and 2) perforation of tape inclusive wafer in one step. The diameter and the depth of the perforation holes were selected in such a way to facilitate etchant diffusion down to the sacrificial layer.

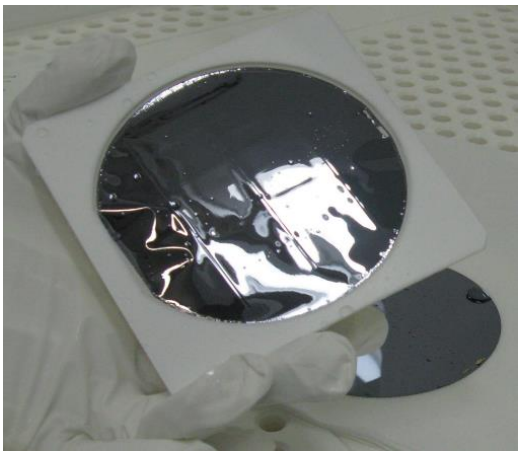

Figure 2: ELOed layer released completely from substrate laminated on tape at ISE.

In order to evaluate the best ELO conditions a number of tests was performed. The tests were based on structured and unstructured wafers, laminated and unlaminated wafers.

Epitaxy structure was defined and grown on germanium substrates. It was structured in a way enable PL measurements of both post ElO wafers and ELOed films. For better ELOed layer handling, the wafers were laminated and framed. Laminated wafers were structured by wet chemical etching and by laser irradiation. A multitude of irradiation conditions were tested and good ELO trenches and with less impacts on the regrowth layer could be generated. We found that the combination of wafer lamination, structuring and lift-off with an optimal etchant solution led to the increased ELO speed. Many samples or ELOed films were successfully released. Nevertheless, further development is still required. Rest layers of wafer could be also successfully removed by etching for a potential wafer reuse. The surface analysis of the regrowth layer has revealed the presence of a high particle density.

8 Final technology evaluation

In the project, several approaches to reduce the manufacturing costs of space solar cells were studied. Different technology building blocks have been investigated in detail and partly confirmed by engineering tests. The processes under development were accompanied by detailed cost calculations and simulations and the cost-effectiveness of the possible measures was considered.

In detail, the epitaxy process has been simulated and optimized for a new reactor type. It was possible to increase reactor growth efficiency by several percent. This can be transferred to production after further studies after the end of the project.

In field of cell processing, a reduction of metallization costs by omitting the final gold layer was evaluated. The extended tests with this modification did not show any anomalies and consultations with customers on a possible implementation are underway. An alternative metallization method to the established vapor deposition process is the galvanic deposition. The corresponding experiments showed that homogeneous metal structures can be produced. However, there are still limitations in terms of conductivity and partly adhesion as well, so that extensive process optimization will be necessary before implementation.

The application of the anti-reflective coating using an atomic layer deposition process showed promising results in terms of homogeneity across the wafers and achievable coating parameters, but the adhesion of the coatings and the reliability within the system proved to be significantly limited, so that developments on the tool would still be necessary before it could be introduced. Since the originally very low price for the tool has also increased noticeably, the cost advantage has become significantly smaller compared to the current level.

The laser ablation of the anti-reflective layer in the area of the contact pads is fast and reliable. Extended tests did not show any anomalies. Further use of this method in specific projects is currently being examined. The TLS separation process proved to be much more complex in the transfer from silicon wafers to germanium as bulk material. As a result, the process time may become very high and the theoretical cost advantage will get hardly justifiably. With the existing process route, the tendency to breakage is greatly increased compared to the dicing-grinding process, so that the process does not appear to be applicable in the current state of development. An intensive, fundamental-based new development of the technology needs to be applied yet.

The direct printing of a mask for the mesa etching process was successfully carried out. However, deviations were still noticeable in the long-term tests. These are due to inhomogeneities of the printed image. As a result, the process times are not yet economical.

Within the topic about a fundamental new cell design and substrate reuse it was possible to lift-off test layers with the ability to grow again onto the host substrate. The developments on the Epitaxial Lift-Off confirm the potential of this technology, but also show that intense and fundamental work is still necessary to establish a safe and economical volume production chain.