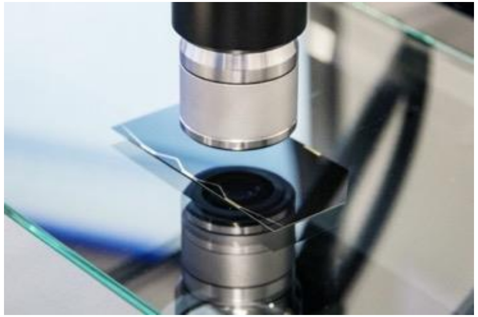




CoffeTaSS - Final Presentation
Contract No 4000134993/21/NL/FE

April 25th 2024 – S. Sommer

AZUR SPACE
A 5N PLUS COMPANY

Table of content

P90 CoffeTaSS - Cost effective Tandem Space Solar cells
Project Factsheet

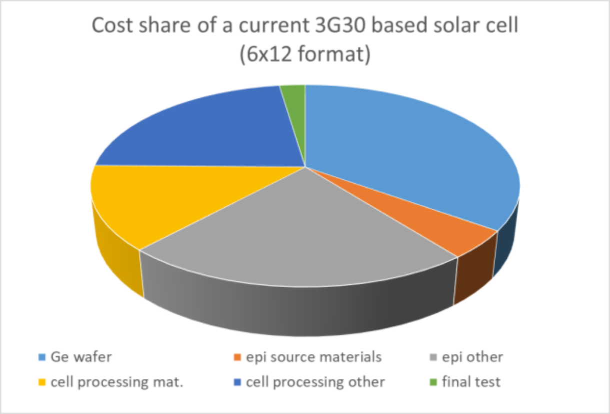
Project objectives:

Cost reduction of advance multi-junction solar cells by reviewing an adapting respective solar cell manufacturing process steps targeting a 25% reduction compared to the state-of-the-art 3G30 cells.

Formal Framework: ESA's General Support Technology Programme (GSTP Element 1 Develop)

Budget: 700 k€

Timeline: 01.08.2021 – 31.07.2023, postponed to 31.03.2024

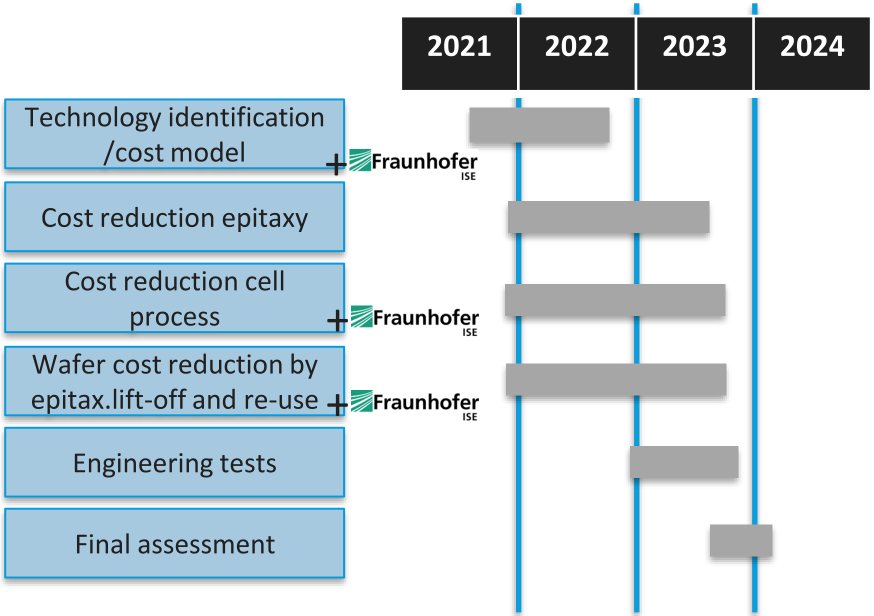


Short-mid-long term cost reduction for
- Epitaxy process
- Cell processing
- Characterisation
- Ge wafer release & re-use

→ **3G30**

→ **new cell**

P90 CoffeTaSS
Tasks and Team



Technology building blocks

- Epitaxy reactor and process modification
- Triple Junction cell optimisation
- Cost effective metal system
- New ARC process
- Laser processes
- Direct printing
- Evaluation

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Simulation of the Improved Hardware and Process Parameters

Challenge:

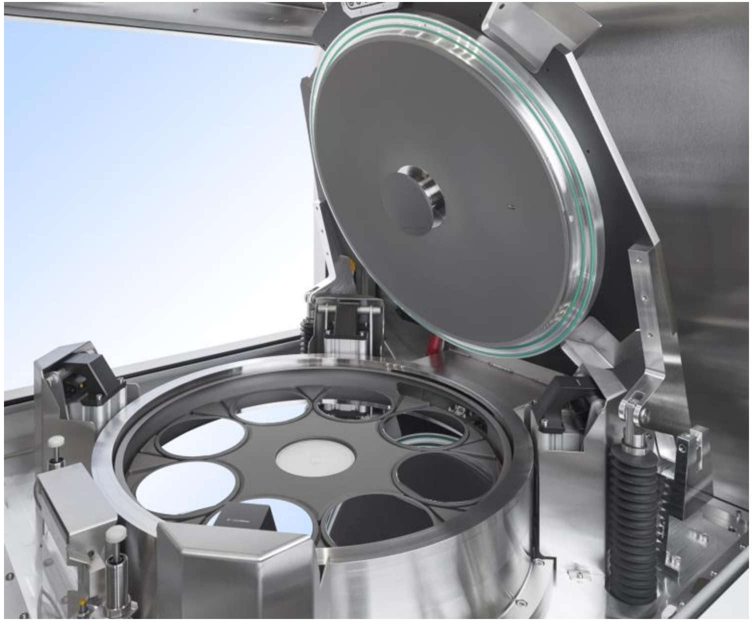
Inlet area losses in G4 (8x6") [1] lower the process efficiency.

Target:

- less inlet area deposition
- higher process efficiency

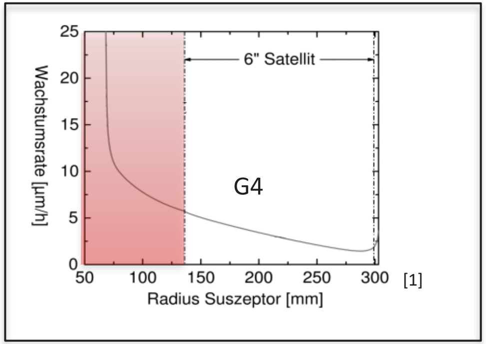
Approach:

1. Optimize inlet area geometry using modified hardware
2. Optimize transport parameters

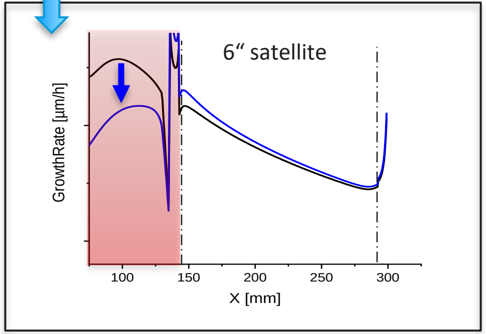


Aixtron: AIX 2800G4-TM - Production chamber ("reactor") with 8x6-inch configuration

Literature model

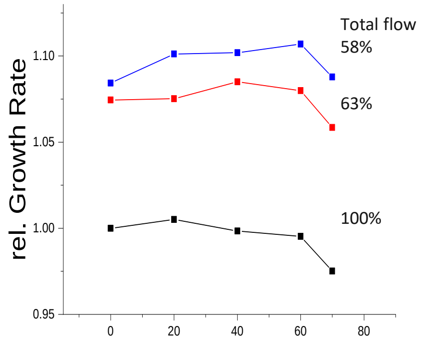


Simulation pretest



[1] R. Kellenbenz, "MOVPE von Mehrfachsolarzellen für die Konzentratoranwendung", Univ. Konstanz, PhD 2015.

Validation of the Improved Hardware and Process Parameters

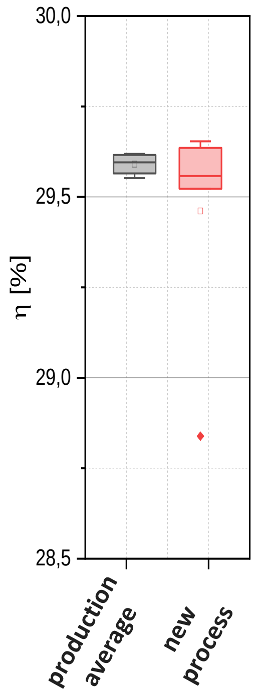


Implementation

- first production run of triple-junction solar cell
- Overall efficiency of the solar cell is unchanged compared to the regular production average.

Cost saving potential

- We managed to reduce the material consumption.
- This will result in further cost savings by
  - prolonged tool uptime
  - longer maintenance intervals



Triple junction cell optimisation

Triple Junction Cell Optimisation

Aim:

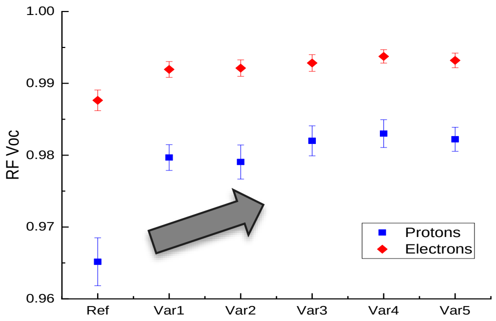
Optimisation of the triple junction solar cell regarding …

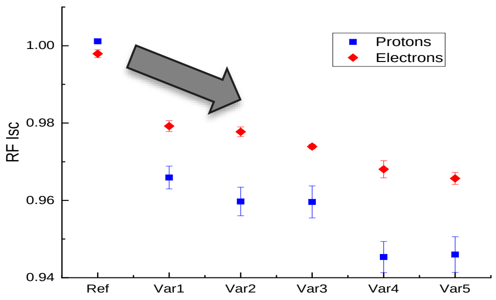
- Process robustness, growth rate and material consumption
- Electrical performance in LEO orbit (corresponding equivalent fluence of 2×10^{14} 1 MeV e/cm^{2})
- Cost (W/€ ratio)

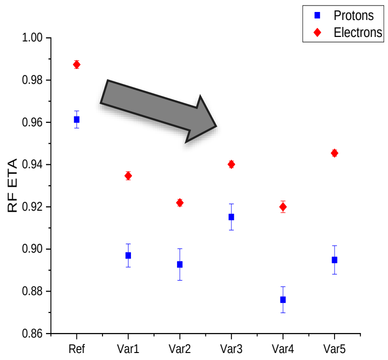
Approach:

- Re-design of top- and middle sub-cells (variation of thickness and doping level) for EOL

EOL re-designs for sub-cells







Electrons: 2×10^{14} 1 MeV e/cm²
Protons : 4.4x10^{10} 1 MeV p/cm²

Final devices show

- increase in Voc
- decrease in Isc
- resulting in a lower EOL performance than reference

→ Aim to lower W/€ ratio not achieved

Low cost metal contacts
- Removal of Au-Flash
- Contact Metal Plating

Low-Cost Metal Contacts
Contacts without gold flash

Motivation:
Au-Flash due to undefined storage conditions
Au-Flash main cost driver in metal system

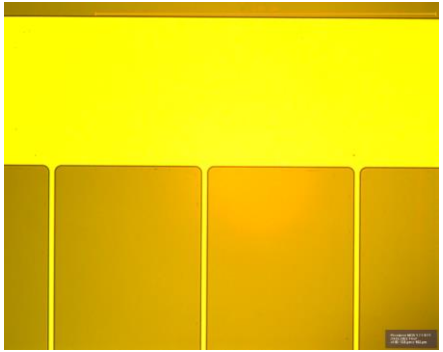
Manufacturing of low-cost metal contact cells at AZUR:

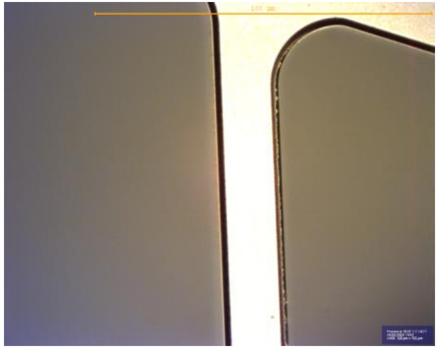
> Selected cell format 12 x 6 cm²

> Preparation of 10 pcs. 6″ wafers with 3G30-Advanced cell structures.

> First step: front side contacts pure silver without gold flash on top.

> Challenging process steps : lift-off, cap etching.





- Lift-off
- Cap etching
- I-V-measurement
- Visual inspection
- Welding tests

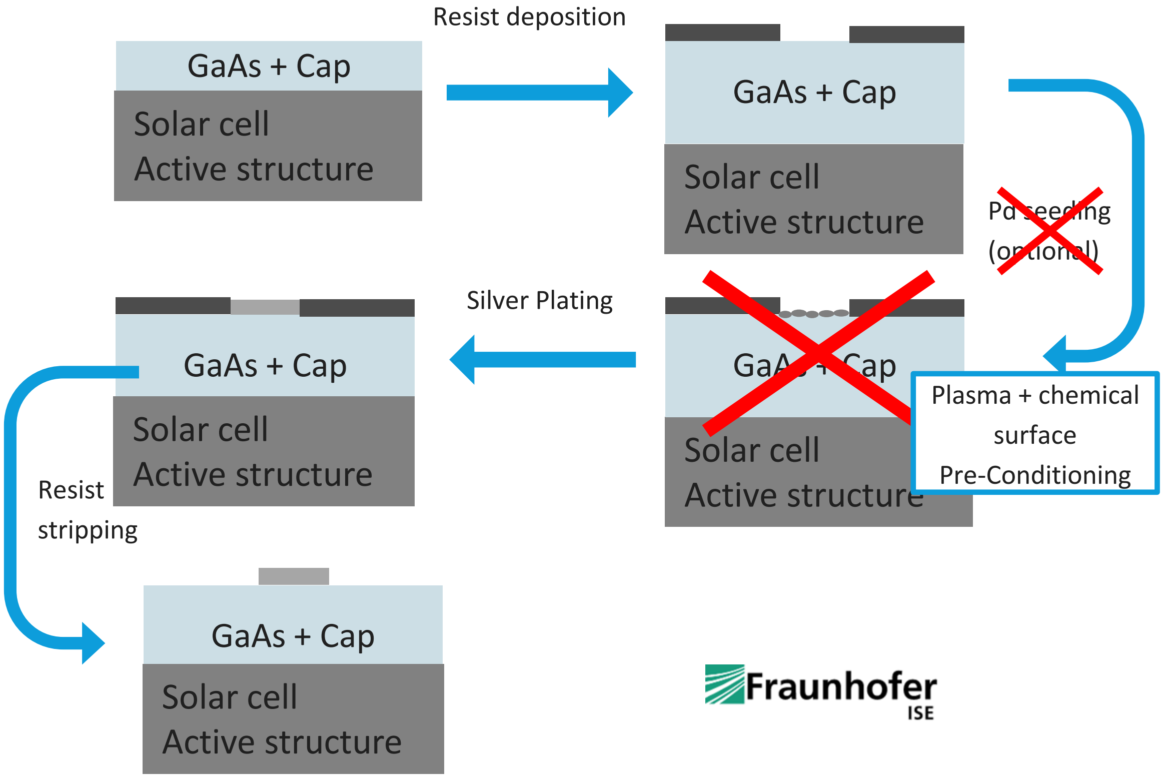
Metal plating - Boundary conditions

Process flow:

- No vacuum deposition of seed layer desired (too costly / too complex)
  → Would be easier for plating, but direct plating also possible
- Preferredly compatible with Azur's standard resist

Metals:

- ISE offers ~~Nickel, Copper~~, **Silver**, ~~Tin~~, Pall~~adium, Zinc, (Gold)~~



Process engineering

Resist evaluation ✓

Plating demonstration ✓

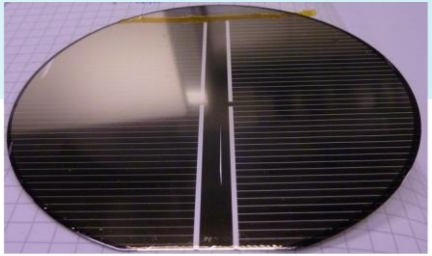
- First simple plating process yields satisfactory results

Adhesion optimization ✓

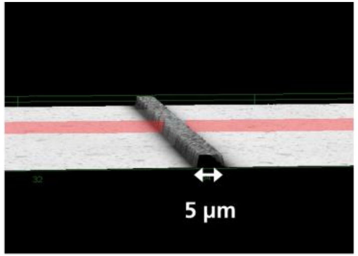
- Combination of chemical and plasma treatment give sufficient adhesion

Working cells ✓

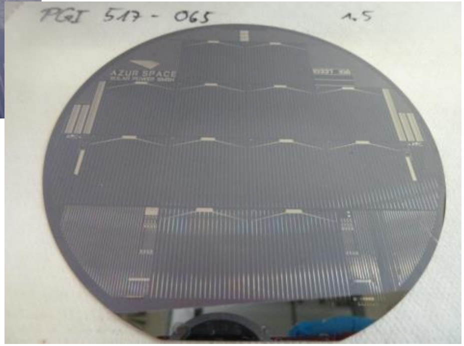
- Plating and cap etching (minor issues) worked, cells @Azur for IV



Silver deposition using AZ10 XT Photoresist on Wafer



3D Microscope image of 5µm contact finger plated into AZ10 XT



Plating of cell batches for Azur

Setup

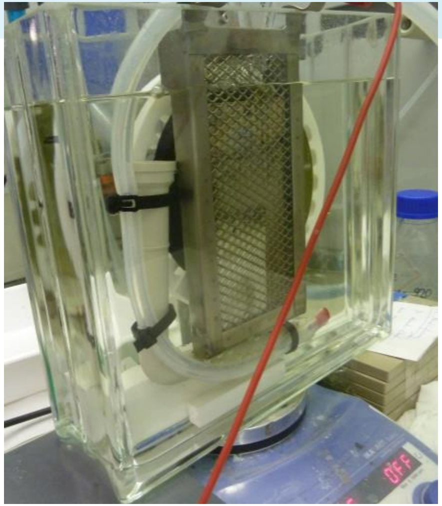
- Laboratory type setup was used
- Total of 27 4“ wafers and 14 6“ wafers were plated
  → 41 in total

Plating result

- Deposition homogeneous and reproducible on larger groups of identical solar cells

Post processing

- No thermal anneal done
- Cap etching and measurements @Azur



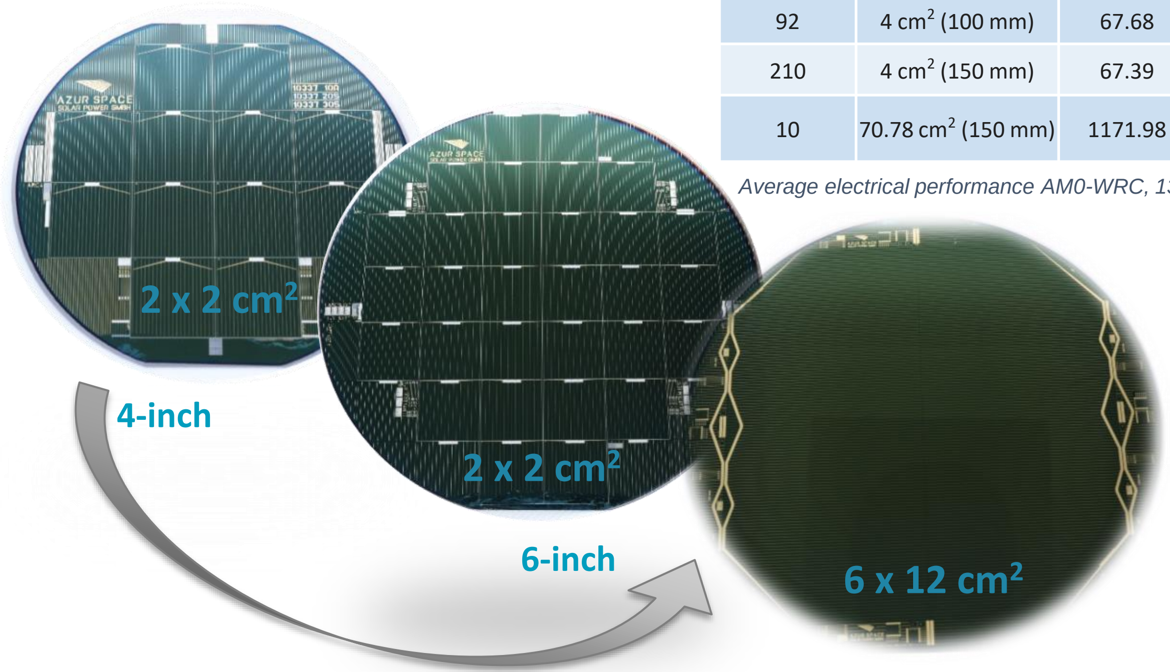
Fraunhofer ISE

Contact Metal Plating

Metal plated wafers after processing:

Quantity	Solar cell area	Isc [mA]	Voc [V]	FF	Efficiency [%]	Metal thickness [µm]
92	4 cm^2 (100 mm)	67.68	2.67	0.83	27.54	2.9 - 6.9
210	4 cm^2 (150 mm)	67.39	2.70	0.82	27.49	1.7 - 4.4
10	70.78 cm^2 (150 mm)	1171.98	2.67	0.70	22.73	1.9 - 6.6

Average electrical performance AM0-WRC, 136,7 mW/cm², 28°C



- issues with adhesion at the edge of the wafers
- metal grid thickness variations
- Tape peel test after 24 h humidity without delamination
- Optimizations about the welding process, adhesion and thickness variation necessary

Low cost anti reflection coating ARC

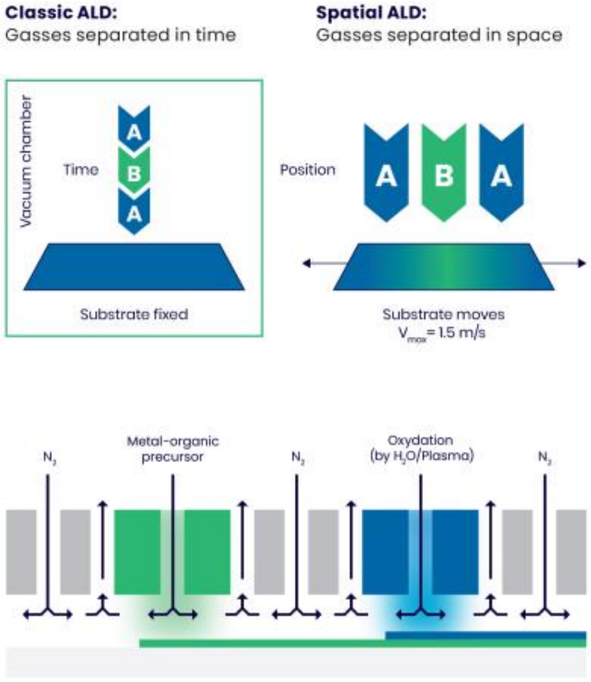
State of the art:

> At AZUR: PVD-ARC plus thermal annealing

> ALD very high uniformity, very thin layers

New Spatial ALD process:

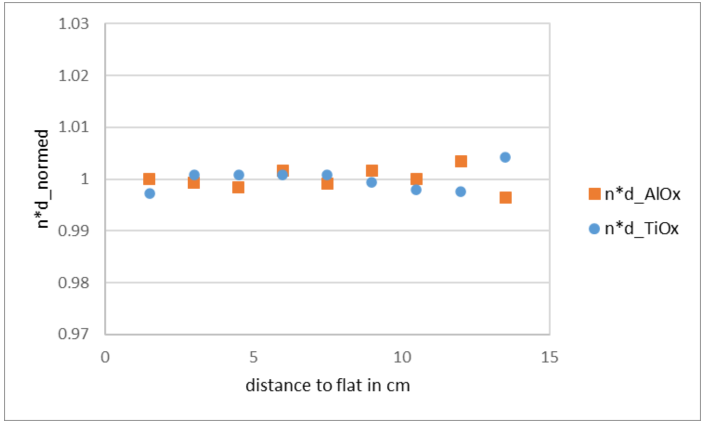
> No vacuum, high throughput, less handling
> → assuming reduced costs



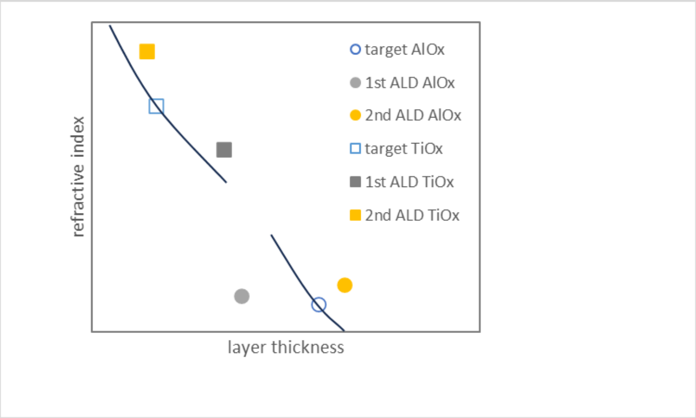
Source: SALD BV

Low cost anti reflection coating ARC

Uniformity



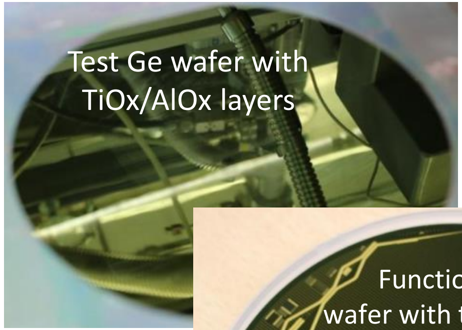
Optical Parameters

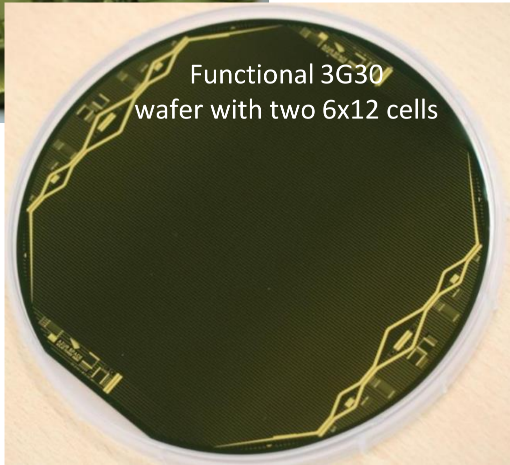


Two iterations to check/adopt parameters:

- Good adhesion on Epi, but partly issues on metal (grid/pads)
- Very uniform
- Satisfying opt. parameters not met; further experiments needed

Low cost anti reflection coating ARC





Nevertheless, one batch with 3G30 cells was tested:

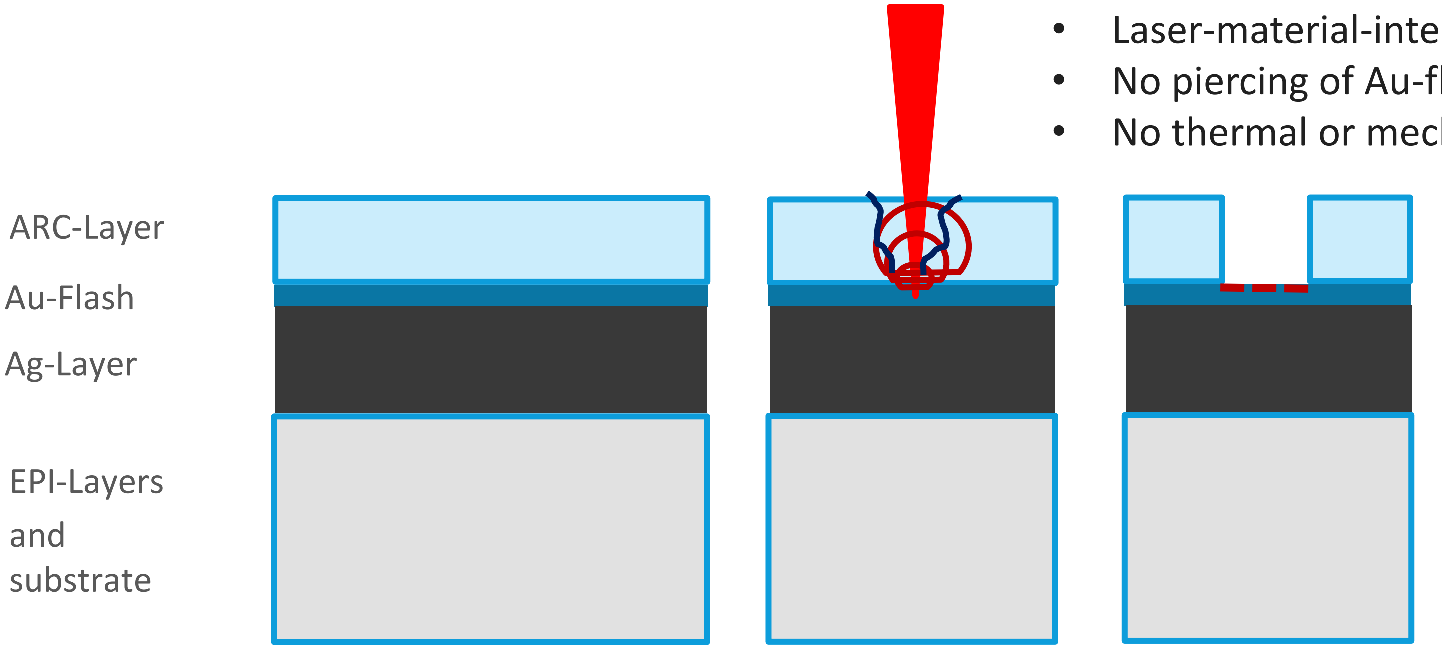
- Same processing up to ARC deposition step
- All wafers send to partner
- ALD deposition at lower and higher temperature (2 var.)
- Reference wafers got std. PVD ARC afterwards at AZUR
- Same processing after ARC deposition

LIV results:

		Isc [mA]	Voc [V]	Imp [mA]	Vmp [V]	FF [-]	eta [%]
References	median	1218	2.701	1182	2.394	0.861	29.2
(14 cells)	mean	1218	2.701	1182	2.393	0.860	29.2
	min.	1213	2.696	1179	2.383	0.856	29.1
	max.	1224	2.706	1187	2.398	0.862	29.4
ALD (low-T)	median	1175	2.698	1143	2.395	0.863	28.3
(14 cells)	Δmedian	-43	-0.003	-39	0.001	0.002	-0.9
	mean	1178	2.699	1146	2.396	0.863	28.4
	min.	1162	2.694	1130	2.388	0.859	28.1
	max.	1199	2.704	1166	2.408	0.868	28.9
ALD (high-T)	median	1188	2.702	1154	2.394	0.862	28.6
(12 cells)	Δmedian	-29	0.001	-28	0.000	0.001	-0.7
	mean	1189	2.701	1153	2.395	0.860	28.5
	min.	1180	2.696	1125	2.388	0.836	27.8
	max.	1201	2.704	1166	2.403	0.866	28.8

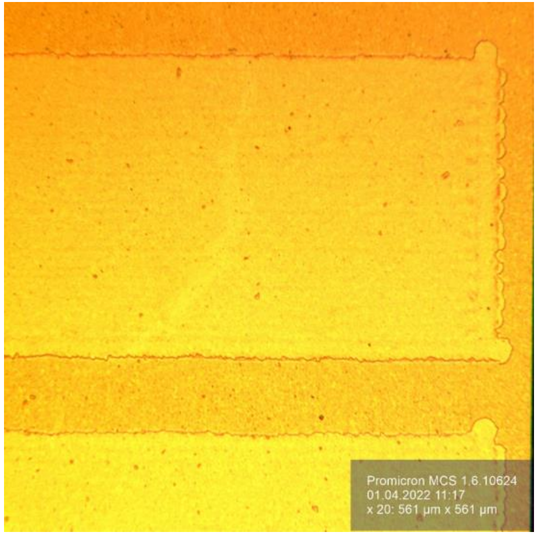
Ablation of Anti-Reflection-Coating

- ARC-Layer transparent for laser irradiation
- Laser-material-interaction below ARC
- No piercing of Au-flash
- No thermal or mechanical shock for epitaxy

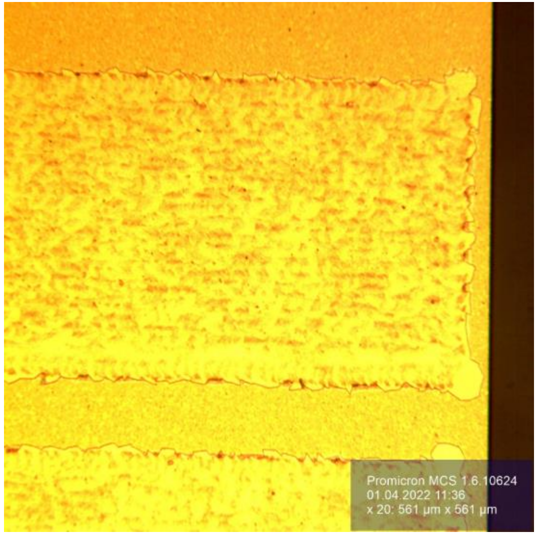


Pad opening with laser ablation

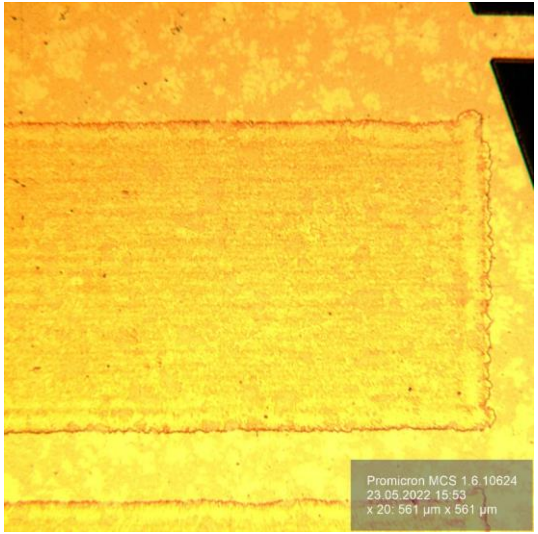
PVD before annealing process



Spatial-ALD



PVD Ag-only after annealing process



ALD-Layer is hard and leads to larger fissures in the ARC at the edge and more impact on the surface

Gold flash not pierced!

Welding and humidity tests are successful!

Laser Pad opening

State of the art:

Removal of ARC with Lithography and etching

resist → exposure → developping → etching → resist removal

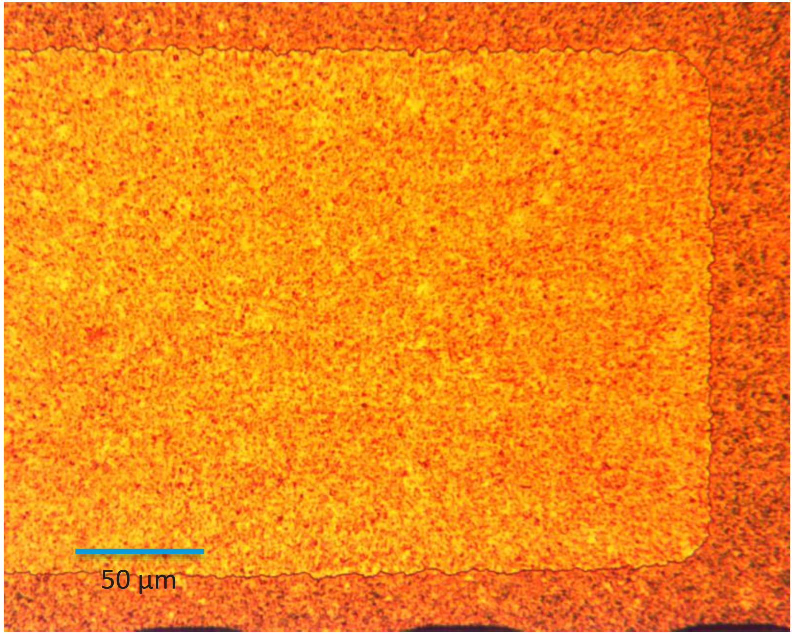
NEW: Direct Laser Ablation

could save resist, developer and enhance throughput

laser ablation → cleaning

Weldability proven for:
- Normal PVD
- ALD
- PVD after annealing
- PVD without Au-flash

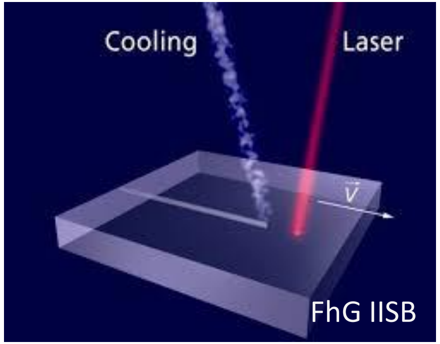
Fast due to relatively small area

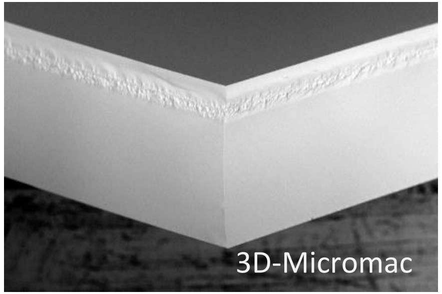


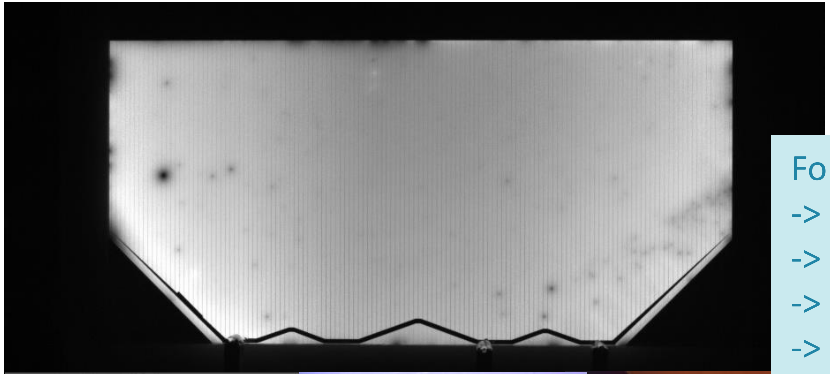
Thermal laser separation (TLS) @ FhG ISE

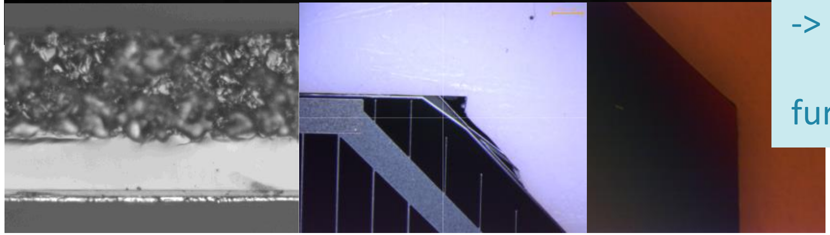
Well proven for Si-Wafers

-> adaption to Ge could substitute Dicing and Mesa









For Ge very deep grooving needed!
-> Slow process speed
-> Inhomogeneous edge
-> Deviations at Cropped corners
-> High breakage at joining
-> Some cells with 28.5 % and 29.6%

further deep development needed

Direct printing instead of photolitography

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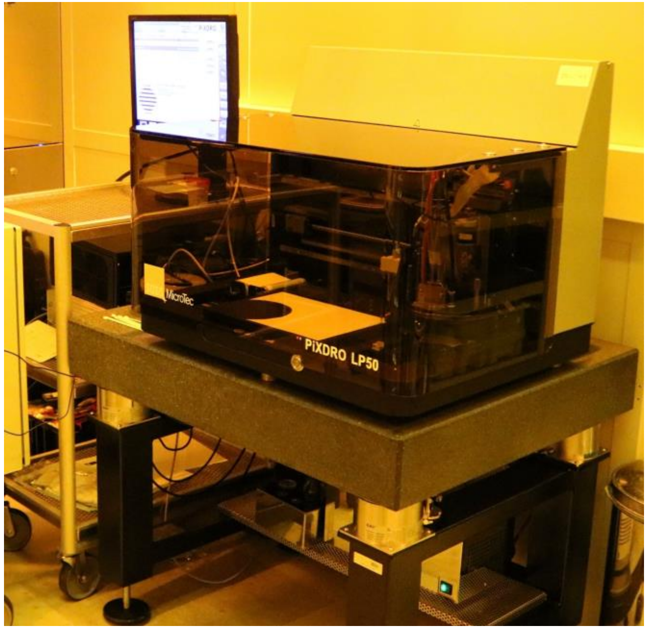
Direct printing instead of photolitography

State of the art:
Mesa-process with Lithography and etching

resist → exposure → developping → etching → resist removal

NEW: Direct Printing
could save resist, developer and enhance throughput

Resist application with direct printing → etching → resist removal

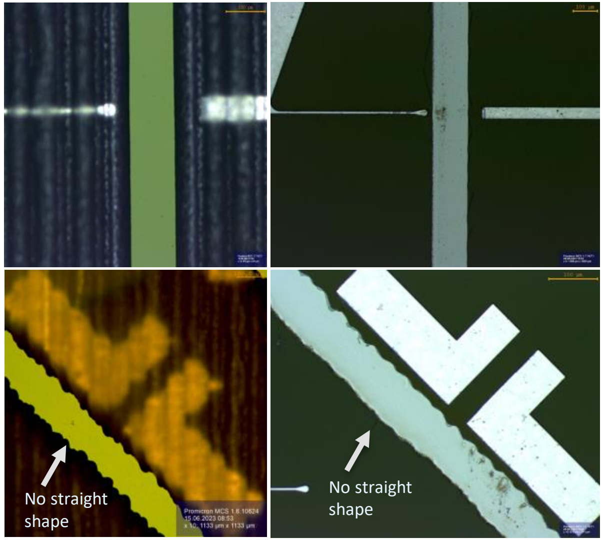


Details of the tool PixDro LP50

- LP50 Inkjet is a development tool
- Industrial print head with 256 nozzles
- Hotmelt inks consist of waxes

Direct printing instead of photolitography

- Mesa structuring with Hotmelt
  - Hotmelt patterning (left)
  - Mesa structure after etching / Hotmelt stripping (ARC / Epi / Germanium) (right)
- Printing of the Mesa line in the vertical direction has a very sharp edge
- Printing of the Mesa line in 45-degree angle to the grid has wavy edges (functionally ok)
  - The first reason is the printing resolution in the slow axis-direction
  - The second reason is because in this direction the droplets are printed wet-in-dry
- Therefore, the flow behavior is different if the Mesa line in the vertical direction and in 45-degree angle to the grid

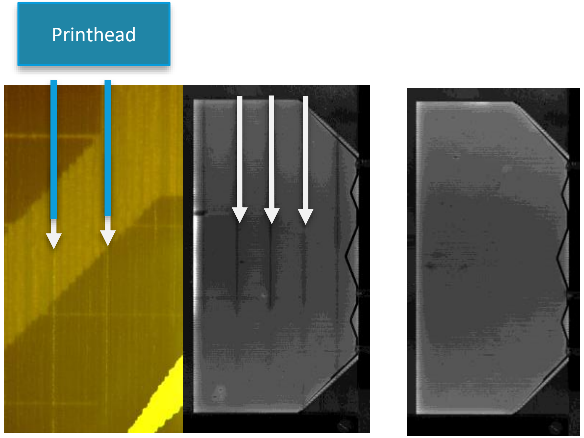


Hotmelt patterning

Mesa structure after etching / Hotmelt stripping

Direct printing instead of photolithography

- The left image shows that the inkjet mask has a periodic variation of the thickness on the stitching area due to imperfection of the printing head.
- Hotmelt lines with lower thickness have stronger appearance of pinholes that leads to the damage of the cell structure during the mesa etch process
- This effect is visible in the EL images of finished solar cells (right)
- Mesa etching with direct printed hotmelt mask successful
- An improvement of the tool (printhead) regarding resolution and alignment needed



Microscop image Hotmelt patterning

EL picture of cell

EL picture of cell w/o pinholes

Conclusion

We demonstrated the following

- ✓ A stable hotmelt that is resistant to the etching media
- ✓ The hotmelt can be removed without residues after processing
- ✓ Inkjet printing of etch masks is as an alternative to photolithography
- ✓ Inkjet printing is a suitable option for high volume production of solar cells

JETx-S inkjet printer

- ✓ With the introduction of the volume production inkjet JETx, the initial issues with the lab LP 50 printer can be greatly mitigated (wavy edges) or eliminated, respectively (pinholes etch damage and missalignment)

New cell concept

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Table of content

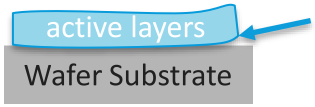
Motivation

- Germanium wafer is a remarkable cost contributor
- Availability of Germanium physically limited and can be subject of export restrictions
- III/V space solar cells are based on Ge (the use of GaAs possible but needs extensive development).

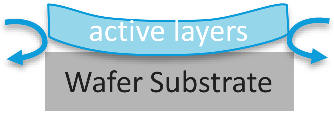
→ **substrate re-use**

Process options for substrate re-use

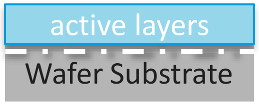
Spalling



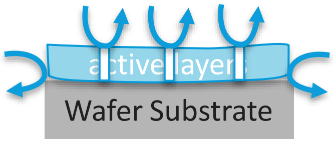
"Full-Area"
Epitaxy Lift Off (ELO)



Porous Ge



"Structured"
Epitaxy Lift Off (ELO)



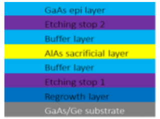
Objectives and Process flow description

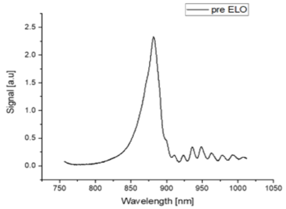
Objectives

Growing double hetero structure (DHS) on germanium substrate; structuring the wafers by wet chemical etching or by laser perforation for enabling high speed lift-off of epitaxy layers (at least 5 samples).

Process flow description

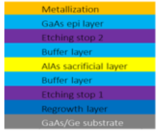
Step 1. Epitaxy wafer





PL of DHS on wafer

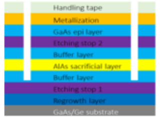
Step 2. FS Metallization



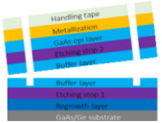
Step 3. Lamination & Structuring

a. Chemical structuring

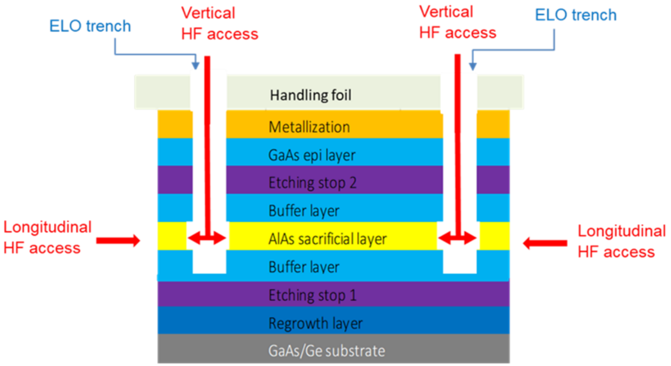
b. Laser structuring



Step 4. ELO process

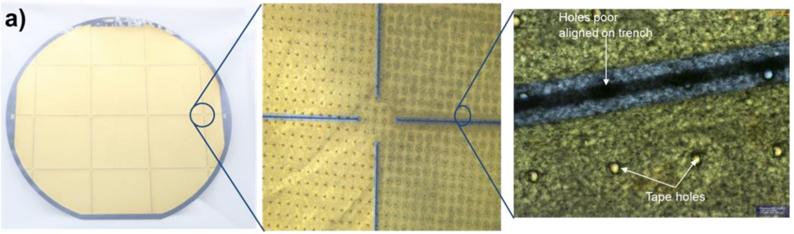


Wafer structuring and etchant access

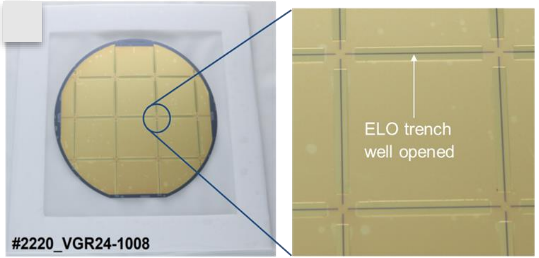


Wet chemical structuring and ELO

Lamination of wet chemical structured wafers



> Lamination: Poor alignment of laser perforated circular holes on ELO trenches

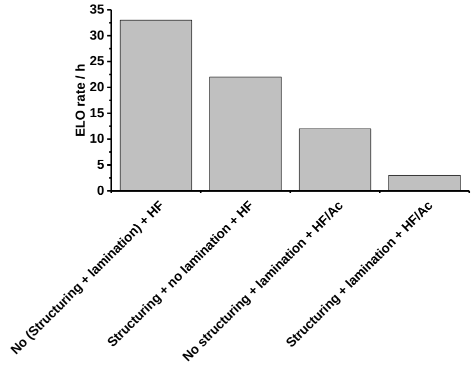


> Lamination: rectangular holes properly aligned on ELO trenches

ELOed layer on tape

ELOed layers:
ELO time 3h

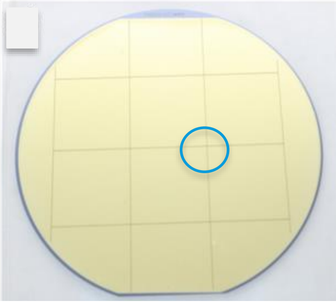
ELO rate



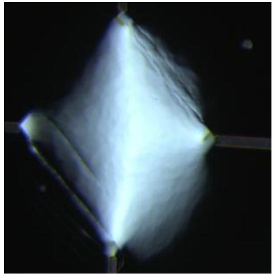
Structuring and lamination increase the ELO rate by 10 times with respect to the conventional process

Laser structuring and ELO

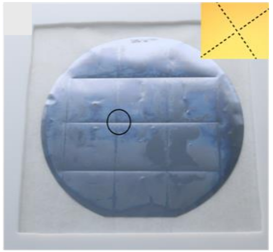
ELO tests @ AZUR

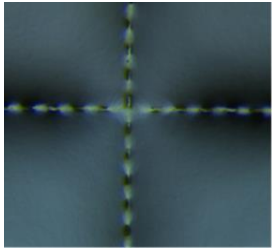


Laminated and laser structured wafer (handling tape side)



Structuring with space: micro-cracks at the trenches crossing points.



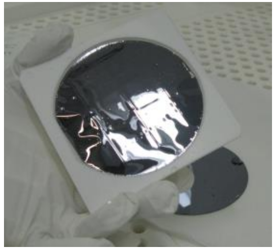


Structuring without space: No cracks at the trenches crossing points.

ELO tests @ ISE

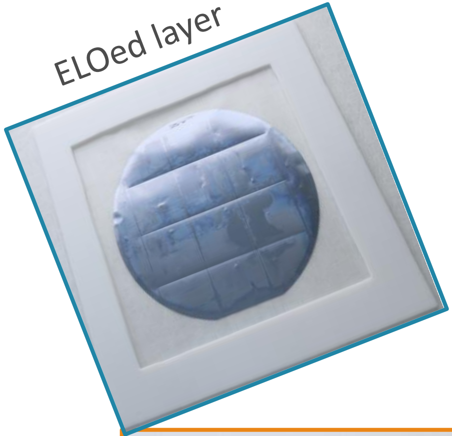
> ELO time between 5h-9h for laser structured samples

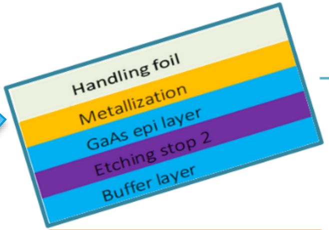
> Poor adhesion of tape observed

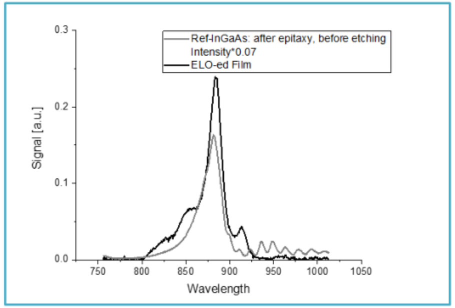


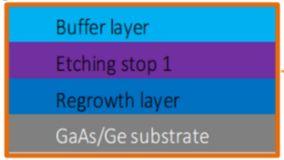
Photoluminescence analysis

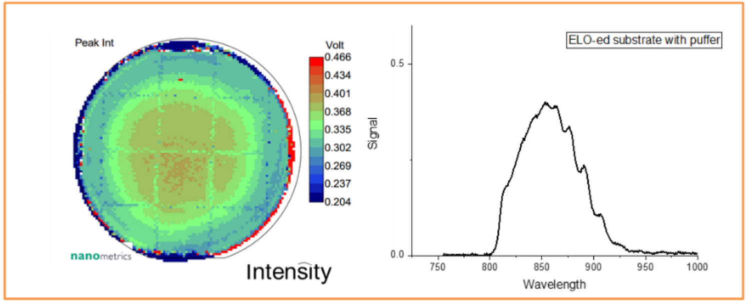
ELOed layer

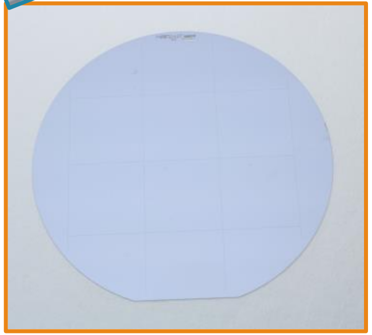








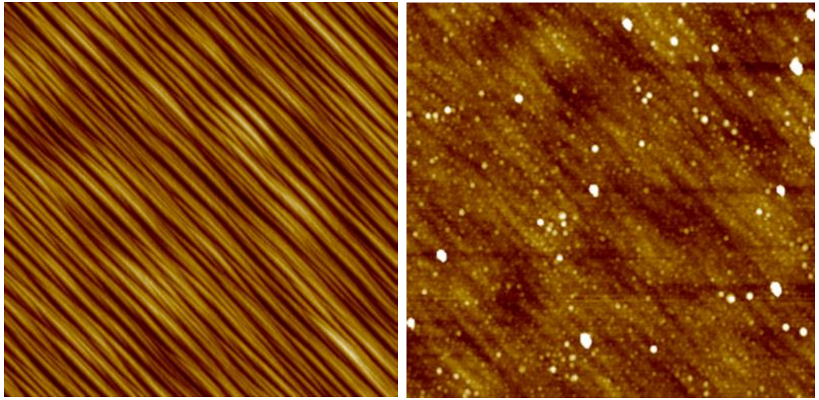




Post ELO host wafer

Substrate ReUse and Overview of ELOed layers

AFM analysis of post ELO Host wafer

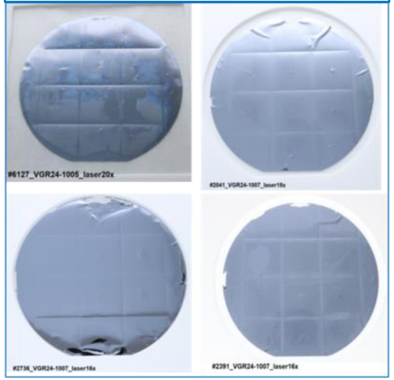


High density residual particles distribution on post ELO HW (Right); reference (left)

ELOed Layers

From chemical structured wafers

From laser structured wafers



> Overall 10 samples were ELOed

Implementation and testing

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Evaluation and Manufacturing of Hardware

WP		samples
310	EPI-Process	Dummy
320	EPI-Structure	Dummy
330	Low-Cost-Metal-Contact	cells
331	Metal Plating (ISE)	Dummy / 4“-wafers
340	Low-Cost AR	cells
350	Cost-efficient Laser Process	cells
351	TLS-Dicing (ISE)	cells
360	Direct Printing	Dummy
410	Lift-Off with substrate reuse	Dummy

4 process routes defined

Manufacturing of Hardware HW1

WP		I	II	III	IV
310	EPI-Process	-	-	-	-
320	EPI-Structure	-	-	-	-
330	Low-Cost-Metal-Contact	42	14	14	-
331	Metal Plating (ISE)	-	-	14 FS	-
340	Low-Cost AR	-	-	-	-
350	Cost-efficient Laser Process	42	14	14	-
351	TLS-Dicing (ISE)	-	-	-	14
360	Direct Printing	-	14	-	-

Route I: low risk
Route II-IV: high risk

Test plan for Engineering Tests

The following Subgroups have been defined for the tests acc. to ECSS E-ST-20-08:

- Subgroup A "Front Side Contact Adherence"
- Subgroup B "BOL Performance"
- Subgroup C "Electron Irradiation"
- Subgroup O "Extended Storage Simulation"

Engineering Test Results
Samples in the Subgroups

Variant	Description	Quantity Subgroup-A	Quantity Subgroup-B	Quantity Subgroup-C	Quantity Subgroup-O
		„FS Contact Adherence“	„BOL Performance“	„Electron Irradiation“	„Extended Storage“
I	Low risk route (w/o AU flash and laser pad opening)	**7**	**4**	**5**	**7**
II	Enhanced risk route (variant I + direct printing for mesa photo-litho)	**8**	**3**	**3**	**8**
III	Enhanced risk route (variant I + front side metal plating	**7**	**4**	**3**	**6**
IV	Enhanced risk route (TLS cutting only)	**2**	**1**	**1**	**2**

Engineering Test Results
Subgroup A “Front Side Contact Adherence”

	I_{SC} [mA]	V_{OC} [V]	P_{MP} [mW]	FF	Eta [%]
Variant I – without Au-flash / Laser pad opening					
Avg.	1227	2.72	2855	0.85	29.51
Variant II – I + direct printing					
Avg.	1229	2.72	2821	0.84	29.15
Variant III – I + plating					
Avg.	1208	2.70	2386	0.73	24.66
Variant IV - TLS					
Avg.	1237	2.72	2685	0.80	27.75

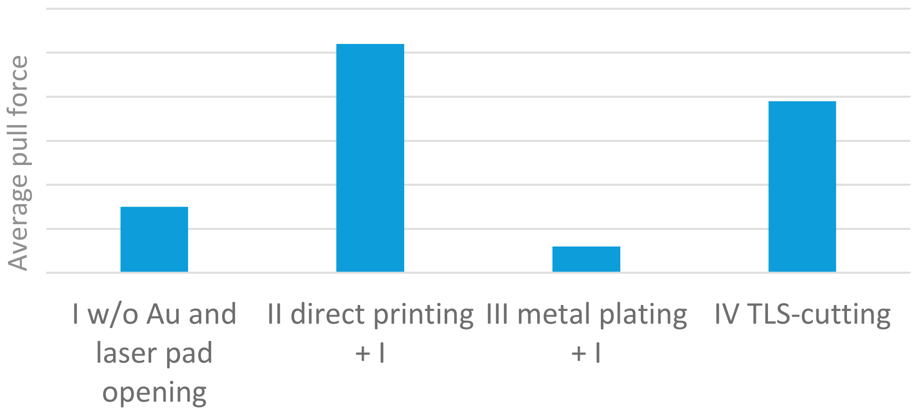
Electrical Performance

Front Side Metal Thickness reduced for plated samples in variant III.

→ Reduced Cell Performance visible in fill factor and efficiency

Shunts at the edges for variant IV TLS-cutting possible

Engineering Test Results
Subgroup A “Front Side Contact Adherence”



Pull Test Results:

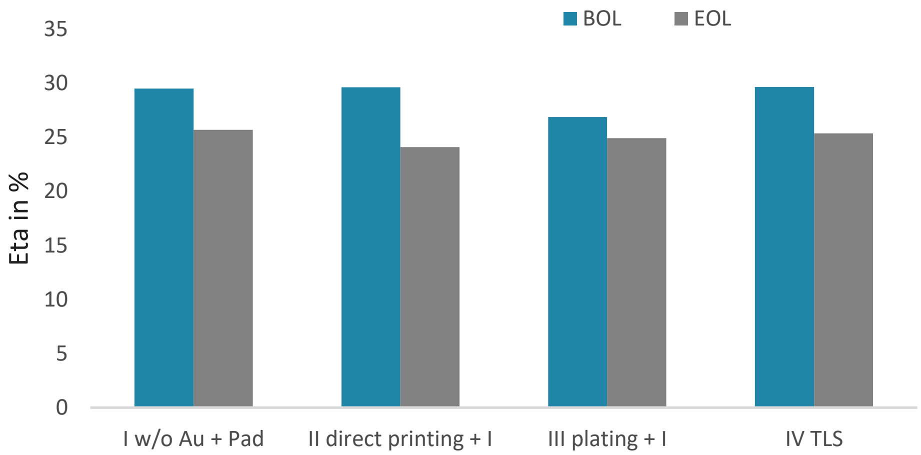
→ low values after humidity test for I observed -> storage conditions?, adaption of welding process

→ higher values after humidity test for II observed -> later manufacturing date

→ Front Side Metal Thickness reduced for plated samples in variant III
    -> adhesion of plating and welding process to be improved!

→ IV with Au, but the TLS cutting process causes cell breakage during interconnector welding

Engineering Test Results
Subgroup C “Electron Irradiation”



Electron Irradiation parameters:
1 MeV, Flux 5e11 e/cm^{2}s, Fluence 1e15 e/cm^2
Photon and Temperature Annealing: AM0, 48h, 25°C; Temperature 24h, 60°C

- Values in expected range for the used epitaxial structure
- Low loss for Variant III - plating caused by low BOL performance

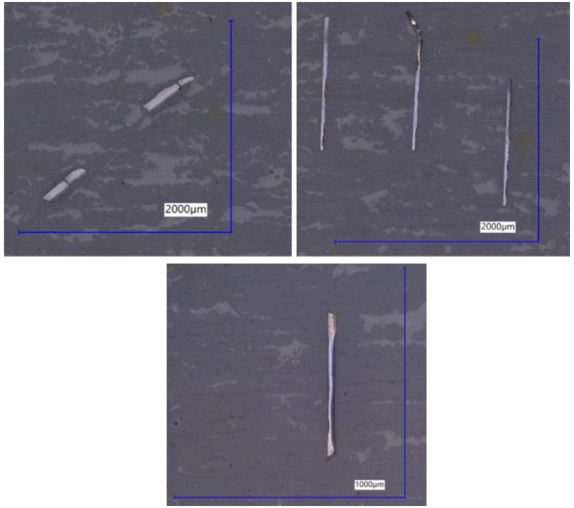
Engineering Test Results
Subgroup O “Extended Storage Simulation”

Detached Grids for
Variant III - plating

30 days Humidity test (60 °C, ≥ 90 %rH)

Thermal cycling:
- Liquid Nitrogen 20 cycles, -196 °C / 160 °C
- 500 cycles -75 °C / 160 °C

→ **Unsuspicious for Variant I and II**
→ Adherence problems within Variant III (plating)

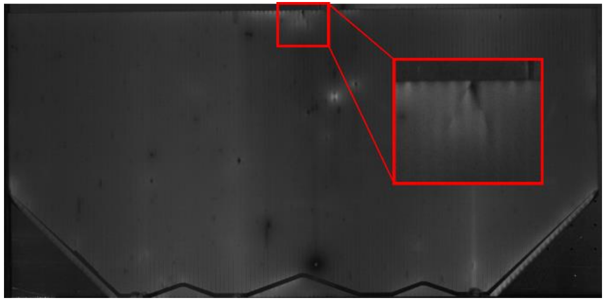


Engineering Test Results
Subgroup O "Extended Storage Simulation"

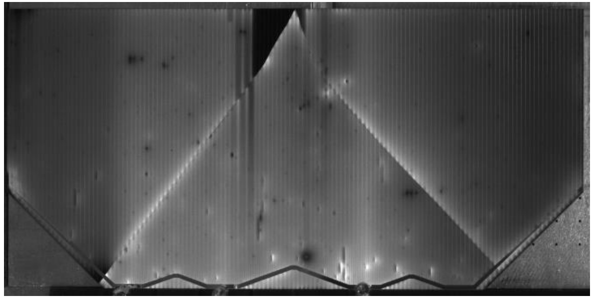
Variant IV - TLS one cell show a crack before thermal cycling

→ This results in cell breakage after cycling

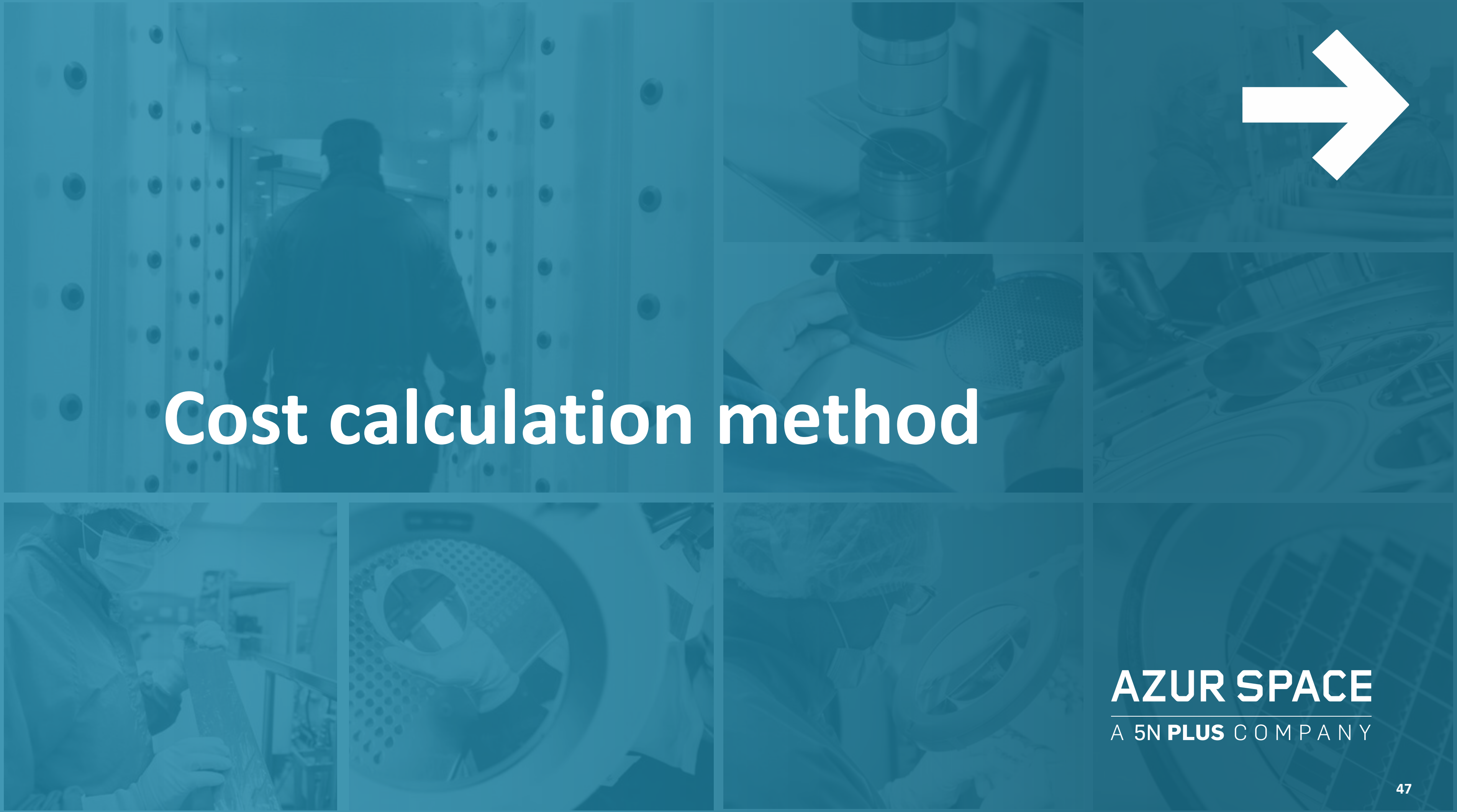
Crack before Thermal Cycling



Broken Cell after Thermal Cycling



Cost calculation method



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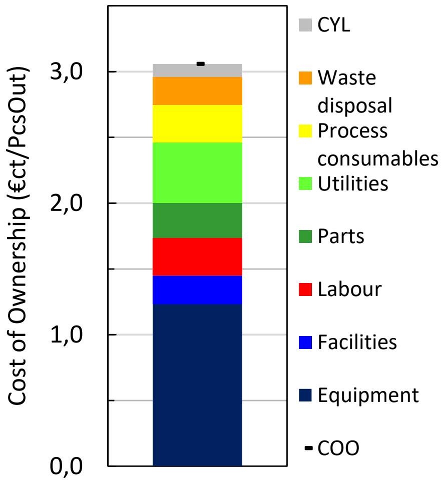
COO-Analysis of PV-Technologies with SCost
Cost elements to represent the cost of ownership of a single step

Cost

- **Equipment:**
  Production facilities and automation incl. delivery, installation, qualification, etc.
- **Building & Facilities:**
  CAPEX and OPEX of factory buildings and infrastructure
- **Labor:** Operators, Technician, Engineer, F&E-Personal
- **Parts:**
  Spare and wear parts
- **Utilities:**
  Electricity, cooling, CDA, exhaust air, DI water, …
- **Process consumables:**
  Production material solid / liquid / gaseous
- **Waste Disposal:**
  Disposal media for internal disposal as well as costs for external disposal
- **Cost of Yield Loss (CYL):** Breakage, misprocessing



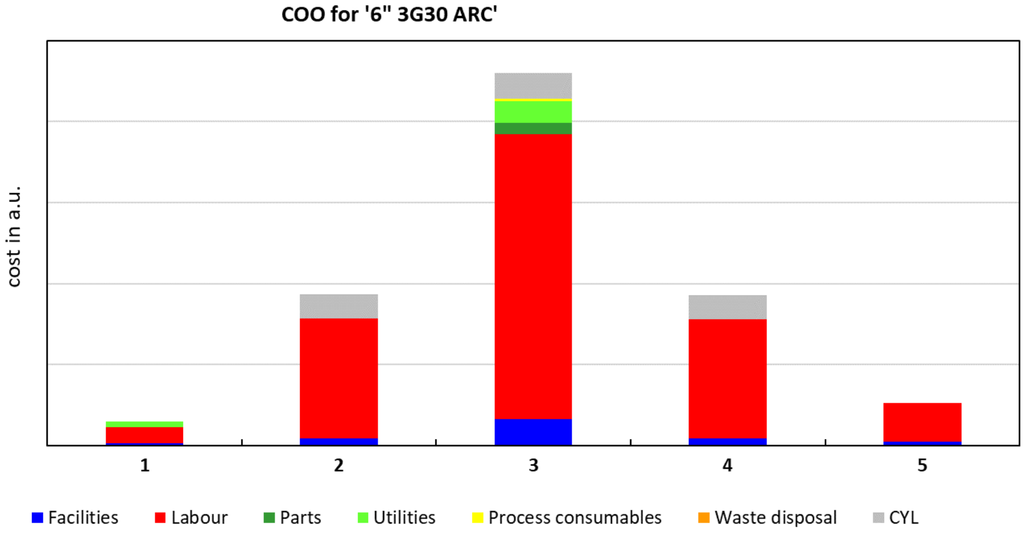
→ **Detailed recording for each production plant/module**

Simulation of new processes and process modifications possible

Fraunhofer ISE

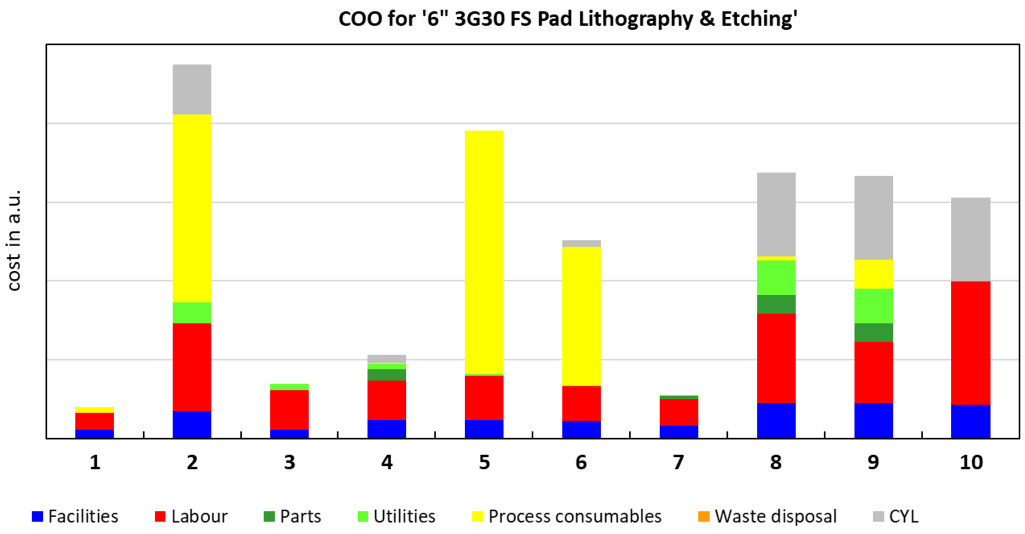
Current technology review - ARC

- ARC deposition is divided into 5 working steps (preparation, loading, process, unloading, inspection)
- Process consumable cost are not major contributors
- Cost drivers
  - Labour
    - Complex loading and unloading mechanism
    - Extensive regular maintenance



Current technology review – Pad lithography & etching

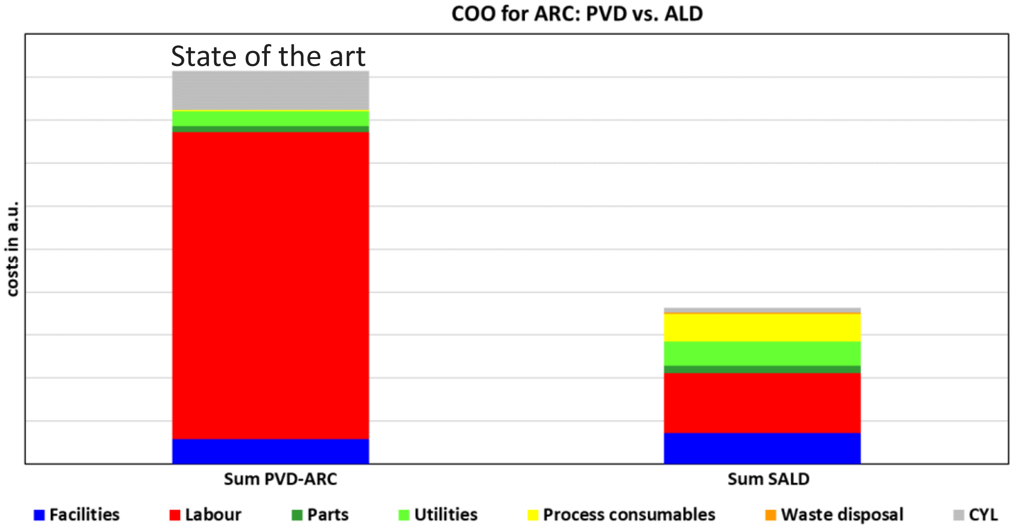
- Pad opening divided into 10 working steps
- Cost drivers
  - Labour cost
    - Many small handling steps required
  - Process consumables
    - Photoresists
    - Developer
    - Regular mask cleaning



Alternative technologies – ARC

- Updated PVD vs. SALD
- Cost reduction potential
  - Labour cost reduction due to cassette to cassette handling
  - Less extensive maintenance expected (according to supplier information)

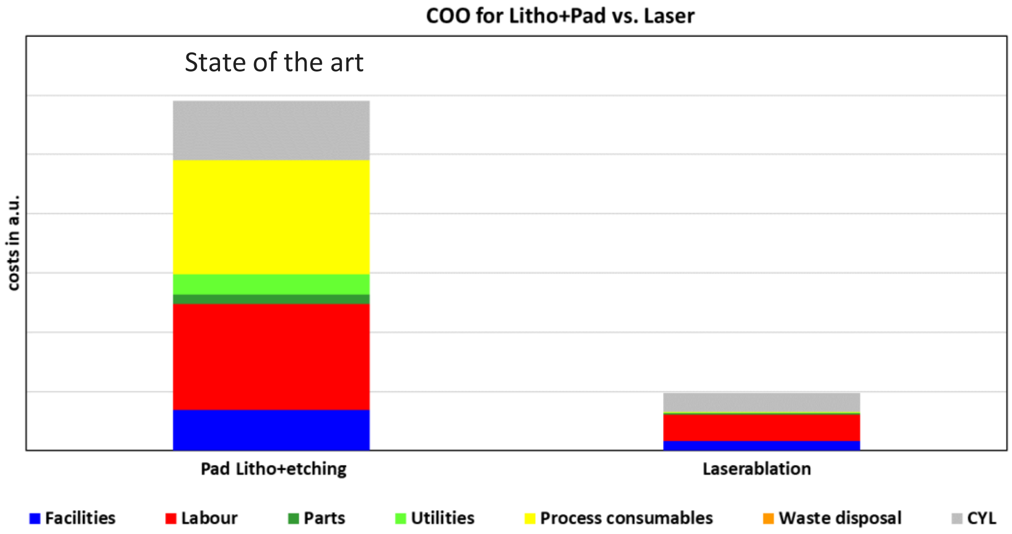
→ 0.7% of total production cost



Alternative technologies – Pad opening

- Updated Pad Litho&etching vs. Laser
- Cost reduction potential
  - No process consumables
  - Lower footprint
  - Less labour cost
    - Far less production steps

  → 2.7% of total production cost



Summary and Outlook

	Cost saving potential
EPI-Process	n.a. (approx.. +4.0 %)
EPI-Structure	n.a.
Low-Cost-Metal-Contact	2.9%
Metal Plating (ISE)	n.a. (approx.. +2.3 %)
Low-Cost AR	0.7 %
Cost-efficient Laser Process	2.7 %
TLS-Dicing (ISE)	2.5%
Direct Printing	1.6 %
Sum cost saving potential: without substrate re-use	Up to 15.1 %

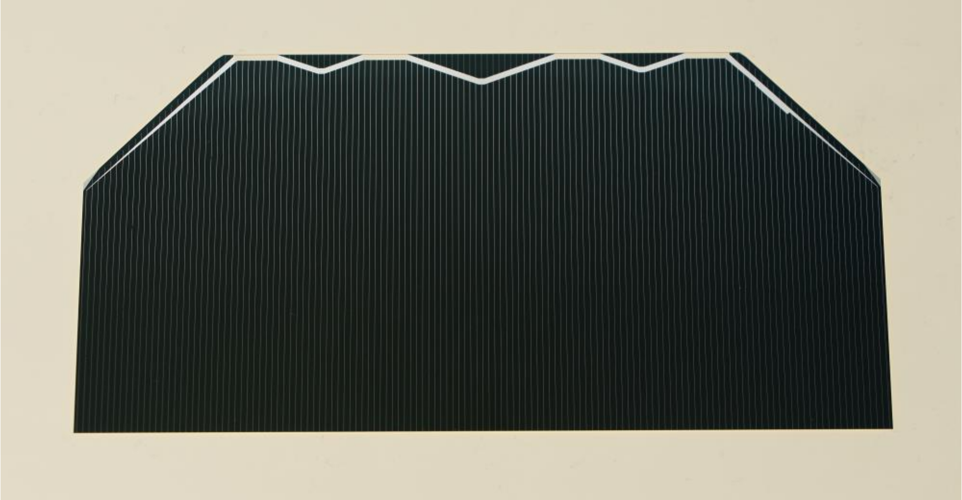
CoffeTaSS
Final Evaluation

WP			
310	EPI-Process	Further development and introduction under planning	✓
320	EPI-Structure	Improvement could not be demonstrated	
330	Low-Cost-Metal-Contact	Limitations in pull-test, further activities in storage conditions or joint process – implementations with lead customers in planning	✓
331	Metal Plating (ISE)	Limitations in conductivity, adhesion and pull-test, further technology development needed	
340	Low-Cost AR	Basic process not stable enough	
350	Cost-efficient Laser Process	Limitations in combination with WP330 – implementation with lead customers in planning	✓
351	TLS-Dicing (ISE)	High breakage – not applicable in current version – intense redesign of machine and process needed	
360	Direct Printing	Limitations in coverage – process optimisation at new industrial tool	✓

CoffeTaSS
Summary and Outlook

Project summary
- 33 months (24 planned)
- 16 Working packages / 20 WP-Leader
- Hardware with 4 split routes manufactured
- Engineering Tests at 168 cells (6x12)
- Potential of cost saving up to 15.1 % confirmed

Follow on activities
- Implementation of specific improvements at pilot customer projects in planning
- Further R&D about ELO in projects running



Thanks to all involved colleagues and partners!

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