DRIFT

Differential RadiatIng FronT-end for DRA telecom applications in K-band
(ESA Contract No. 4000136725/22/NL/MGu)

Deliverable FR

Final Report

Customer:	The European Space Agency (ESA)
Customer Reference:	4000136725/22/NL/MGu
Document Name:	Final Report
Submission Date:	1st Dec 2024
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1.1. ACRONYMS AND ABBREVIATIONS

AD	Applicable Document
ECSS	European Cooperation for Space Standardisation
ESA	European Space Agency
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HPA	High Power Amplifier
IM3	3rd order intermodulation
MIM	Metal-Insulator-Metal (capacitor)
MMIC	Monolithic Microwave Integrated Circuit
MPW	Multi-project Wafer (run)
NOP	Nominal Operating Point
NPR	Noise to Power Ratio
OBO	Output power Back-Off
PAE	Power Added Efficiency
Pavs	Available Source Power
PCB	Printed Circuit Board
PDK	Process Design Kit
RD	Reference Document
RF	Radiofrequency
SoW	Statement of Work
Ta	Ambient temperature
TBC	To Be Confirmed
TBD	To Be Determined
TNO	Netherlands Organisation for Applied Scientific Research
WG	Waveguide
WP	Work Package

1.2. APPLICABLE DOCUMENTS

[AD-1] ESA Statement of Work “DIFFERENTIAL RADIATING FRONT-END FOR DRA TELECOM APPLICATIONS IN K-BAND - EXPRO PLUS” ESA-TEC-TDE-SOW-023321, rev 1.1, 09/06/2021

[AD-2] Proposal in response to ESA ITT AO/1-10761/21/NL/MGu, “DIFFERENTIAL RADIATING FRONT-END FOR DRA TELECOM APPLICATIONS IN K-BAND", TNO-OFF-2021-1006930

[AD-3] 4000136725/22/NL/MGu_D1_Reference_Architecture_FE_Requirements_Report.docx”.

[AD-4] 100342979 - MOM Contract negotiation reference ESA_2022-01-28

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2. Introduction

2.1. Scope

This final report is the output of Task 203: “Ka-band differential radiating front-end evaluation and technology roadmap” of the project “Differential radiating front-end for DRA telecom applications in K-band”, according to ESA Statement of Work [AD-01].

2.2. Document outline

The Final Report shall provide a complete description of all the work done during the activity and shall be self-standing, not requiring to be read in conjunction with reports previously issued. It shall cover the whole scope of the activity, i.e. a comprehensive introduction of the context, a description of the programme of work and report on the activities performed and the main results achieved.

Context – background / project’s objective

Program – detail the work SoW
Activities – What was done
Results - Results

This document describes the DRIFT demonstrator assembly steps that have been performed on the PCB assembly, heat sink attachment, differential HPA MMIC and diecap attach and bonding and finally integration with the Waveguide. In addition, assembly details of the passive waveguide exciter and HPA test structure are included. For reference the design of the HPA is reported in [2]. Goal of this assembly and integration report is to provide an overview of the steps required to get to the final demonstrator.

3. Context

3.1. Background

Satellite communication system evolution is trending towards a growing demand for higher data throughput and flexible traffic allocation. Satellite communications services are evolving to meet these demands. Currently, Very High Throughput Systems increase capacity by:

- Allocating almost the full spectrum at K-band for the user-link.
- Using larger antennas to generate a higher number of smaller, fixed beams.

However, flexibility in coverage has become increasingly important to support long-term traffic evolution over the satellite's lifetime. This includes providing hot spots for occasional traffic peaks and market testing of new missions. The flexibility of multi-beam active antennas is pivotal in addressing these demands, allowing enhanced frequency reuse and efficient capacity allocation. Additionally, active arrays inherently improve linearity via intermodulation dilution, enabling HPAs to operate at higher compression levels, thereby enhancing efficiency.

Furthermore Direct Radiating Arrays (DRAs) offer transformative potential by enabling satellite data services akin to terrestrial cellular networks, operating primarily in Ku and K/Ka bands. Active Direct Radiating Arrays (DRA) are an efficient solution for reconfigurable multibeam transmit antennas as they offer:

- Power exchange among beams amplified by the same High Power Amplifiers (HPAs).
- Distributed amplification across numerous low-power MMIC HPAs.
- High reliability due to graceful degradation, avoiding cold redundancies.
- Increased downlink capacity per user in the beam.
- Higher G/T of the return link.

The realization of efficient active DRAs, containing hundreds to thousands of active radiating elements, requires major innovations, particularly in High Power Amplifier (HPA) Monolithic Microwave Integrated Circuits (MMICs) and HPA-antenna transitions. Despite progress in recent years, especially in K/Ka-band HPA design influenced by 5G developments, a novel approach to HPA-antenna integration is essential to optimize the trade-offs among power, linearity, efficiency, and polarization discrimination.

While significant progress has been made in HPA design and antennas at K/Ka band (driven by 5G activities), developing a new approach to the HPA-antenna transition is essential. This is crucial to achieve ultimate performance levels in terms of power-linearity-efficiency trade-off and polarization discrimination.

Advances in enabling technologies such as III-V semiconductor technology underpin high-performance DRAs, facilitating MMICs with RF outputs of several Watts up to Ka-band. Key enablers of high-performance DRAs include:

- HPA MMIC efficiency.
- Low-loss interconnects between the devices' output and the antenna structure.

A promising approach involves differential topologies to reduce on-chip losses by integrating power-combining structures directly within the coupling between MMICs and waveguides. This strategy enhances MMIC output power and linearity while supporting trade-offs to meet system requirements.

Achieving optimal system performance requires minimizing losses through efficient MMIC design and integration. The design process of active antenna elements must consider both MMIC design and various integration aspects. To achieve the high output powers required for DRA elements, MMICs must combine the power of multiple transistor cells at their output. On-chip combining networks, a source of inherent losses in any power amplifier MMIC, can be reduced by employing a differential topology for the active circuitry. This allows power combination directly through the coupling structure between the MMIC and the waveguide, instead of on the MMIC itself, resulting in higher output power.

High Throughput Satellites (HTS) exemplify the shift in satellite communications, delivering up to 20 times the throughput of traditional Fixed Satellite Services (FSS) systems. Emerging applications, such as IoT connectivity and 5G network extensions, drive this growth. Future systems will increasingly leverage DRAs for reconfigurable multibeam coverage, addressing diverse needs like evolving traffic patterns, "hot spots," and new market testing.

Innovations in DRAs and associated satellite technologies are critical to achieving the flexibility, efficiency, and scalability required for modern SATCOM systems, ensuring they meet emerging demands and long-term operational goals. This ongoing evolution underscores the vital role of DRAs in advancing satellite communications.

3.2. Project's Objective

The project's objective is to develop, manufacture and demonstrate by means of test a highly efficient differential radiating front-end for Ka-band satellite downlink, in a compact stand-alone unit.

This is to be achieved by first designing a high power, high efficiency and high linearity MMIC as a baseline for the activity. The MMIC should not be using on-chip power combining structures and have a single-ended interface at the input and a differential interface at its output. A low-loss MMIC to waveguide transition should ensure an efficient power coupling into the waveguide. Preferably, the MMIC to waveguide transition should take over part of the output matching functions to further reduce the overall RF losses after the final transistor stage. The final building block to design is the antenna, which has to be low-loss, support the differential feeding and preferably a polarisation switching. To verify the performance of the different building blocks, test structures have to be designed that allow the evaluation of the performance of the different building blocks.

In the summary the main objectives of the tendered activity are:

- Design of a high power, high efficiency and high linearity differential MMIC HPA;
- Design of a low-loss MMIC-to-waveguide transition;
- Development of the final building block, which should support differential feeding and preferably have polarisation switching;
- Demonstration of performance of developed concepts through manufacturing and testing of the building blocks, particularly with respect to loss and polarization discrimination.

At the end of the activity, a manufactured and fully assembled BB unit is to be delivered that is demonstrating compliance with the requirements through testing. The current TRL is estimated to be 2, the activity target is to achieve TRL 4.

4. Program of Work

4.1. Consortium

TNO will lead this project and will be supported in the requirement consolidation, technology review and road-mapping by Thales Alenia Space France (TAS) and by Altum RF.

TAS is one of the major large system integrators of SATCOM RF payloads and has significant experience in the Active Antenna design and development. Since more than 25 years, with more than 110 Active or Reconfigurable Antennas (from L to Ka band) TAS is delivering for Commercial and Military markets. Their experience makes TAS the ideal partner for TNO to develop a novel integrated active radiating element for such systems.

Altum RF is a Netherlands-based fabless semiconductor SME. It was founded in 2018 by a team of industry 'veterans' with successful track records with NXP, MACOM, ADI/Hittite. For the SATCOM communication market, Altum RF is developing a family of GaAs and GaN amplifiers. In 2020, Altum

4.2. Project's Work Breakdown Structure

The work breakdown structure follows the Statement of Work [AD-1] issued by ESA. The project is broken into 6 work packages, which are given in more detail in Table 4.1 including duration and WBS responsible party.

Table 4.1 Work breakdown structure

WP	SoW Task	Description	Start date (Months)	End date (Months)	Responsible
WP0	-	Project management	T0	T0 + 24	TNO
WP1	101	DRA architecture consolidation, DRA antenna element requirements derivation and technology view	T0	T0 + 3	TNO
WP2	102	Preliminary design and analysis	T0 + 3	T0 + 5	TNO
WP3	103	Detailed design and analysis	T0 + 5	T0 + 12	TNO
WP4	201	Manufacture and assembly of the differential radiating front-end	T0 + 12	T0 + 18	TNO
WP5	202	Testing of the radiating front-end(s)	T0 + 18	T0 + 22	TNO
WP6	203	K-band differential radiating front-end evaluation and technology roadmap	T0 + 22	T0 +24	TNO

TNO will lead the project though parts of the work in the WP1.1 to TAS and part of WP1.2 to Altum RF will be subcontract. All subcontractors will contribute to WP6. The remaining tasks of the project will be covered by TNO, with support from the Subcontractors, where necessary.

4.3. Project's Work Logic

The project's work logic can be seen in Figure 4-1. The project has 2 distinct phases: a design phase (Phase1) and build and test phase (Phase 2). Phase 1 details the system requirements, the preliminary and critical design phases. Altum RF will perform the Technology review and TAS will perform the requirements analysis is WP 1.1 and WP 1.2. Phase 1 will conclude after a successful Critical Design Review (CDR).

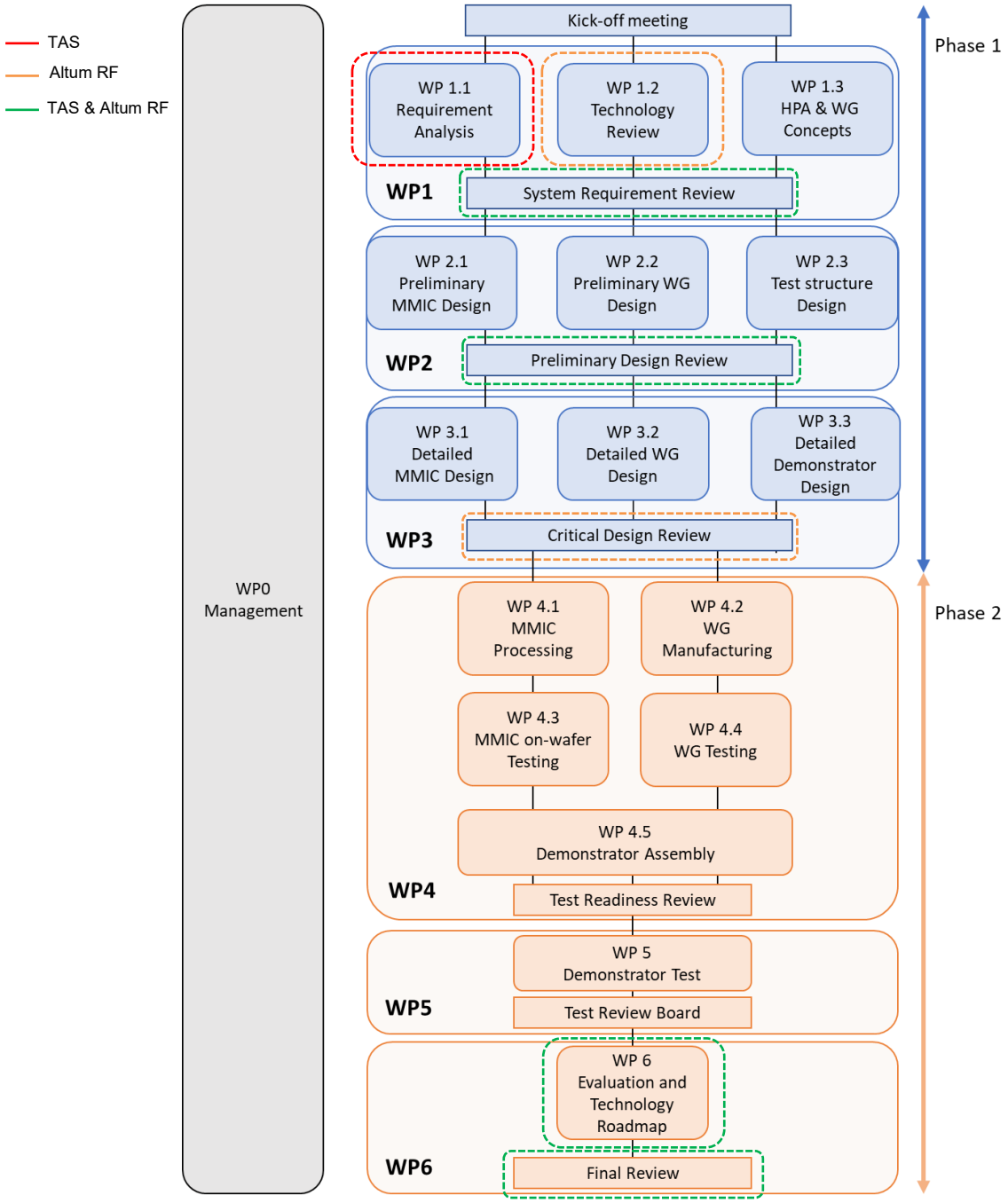


Figure 4-1 project's workflow.

Phase 2 details MMIC fabrication, PCB and wave guide manufacturing and demonstrator assembly and test. Phase 2 will conclude after a successful Final Review (FR), which shall address all of the project's specification points as detailed in section **Error! Reference source not found.**.

4.4. Project's milestones

Table 4.2 shows the schedule and milestone plan along with estimated dates and locations. The Reviews will be organised in accordance with Section 4.3 'Reviews' section of the SoW [AD-1]. Progress meetings between TNO and ESA: Interval scheduling of progress meetings will be in accordance with the SoW. The progress meetings will be held at ESA premises or by teleconference.

Table 4.2 Schedule and milestone plan.

Meeting description	Milestone	Period	Location
Negotiation			ESTEC
KO	Start	T0	Teleconference
SRR	End of Task 101	T0 + 3	Teleconference
PDR	End of Task 102	T0 + 5	ESTEC
CDR	End of Task 103	T0 + 12	Contractor's premises
TRR	End of Task 201	T0 + 18	Teleconference
TRB	End of Task 202	T0 + 22	Teleconference
FRe	End of Task 203	T0 + 24	ESTEC

In addition to the formal reviews and progress meetings with the ESA, TNO will perform internal meetings to ensure technical and programmatic progress. Working meetings to discuss actual technical issues will be held at all levels within the project when deemed useful or necessary. The working meetings will also take place as tele/videoconferences where possible between TNO, TAS and Altum RF. ESA will have the right to attend any of the above meetings after informing TNO in advance of its intention to participate.

4.5. Deliverable items

This section presents the deliverable items in terms of documents, hardware, and software. Table 4.3Table 4.3 illustrates all deliverable documents cross referenced against its SoW DI, which WP it belongs to and the milestone. Table 4.4 highlights all deliverable hardware and software cross referenced with its milestone and quantity.

Table 4.3: Overview of document deliverables.

DI	Document	WP output	Milestone
D1	Reference architecture and front-end requirements report	WP1	SRR
D2	Technology survey report	WP1	SRR
D3	Baseline design report	WP2	PDR
D4	Test plan	WP2	PDR
D5	Detailed design report	WP3	CDR
D6	Integration and assembly process report	WP3	CDR
D7	Critical component manufacture and test report	WP4	TRR
D8	Assembly and integration report	WP4	TRR
D9	Test results of K-band radiating front-end(s)	WP5	TRB
D10	Activity evaluation and development plan	WP6	FR
D11	Inventory and asset record	WP0	FR
PH	Photographic documentation	WP0	FR
Photo	High resolution pictures	WP0	FR
TDP	Technical data package	WP0	FR
AB	Abstract	WP0	FR
TAS	Technology achievement summary	WP0	FR
FP	Final presentation	WP0	FR
SR	Summary report	WP0	FR
ESR	Executive summary report	WP0	FR
FR	Final report	WP0	FR
OCD	Contract closure documentation	WP0	FR

Table 4.4: Overview of hardware and software deliverables.

HWID	Deliverable	Milestone	Quantity
HW1	Breadboard(s) of key building block(s) with critical functions and interfaces	FRe	TBD
HW2	MMIC Samples run 1 (10 functional samples of each circuit type)	FRe	10
HW3	MMIC Samples run 2 (10 functional samples of each circuit type). Applicable only in case or MMIC re-design.	FRe	10
HW4	K-band radiating front-end demonstrator	FRe	1
SW1	Simulation files (MMICs, package, radiating elements) from Task 102	FRe	1
SW2	Manufacturing files (GDS, step) from Task 102	FRe	1
SW3	Simulation files (MMICs, package, radiating elements) from Task 103	FRe	1
SW4	Manufacturing files (MMICs, package, radiating elements) from Task 103	FRe	1

4.6. Baseline project plan

The initial project plan duration was 2 years. The project's T0 date was in 10/03/2022. The project was initially divided into roughly 1 year design phase and 1 year build and test. The baseline project plan can be seen in Figure 4-2.

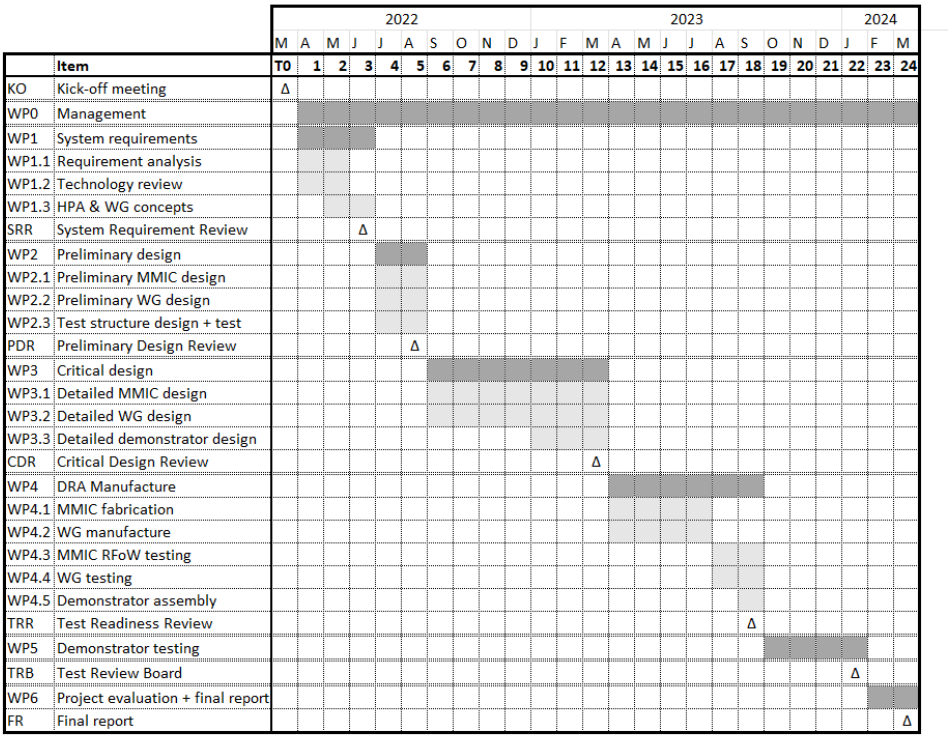


Figure 4-2 DRIFT baseline project plan

DRIFT Actual project timeline

		2022										2023												2024										
		M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D
	Item	**T0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**
KO	Kick-off meeting	Δ																																	
WP0	Management																																		
WP1	System requirements																																		
WP2	Preliminary design																																		
WP3	Critical design HPA																																		
																	Δ																		
WP3	Critical design WG																																		
CDR	WG Critical design																										Δ								
WP4	DRA Manufacture																																		
WP4.1	MMIC fabrication																																		
WP4.2	WG manufacture																																		
WP4.3	MMIC RFoW testing																																		
WP4.5	Demonstrator assembly																																		
TRR	Test Readiness Review																																Δ		
WP5	Demonstrator testing																																		
TRB	Test Review Board																																		Δ
WP6	Project evaluation + final report																																		
FR	Final report																																		Δ

Figure 4-3 DRIFT actual project timeline.

Project DRIFT had in total 9 months of delay as shown by Figure 4-3. The reasons for the project delay will be described. The project's work was divided into 2 technical blocks: HPA and Waveguide design. The HPA work package realised the critical design review with 2 months delay. The reason for the delay is mainly attributed to the wafer fabrication run. As the project didn't have sufficient funds to purchase its own wafer run. Project DRIFT occupied space on another's TNO project wafer run which was scheduled to run in July 2023. All remaining HPA activities have been executed as per the plan.

The waveguide design is where most of the 9 months project delay was realised. The waveguide design is broken into 2 sub blocks: waveguide feed and waveguide design. The initial preliminary waveguide feed and waveguide design approach resulted in a unsatisfactory RF loss and a long PCB lead time from manufacture ACB (14 weeks), which resulted in the DRIFT team having to re-think their waveguide design approach. The unplanned redesign of the waveguide feed, including its design, build, and testing, had to be repeated. This resulted in a total delay of 8 months from the initially planned PDR date to the actual date. However, the impact of the delay was mitigated by the HPA MMIC wafer run, which had a long lead time of 4 months.

Further delays where realised in the DRIFT demonstrator assembly in preparation for the test readiness review (TRR). The accumulation of delays lead to the TRR being held 12 months after the baseline date. The redesign activities and delays resulted in project budgetary pressure and required some testing activities to be removed which has led to a total project delay of 9 months. The final review is scheduled for the 13/12/2024.

5. DRIFT Design Phase

This section will detail all activities within the project's 1st phase (system definition and design phases). The major headings are sub divided as per their major milestone.

5.1. System's Requirement Review (SRR)

The system requirements consists of 3 sub work packages: WP1.1 system requirements, WP1.2 and WP1.3

5.1.1. Requirement Analysis (WP1.1)

TAS identified that an active array antenna for the GEO-satellite in Ka-Band would best suit a secondary mission, complementing the main mission covering regions like Europe and CONUS4 with fixed broadband beams. This secondary broadband Multimedia mission in Ka-Band could offer an extra capacity, power exchange among the beams and coverage reconfigurability over the full Earth.

The secondary mission aims to provide additional, flexible capacity to extend beyond the main coverage:

- The main mission offers fixed, uniform geographic capacity with fixed beam positions, bandwidth, and power.
- If demand exceeds a beam's capacity, the secondary mission can provide extra capacity by directing steerable spot beams to the high-demand region, using an active DRA for flexibility in coverage and power allocation.

Advantages of using active DRAs (one for transmit, one for receive) include:

- Accommodation on the spacecraft Earth deck, complementing main Rx/Tx reflector antennas.
- Ability to scan multiple spot beams globally with a single antenna, without pointing.
- Flexible power allocation among steerable spot beams, limited only by the HPA's maximum output power, avoiding oversizing to match traffic variations.

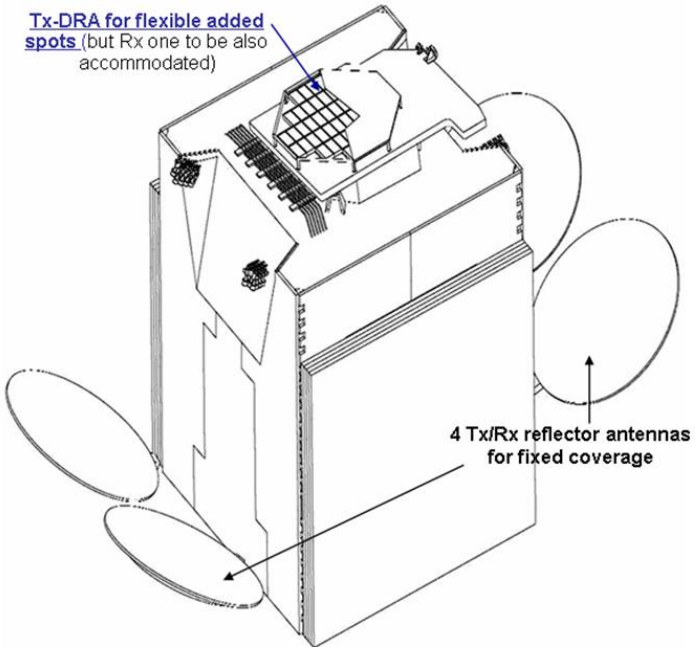


Figure 5-1: Example of combining 4 'SFB' reflector antennas on East-West walls, and a DRA on Earth panel

A phased array definition is necessary to specify the critical parameters for the differential front-end radiating module (FERM) and especially the definition of the FERM demonstrator to be built. The following areas where evaluated for the phased array definition are:

- the array lattice choice and dimension, concluding:
  - Hexagonal lattice
  - Scanning angle 8.7° and array lattice distance 3.5λ
- the radiating element directivity, concluding:
  - Radiating directivity > 20.1dBi
- the dimension of the phased array, concluding:
  - 256 circular horns with a hexagonal lattice and the array's diameter is 885 mm.

Transmit phased array antenna frequency reuse scheme and amplitude distribution

Due to the wide bandwidth 2900MHz, and the possibility to share the bandwidth between the beams, we have retained a frequency reuse scheme of 7 colors as illustrated in figure 4.8.

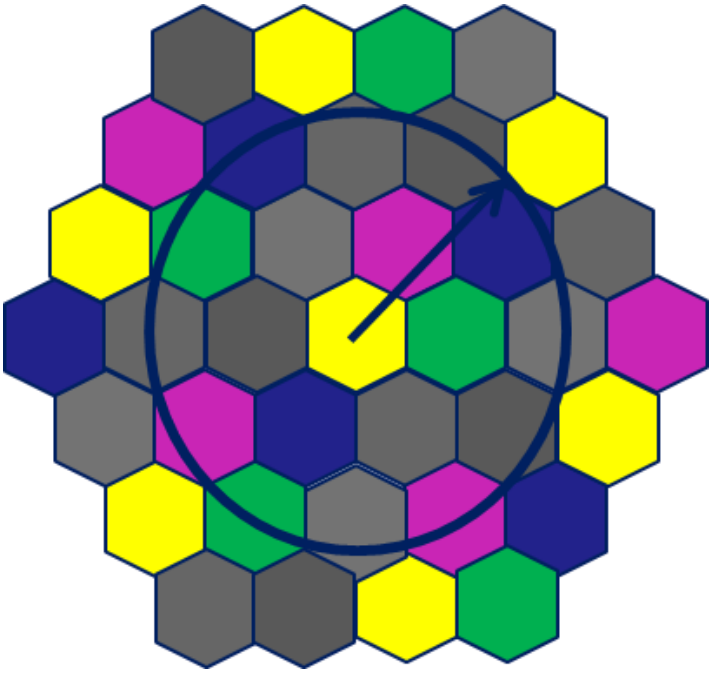


Figure 5-2 : frequency reuse scheme (7 colors)

The reuse distance is given by the following formula : $d\ reuse = \sqrt{13} \times r\ beam$

The isolation between beams for this mission will be managed by the system and offers an infinity of configurations for frequency. Moreover, the pattern of uniformly excited circular DRA is well known [J1(u)/u] and offers a low first side lobe level at 17.5dB. For this study an amplitude distribution uniform on the radiating antenna surface shall be considered, which gives the best efficiency of the power radiated.

Pattern beamwidth θ3B and beam diameter

The synthesis of the DRA 256RE pattern beamwidth θ3dB is presented in the Table 5-1.

DRA 256RE pattern beamwidth θ3dB			
	F=17300MHz	F=18875MHz	F=20200MHz
Nadir beam	1.16°	1.08°	1°

Edge of the coverage	1.2°	1.15°	1.02°

Table 5-1: Transmit phased array antenna 256RE pattern beamwidth θ3dB

The beam diameter on the ground considered is : 1.15°. The reuse distance for the scheme 7 colours is : 2.07°

Aggregate directivity evaluation

The synthesis of the DRA 256RE directivity pattern on the earth coverage is presented in Table 5-2

DRA 256RE directivity pattern synthesis			
	F=17300MHz	F=18875MHz	F=20200MHz
Nadir beam	42.9dBi	43.6dBi	44.2dBi
Edge of the coverage	41.3dBi	41.75dBi	42.05dBi
Aggregate directivity in the coverage	42.1dBi	42.6dBi	43.1dBi

Table 5-2: Transmit phased array antenna 256RE directivity pattern synthesis

Transmit phased array antenna aggregate gain budget

Transmit phased array antenna aggregate gain takes into account the following losses budget :

- Output losses due to radiating element, polarizer, filter and HPA MMIC transition is : 0,6dB (output losses reference plane is output HPA MMIC),
- A/Phi errors : 0.2dB
- Active chains failure (10%) : 10xlog(230/256)=0.5dB
- Uncertainties: 0.1dB.

Table 5-3 presents the transmit phased array aggregate gain budget:

DRA EOL aggregate gain budget	
Average directivity in the frequency bandwidth on the coverage dBi	42.6
Output losses dB	0.6
A,Phi errors dB	0.2
Satellite instability (0.08°) dB	0.1
Directivity losses due to active chains failure (10%) dB	0.5
Uncertainties dB	0.2
DRA 256 RE EOL aggregate gain dB	***41***

Table 5-3: Transmit phased array antenna 256RE gain budget

The end of life aggregate gain considered for this study is : 41dB

Transmit phased array EIRP budget

The transmit antenna EIRP density of 37 dBW/MHz is required by the mission, the proposed processed band is 2900 MHz (example: 12 beams with 240 MHz), which give an antenna EIRP as illustrated table 4.6.

Antenna EIRP requirement	
EIRP density dBW/MHz	37
Processed band MHz	2900
Antenna EIRP requirement dBW	***71.6***

Table 5-4: DRA EIRP requirement

The DRA EIRP considered is 71.6dBW.

HPA operational RF output power requirement

The EIRP requirement, the EOL aggregate gain and the active chain failure rate drive the EOL HPA output power.Table 4.7 presents the HPA operational RF output power budget:

EOL HPA operational RF output power budget	
Antenna EIRP dBW	71.6
Antenna EOL aggregate Gain dB	41

Antenna RF output power W	1150
Number of Active chains failure considered 10%	26
HPA operational RF output power W	***5***

Table 5-5: HPA operational RF output power budget

The end-of-life HPA operational RF output power budget retained for this study is 5W.

HPA operational conducted Noise Power Ratio (NPR) requirement

Conducted NPR quantifies the impact of intermodulation (IM) on the conducted signal. The NPR is defined as the ratio between the useful signal and the intermodulation (into the notch).

Radiated NPR quantifies the impact of Intermodulation (IM) on the radiated signal.

IMs spreading over the full earth view angular domain (+/-8.7°), the radiated NPR pattern directivity is lower than the user beam. TAS-F has shown on different programs that a radiated NPR improvement of approximately 5dB compared to the conducted NPR is optimal, therefore in this study a HPA conducted NPR of 15dB is proposed.

Secondary mission power consumption budget and HPA MMIC PAE requirement

Table 5-6 presents a power consumption budget of the secondary mission and then define the requirement of the HPA PAE @ operational functioning point (15dB NPR) :

HPA PAE @ operational functioning point 15 dB NPR	
Transmit Phased array power consumption requirement kW	***< 5***
EOL Active chains number	230
HPA PAE @ operational functioning point 15 dB NPR %	***35***
HPA RF output power @ operational functioning point 15 dB NPR W	5
HPA power consumption @ operational functioning point 15 dB NPR W	14.3
Low level RF active components + post regulation + TMTC consumption per chain W	0.5
DC converter efficiency %	85
Transmit Phased array power consumption @ operational functioning point 15 dB NPR computation kW	4
Receive Phased array power consumtion kW	0.7
Secondary mission power consumption kW	**4.7**

Table 5-6: Secondary mission power consumption power budget

The main contributor of the secondary mission power consumption is the Transmit phased array antenna (86%) and particularly the HPA power consumption. A HPA MMIC PAE @ operational functioning point 15dB NPR higher 35% will permit to reach the objective of the secondary mission power consumption < 5kW.

End-to-end link budget conclusion

Throughout the document all link budget calculations can be clearly seen but scattered over different sections of the report. This section is to summaries all of the link budget calculation into one easy to read table as seen in Table 5-7.

Down link performances	
Satellite altitude km	40 000
Frequency bandwidth GHz	17-3 – 20.2
Free space loss dB	210,6
Atmospheric attenuation with rain dB	7
Total attenuation dB	***217,6***
Low cost Users Terminal	
G/T Ka Band terminal (low cost) dB/K	12
Terminal pointing error dB	0.3
Bandwidth per terminal and per beam MHz	***250***
DRA EOL aggregate gain budget	
Average directivity in the frequency bandwidth on the coverage dBi	42.6
Output losses dB	0.6
A,Phi errors dB	0.2
Satellite instability (0.08°) dB	0.1
Directivity losses due to active chains failure (10%) dB	0.5
Uncertainties dB	0.2
DRA 256 RE EOL aggregate gain dB	***41***
Antenna EIRP requirement	
EIRP density dBW/MHz	37
Processed band MHz	2900
Antenna EIRP requirement dBW	***71.6***
EOL HPA operational RF output power budget	
Antenna EIRP dBW	71.6

Antenna EOL aggregate Gain dB	41
Antenna RF output power W	1150
Number of Active chains failure considered 10%	26
HPA operational RF output power W	***5***
Es/N0 performances	
C/N	-0.2
C/I dB	14
NPR dB	20
C/(N+Im+I) dB	-0.37
Implementation losses dB	1.5
Required Es/N0 dB	***-1.87***
Data rate performances	
Achieved modcod	QPSK 13/45
Achieved spectral efficiency bps/Hz	0.55
Modcod Es/N0 dB	-2.03
Average data rate Mbps	***139***

Table 5-7: End-to-end link budget summary table

5.1.2. Technology Review (WP1.2)

Table 5-8 provides a qualitative overview and assessment of the identified European foundry options. Among the foundries with the necessary technical capabilities, we have identified four sources in Europe. However, two of these sources are primarily focused on research and do not offer a fast and clear path to cost-effective industrialization. Consequently, the Ferdinand Braun Institute and Fraunhofer IAF in Germany are not suitable options for this project."

Table 5-8: GaN European foundries.

	UMS-France/ Germany 0.15um GaN/SiC	OMMIC-France 0.1um GaN/Si & GaN SiC	Fraunhofer IAF-Germany 0.1 um GaN/SiC	Ferdinand Braun- Germany 0.15 um GaN/SiC
RF Performance @20 GHz	+	+	+	+
Maturity	Yes	+/-	research	research
Space qualified	Yes	In progress	?	?
Cost	High need volume to drive lower	High need volume to drive lower	research	research
Wafer Diameter (mm)	100	75/150	100	75/100
PDK / Design Support	+	+	+/-	-
Accessibility (MPW services)	+	+	- Ad hoc	- Ad hoc
Reliability	+	+	TBA	+

Table 5-9 examines, in detail, the technical features and capabilities of OMMIC and UMS. The UMS 0.15um GaN HEMT process (GH15) is a proven technology for K/Ka band amplifiers, and the consortium expect it to meet most of the requirements. From a cost perspective, OMMIC's GaN on silicon process is an interesting option, especially if the 150mm process becomes available. However, at the time of writing, the 150mm process is still in development, with only the 75mm process currently available. Additionally, there are significant concerns regarding the thermal properties of GaN on silicon. Since its thermal conductivity is not as good as that of the SiC substrate, the design will need to account for this, resulting in lower PAE and reflected in the lower power density per mm.

Considering all the factors mentioned, the GH15 technology from UMS has been selected as the preferred technology for this project. It meets the required technical performance and is considered sufficiently mature for development and subsequent industrialization. Furthermore, the thermal properties of SiC are highly beneficial.

Table 5-9 : Technical features of the commercially available GaN technologies from European Foundries.

Technology	UMS GH25	UMS GH15	OMMIC D01GH	OMMIC D006GH
Frequency	DC-20 GHz	DC-35 GHz	DC – 50 GHz	DC – 90 GHz
Gate Length	0.25µm	0.15µm	0.1µm	0.06µm
Power Density	4.5W/mm	3.5W/mm	3.3W/mm	3.3W/mm
Noise	high NFmin at 20 GHz	2.0 dB @ 20 GHz	1.6 dB @ 20 GHz	1.5 dB @ 20 GHz

Gain	limited gain at 20 GHz	13dB @ 20GHz, 0.4mm FET	12dB @ 20GHz, 0.42mm FET	12.5dB @ 20GHz, 0.42mm FET
Voltage Break down	> 100 V	> 70 V	40 V	40 V
VDS_DC	30 V	20 V	12 V	12 V
Cut off freq.	25 GHz	> 35 GHz	110 GHz	150 GHz
Fmax	> 50 GHz	> 100 GHz	160 GHz	190 GHz
Vpinch	-3.4 V	-3.2 V	-1.5 V	-1.5 V
Gm max	300mS/mm	390mS/mm	800mS/mm	900mS/mm
T_j max	200°C	200°C	200°C	200°C
Space Grade	Space Evaluated	Space Evaluated	In 2020	Planned
Status	Production	Available since 2020	Market Introduction	In Development
Substrate	SiC	SiC	Si	Si

5.1.3. HPA and WG Concepts (WP 1.3)

Table 5-10 provides a summary of the performance metrics for GaN high-power amplifiers operating in the 17–21 GHz frequency range (K-band). The listed Peak Power-Added Efficiency (PAE) values correspond to saturation levels, and where available, include PAE measurements at specified Noise Power Ratio (NPR) linearity thresholds.

Table 5-10: Summary of K-band HPA and their critical performance metrics.

Reference	Type*	Frequency [GHz]	Saturated Output Power [W]	Peak PAE [%]	Linearity efficiency comment	Foundry	Technology
[2]	AB	17.3-20.2	10	35		UMS	0.15um GaN on SiC
[3]	Doherty	17.3-20.3	3	30	20% PAE at 6dB OBO	OMMIC	D01GH GaN on Si
[4]	90deg bal AB	17.3-20.2	8.7	28		OMMIC	D01GH GaN on Si
[5] 1st design	AB	17.0-20.2	10	38	37% PAE at 15dB NPR	Northrop Grumman	NGAS 0.2um AlGaN/GaN on SiCc
[5] 2nd design	AB	17.0-20.2	8.5	46	45% PAE at 18dB NPR	Northrop Grumman	NGAS 0.2um AlGaN/GaN on SiC
[6]	AB	20.8-22.4	9	35	30% PAE at -25dBc IMD3	Triquint	TQGaN15 AlGaN/GaN on Sic

[7]		AB	18.5-24	4	40		Qorvo	0.15um GaN on SiC
[8]		Doherty	16.3-20.3	5	23	23% PAE at 17dB NPR 19% PAE at 6dB OBO	OMMIC	0.10um GaN on Si
[9]		Doherty	18.5-21.5	3	37	27% PAE at 15dB NPR	IAF	0.10um GaN on SiC
[10]	AB	18.0-19.0	10	30		IAF	0.25um GaN on SiC	
[11]	AB	17.0-20.2	12.5	36		OMMIC	0.10um GaN on Si	
[12]	AB	17.7-21.0	4	30	26% PAE at 15dB NPR	-	GaN	

*) AB is used to identify "normal" reactively matched HPAs, although the exact operating mode might be different than class-AB

This overview highlights two primary amplifier architectures: classical reactively matched Class AB and Doherty amplifiers. The Doherty architecture is particularly advantageous for applications requiring high efficiency at significant power back-off levels, such as 6 dB output power back-off. Class AB designs demonstrate strong peak Power-Added Efficiency (PAE) levels; however, the limited designs reporting PAE at specific Noise Power Ratio (NPR) levels typically achieve only around 25% efficiency. An exception is observed in a design by Northrop Grumman [5], where the PAE at 15 dB or 18 dB NPR levels nearly matches the peak PAE. Additional details on the publications summarized in Table 5-10 are discussed on the following pages.

PCB and Mounting Technologies

For this project, the MMIC will be mounted as a bare die to avoid the losses introduced by packaging. The module housing will provide protection for the MMIC. There are three possible mounting techniques, as shown in Figure 5-3 face-up using wire-bonding, face-up using hot-vias transitions in the MMIC, and face-down using flip-chip mounting.

The main advantage of face-up wire-bond mounting is the excellent thermal contact between the MMIC backside and the heat sink, which can be achieved using either AuSn soldering or high thermal conductivity epoxies for die attachment.

Flip-chip mounting offers the benefit of reduced parasitic in the RF transition, but it complicates cooling the backside of the MMIC. Semiconductor technology that supports hot-vias allows for low-loss RF transitions with a classical face-up mounting technique, but the thermal contact to the heat sink is less effective due to the need for thermal vias in the PCB.

Since the hot-via and flip-chip options are not yet available for the selected UMS GH15 technology, face-up wire-bonding will be used.

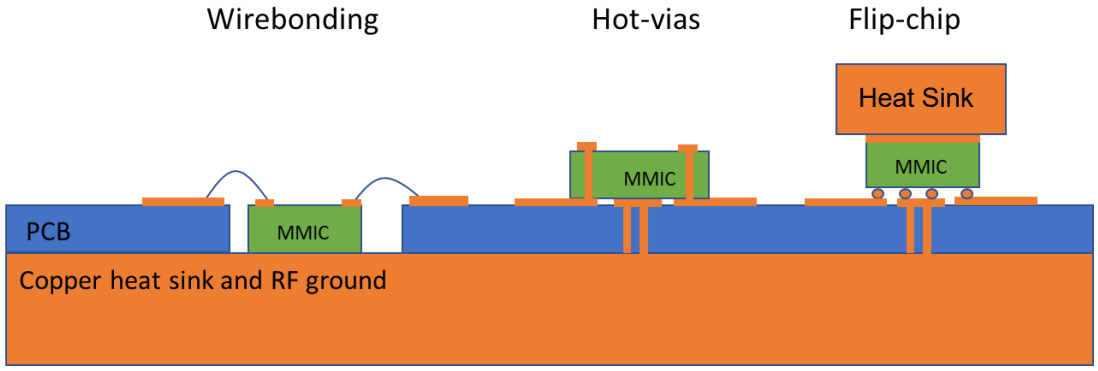
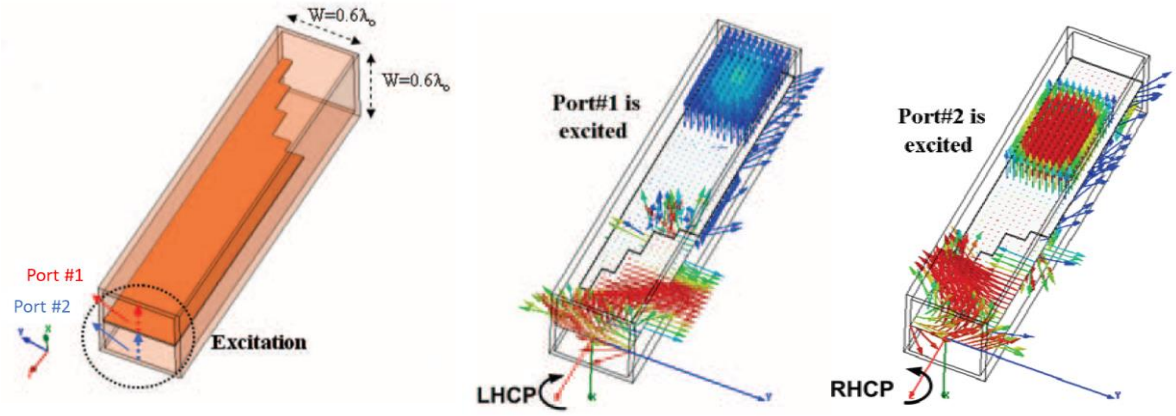


Figure 5-3 : Overview of MMIC mounting technologies.

Circular polarised waveguide horn antennas

Waveguide horn antennas are a proven technology used as feeds for reflector antennas in SATCOM payloads, typically in focal plane arrays. They offer better thermal management and lower losses compared to PCB-based solution; despite their higher profile, their rigidity compensates for this. They also enhance the directivity of the front-end radiating module (FERM) and provide a transition to a flared horn extension.

These properties, along with their substantial bandwidth, make waveguide technology ideal for FERMs. A method for achieving dual circular polarization from a single polarized source using waveguides was introduced in [14]. It involves placing a septum longitudinally in the centre of a square waveguide, as shown in Figure *5-4* (a) ([13]).



(a) *(b)*

Figure 5-4: (a) Geometry of the square waveguide with a stepped septum circular polariser from [[13]], and (b) field distribution due to even mode excitation (left) and odd mode excitation (right). Note that the length orientation of the waveguides in (b) is opposite to the one shown in (a).

The design introduces two stacked rectangular waveguides up to the septum, which then connect to a square waveguide. With proper electrical dimensions, the stacked guides operate in their fundamental mode (TE10), while the square guide supports the orthogonal mode (TE01). A well-shaped septum ensures good matching and phase shift between the modes, enabling various polarizations based on how the input ports are excited. For this application, switchable RHCP and LHCP circular polarizations are achieved by activating one rectangular waveguide at a time. Activating both simultaneously generates a linear polarized output, with the polarization direction depending on their phase relationship.

Figure *5-5* shows a 3D impression of the septum arrangement for dual circular polarizations. To increase the directivity and filter out grating lobes when scanning the main beam, a square tapered end section, such as a pyramidal horn, can be used. The illustrated stepped tapered horn section could also be composed of smooth surfaces.

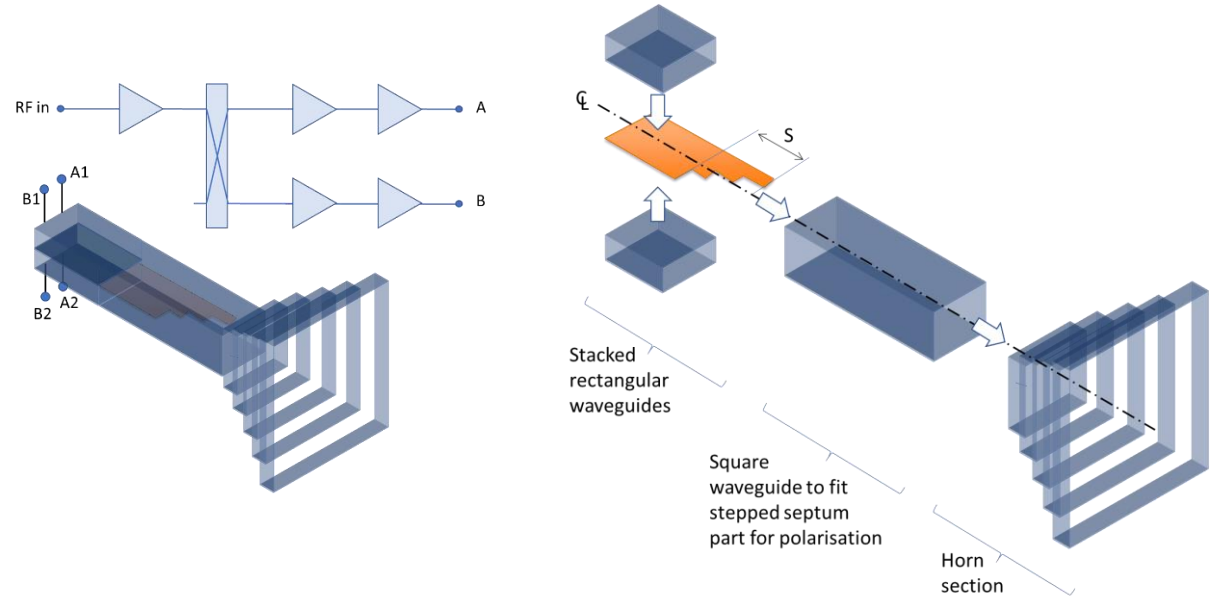


Figure 5-5: (a) 3D impression of the arrangement including the septum in a square waveguide to obtain the two dual circular polarisations. Note also that both rectangular waveguides will have access points to connect with a differential HPA. (b) Exploded view indicating the distinctive sections of the arrangement. The square waveguide will accommodate length S of the septum.

Alternative ways of obtaining dual circular polarisation for a radiation front end suitable for waveguide technology are also shortly indicated here for completeness. For example, on the basis of a square waveguide it could be obtained also by exciting the guide in four points, and using the differential output of the amplifier to drive each perpendicular pair of feeding points Figure *5-6*, showing only one polarisation sense.

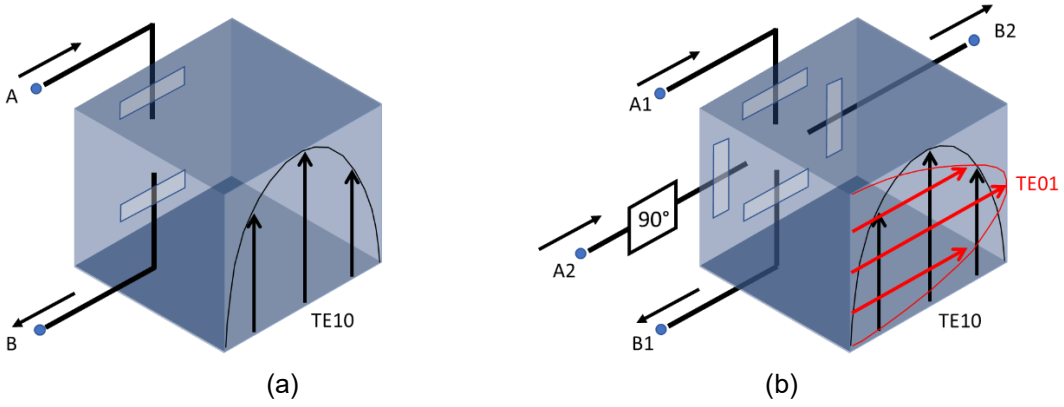


Figure 5-6: Feeding scheme of square waveguide supporting dual circular polarisation. (a) Differentially fed resulting in linear polarisation and (b) Differentially fed resulting in circular polarisation (only one polarisation sense shown). Amplifier output lines connect to parallel slots.

However, obtaining the two polarisations with the proper phase difference would require introducing an additional phase shift in one of the amplifier RF outputs. The introduction of an extra component in one RF path will affect polarisation purity. Furthermore, there will also be a need for additional amplifiers and switches in the IC as well to make the dual circular polarisation work. At the target frequency the introduction of a switch will increase losses, and the extra amplifier will reduce PAE as one of the amplifiers per IC will always be off. Moreover, it would pose constraints in the choice of the type of excitation used for the waveguide. Using the septum as a structural solution for polarising the linear input field will require some waveguide length but it is considered to be more efficient compared to polarising the field using a four-point excitation scheme. For this reason, the concept in *Figure 5-6* is considered less suitable for the current study and will therefore not be further explored.

MMIC Design Topology

For the initial analysis of the differential high-power amplifier, the following steps were taken:

1. Transistor performance analysis for power and efficiency at the given linearity specification
2. Choice of balun
3. Amplifier topology options.

The UMS GH15 technology was chosen for this project. To evaluate transistor performance, simulations were conducted to assess the impact of the number of gate fingers (N=4, 6, 8, 10) and unit gate width (Wu=75µm, 100µm, 125µm) on power gain, output power, and PAE. Although the largest transistor size available in GH15 is 12x175µm, UMS recommends a maximum of 10x125µm due to potential instability issues. Load-pull simulations were performed for each transistor size to find a compromise load between maximum output power and PAE, both with and without 2nd harmonic load tuning. In case of no 2^{nd} harmonic tuning, all harmonic loads are terminated in 50Ohm. For the case with 2^{nd} harmonic tuning the optimum phase of the 2^{nd} harmonic load (with reflection magnitude of 1) has been determined and a new load-pull simulation has been performed to find the new compromise load.

Key observations from the transistor comparison are:

- The power density decreases mainly as function of unit gate width, and also partly as function of total gate width, although the trend is not very clear. It can also be seen that 2^{nd} harmonic tuning also helps to improve the power density when a compromise load between power and PAE is used.
- The power gain mainly drops as function of unit gate width, and a smaller gate width will be preferred. But for a transistor with a total gate width of 1000um there is little difference between the power gain of an 8x125um and 10x100um transistor. The low power gain of the output stage results in a significant impact of the proceeding stages on overall amplifier PAE and as a result optimization of the PAE of these proceeding stages is of crucial importance.
- The simulation of the PAE clearly shows the effect of the 2^{nd} harmonic load tuning, gaining up to 5%pt in PAE. The PAE is slightly decreasing as function of unit gate width, but there is no clear trend of the PAE versus total gate width. The PAE for the 8x125um (in case of harmonic tuning) is equal to the PAE of the 10x100um.
- For the physical layout of the HPA there is also a trade-off between the required power level and the total height of the chip, which is often determined by the total height of the transistors in the output stage. To limit the height and/or allow more spacing between the transistors for heat spreading, an 8x125um is preferred over a 10x100um size.

Single-ended to differential conversion can be achieved using either an active circuit or a passive hybrid. Active circuits provide gain but at the cost of power dissipation, compression point, and linearity. Therefore, passive circuits are preferred, despite requiring more MMIC area. Options include:

- LC lumped element balun
- Marchand coupled line balun
- Rat-race hybrid
- Transformer-based balun

The rat-race hybrid offers excellent phase and amplitude balance but is too large for MMIC integration. A straightforward Marchand balun is also too large, but it can be folded to fit within the MMIC height [15] or implemented using spiral coupled lines [16] & [17]. An LC balun is useful when space is limited but has higher loss and more spreading. Transformer-based baluns are compact but have poor phase and amplitude balance over a narrow bandwidth. Therefore, a coupled line balun, either folded or spiral, will be used.

Amplifier Topology Options

As starting point for the HPA topology calculation the performance of an 8x125um transistor has been used, obtained from simulating the GH15-10 PDK model at 70°C and shown in Figure 5-7. The nominal operating point for 15 dB NPR (green marker) is at around 3 dB output power back-off from the maximum PAE point (blue marker).

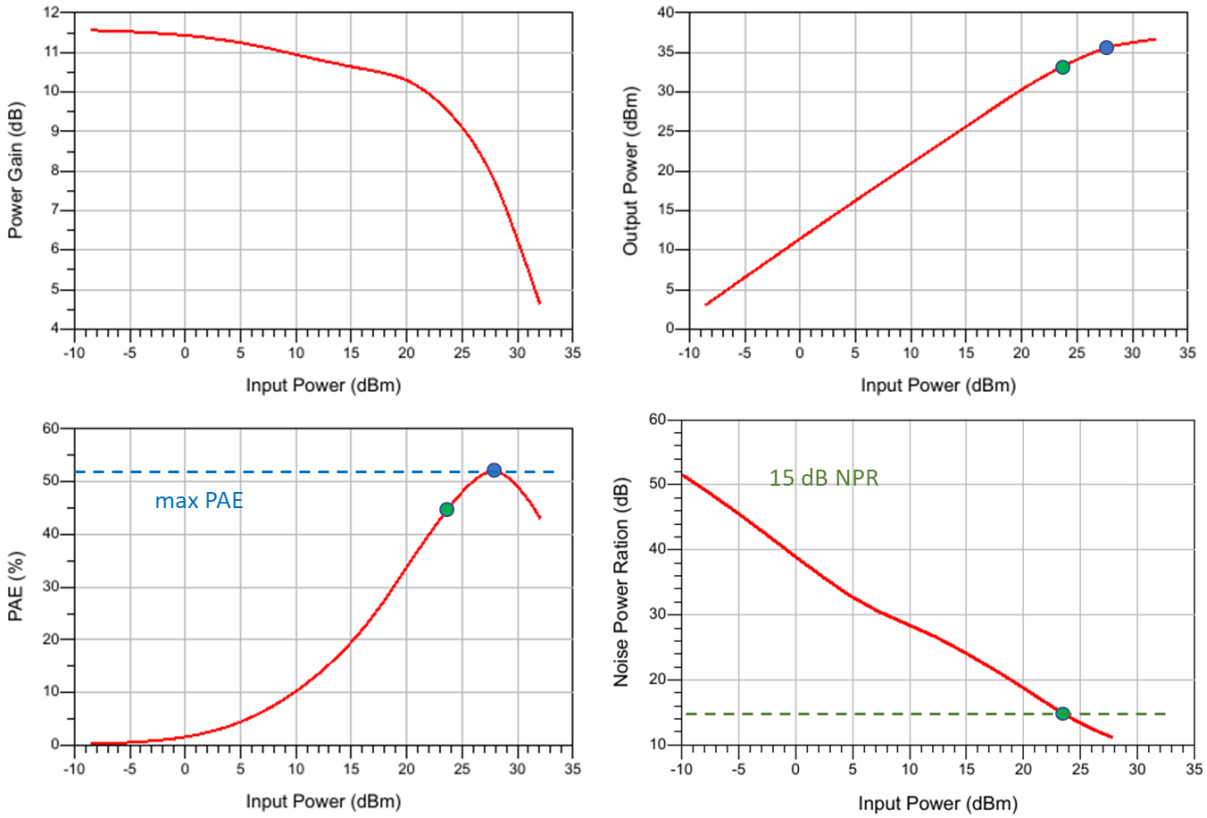


Figure 5-7 : Simulated 8x125um transistor performance at Vd=20V, Vg=-3.0V, Frequency 20GHz, compromise load including harmonic source and load tuning, Ta=70°C.

Using this power-sweep data the performance of several topologies has been calculated. The specified power gain is 20 dB, resulting in a three-stage design. To save MMIC area the first stage can be single ended, with the balun in between the first and second stage.

The following (initial) topology has been selected based on our performance analysis:

- Stage 1: 1x8x60um, followed by a balun
- Stage 2: 2x8x75um
- Stage 3: 4x8x125um

For this topology the following matching network losses are assumed:

- Input loss = 3 dB
- Interstage 1 loss = 4 dB (this includes the loss of the balun)
- Interstage 2 loss = 2.5 dB
- Output loss = 0.6 dB

The performance of this topology has been analysed as a function of total loss in the output (MMIC output matching network + transition to PCB + transition to waveguide), for saturation (maximum PAE point) and in 3 dB output power back-off. The result are: a total loss of approximately 0.6 dB (state-of-the-art) the overall PAE is 31.5%, saturated output power > 41 dBm, output power (@3 dB back-off) > 38 dBm with a PAE is > 31% and the power gain > 22 dB.

Module Concepts

Two main types of module concepts could be considered: a planar or a brick-type approach. A fully planar configuration, as currently proposed in Ka-band array antennas for 5G applications is for this project not suitable because of the high power and high dissipation levels involved, and the corresponding heat pipes for cooling, which could not be accommodated in such architecture.

Alternatively, a hybrid concept could be considered, see Figure 5-8. In this case the waveguide is mounted perpendicularly to the PCB containing the HPAs. Since the main part of front-end module (FEM) electronics is still expected to have a brick-style, a transition must be made for the DC and RF signals from this front-end part to the feeding structure, using connectors. As this connection applies to the RF input signal of the HPA the additional loss does not play a significant part in the overall efficiency. The HPA will be mounted on a metal heat sink, which is thermally connected to a Heat Pipe (HP). This concept is shown in Figure 5-8.

For the brick-type concept, shown in Figure 5-9 the waveguide is mounted in-line with the PBC. No additional interface from the front-end electronics is needed, but the mounting of the waveguide and construction of the feed might be more challenging.

In both concepts there will be 1 module that will house both polarisation feeds to facilitate the overall antenna assembly. More details on possible implementations of the feeding structures for these two types of module concept are given in the following two Sections.

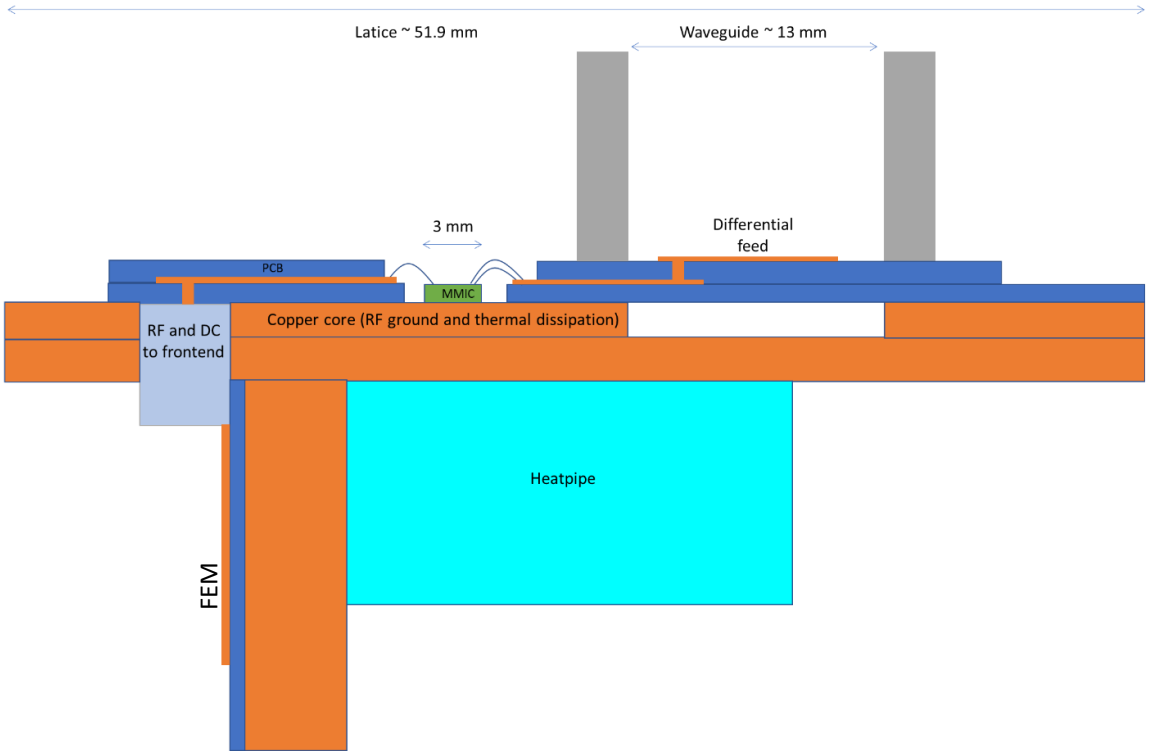


Figure 5-8 : Cross-section example for the case of a planar waveguide feed (hybrid architecture), with the MMIC and waveguide both on the top side of the PCB, showing only 1 polarisation (not fully to scale).

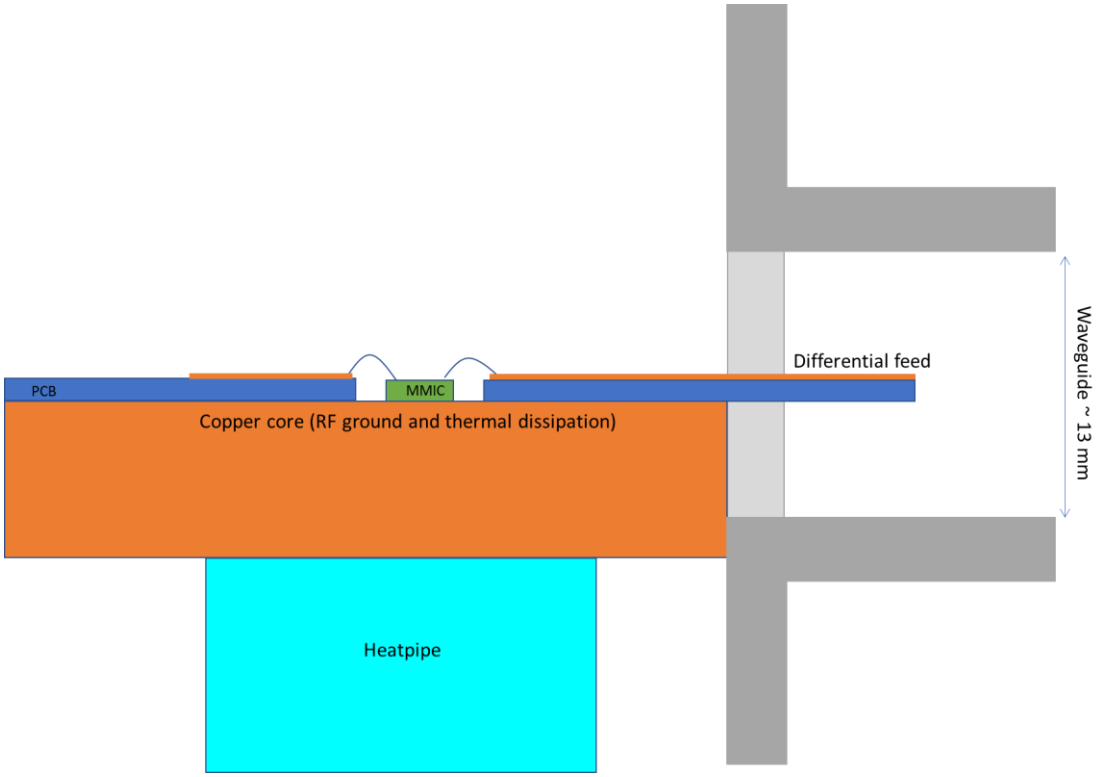


Figure 5-9 : Cross-section example for the case of an E-plane inline waveguide feed (brick architecture), only showing 1 polarization (not fully to scale).

Advise from TAS's experience, both RF and thermo-mechanical design considerations are crucial when choosing a module concept:

- Compliance with the Direct Radiating Array layout (Section 2.5), constraining the X-Y dimensions of the exciter and RF chain
- Compatibility of PCB design with available production processes
- Thermo-elastic management between Heat Pipe (HP) and RF+DC assembly
- Testability requirements, e.g., defining a test module with RF+DC assembly, without HP, assembled at the antenna level
- Structure stiffness at the antenna level: in X and Z axes along the HP, and transverse in Y
- Mechanical parts tolerances due to 3D design (2 PCB planes)
- Number of parts and corresponding assembly cost
- Electromagnetic Compatibility (EMC) and RF+DC interconnection
- Number of heat pipes at the antenna level
- Exciter performance in waveguide: bandwidth

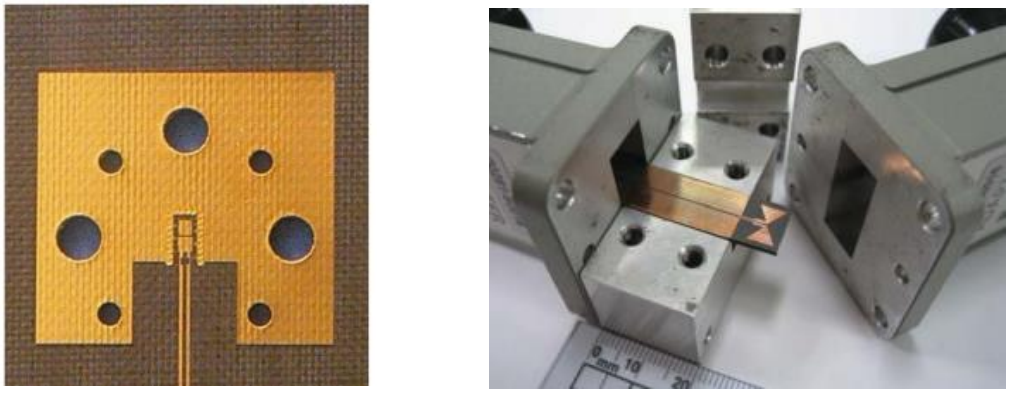
For EMC shielding, the number of parts should be limited to reduce junctions. In the hybrid configuration, the PCB interconnection with the FEM's RF+DC assembly is at a right angle to the HP assembly, introducing mechanical constraints. Achieving the required ~15% bandwidth might be challenging, as the patch may have a smaller band. The total number of parts is crucial for cost and optimization flexibility. The current TAS brick-type configuration, where one heat pipe cools two modules, offers an industrial advantage. Therefore, the brick-type module concept is preferred for this project.

Wave guide exciter concepts

Transforming a single polarized field to RHCP or LHCP is managed by a polarizer within the waveguide. However, transitioning from HPA output ports to the waveguide interior requires careful consideration of manufacturability, thermal control, integration, and efficiency.

Transition types like a differentially fed patch [19] at the waveguide root and a dipole inside the waveguide [20] are good starting points for hybrid and brick module architectures. These concepts need different design approaches, especially structurally. A brick-type system is preferred for thermal control but can use either transition type. Examples of both are shown in Figure *5-10*.

While the transformation from a single polarised field to either a RHCP or a LHCP field (and vice versa) is solved through a polariser within the waveguide composition, the transition from the HPA output ports to the rectangular waveguide interior needs separate attention. In order to make this transition work, careful considerations must be made, which focus on aspects like manufacturability, thermal control, integration and efficiency.



(a) (b)

Figure 5-10 : Differentially-fed patch exciter at V-band [19] *(a), slot line coupled bow-tie exciter at X-band* [20] *(b).*

Radiating front-end losses arise from multiple effects, including transforming differential line fields to waveguide mode and optimizing power transfer with a matching network. The network's design depends on the HPA architecture and transistor choices. To maximize efficiency, it's important to decide if the matching network should be on the PCB or part of the on-chip design. Investigating direct matching, where the HPA-exciter input impedance matches the HPA output impedance, is also crucial. These aspects will be covered in the preliminary design phase.

HPA and WG Concept Conclusion

A brick-type module architecture is proposed for the preliminary design phase due to its suitability.
The following key points from the HPA and waveguide concepts shall be considered for the preliminary design phase:

- Transition loss from HPA output to waveguide exciter on PCB significantly impacts efficiency.
- Differential configuration advantages, such as loss reduction, will be investigated.
- Approaches to further reduce total loss will be assessed, including proper matching of HPA to load and minimizing PCB feeding structure loss.
- Two HPA concepts will be compared: a reference design with isolated HPAs and an improved design using differential mode.
- The goal is to maximize efficiency while meeting linearity requirements.
- GH15-10 technology from UMS will be used for its technical performance and maturity.
- Inline feeding of the waveguide supports the brick-type architecture, with a waveguide exciter and septum polarizer designed for this purpose.
- Differentially fed antennas, like dipole and Vivaldi, will be considered for their potential to reduce loss.

5.2. HPA Preliminary Design Review (PDR) (WP 2.1)

Preliminary HPA design phase evaluated 3 design approaches: differential, gate drain capacitance (Cgd) and co-design. Based on the front-end specifications the following MMIC specifications shown in Table 5-11 have been derived.

Table 5-11 : HPA MMIC specification.

Parameter	Specification
Frequency range	17.3 – 20.2 GHz
Input Return Loss	> 15 dB
Output power @ 15dB NPR	> 37 dBm
PAE @ 15 dB NPR	> 35%
DC power consumption	< 14.3 W
Linear gain	> 20 dB
Temperature (MMIC backside)	20°C – 80°C
Maximum junction temperature [1]	160°C

Note that these specifications apply to the input/output pad on the MMIC, and do not include the transition from MMIC to PCB. This transition is part of the waveguide feed design.

The preliminary DRIFT MMIC design will use UMS GH15 GaN-on-SiC technology, specifically the GH15-10 PDK v4.2.1, which lacks the BCB option and high-density capacitors as stated in section 5.1.2. Although GH15-11, which includes these features, is available, its use in the foundry run is uncertain, therefore GH15-10 will be used. The recommended drain bias voltage for space applications is 20V [18], which will be the nominal value.

5.2.1. GH15 transistor (FET) performance verification

Load pull measurements on GH15-10 transistor samples were conducted to validate the large signal PDK model using an active multi-harmonic setup with a Rhode&Schwarz 4-port network analyzer as seen in Figure 5-11. Due to limited fundamental and 2nd harmonic drive power, only small transistors were measured, with the largest being 8x75µm. Most measurements were on 8x50µm transistors, with some on 6x50µm and 4x50µm. Calibration was done up to the probe-tip reference plane using a dedicated substrate, and de-embedding to the gate and drain reference planes was performed using multi-line TRL structures on the GH15 test sample.

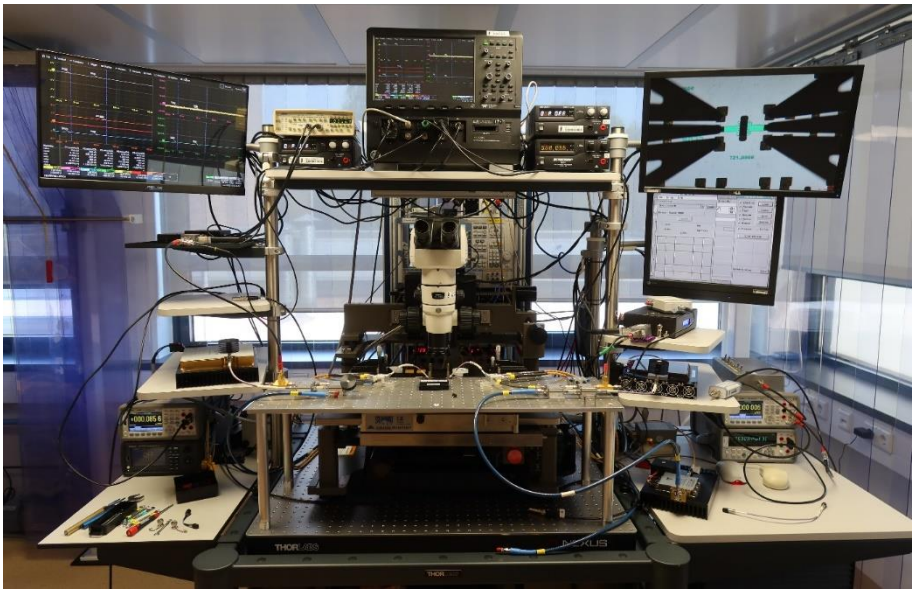


Figure 5-11 : Active load pull setup (with the ZVA at the back side of the probe station).

FET verification measurements

To verify the UMS PDK model, load pull and power sweep measurements were performed on GH15 transistors (sizes: 8x75µm, 8x50µm, 6x50µm, 4x50µm) under CW conditions. The gate bias in simulations was adjusted to match the small signal drain current in measurements, with a 0.22V offset. The FET comparison analysis examined (at the compromise load): power and PAE contours, power sweep performance including DC and AM/AM and AM/PM and 2nd harmonic termination. The measurements were done at frequencies: 18, 19 and 20 GHz.

The analysis comparison for 18GHz is shown In Figure 5-12; the measured and simulated load pull contours for 8x50µm FET show good agreement. Figure 5-13, measured and simulated power sweep at compromise load match well, though simulated AM/PM curve shows more phase compression. Figure 5-14, gain compression is accurately simulated at 18.0 GHz, but phase compression is overestimated. Figure 5-15, maximum PAE achieved with second harmonic phase around 90-120 degrees. Similar results were observed at frequencies 19 and 20 GHz.

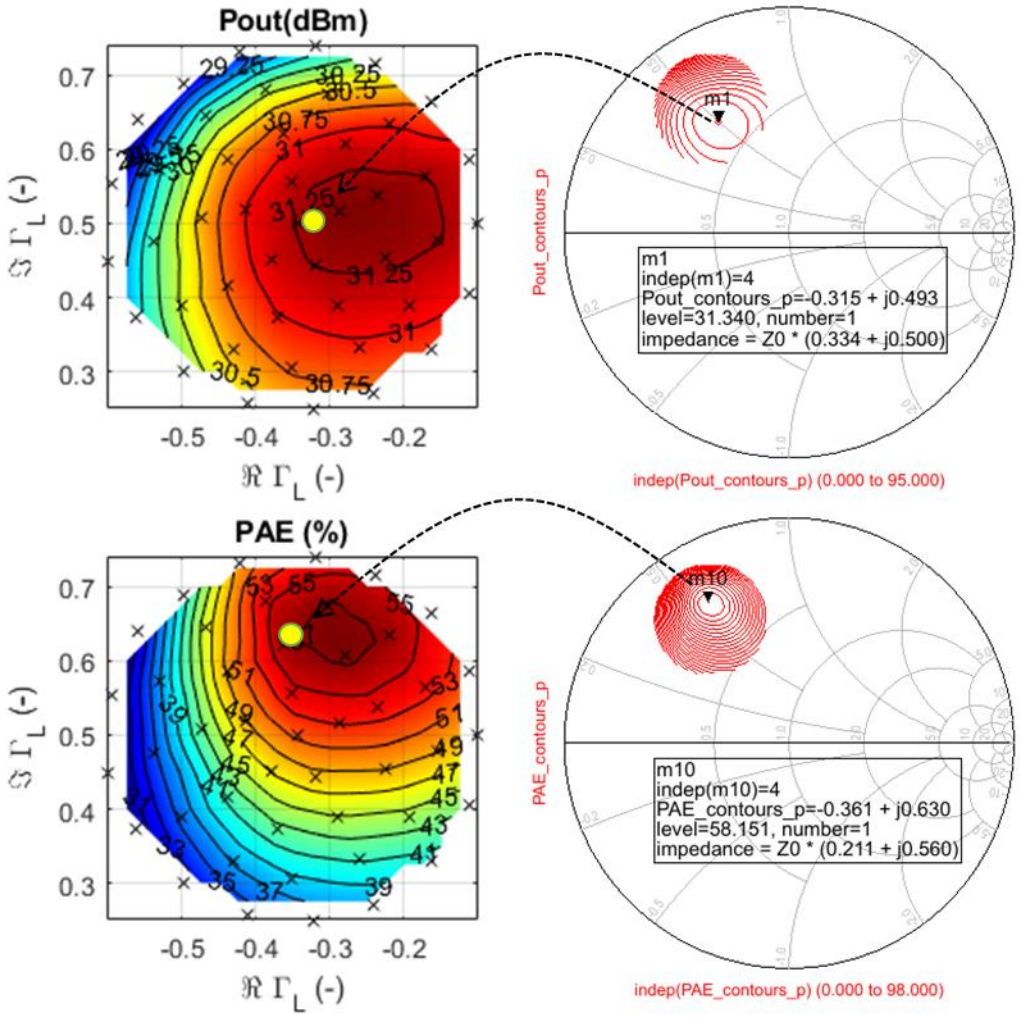


Figure 5-12 : Comparison of measured (left) and simulated (right) load pull contours for the 8x50um transistor, at Vd=20V, Vg=-2.9V, 18.0 GHz, Ta=25°C, without 2nd harmonic load optimization.

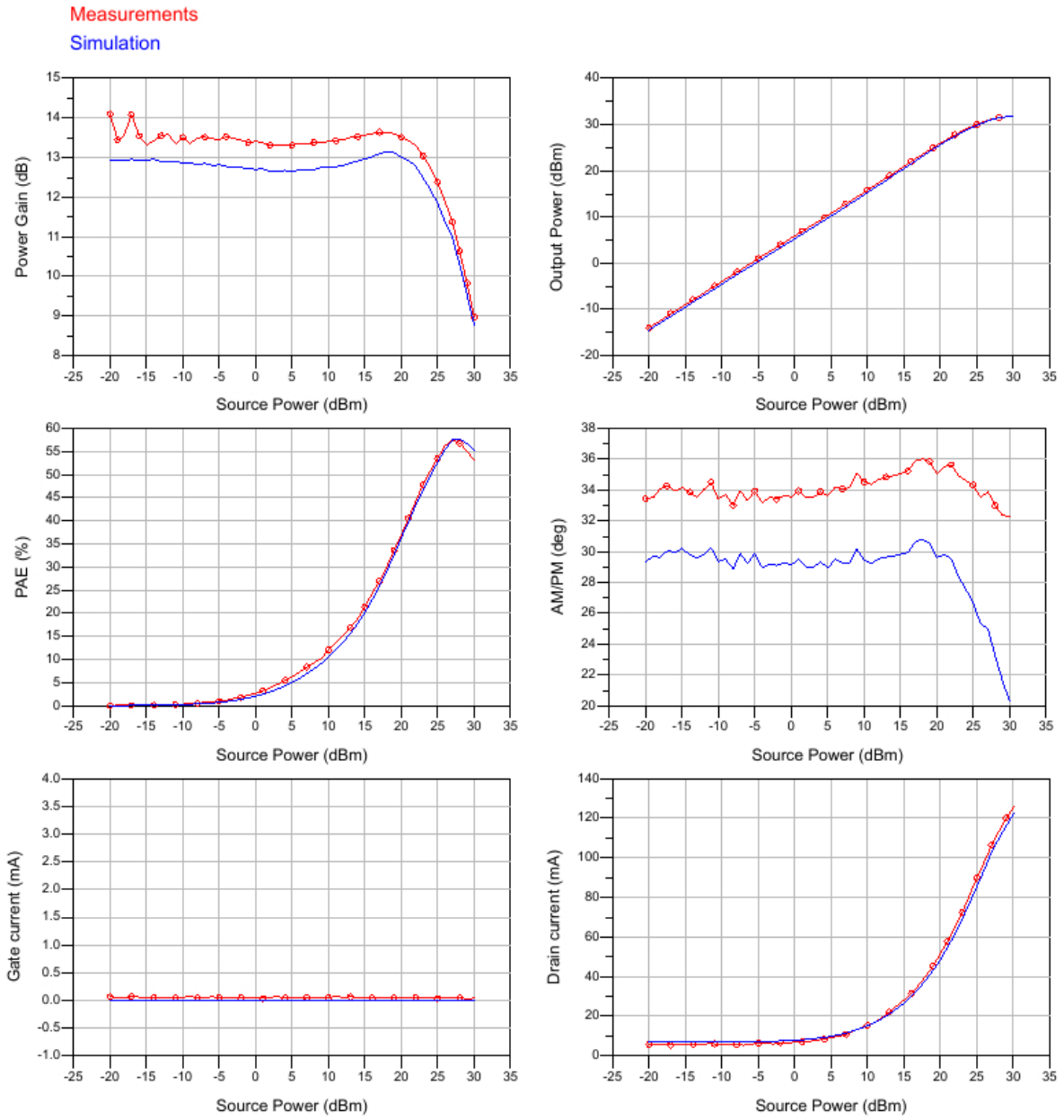


Figure 5-13 : Comparison of measured and simulated power sweep for the 8x50um transistor, at Vd=20V, Vg=-2.9V, 18.0 GHz, Ta=25°C, fundamental load = -0.3 +j 0.6, without 2nd harmonic load optimization.

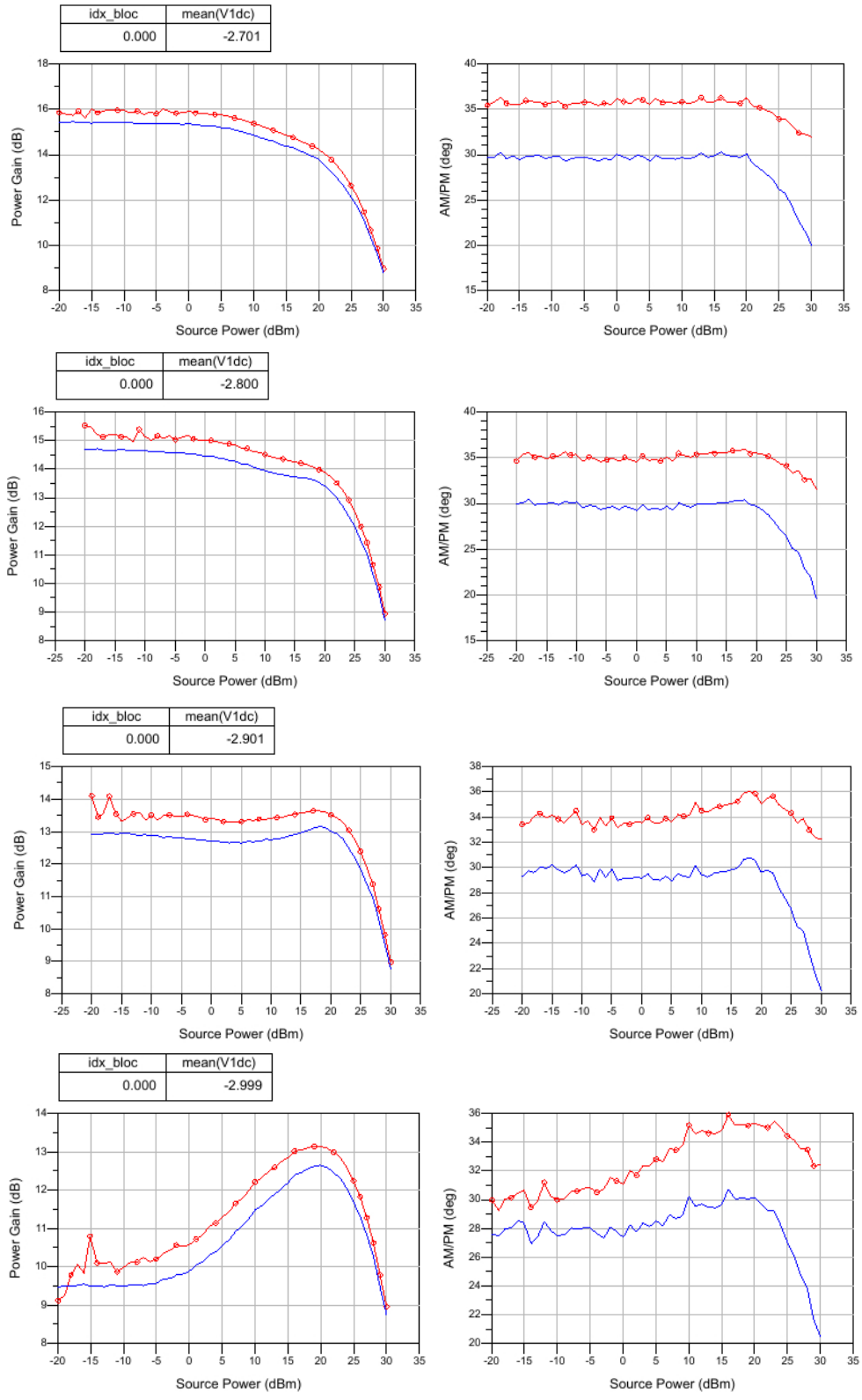


Figure 5-14 : Comparison of measured and simulated power sweep, showing the gain and phase compression for the 8x50um transistor versus Vg, at Vd=20V, 18.0 GHz, Ta=25°C, fundamental load = -0.3 +j 0.6, without 2nd harmonic load optimization.

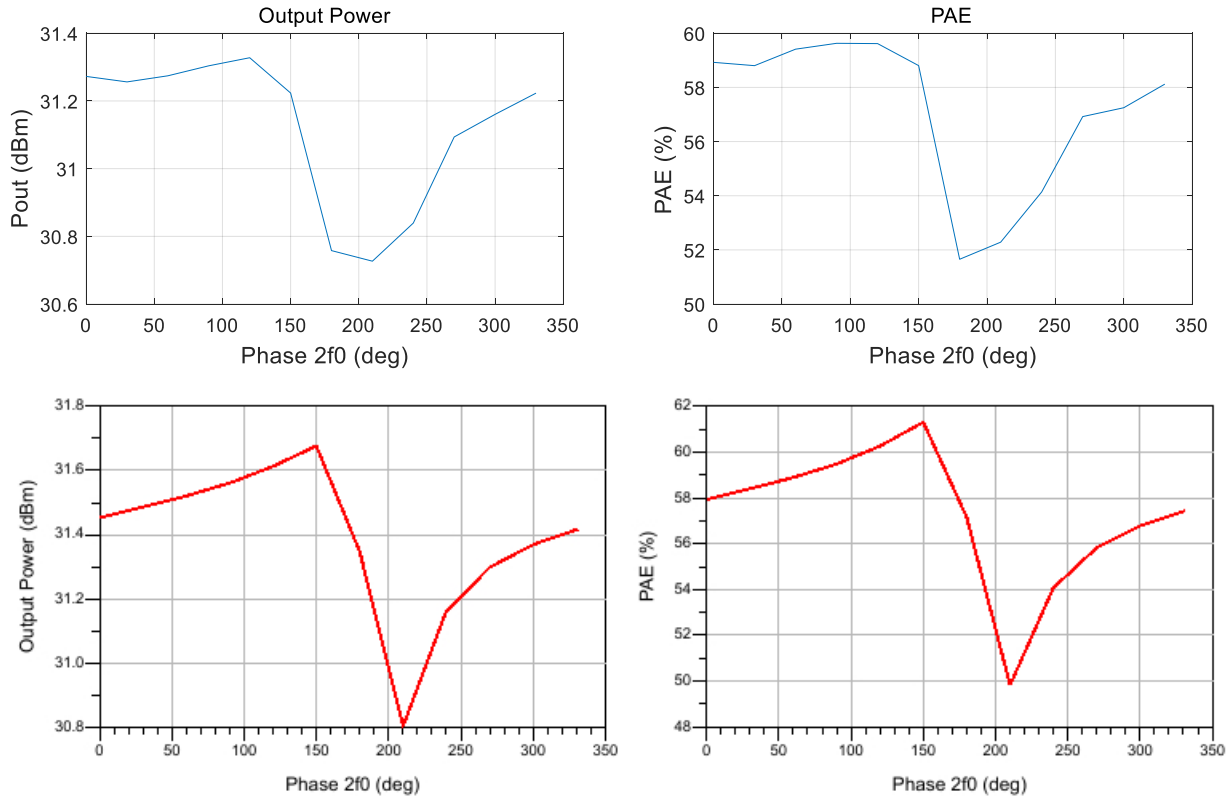


Figure 5-15 : Measured (top) and simulated (bottom) output power and PAE for the 8x50um transistor versus phase of the 2nd harmonic load (mag=1), at Pavs=27dBm, Vd=20V, Vg=-2.9V, 18.0 GHz, Ta=25°C, fundamental load = -0.3 +j 0.6.

5.2.2. FET verification conclusion

The same measurement and simulation comparison was performed on FET sizes: 8x75um, 6x50um and 4x50um also. To conclude, a limited set of measurements has been done on a few GH15 transistor samples to understand the accuracy of the large signal transistor model in the PDK in the frequency and bias range of interest. Although this is not a full verification of the PDK, the following observations can be made:

- The measured location of the output power and PAE maxima show a slight shift with respect to the simulated values.
- The measured output power and PAE power sweeps correspond well to the PDK model.
- The measured behaviour with respect to the 2nd harmonic load location corresponds well with the simulations.
- The measured gain is a bit higher than simulated.
- Depending on the gate bias there is some deviation between the measured and simulated phase compression.
- Overall it can be concluded that the PDK model is good enough to be used for the design.

5.2.3. Balun Design

To excite the differential HPA, a balun is required to convert the single-ended input to a 180° out-of-phase differential signal. Several options were considered:

- Lumped element LC/CL network
- Marchand balun (folded to reduce size)
- Marchand balun with inductor-like folded layout
- Active balun (discarded due to poor phase balance)

A Marchand-type balun is chosen for this project. UMS design rules require minimum spacings of 10µm for long metal lines and 20µm for thick metal lines, limiting achievable impedance levels. The balun, part of the HPA matching networks, can have a 50Ω input impedance and a differential output impedance close to 200Ω, with performance optimised by tuning the microstrip line length between the balun halves. A typical balun layout can be seen in Figure 5-16

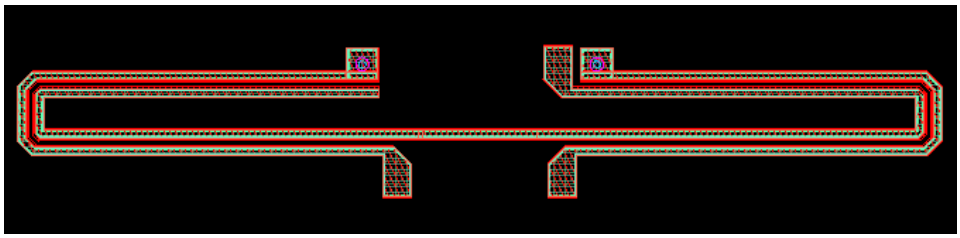


Figure 5-16 : Basic layout of the folded Marchand balun, line width 24um, spacing 10um, total height is 2 mm.

The balun can be realized with an insertion loss less than 0.7 dB, with an amplitude error around 0.1 dB, phase error of 1.2°, and good port matching. The final performance will of course depend on the actual load impedance inside the HPA, and some tuning of the balun layout will be needed during the detailed design.

5.2.4. Baseline HPA Topology

The baseline HPA, is a standard HPA, matched to a 50ohm environment. Initially a 3-stage HPA was foreseen, with relatively large transistors (8x125um) in the output stage. However, during the PDR it was found that transistors with a smaller unit gate width, like an 8x50um or 8x60um, provide more gain, such that a 2-stage design can also achieve the required small-signal gain specification. The total size of the output stage has not changed much, so in the new topology 4 transistors (seen in Figure 5-17) are used in half of the output stage, while originally 2 larger transistors were foreseen. In the current design the 8x60um transistor for the output stage was selected because with this transistor size the output power specification of >37 dBm could be achieved.

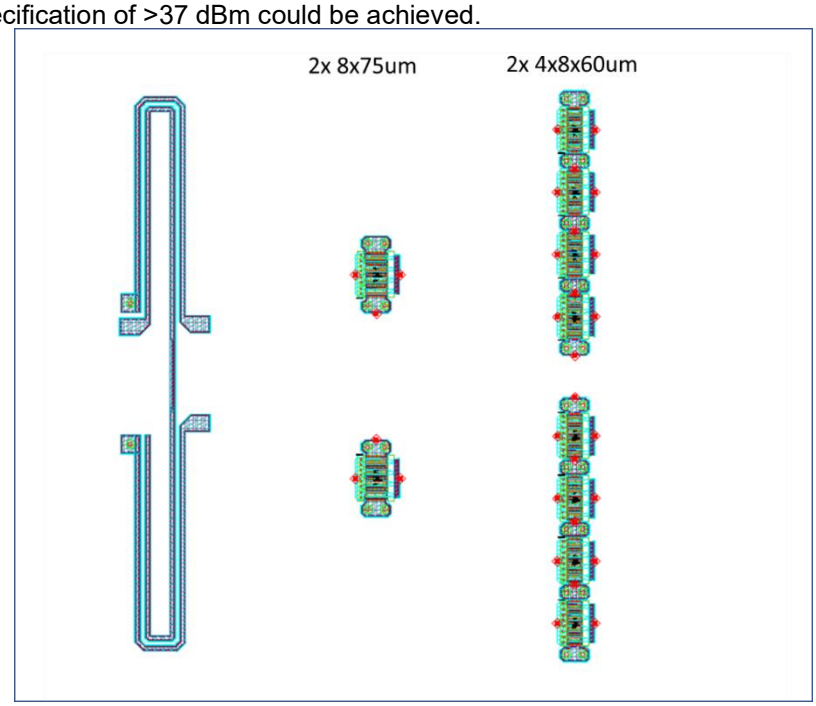


Figure 5-17 : Updated HPA topology.

Transistor load pull simulation

For the selected transistor in the output stage load pull simulations at different frequencies have been performed to obtain an equivalent RC model of the optimum output impedance. A compromise load

impedance has been chosen, in between the optimum output power and optimum efficiency load. Figure 5-18 shows an example of such a simulation result. As initial gate bias a deep class-AB bias point of -3.1 V has been chosen.

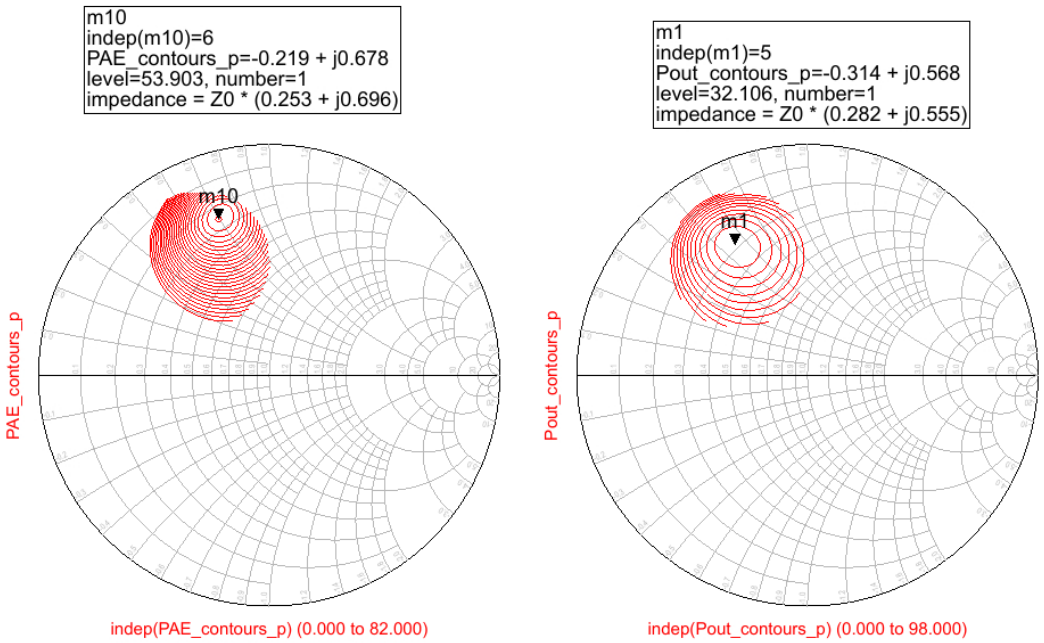


Figure 5-18 : Example load pull simulation of an 8x60um transistor at Vd=20V, Vg=-3.1V, Pavs=22dBm, 18.8 GHz, Ta=80°C, no 2nd harmonic optimization.

As already shown for the PDK evaluation the 2nd harmonic load can have a big impact on the PAE. Figure 5-19 shows the PAE load pull contour for the 2nd harmonic load, at the compromise fundamental load (reflection coefficient -0.26+j*0.62). As can be seen, the PAE maximum occurs for a load magnitude of 1 with phase 73°. There is quite a large impedance area that results in a good PAE, including loads around 50ohm. However, there is a specific area, around a phase of 150° which should be prevented since these impedances will result in a drastic reduction of the PAE. During the design of the output matching network it will be verified that the 2nd harmonic load is in the area with a high PAE.

It is also possible to perform 2-tone load pull simulations to find the best IM3 performance, but this will result in a load that is far away from the optimum power and PAE load, and therefore does not give any useful design information.

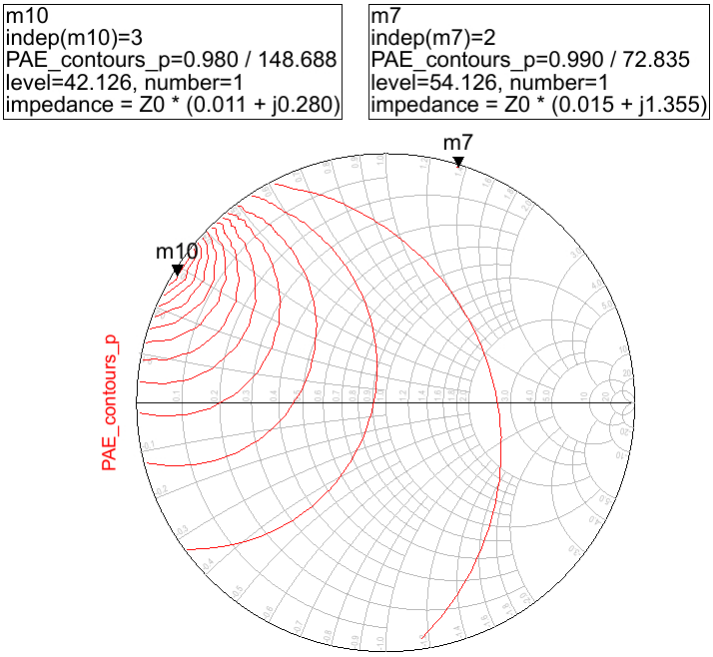


Figure 5-19 : Impact of the 2nd harmonic load impedance of the PAE.

Transistor stability

Concerning stability there are several design options, ranging from the most safe option (i.e. make the transistors unconditionally stable) with the highest loss, to a more risky options, where stability is analysed at the full MMIC level. The latter option will provide the best performance (lower insertion loss in the matching networks) but does also require more detailed stability analysis at MMIC level. Initial SS transistor stability at the nominal bias point Vd 20 V and Vg -3.1 V, resulted in a stable transistor over the entire design bandwidth, though potential instability at the lower and higher frequencies. A parallel RC network improves stability at the high frequencies and lower frequencies to be solved in the implemented bias network.

The large signal stability, including possible loop oscillations, will be analysed for the transistors inside the full HPA design. During the design of the full HPA it will be checked by simulation if such an RC network is required or that other stability measures, with less loss, might give a better overall performance.

Output matching network design

Based on the optimum 8x60um transistor load determined from load pull simulations, the PDR output matching network has been designed. This design contains PDK components and partly Momentum simulations, for structures that are difficult to model with the PDK components. Initially it is assumed that the antenna feed, including the bond-wire transition from MMIC to PCB, provides a 50ohm load to the HPA. In a later stage this matching network will be tuned to the actual impedance presented by the antenna feed. The matching network has been designed to be as compact as possible, by directly combining the 4 transistors, with a bias stub in the second combination step. After the combiner one LC low-pass section is included, followed by a DC blocking capacitor. The simulated performance is shown in Figure 5-20. The matching to the optimum load is better than 20 dB and the loss varies between 0.40 and 0.45 dB.

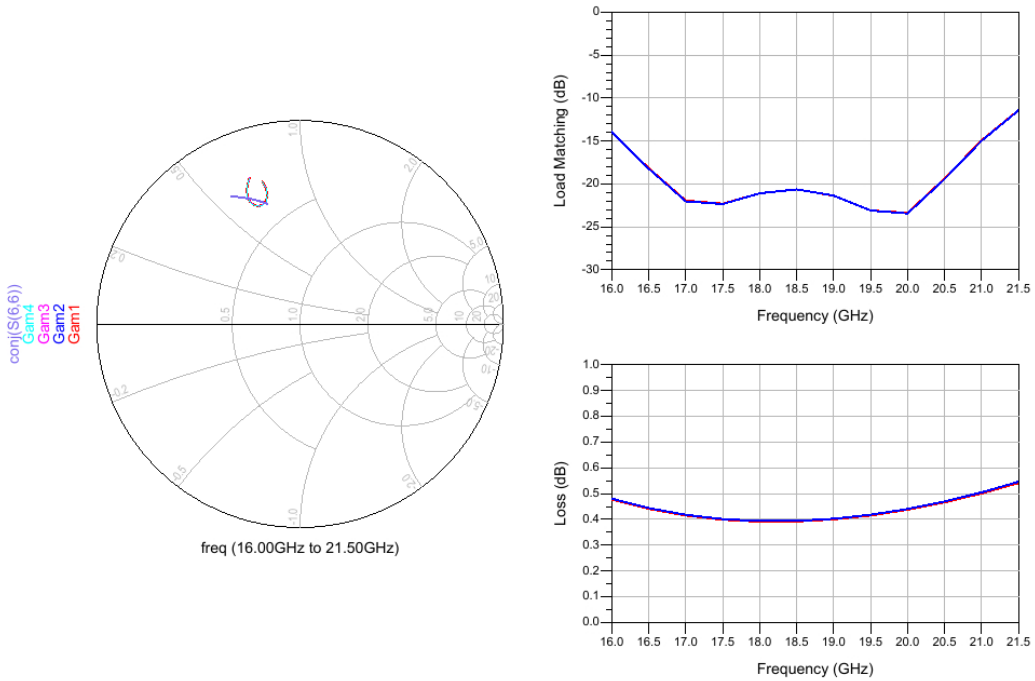


Figure 5-20 : Simulated performance of the initial output matching network.

Interstage matching network design

The interstage matching networks matches the input impedance of the 4x8x60um transistors of the output stage to the optimum load of the 8x75um transistor of the first stage. In this PDR interstage design the RC stability network is included in series with each gate of the 8x60um transistors, but this network could be removed depending on the overall stability simulations. The gate bias is supplied via a high ohmic (series inductor) connection. The simulated performance is shown in Figure 5-21. The matching to the optimum load is much worse than for the output matching, but this is often the case in multi-stage power amplifiers.

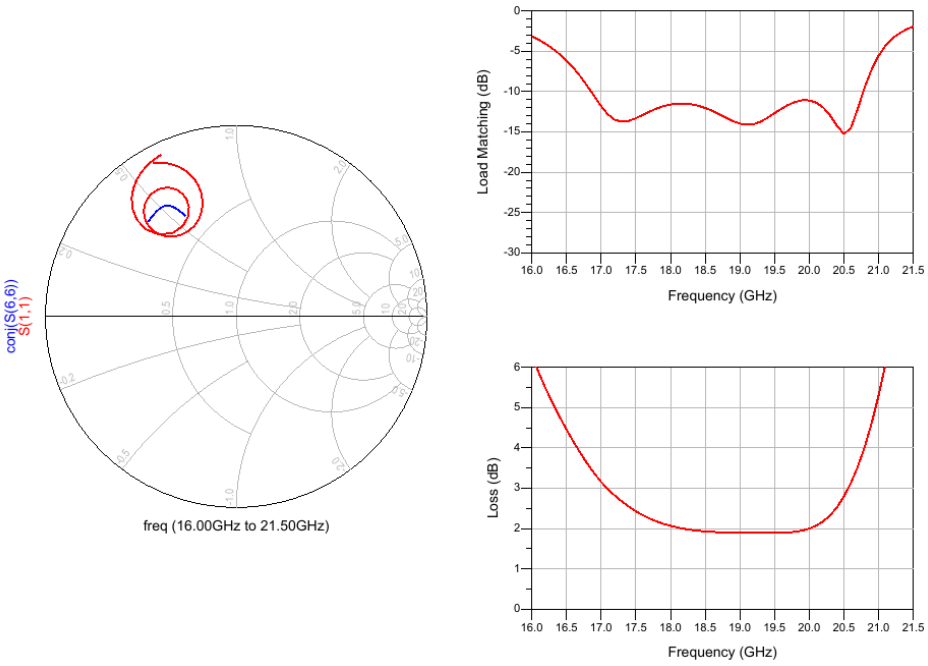


Figure 5-21 : Simulated performance of the initial interstage matching network.

Input matching network design

The input matching network matches the input impedance of the 8x75um transistor to the output impedance of the balun, which is approximately 94 ohm. No RC stability network is included for the 8x75um transistor, but overall stability simulations will analyse if this is possible or not. The input matching network has been optimized including the balun and Figure 5-22 shows the simulated performance of this network, including the balun.

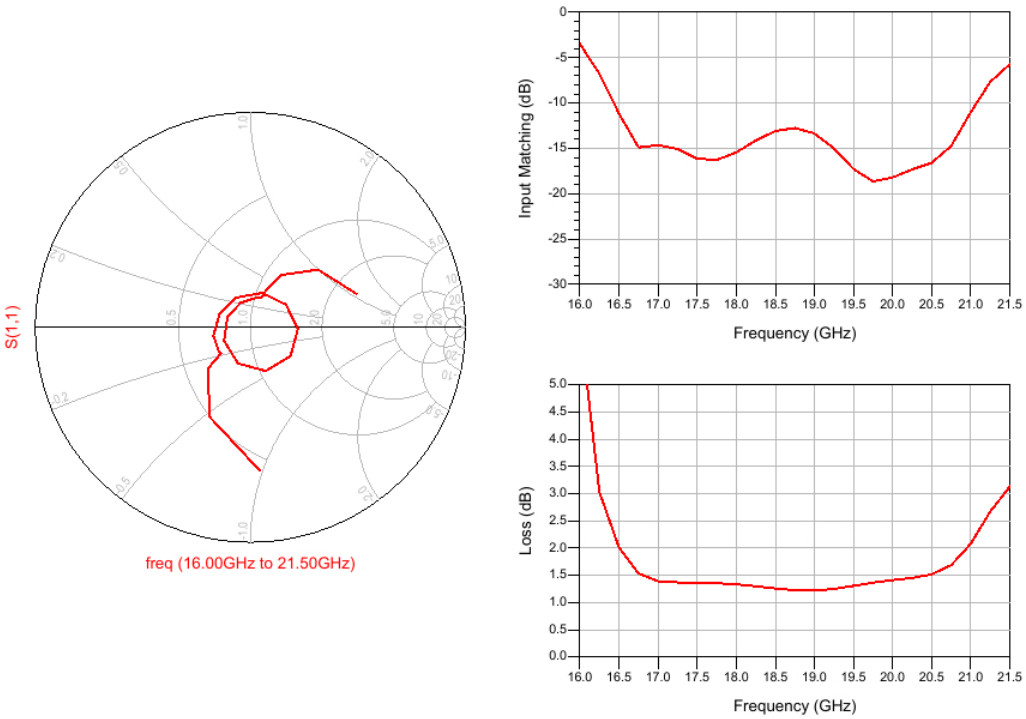


Figure 5-22 : Simulated performance of the initial input matching network, including the balun.

Overall baseline HPA performance

The performance of the HPA has been simulated with the actual differential waveguide feed as load. Figure 5-23 shows these reference planes for the simulation. That means that the calculated output power, efficiency and linearity do not include the loss of the feed, but do include the non-ideal load of this feed. However, the 2-port S-parameter simulations do include the waveguide feed structure. Note that the current waveguide feed design does not yet include the polarizer.

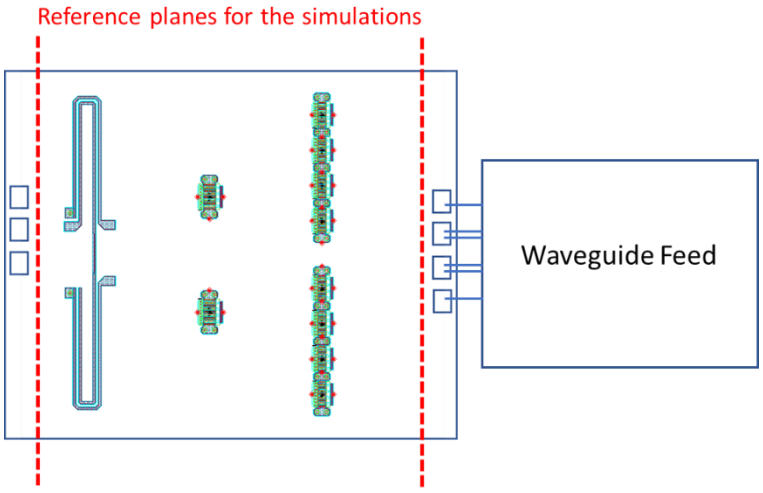


Figure 5-23 : Refence planes for the simulated HPA performance.

Unless otherwise specified the simulations have been performed at:

- Vd = 20 V
- Vg = -3.1 V
- Ta = 80°C (backside MMIC temperature)

5.2.5. S-parameters

Figure 5-24 and Figure 5-25 show the S-parameters under nominal bias conditions. For the wide-band simulation an ideal balun has been used at the output because the differential waveguide feed simulation data is not available over this wide frequency range. No gain peaks outside the band on interest are visible and the input and output matching are always passive (dB(S11) and dB(S22) < 0).

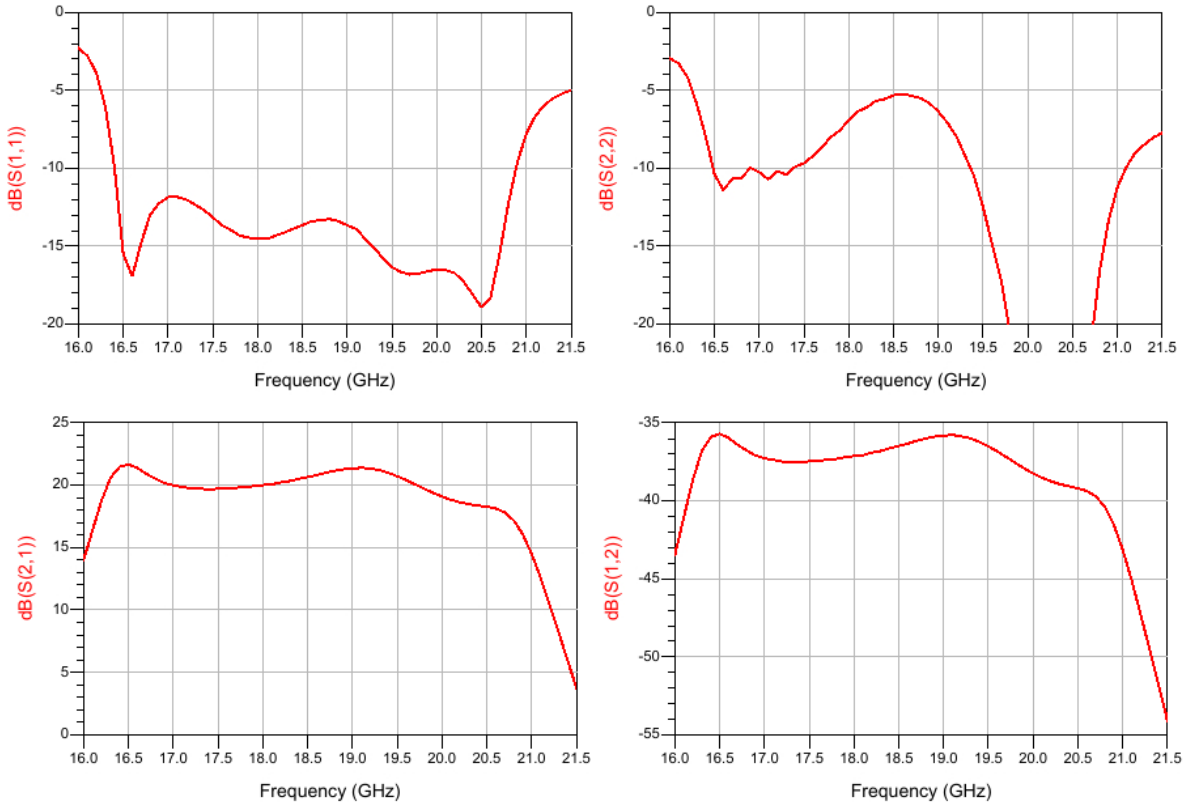


Figure 5-24 : Small-signal S-parameters for the HPA including the waveguide feed.

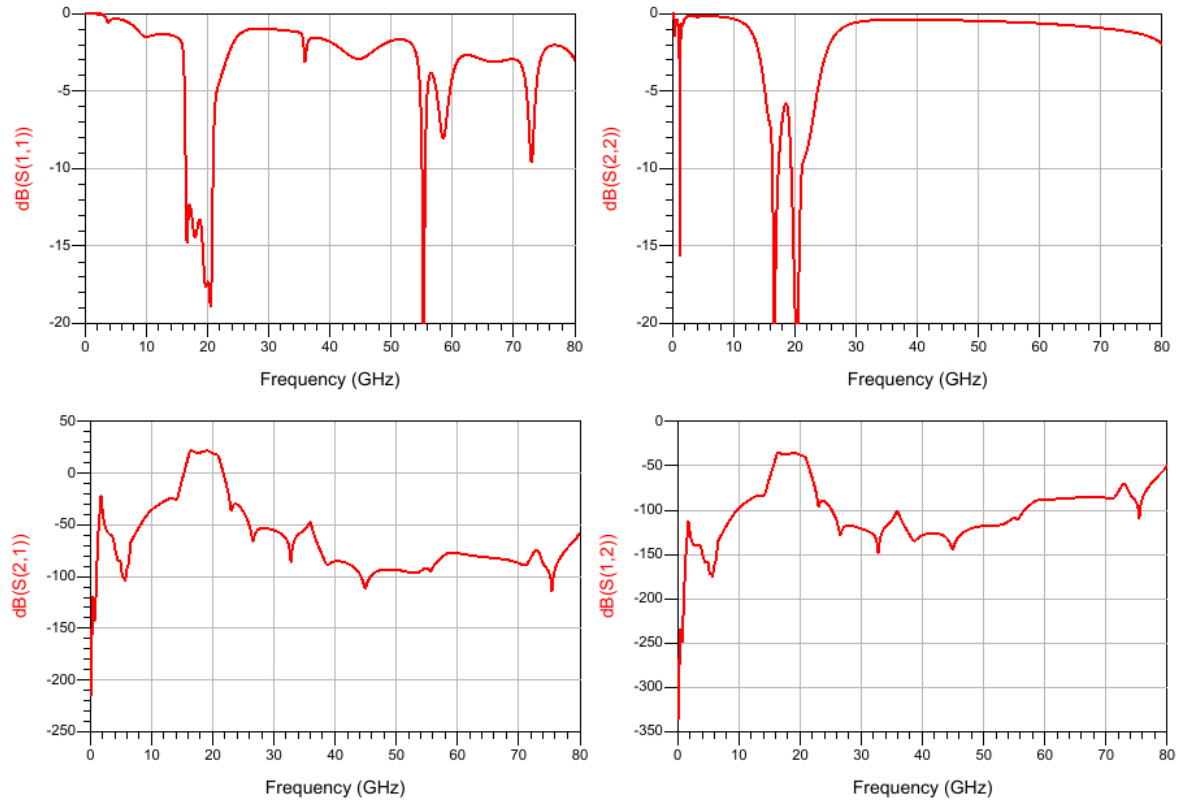


Figure 5-25 : Wide-band small-signal S-parameters for the HPA including an ideal balun at the output.

5.2.6. Large-signal performance

Figure 5-26 shows the large signal performance for a source power of 15 to 25 dBm. The saturated output power is larger than 40 dBm and a peak efficiency of 40% is achieved up to 20 GHz

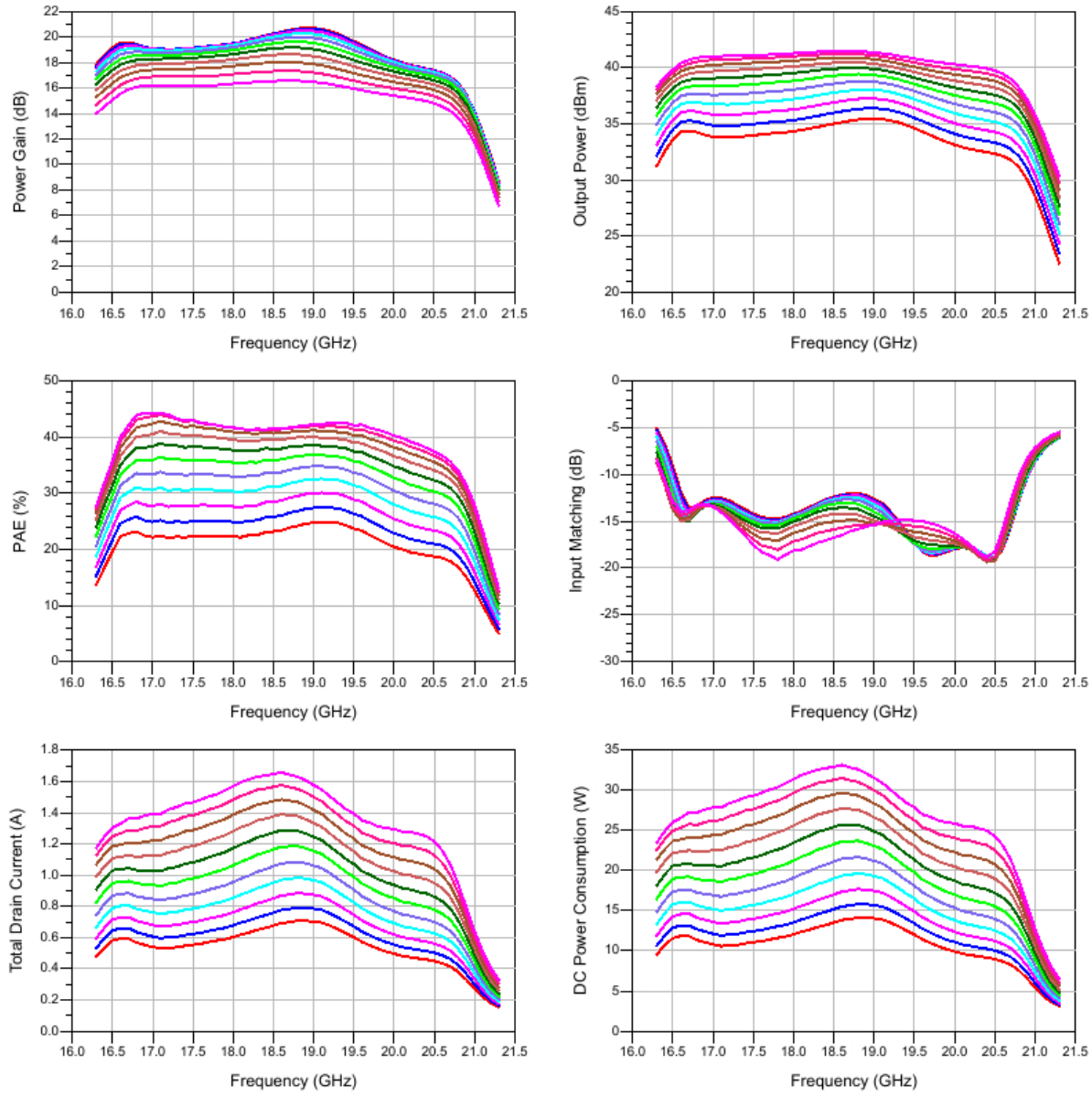


Figure 5-26 : Large-signal performance for Pavs = 15 – 25 dBm.

Figure 5-27 shows power sweep simulations at 17.3, 18.8 and 20.3 GHz (note, the actual frequency band is 17.3-20.2 GHz). At the high side of the bandwidth the efficiency drops.

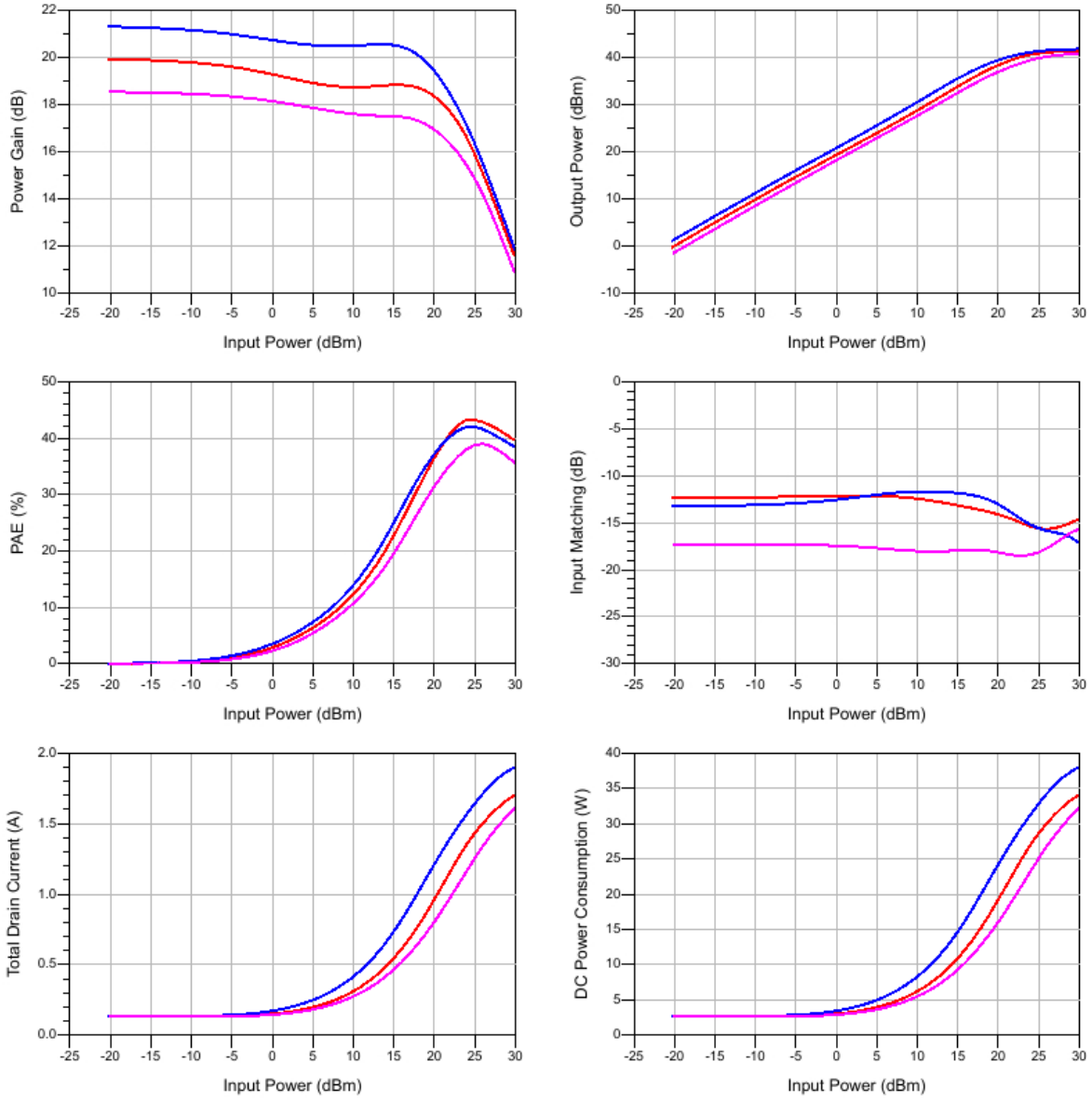


Figure 5-27 : Large-signal power-sweep at 17.3 GHz (red), 18.8 GHz (blue) and 20.3 GHz (magenta).

Figure 5-28 shows power sweep simulation as function of gate bias voltage. In saturation the gate bias voltage does not have much impact on the performance. However, there is a large impact on the AM/AM and AM/PM performance. For the design a gate bias of -3.1 V (blue curve) has been used since this results in the least gain and phase compression variation. Figure 5-29 shows a similar sweep but now versus frequency at a fixed source power level, corresponding to the maximum efficiency point.

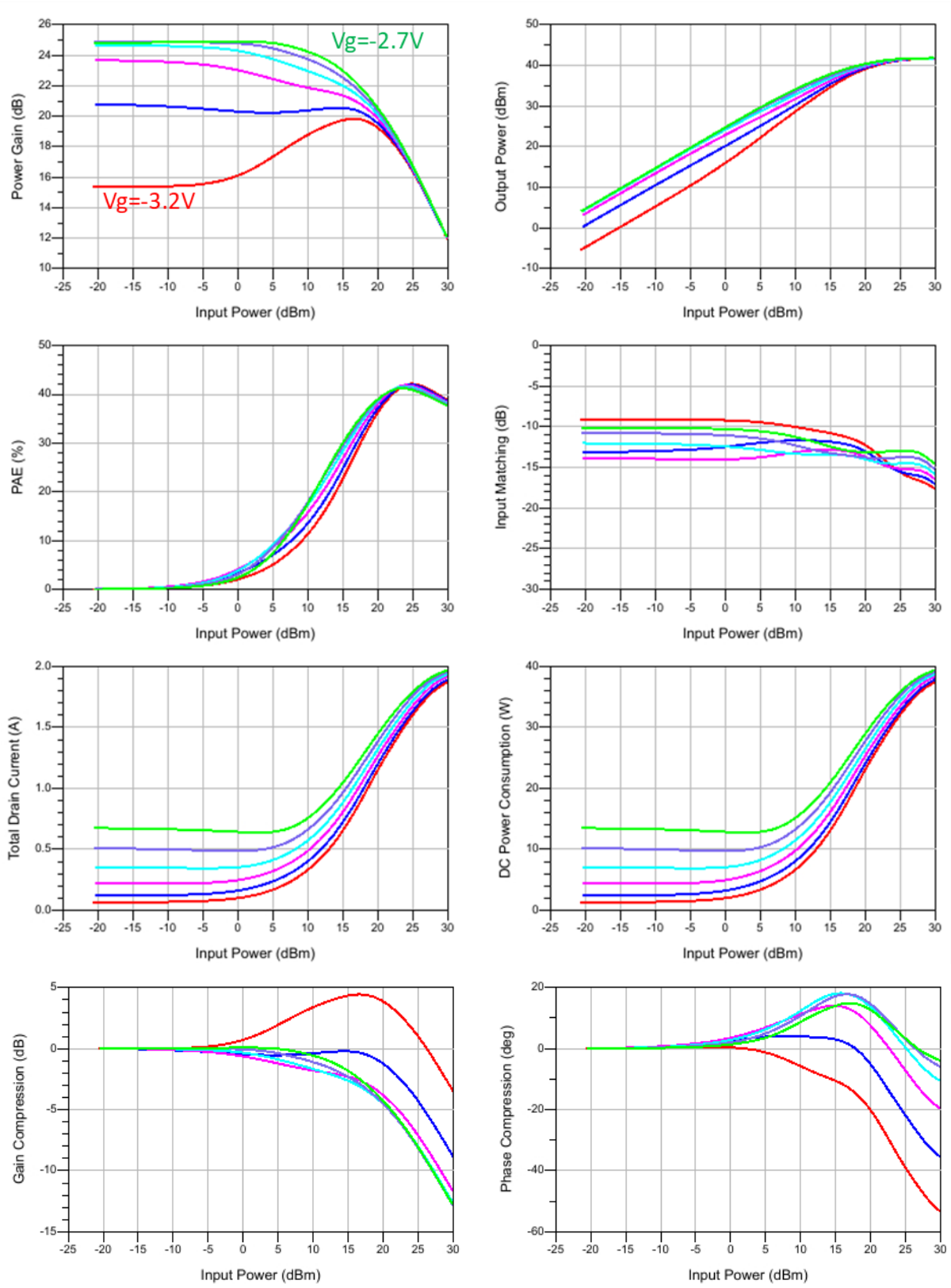


Figure 5-28 : Power sweeps at 18.8 GHz for Vg = -3.2 to -2.7 V.

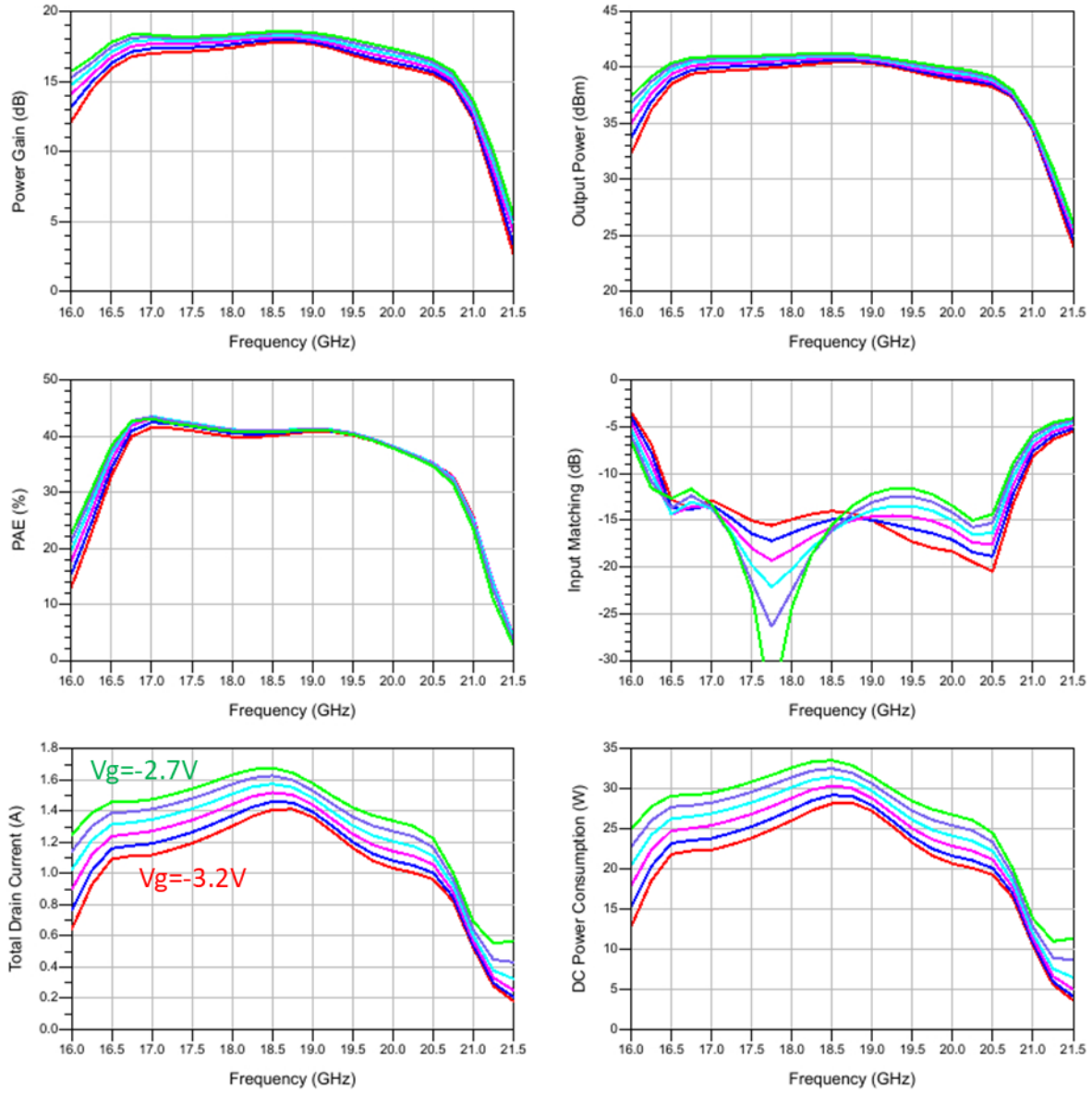


Figure 5-29 : Frequency sweeps at 23 dBm source power for Vg = -3.2 to -2.7 V.

For the switchable polarization two HPAs will be used, fed via a Wilkinson power divider. Gate switching could be used to power down the HPA that is not used. A gate bias more negative than -8 V will keep the isolation of the HPA in off-mode at 30 dB. If this isolation level is not high enough than also drain switching will be needed, or a real SPDT switch is needed at the inputs of the HPA.

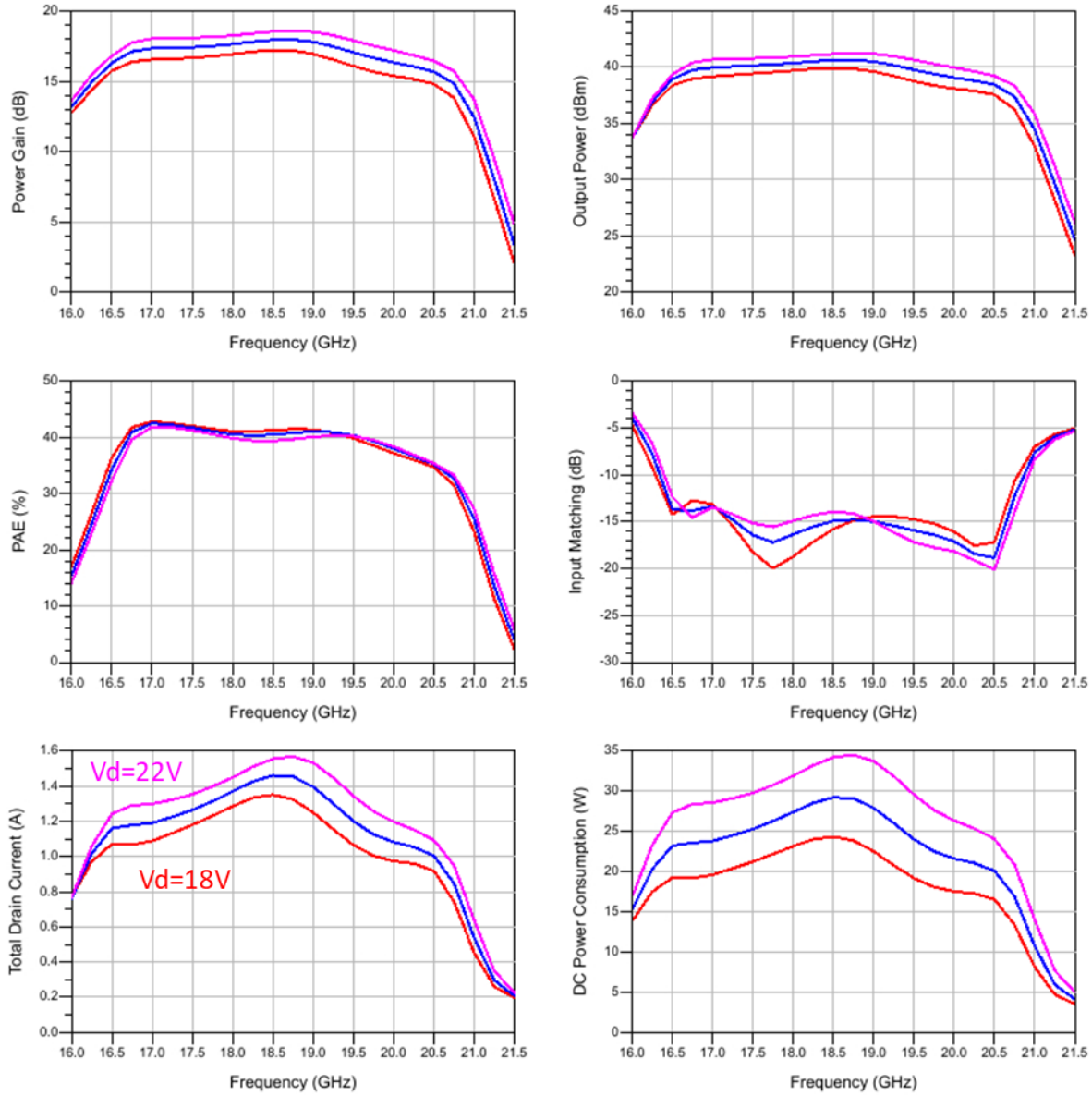


Figure 5-30 : Frequency sweeps at 23 dBm source power for Vd = 18, 20 and 22 V.

The process spreading for passive and active components will results in a frequency shift and performance variation. The main parameter that causes performance variation is the spreading of the MIM capacitor. The PDK capacitor definition has a uniform distribution of +/- 9%, which is a worst case assumption since the real variation will be gaussian. It was found that the effect of +/- 9% MIM capacitor variation on the large signal performance at a fixed source power resulted in a 800 MHz frequency shift. The current design is centred between 17-20 GHz, therefore some tuning to a bit higher frequency is required.

To include also the effect of other technology parameter variations, including the threshold voltage variation of the transistors, a Monte Carlo simulation showed that at the high-side of the specified bandwidth some more margin is needed.

5.2.7. Sensitivity to load variation

So far the performance simulations have been performed with the initial differential feed design as load for the HPA. In the actual implementation the load seen by the HPA might change, due to for example processing and assembly tolerances. Although the load of the initial feed design is very well matched (better than 15 dB), the use of an ideal 50ohm load will show a slightly different performance, as shown in Figure 5-31. The actual feed design introduces some band limitation at low frequencies, and a small reduction in PAE can be seen.

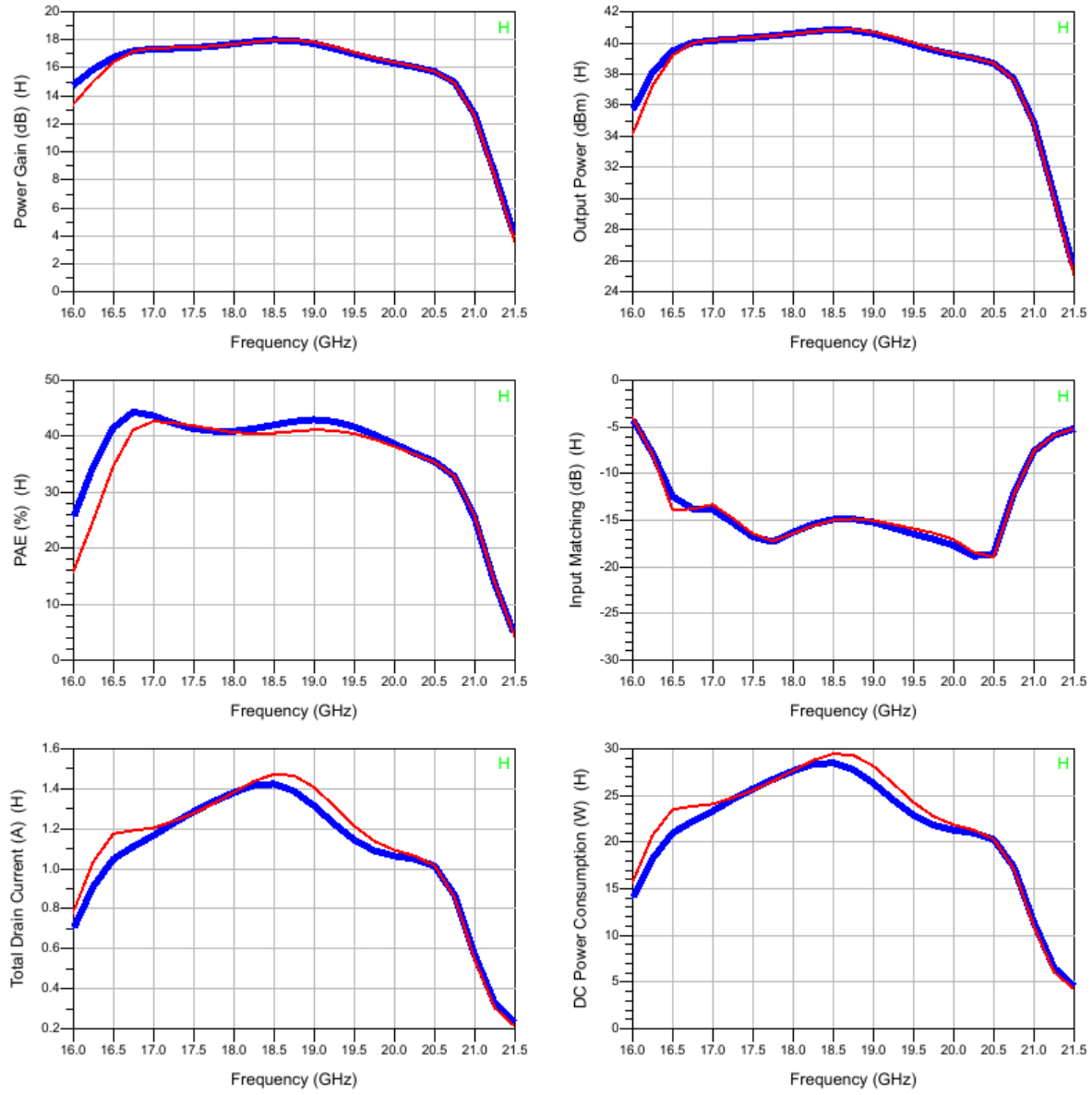


Figure 5-31 : Difference between the actual differential feed load (red) and an ideal 50ohm load (blue), at 23 dBm source power.

To analyse shows the impact of a varying load phase with 15 dB return loss, a simulation power sweep at 18.8 GHz was performed. The variation in peak PAE is about 5%, but for a few dB backoff the variation can be as high as 10% was found.

5.2.8. Linearity simulations

To check the linearity performance NPR calculations need to be performed. However, the AM/AM, AM/PM and the 2-tone IM3 simulations can already give some linearity estimate. It has been found experimentally that the IM3 – 4 dB gives a reasonable estimate of the NPR. Figure 5-32 shows the gain

and phase compression for 3 frequencies. Ideally this compression behaviour should remain constant over the specified bandwidth, but some variation is visible. Figure 5-33 shows the estimated NPR performance based on a 2-tone IM3 simulation. At the low-side of the band the 15 dB NPR point results in a good efficiency, however for the other 2 frequencies the PAE is still too low.

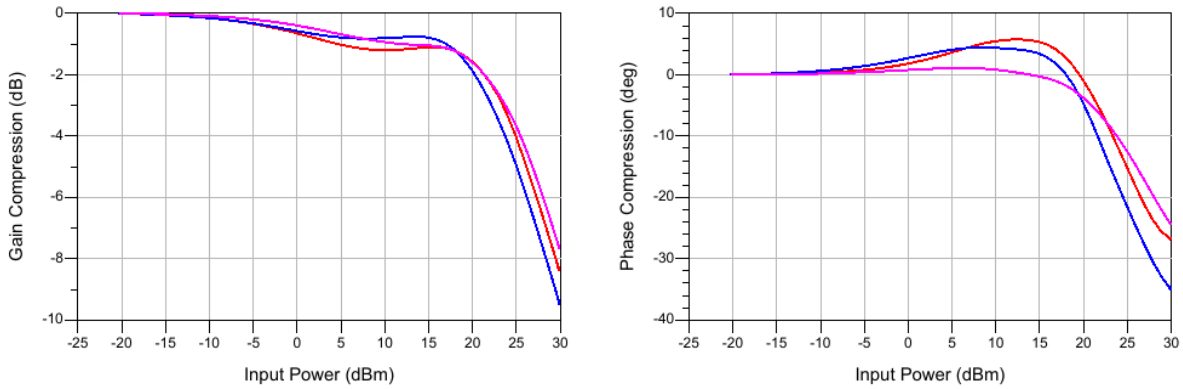


Figure 5-32 : Gain and phase compression at 17.3 GHz (red), 18.8 GHz (blue) and 20.3 GHz (magenta).

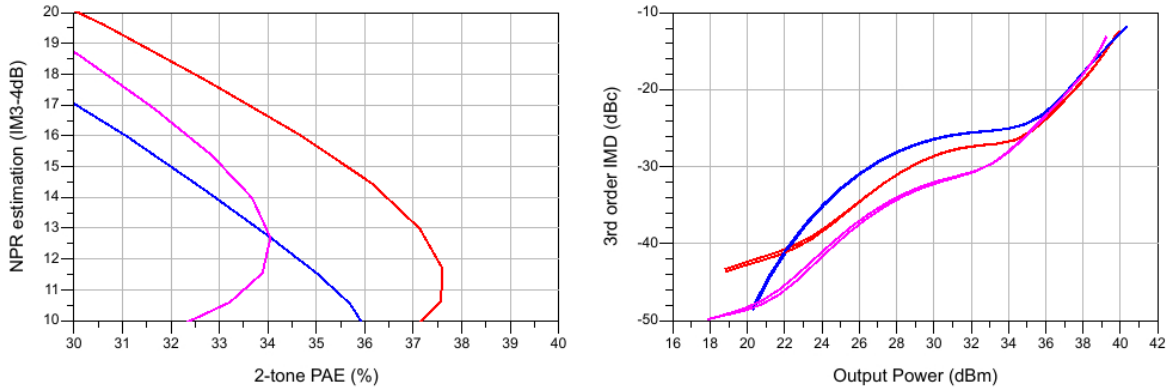


Figure 5-33 : Estimated NPR-PAE performance and IM3 at 17.3 GHz (red), 18.8 GHz (blue) and 20.3 GHz (magenta).

Table 5-12 shows the output power, NPR and PAE performance calculated with IMAL based on the single-tone power sweep simulation data. The trend predicted by IMAL corresponds with the 2-tone IM3 simulation, although the exact values are a differ slightly. At 17.3 GHz the 15 dB NPR point gives a good PAE, while for the other 2 frequencies the PAE is reduced, down to 32%. The output power specification of >37 dBm is achieved for 15 dB NPR but the PAE specification of >35% not yet.

Table 5-12 : IMAL results at 17.3, 18.8 and 20.3 GHz, for Vd=20V, Vg=-3.1V, Ta=80°C.

Frequency (GHz)	Pout (dBm)	NPR (dB)	PAE (%)	Pdc (W)
17.3	37.74	15.09	34.99	16.7
18.8	37.68	14.98	32.32	17.9
20.3	37.50	14.95	32.86	16.6

NPR can be optimized by tuning the gate bias also, including using a different gate bias value for the first and second stage. 2-tone ADS simulations have been used to find the best optimum, followed by an NPR calculation for this operating point. First a small sweep of the gate bias voltage has been done, including the IMAL calculations. The gate bias voltage has a large impact on the AM/AM and AM/PM behaviour, as shown in Figure 5-34. However, the resulting PAE at 15dB NPR, calculated with IMAL, shows almost no impact of this gate voltage variation, as shown in Figure 5-35.

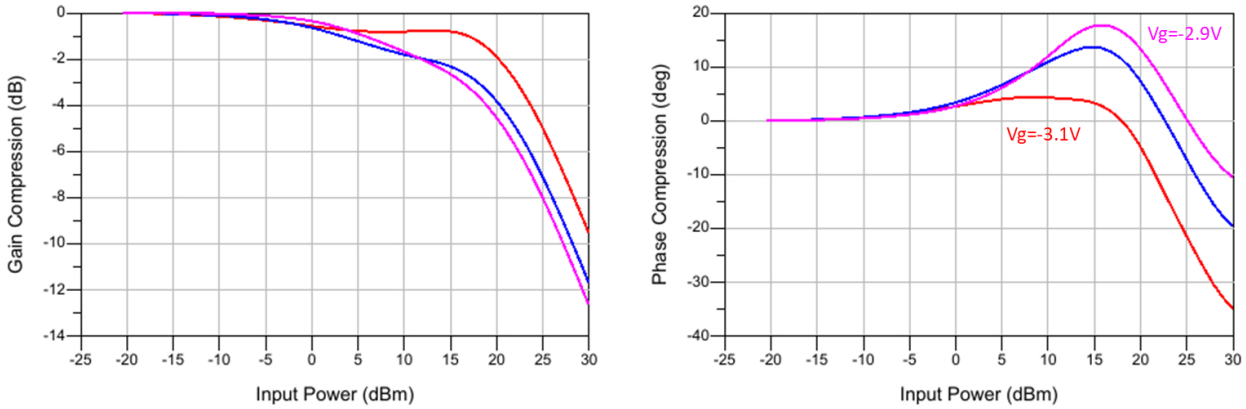


Figure 5-34 : Power sweep at 18.8 GHz, Vd=20V, Ta=80°C, for Vg=-3.1 to -2.9 V.

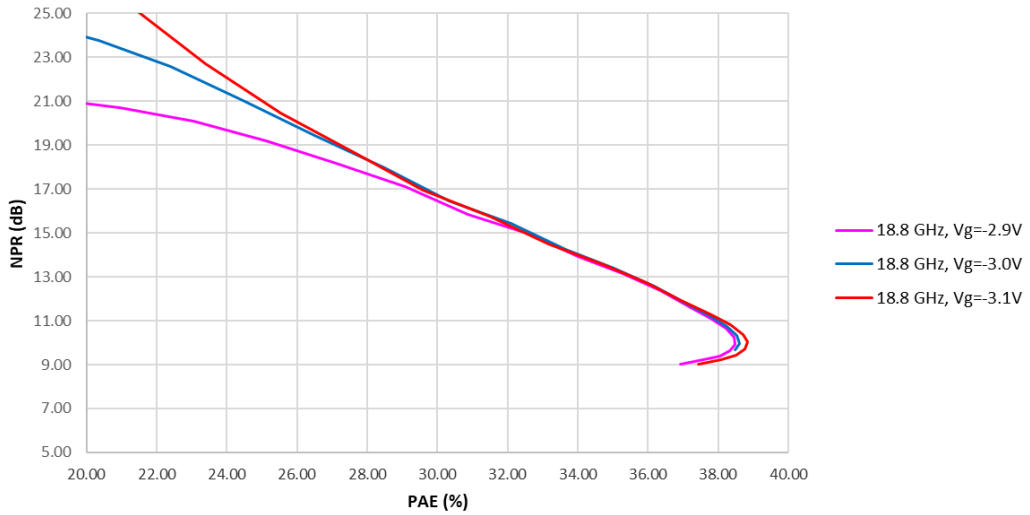


Figure 5-35 : IMAL calculation at 18.8 GHz, Vd=20V, Ta=80°C, for Vg=-3.1 to -2.9 V.

The ADS 2-tone IM3 simulations using different gate bias voltage for the first and second stage showed that a slight improvement in linearity can be achieved. The best IM3-PAE result was obtained at Vg1=-2.9V and Vg2=-3.1V. However the improvement is negligible.

5.2.9. Stability

A small-signal stability check has been performed at the input and output, to check unconditional stability for any source and load impedance. This S-parameter analysis has been performed over a range of gate and drain bias voltages. Figure 5-36 shows that there is no gain outside the intended band. The calculated stability factor, shown in Figure 5-37 does show a potential issue below 700 MHz. For now this is not considered as a big issue and it will be looked into during the detailed design.

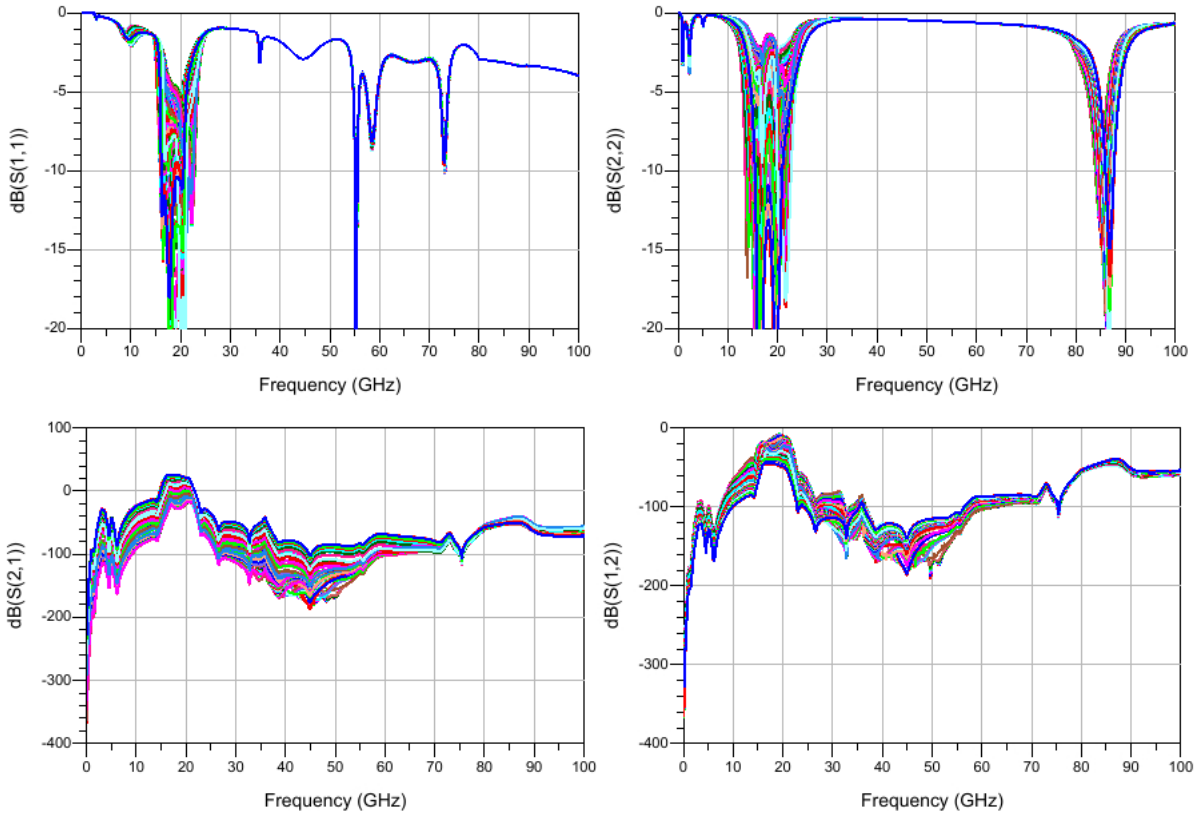


Figure 5-36 : S-parameters for Vd = 2 to 20 V and Vg = -5 to -2 V.

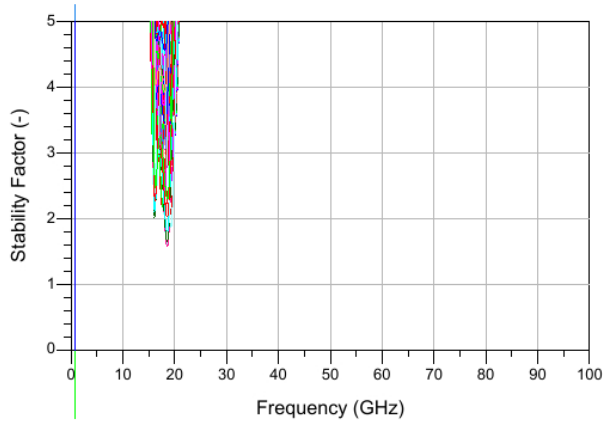


Figure 5-37 : Calculated stability factor from the S-parameter simulation for Vd = 2 to 20 V and Vg = -5 to -2 V.

Loop-gain stability analysis has been performed using the “Winslow probe” in ADS. These probes are located at the gate and drain of each transistor. The analysis resulted in a stable design.

5.2.10. Co-design analysis

Co-design was also considered to reduce the overall losses in the output matching. Using co-design the antenna impedance will be matched to the load required by the transistors, without using an on-chip matching network, or with a reduced matching network. Figure 5-38 shows the impact of using a lower on-chip output impedance on the expected loss of the matching network. A lower impedance will result in a lower loss, except when there is a small resistive part present at the low impedance point, such as

caused by a bondwire transition. A single gold bondwire (25 um diameter) has about 0.25ohm series resistance at 20 GHz.

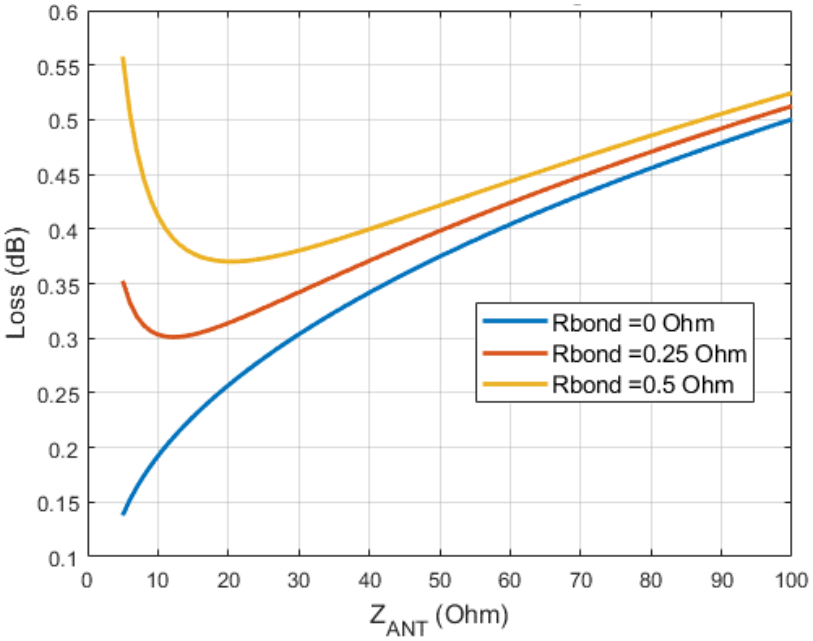


Figure 5-38 : Example simulation of the impact of the series resistance of a bondwire on the loss of the output matching at 18.8 GHz.

Co-design has been disregarded in the preliminary design because the loss of the bond wires would result in a similar overall transmission loss. Furthermore, it is not easy to design the antenna feed in a lower impedance within the given design rules and available materials for the PCB. Therefore, co-design using a lower impedance at the MMIC output is not considered to be a useful option.

5.2.11. Cgd compensation

The non-linearity of a transistor is mainly caused by the non-linearity of the transconductance and the non-linearity of the input capacitance. The non-linearity of the input capacitance is partly caused by Cgd. When a 180deg out of phase copy of the output signal is available, such as in a differential amplifier, this Cgd can be neutralized and this might have an advantage on the linearity. Figure 5-39 shows a possible implementation of such neutralization in a differential amplifier.

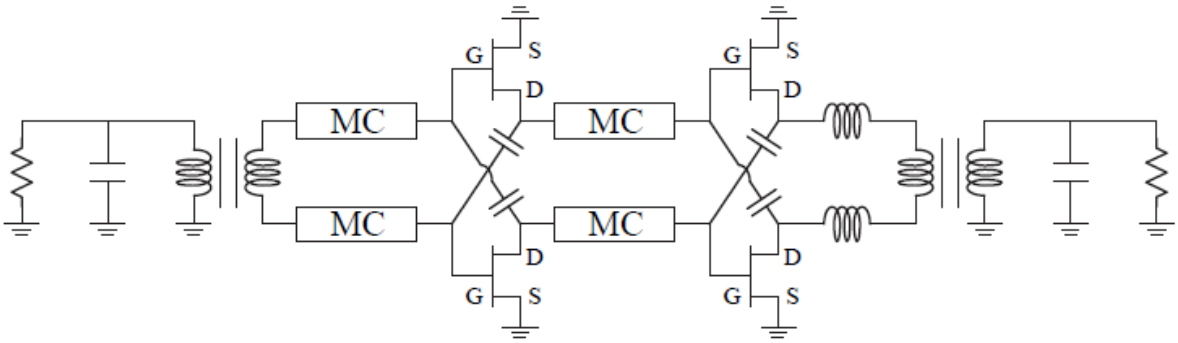


Figure 5-39 : Possible Implementation of the capacitance neutralization.

The capacitance neutralization analysis has shown that using capacitance neutralization does not result in an efficiency improvement at 15 dB NPR and that it is unpractical to realise such a feedback in a realistic high-power amplifier design. Therefore this option is not further explored.

5.2.12. Baseline HPA Conclusions

Based on the front-end and MMIC specifications, and on the verification of the GH15 PDK models by load pull measurements, an initial MMIC design has been performed. Several design options to further improve the performance, such as co-design and capacitive neutralization, have been explored, but have not resulted in a potentially improved performance. The simulation results and compliancy of the current design are shown in Table 5-13. This current design is based on PDK models, and some smaller parts simulated with Momentum, and is intended to get an estimate of the final performance. At this stage of the design no overall optimization of the performance has been performed yet. During the detailed design the matching networks will be optimized further and fully simulated in Momentum.

Table 5-13 : HPA MMIC compliancy with specifications.

Parameter	Specification	Simulation	Compliant?
Frequency range	17.3 – 20.2 GHz	17.3 – 20.2 GHz	By design
Input Return Loss	> 15 dB	> 12 dB	No
Output power @ 15dB NPR	> 37 dBm	> 37.5 dBm	Yes
PAE @ 15 dB NPR	> 35%	> 32%	No
DC power consumption	< 14.3 W	< 17.9 W	No
Linear gain	> 20 dB	> 20 dB	Yes
Temperature (MMIC backside)	20°C – 80°C	80°C	By design
Maximum junction temperature [1]	160°C	< 140°C	Yes

With respect to the simulated performance and non-compliancies the following observations can be made:

- The input return loss can be further optimized, and will also need to include the transition from PCB to MMIC, which is not yet the case. To make the input return loss more constant versus gate bias some extra loss (in the form of for example an RC stability network or small series resistor in the gate) might be needed.
- The PAE at 15 dB NPR is difficult to achieve, and it has also proven to be difficult to identify which parts of the HPA design have the most impact on this performance figure. That makes it difficult to optimize for the best PAE-NPR performance.
- The DC power consumption has been defined such that is corresponds exactly to the specified PAE and output power values. So as soon as the output power is slightly higher than specified (0.5 dB in the current design) the DC power consumption will already be too high, even at 35% PAE.

5.3. Preliminary Waveguide and Waveguide Feed Design (WP 2.2)

The waveguide feed specification can be seen in Table 5-11. The radiating front-end will be part of an array organised in an hexagonal lattice defined through dimension *d*, see Figure *5-40*. The loss of the waveguide feed is the critical parameter in this design.

Table 5-14 : Waveguide feeder specification.

Parameter	Specification
Frequency range	17.3 – 20.2 GHz
Input Return Loss	> 15 dB
Polarisation	CP (switchable)
XPD (AR)	>30dB (<0.58dB)
Beam scan maximum	8.7°
Hexagonal lattice	d = 51.9mm
RF input impedance	50Ω or co-design
Loss	0.6dB

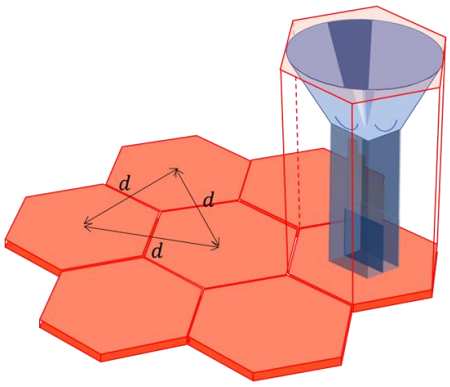


Figure 5-40: radiating front-end in a hexagonal grid

It should be noted that the loss specification applies to the reference plane A as indicated in Figure 5-41. Therefore, it includes the bond wire(s) connecting the MMIC pads to the waveguide feeder transmission (TL) line, i.e. MMIC to PCB transition.

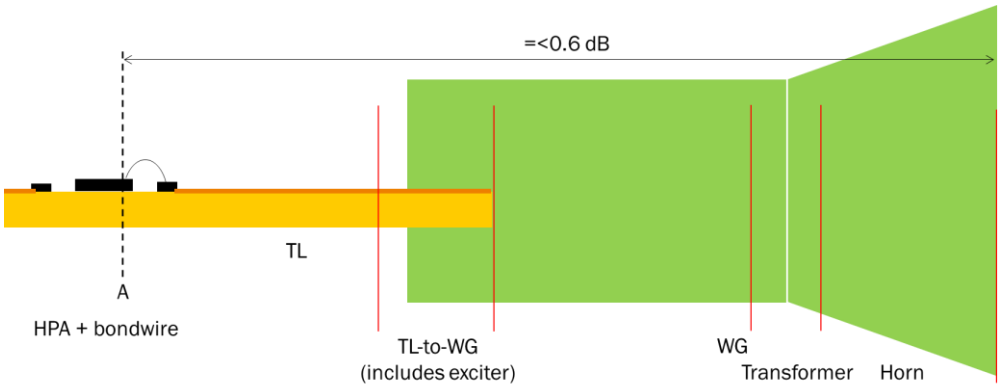


Figure 5-41: Schematic representation of the relevant front-end radiation section defining the loss indicated in Table 5-11.

Technology

The waveguide feed concept shall use a 4-layer PCB stack as shown in Figure 5-42. The 4-layer PCB stack has the benefit of increasing the panel stability and provides a shielded entrance for electromagnetic waves in the waveguide. The differential line, in a strip line environment, is shielded by ground planes on top (L0) and bottom (L3), with waveguide walls connecting to L0 and L3.

Rogers RO3003 is chosen as the base material for low losses, bonded with Rogers 2929-Bond ply. Core thicknesses are equal (t0 = t2), with t1 to be determined.

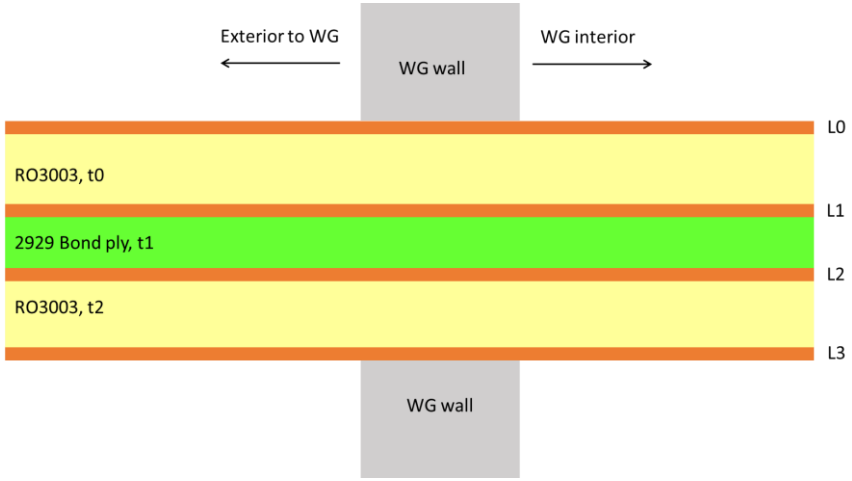


Figure 5-42: Layer stack definition for the waveguide feeder concepts. (a) L0 and L3 are closed copper GND planes connecting to the waveguide wall.

5.3.1. Waveguide feed designs for rectangular interior

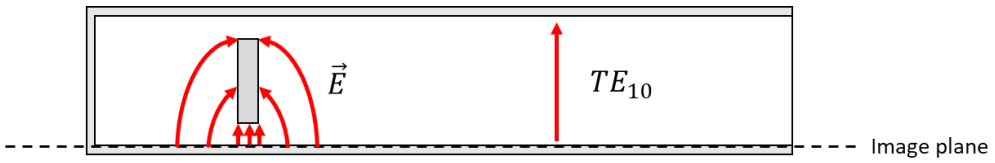
To efficiently excite the fundamental mode of the rectangular waveguide (TE10), the feed design should optimally generate field components that match the distribution of the TE10-mode inside the guide. A number of options exist to do this, and, implementing a PCB does not limit this range. In fact, using a PCB even generates additional options next to the classic solutions like an E-probe or an H-probe.

Manufacturing does give rise to special attention in making the connection between two different technologies work. This especially entails interfacing relatively large surfaces of copper with the waveguide material. Applying PCB however presents the option to exclude cabling and make the ultra-short connections we look for.

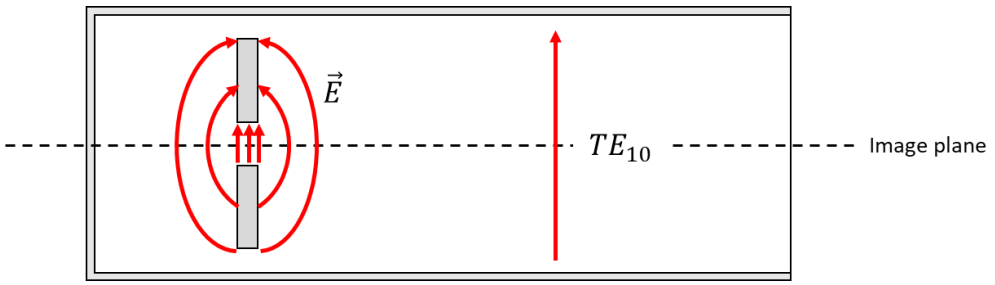
For the simulation models a standard sized waveguide for K-band applications has been implemented. In particular WR-42 having a cross-section size: 4.318 x 10.668 mm^2, which incorporates a cut-off frequency of 14.3GHz.

Dipole

The dipole waveguide feed can be envisaged simply by mirroring the standard E-probe (monopole) in the waveguide bottom wall where it protrudes from, see Figure 5-43. Both a monopole and a dipole can be etched on a PCB to couple to the waveguide mode. At the best the PCB is placed in the guide's centre parallel to its longitudinal axis. Another condition and an important parameter is the distance of the exciter from the guide's back wall, which should be in the order of a quarter of the guided wavelength at the highest frequency of interest.



(a)



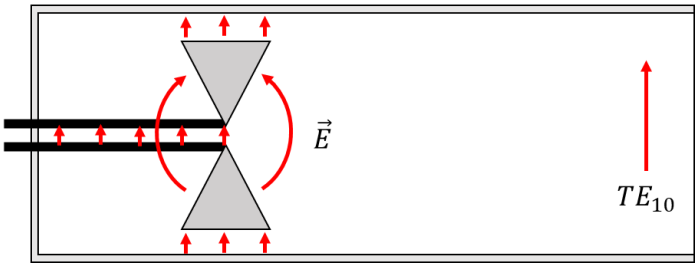
(b)

Figure 5-43 : (a) Monopole (E-probe) in waveguide to excite the fundamental waveguide mode, and (b) from image theory two monopoles generate the same field configuration and compose exactly a dipole.

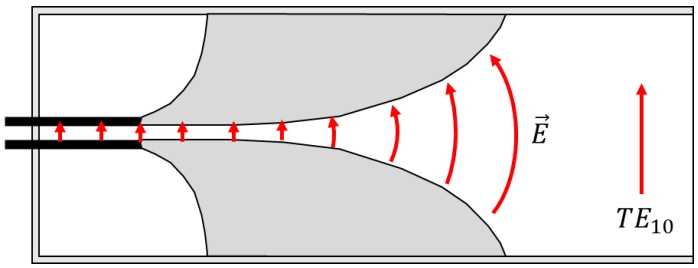
A dipole is narrow band in nature if it is designed as a narrow piece of straight printed copper. In PCB technology there are several options to increase its bandwidth, such as adding parasitic elements, making it more bulky, and/or giving it a specific shape. Which method to apply depends on the requirements in terms of bandwidth. Giving it a different shape is here found to be sufficient and it exists in creating a linearly tapered shape starting narrow at the feeding line and becoming wider at the dipole ends, see Figure 5-44(a). Such a dipole is sometimes also referred to as a bow tie radiator.

Vivaldi

Next to the dipole also a so-called Vivaldi radiator can be applied. Such a radiator has its outline mathematically defined by an exponential curvature. In the current application there are two of such curvatures defined and implemented of which the rates (of curve growth) are used as design parameters. A prominent difference with the dipole exciter is that the extremes of the Vivaldi arms are in direct contact with the waveguide wall, see Figure 5-44(b). Whereas those of the dipole are not, allowing for field lines to exist between them and waveguide walls thus contributing to the matching performance.



(a)



(b)

Figure 5-44 : (a) Dipole with feeding differential line entering waveguide to excite the fundamental waveguide mode, and (b) case Vivaldi.

Patch

In case of a hybrid architectural approach, excitation of the TE10-mode seems best done with use of a patch radiator. Such a patch can easily be fed with a differential line to make it radiate. In [18] suggestions have been given to dimension such an exciter, which have been scaled for it to work at the frequency range for the current application. For bandwidth increase a parasitic patch is present in close proximity to the active patch. Gaps between the radiating edges of the patches and the waveguide walls are design parameters, just like the gap between the patches and foremost the length of the active patch. This length should be long enough the field coming off the patch to efficiently couple with the TE10-mode. Shown in Figure 5-44 are the field lines generated by the patch edges: these will, while progressing into the guide, line up and continue as a waveguide mode. As is the case with classical microstrip line fed patches, this patch also has an insert to optimise matching to the differential line.

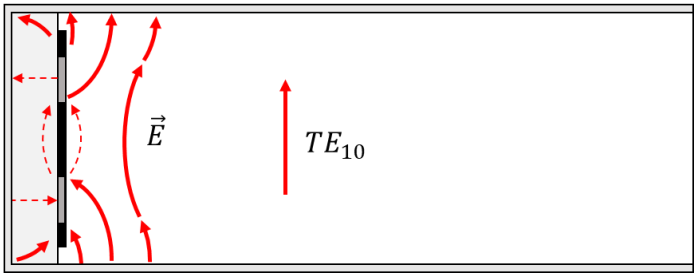


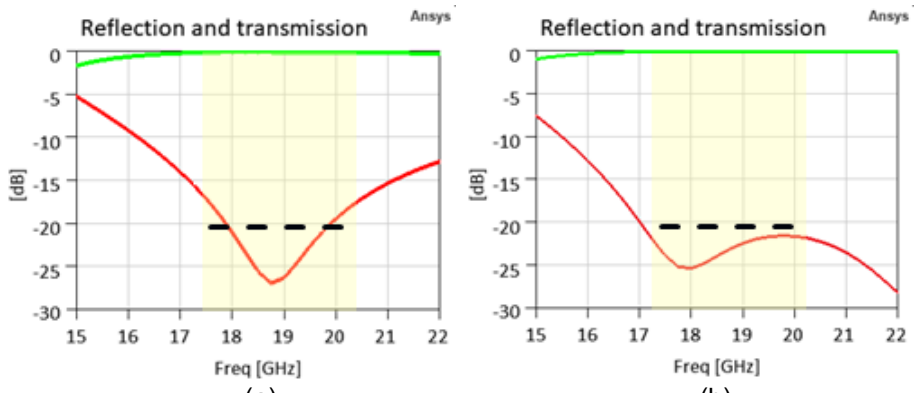
Figure 5-45 : Substrate hosting differential feeding line and patch placed on the back wall of the waveguide interior. Structure is observed looking along the differential line (two light grey rectangles), the differential mode field lines are dashed.

Both exciter types have been parametrically defined and simulated using a finite element method (FEM) modeler. Simulated results in terms of the scattering parameters and losses are visualised in Figure *5-46*. Indicated losses, shown in the graphs of Figure *5-46*, respectively reflection- (RL) and insertion loss (IL) are defined as follows:

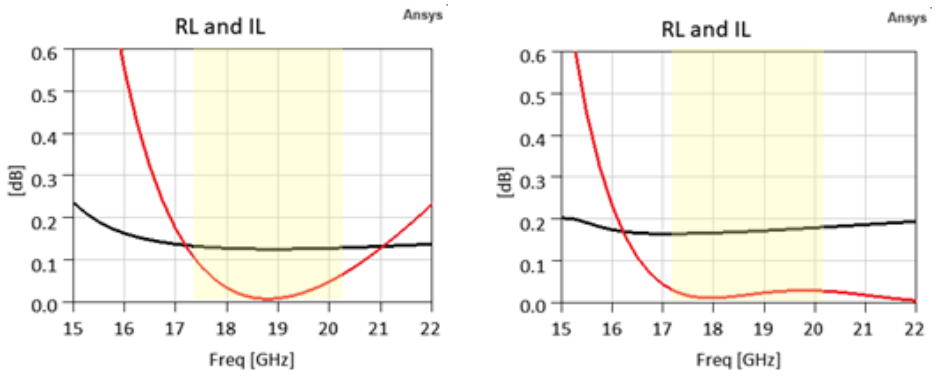
$$RL = 10log_{10}\left(\frac{1}{1-|S_{11}|^2}\right)$$

and

$$IL = 10log_{10}\left(\frac{1-|S_{11}|^2}{|S_{21}|^2}\right)$$

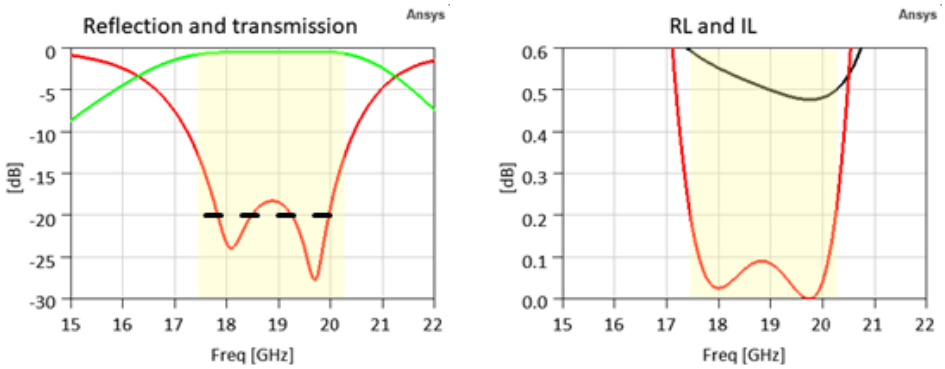


(a) (b)



(c) (d)

Figure 5-46 : (a) and (c) reflection (red) and transmission (green) performance in case of respectively the dipole and Vivaldi exciter. (b) and (d) losses idem, RL (red), IL (black).



(a) (b)

Figure 5-47 : (a) Reflection and transmission case patch exciter, and (b) losses RL (red), IL (black).

From the graphs it shows that the Vivaldi inherently is of a more wideband nature, although that of the dipole can be made more wide as will be shown later on in this report. The patch does not have a potential to become more wideband. Apart from this it also shows much higher insertion loss than the other two exciters. Next to the patch being a resonant structure that can carry high current densities across it resulting in relatively high dissipation, it also requires an impedance transforming line adding up to these losses. The losses of the Vivaldi are higher than that of the dipole as the currents encounter more material as they pass through it.

The patch has been included in this study to better justify the industrially preferred choice of the brick (or in line) architecture over the hybrid architecture. Direct comparison between brick type and hybrid type of exciters immediately clarifies that both the dipole and Vivaldi clearly outperform the patch and the latter, together with the hybrid architecture, will not be further pursued.

5.3.2. Waveguide feed designs for semi-circular interior

Square input sections to conical horns are not commercially available though they can be made. However to ensure a smooth transition and minimise losses a fully circular waveguide shall be investigated and compared to a rectangular wave guide. The model change incorporating the shift from a rectangular to sCWG is shown in Figure 5-48.

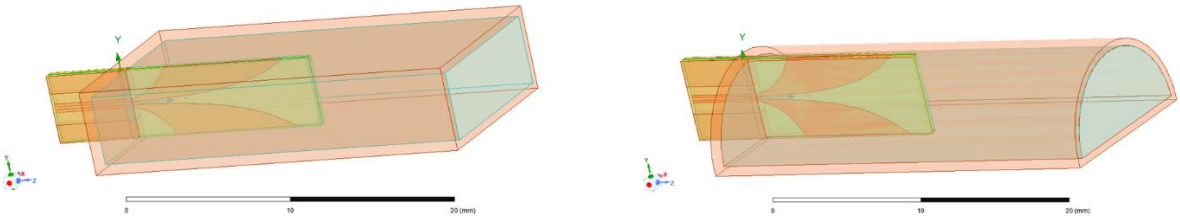


Figure 5-48 : (a) Vivaldi exciter in rectangular, and (b) semi-circular waveguide.

In order to further push the losses to lower values also different materials were implemented. Where a start was made with RO4350B which is a hydrocarbon based material with woven glass, also the case with RO3003 which is a Teflon based material, has been considered. The latter incorporates a significantly lower loss tangent (1/1000) compared to that of the former which is almost 4 times higher. The simulation comparison between rectangular and semi-circular waveguides showed that the change in waveguide shape does not affect performance, despite a shift to higher frequencies, which can be optimized. The models remain wideband. The switch to Teflon-based substrate reduces insertion losses by 0.1 dB. Despite its machining and bonding challenges, Teflon is chosen for future designs.

5.3.3. Septum polarizer

It is expected that the polarizer's contribution to the losses will be minor and that it will not interfere significantly to the scattering performance. The main design effort in this preliminary design phase has therefore been placed in the actual performance of purely the transition from the exciter's input transmission line to the waveguide interior.

In Figure 5-49 isolated septum polarizer models are shown. As the model in Figure 5-49a involves a lot of parameters to vary (2 for each discrete step, i.e. height and length of the step), it will also requires a lot of variations to find the best result. The combination of discrete steps can however be approximated by an exponential curve which only incorporates two parameters to vary, i.e. length and rate of decay. This model has been used to relatively quickly find a well performing polarizer design to subsequently assess overall exciter + polarizer design.

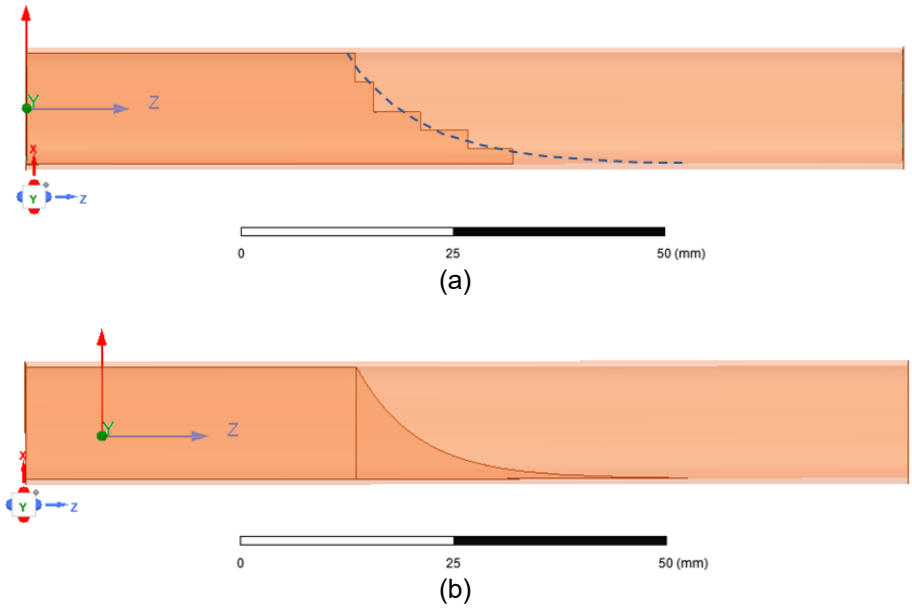


Figure 5-49: Septum simulation models. (a) Discrete steps, (b) continuous.

Scattering behavior of this four-port network (circular waveguide section can accommodate two orthogonal TE11 modes) is visualized in Figure 5-50. From Figure 5-50(a) it is clear that there is an

imbalance in the power that couples from the single input to the two TE11 modes. Where the one transmission coefficient is somewhat higher than –3dB the other is somewhat lower than –3dB. This will affect the quality of the circular polarization axial ratio. Both input ports are however well matched. Figure 5-50c indicates the phase difference between the excited orthogonal modes TE11x and TE11y. Ideally for this simulation it should be 90°, and deviates from this on average 15° in the frequency range of interest. The stepped septum polarizer has the best performance.

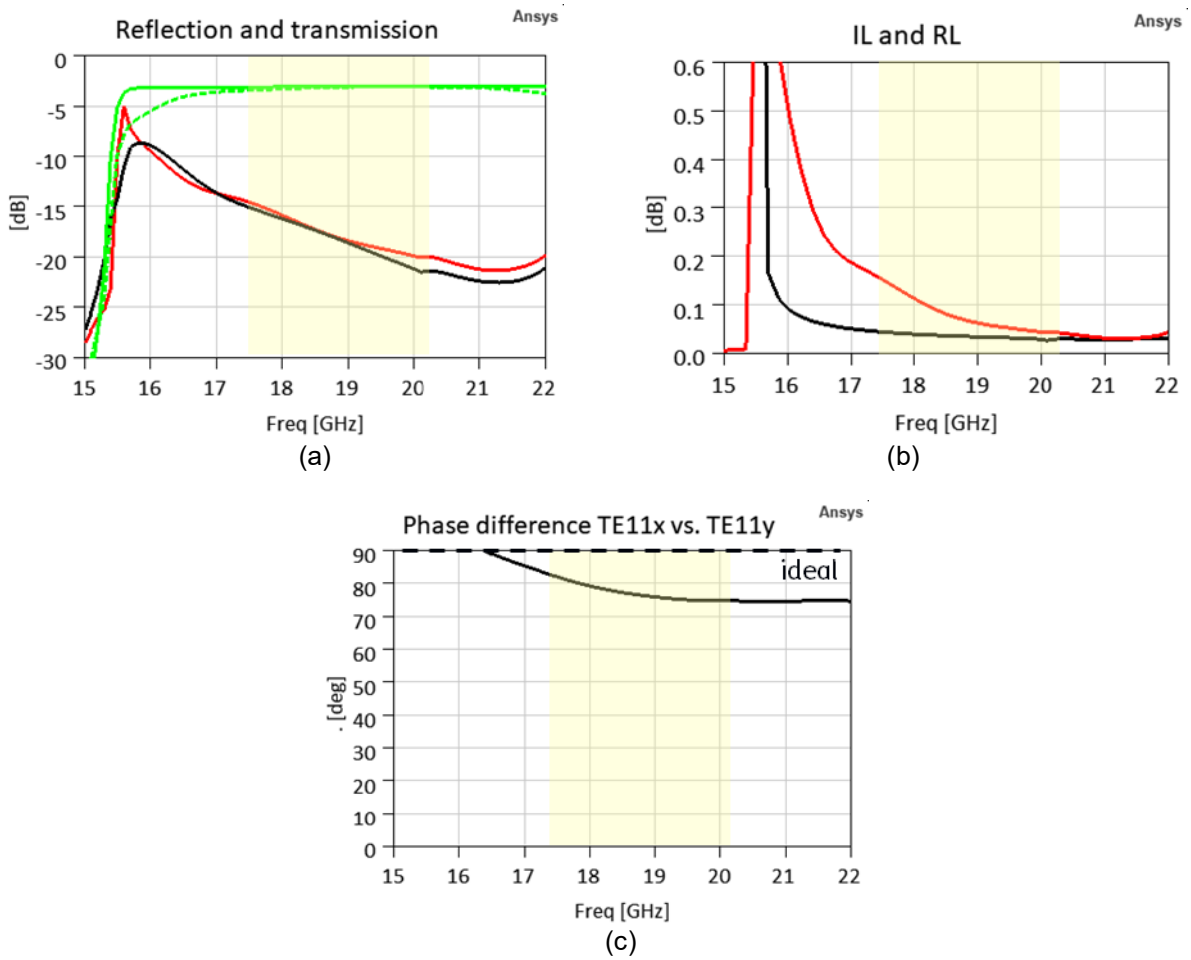


Figure 5-50: Septum polariser performance. (a) S-parameters: transmission to the fundamental orthogonal modes TE11x and TE11y (green solid and dashed), reflection (red) and cross-talk to other input (black). (b) Losses, reflection loss (red) and insertion loss (black). (c) Phase difference between the two orthogonal modes (solid black).

5.3.4. Waveguide Cascaded Performance

A waveguide simulation with two Vivaldi exciters and the septum polarizer connecting to a circular waveguide has been performed as shown in Figure 5-51.

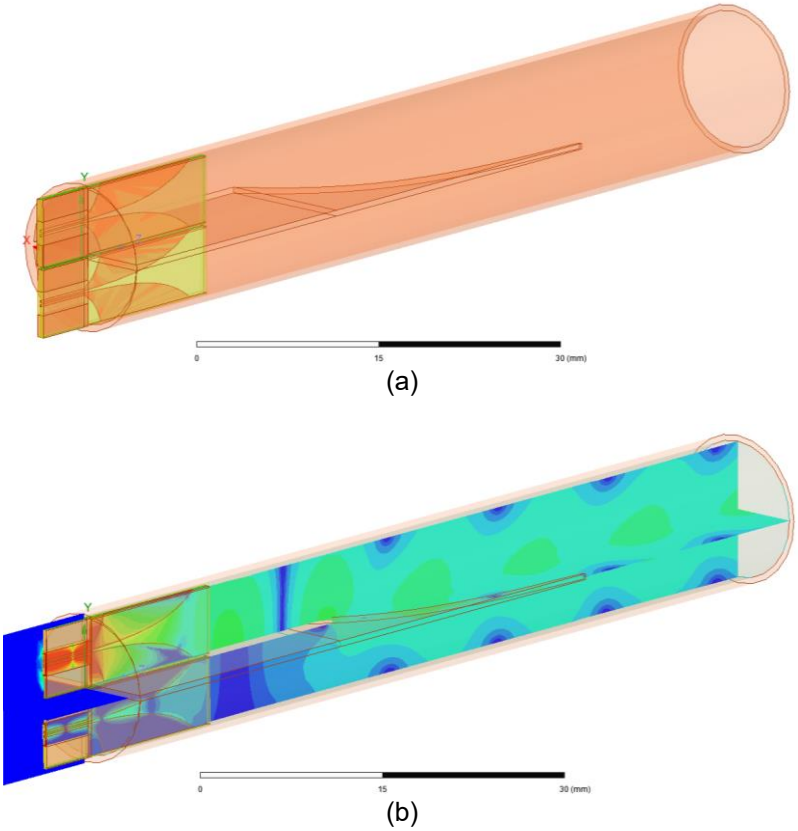
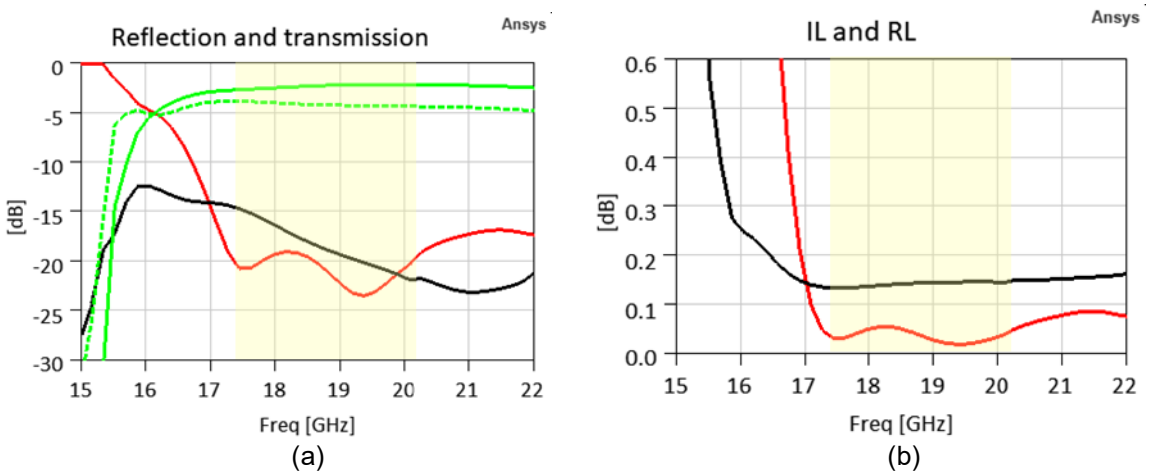
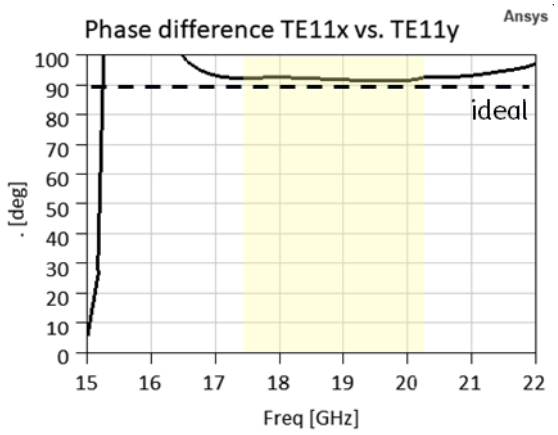


Figure 5-51: (a) Model including two exciters and the septum polariser. (b) Magnitude of the electric field distribution (logarithmic) at 19 GHz. Total length of the model is in the order of 55mm, excluding the length of empty circular waveguide.

In Figure 5-52 the performance of the cascade (exciter + polarizer + empty circular WG) is shown. The scattering parameters are presented in Figure 5-52a, and it shows that both the cross-talk and the reflection are either consolidated (cross-talk) or improved (reflection). What also shows is the fact that the amplitudes of both orthogonal modes TE11x and TE11y are not equally split, i.e. one is coupled more whereas the other less. In the end this would mean that the polarization will not be nicely circular but rather elliptical, it will induce reduced XPD. Figure 5-52c however, does show that the phase difference between these coupled modes tends towards the ideal 90° required for circular polarization.





(c)

Figure 5-52: Septum polariser performance. (a) S-parameters: transmission to the fundamental orthogonal modes TE11x and TE11y (green solid and dashed), reflection (red) and cross-talk to other input (black). (b) Losses, reflection loss (red) and insertion loss (black). (c) Phase difference between the two orthogonal modes (solid black)

When observing the losses in both cases it can be concluded that the presence of the septum polariser introduces about 0.1dB of extra insertion loss, where the reflection loss due to the combination (just as the phase difference between the modes) clearly benefits from the cascade.

Wave guide exciter designs

After serval Vivaldi and Dipole design cycles and discussions with the PCB manufacture the following design changes were made:

- Bonding material between the two substrates (was Rogers 2929 bond ply, became Rogers RO4450T for reasons of stability during the bonding process (less float))
- Drill hole sizes and accompanying annular ring sizes
- Displacement of vias and larger via spacing.

Both the Vivaldi and Dipole design final PCB layer stack-up with manufacturers ACB Atlantec is shown in Figure 5-53.

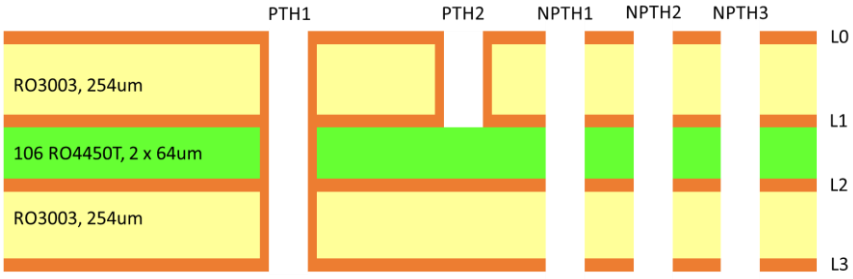
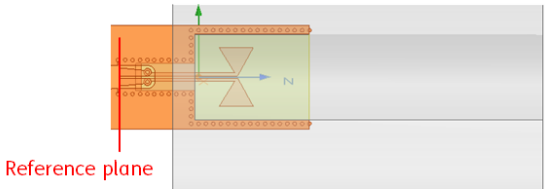
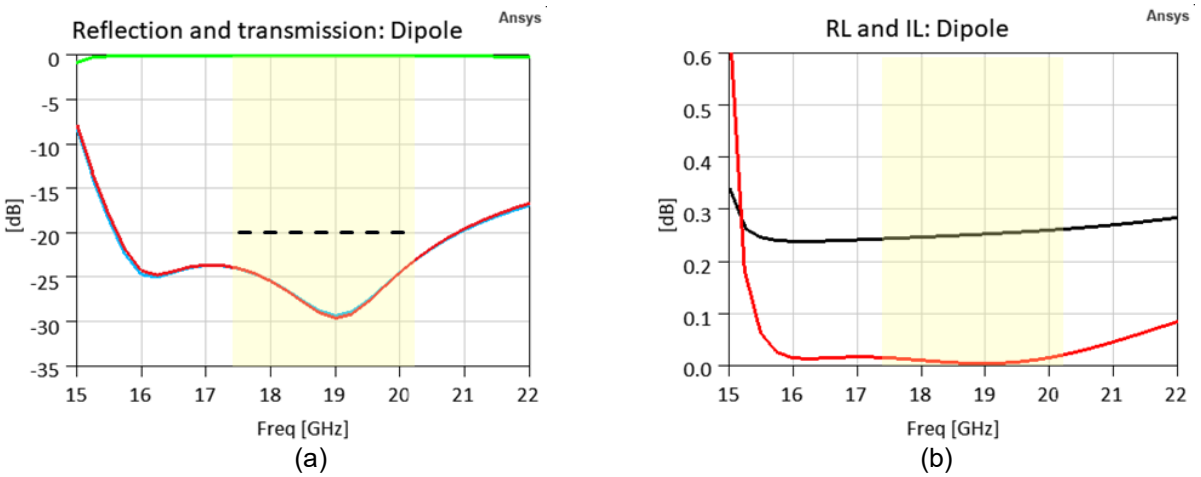


Figure 5-53: Layer stack used for the prototype PCBs. Also the different PTHs and NPTHs are indicated. The latter are necessary for mounting purposes (screws).

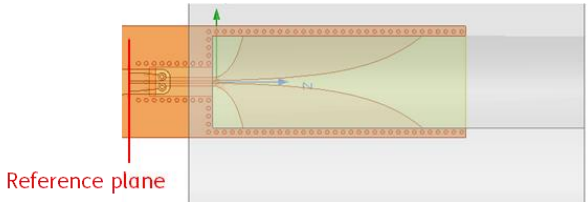
The tuned dipole and Vivaldi exciters in a sCWG are presented in Figure 5-55 and Figure 5-55 respectively.

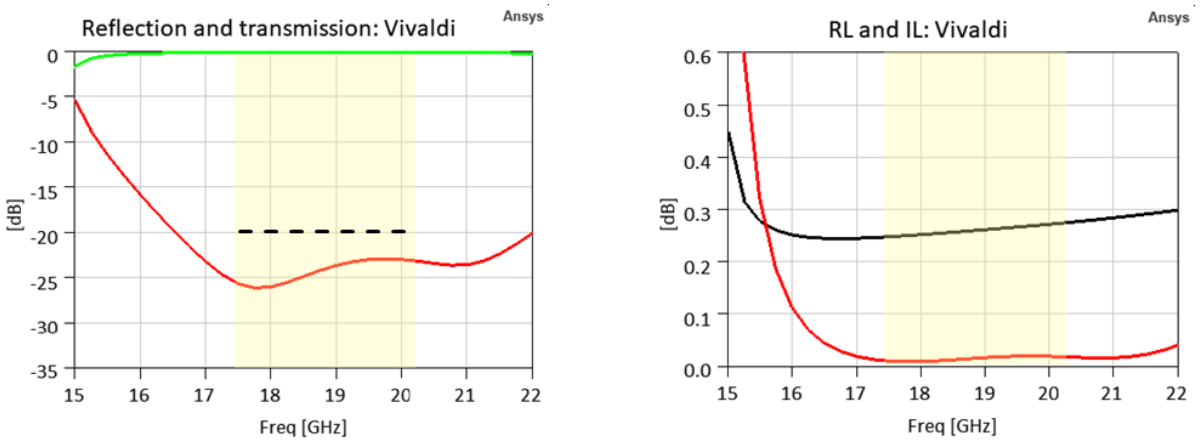




(a) (b)

Figure 5-54: Dipole exciter tuned performances. (a) Reflection and transmission, and (b) reflection- (red) and insertion (black) losses. Results are valid referenced to indicated plane in schematic.





(a) (b)

Figure 5-55: Vivaldi exciter tuned performances. (a) Reflection and transmission, and (b) reflection- (red) and insertion (black) losses. Results are valid reference to indicated plane in schematic.

Both exciters operate well across the frequency range of interest. Reflection levels are well below specification and very wide band. Losses are dominated by the insertion loss (material) and on average at 0.25dB and comparable for both.

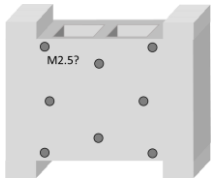
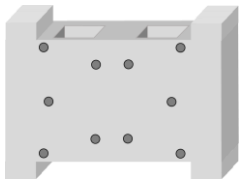
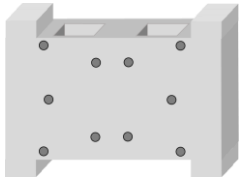
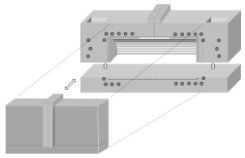
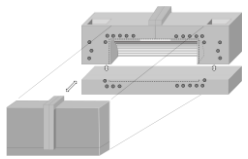
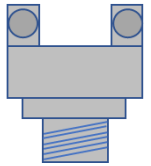
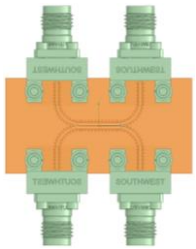
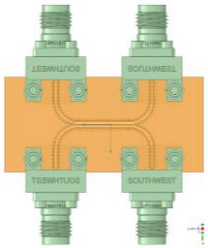
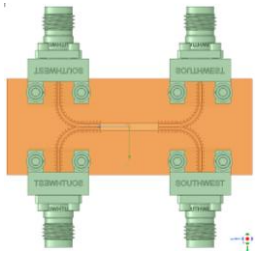
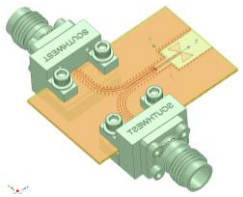
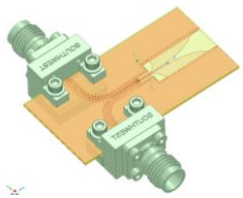
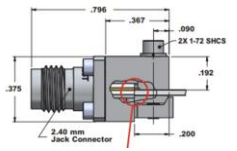
Production

Atlantec in France has been selected for production of the exciters together with the required calibration standards. This manufacturer is able to work with Teflon based substrate materials. Compared to the often applied Rogers 4000-series, which are hydrocarbon ceramic based substrates, the Teflon based materials require dedicated production lines and techniques to output multi-layer PCBs. ACB have very manufacturing lead time of 14 weeks.

5.3.5. Wave Guide Exciter Test Structures

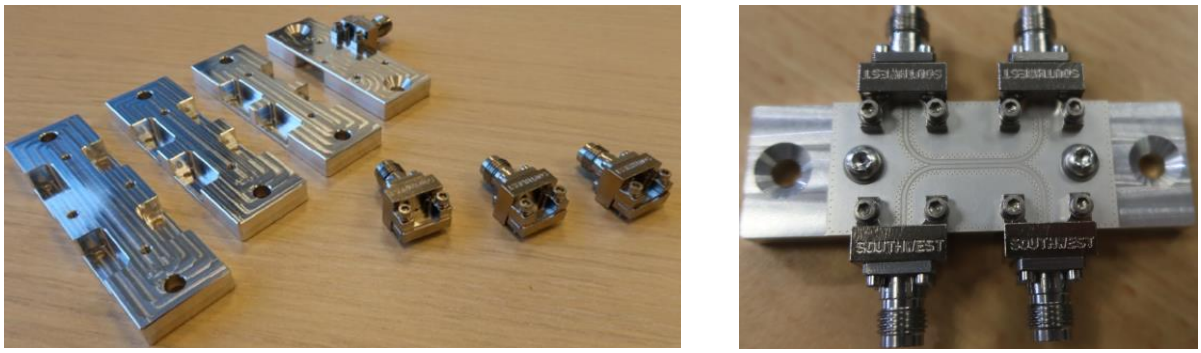
The wave guide test structures can be seen Table 5-15. It shows the required support structures made by the TNO workshop and the PCBs made by ACB Atlantec France. Also indicated is the type of coaxial connector suitable for the frequency range and transmission line dimensions. This connector is a high-end component to aid an efficient transition from coaxial cable to GCPW and is non-soldered to the PCB. As such it can be reused to connect to another PCB if treated well. The support structures are necessary to ensure a stable fixture on which the small PCBs can be mounted and also help to fix the connectors in a structurally sound way to the PCBs. In the table the PCBs are shown including the connectors for the purpose of creating an impression of the final product sizes.

Table 5-15 : Defined PCB products and accompanying support structures.

Structure	Through standard	Line standards	Reflect standard	Dipole exciter	Vivaldi exciter	Connector
Support	Type A 	Type B 	Type C 	Type D 	Type E 	Southwest purchase (10x) 
PCB				2x 	2x 	

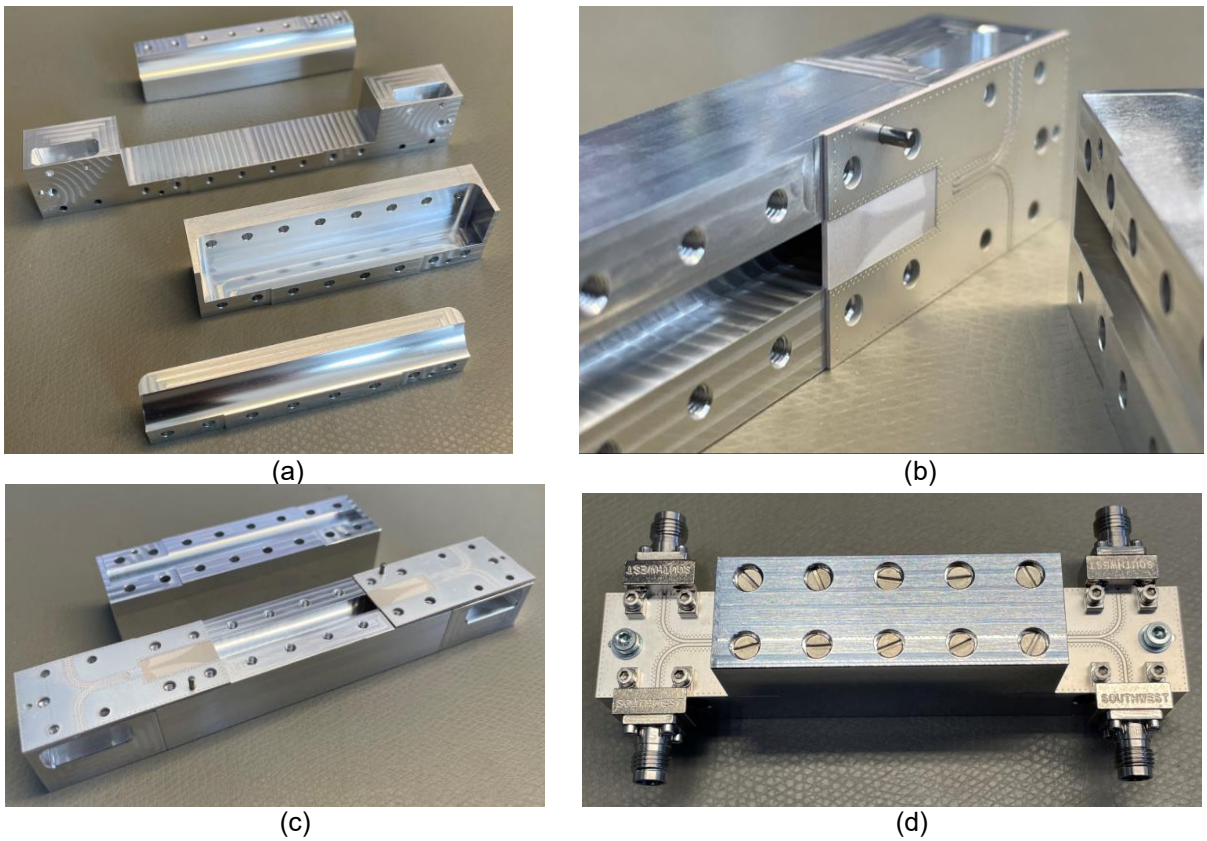
5.3.6. Waveguide Feed Test Structures (WP 2.3)

After several iterations and setbacks[1] the PCB products were finally delivered by ACB Atlantec. Production of the support structures were already completed well before by the TNO workshop EMA. The structures (aluminium) incorporating the sCWGs could only be completed upon receiving the PCB products. Reason for this is that the final thickness of the PCBs is not known beforehand (is a production variable) and must be known to enable finalization of the test structures where the exciter PCBs are to be integrated with. In the different products have been visualized.



(a) (b)

Figure 5-56: (a) Support structure for the calibration standards (TRL). (b) Mounted Through standard.



(a) (b)

(c) (d)

[1] These setbacks consisted in several delays on the side of ACB Atlantec and them ordering the wrong substrate material.

Figure 5-57: (a) Aluminium parts for the back-to-back exciter test structure. (b) Partially mounted Vivaldi exciter in test structure. (c) Full view on open back-to-back test structure, and (d) closed test structure including Southwest RF-connectors.

Measurements

After assembly of the test structures the measurements have been performed. The test setup is shown in Figure 5-58. It makes use of a Keysight 4-port PNA-X network analyser N5245B which can be used for a frequency range from 10MHz up to 50GHz

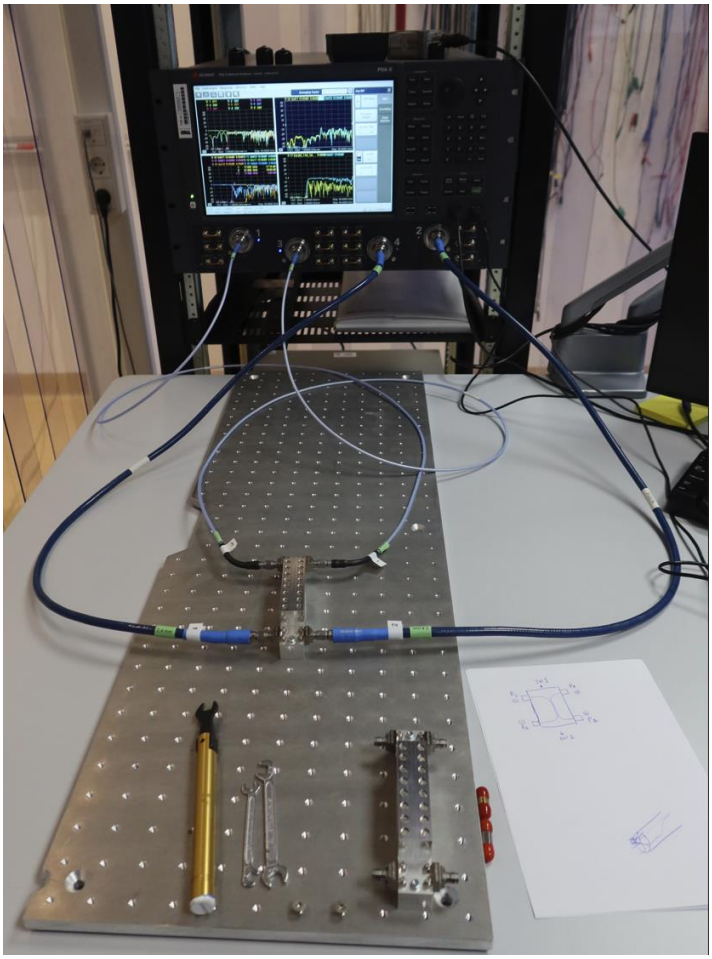


Figure 5-58: None of the important RF-PTHs that are present in the PCB products have been placed correctly. With reference to schematic of Figure 5-53 these relate to PTH2.

5.3.7. Dipole and Vivaldi waveguide feed measured results

Both the Vivaldi and Dipole wave guide exciters where measured and the comparison results (measured and simulated) are shown in Figure 5-59 and Figure 5-60. Unfortunately the preliminary wave guide exciters did not meet the 0.6 dB loss specification; yielding an insertion loss > 1 dB for both wave guide feed types.

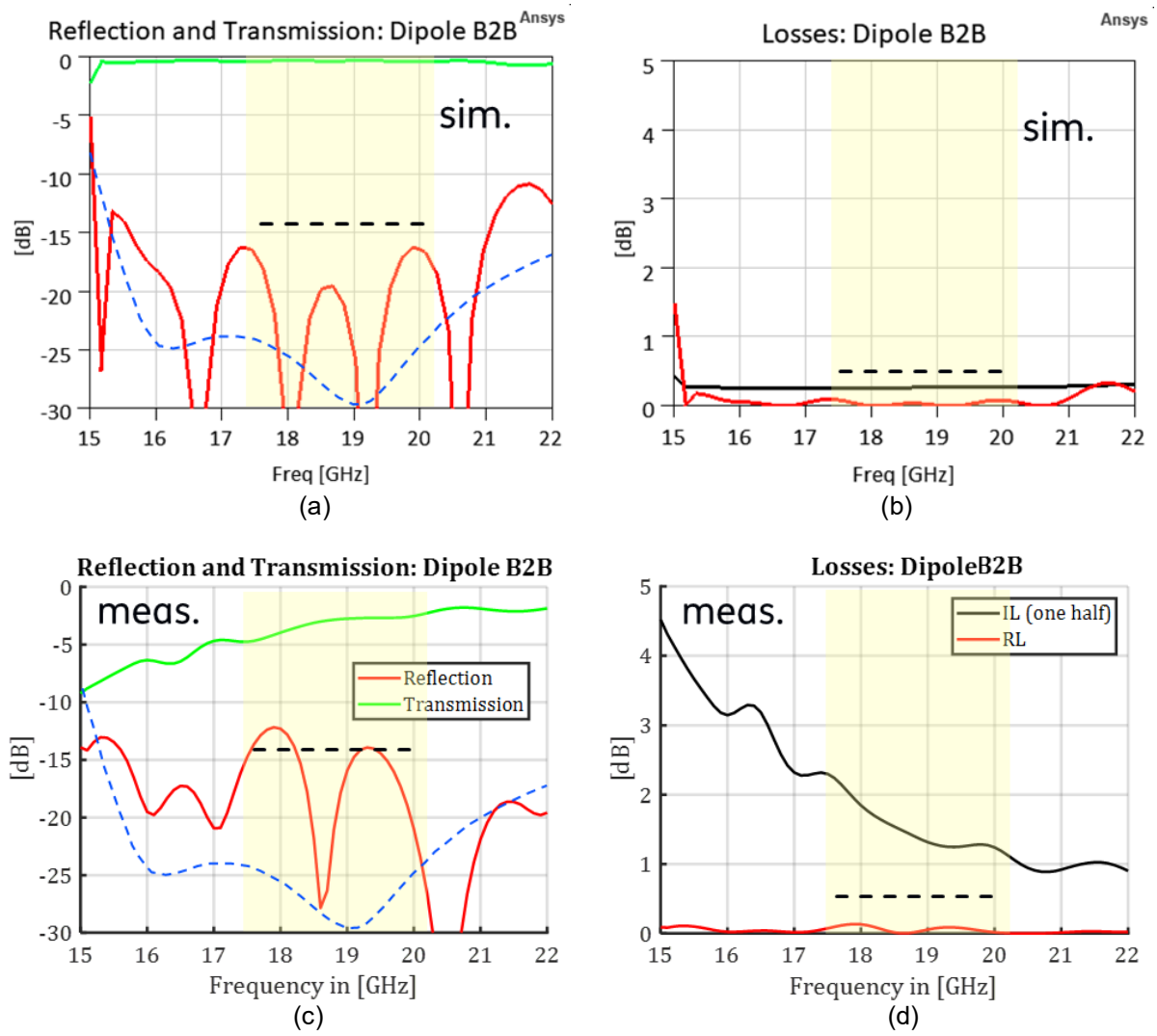


Figure 5-59: (a), (b) Simulated and (c), (d) measured results for the dipole exciter in a back-to-back (B2B) configuration. (a), and (c) reflection (red) and transmission (green) respectively simulated and measured. (b), and (d) reflection- (red) and insertion (black) loss respectively simulated and measured. The insertion loss has been compensated by ½ to arrive at the single transition loss. Note the insertion of the blue dashed line which represents the reflection of a single dipole exciter connected to a sCWG as shown in Figure 5-54a.

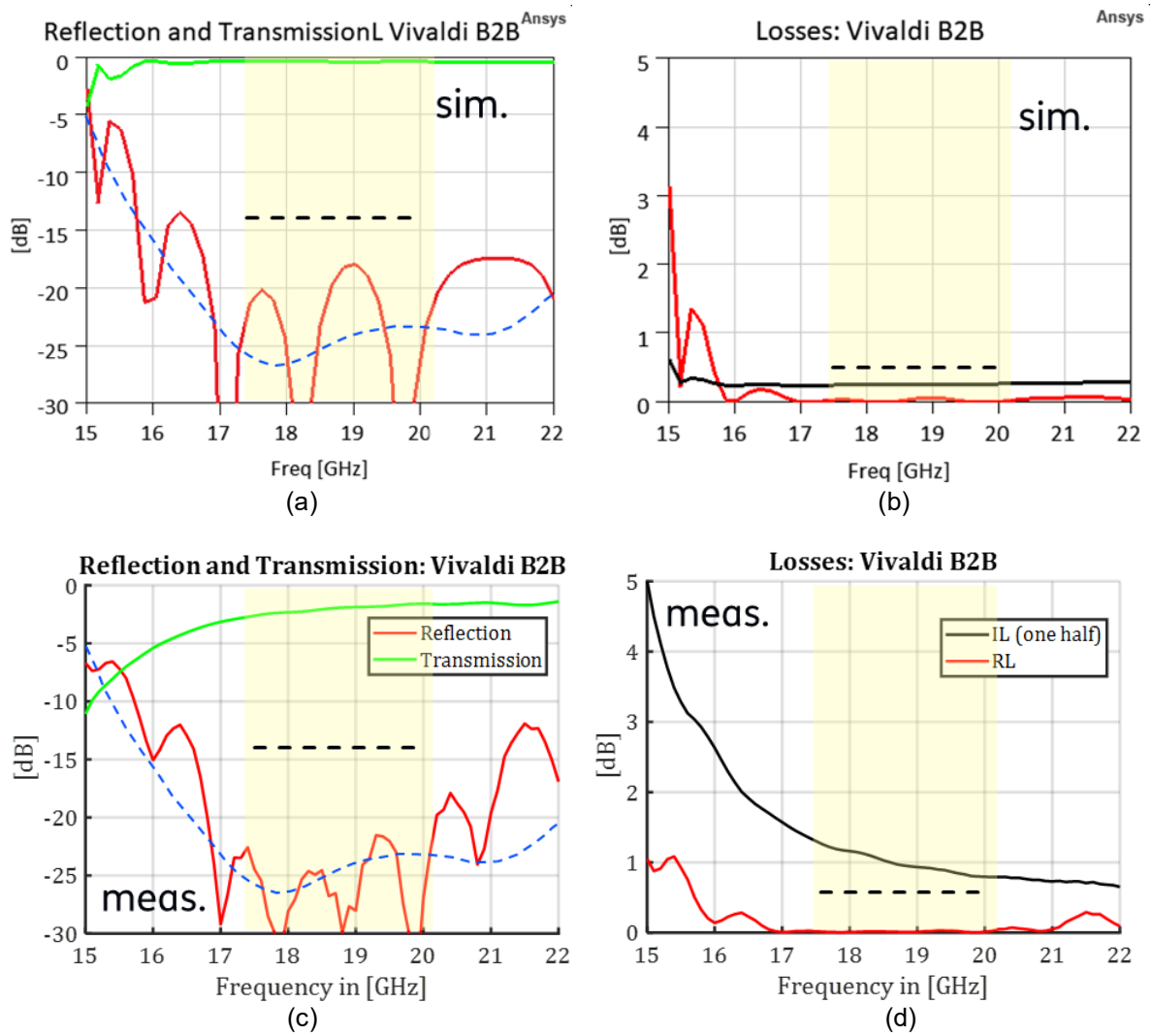


Figure 5-60: (a), (b) Simulated and (c), (d) measured results for the Vivaldi exciter in a back-to-back (B2B) configuration. (a), and (c) reflection (red) and transmission (green) respectively simulated and measured. (b), and (d) reflection- (red) and insertion (black) loss respectively simulated and measured. The insertion loss has been compensated by ½ to arrive at the single transition loss. Note the insertion of the blue dashed line which represents the reflection of a single dipole exciter connected to a sCWG as shown in Figure 5-55a.

The waveguide test structure increased loss can be caused by the following factors:

- PCB performance
- Wave guide assemble and poor RF connection
- PCB manufacturing error
- Waveguide design

To evaluate PCB performance, waveguide assemble, poor RF connection and PCB manufacturing error 10 repeated measurements over both different combinations of Vivaldi and Dipole PCBs where performed. In addition a sample of PCB's where X-rayed to examine the internal metal layers and via connections. The 10 repeated waveguide measurement resulted in similar waveguide feed loss (> 1 dB) and good return loss. The X-rays confirmed that all internal connection where made. In addition, each repeated wave guide tests requires a complete dismantle and re-assemble of the waveguide structure, which also rules out the wave guide assemble and poor RF connection as the loss mechanism.

The waveguide feed and WG simulations, which was defined prior to the construction of the assembly, was rivisited. The single Vivaldi model simulation included gaps that are also present in the assembly. However it was found that not all of the gaps that finally ended up in the manufactured assembly were

defined in the simulator. Therefore it was decided to revisit the simulation, but now applied to the back-to-back dipole case with a 40mm empty waveguide. All gaps have been defined (Figure 5-61) and simulated, results are shown in Figure 5-62.

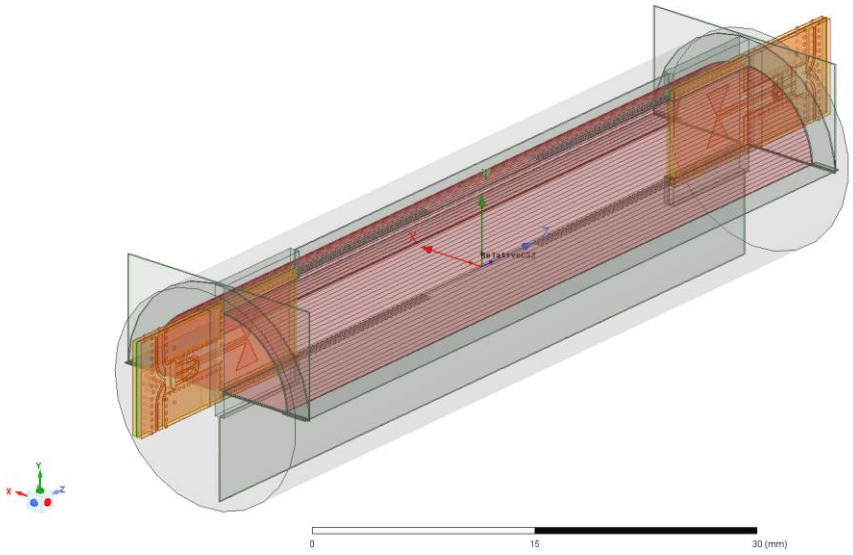


Figure 5-61: Model better representing the realised test assembly. The gaps as they are mentioned in the text are shown with a light green colour.

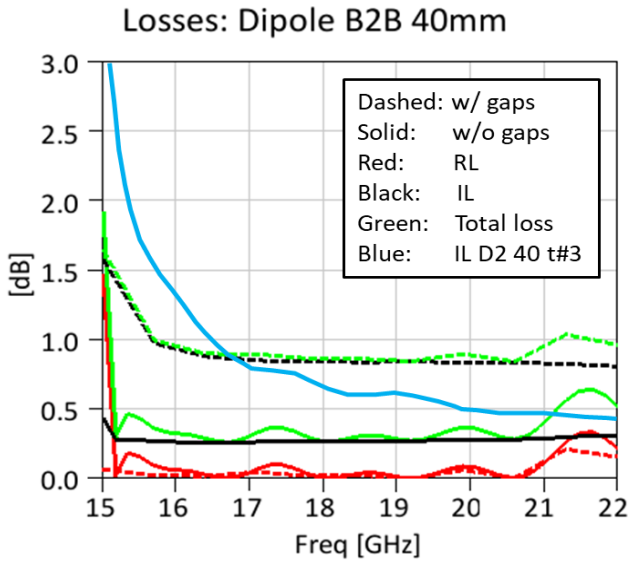


Figure 5-62: Comparison of the losses (see legend) between the structure with and without perfect aluminium connections (i.e. gaps), for the 40mm back-to-back dipole case. Losses in the structure with gaps start to resemble those that were measured. Characteristic are the high roll off at the lower frequency extreme and the counter intuitive monotonic decrease with higher frequency.

Though the loss mechanism is evident, the simulations agreement is still poor. The gaps are placed at the position where they are also present in the assembly but can definitely be further optimised. Also the thickness of the gaps have been set to be between 50 and 100um which in practice will be less. The material filling up the gaps is give the following dielectric properties: Dk = 3 and Df = 0.5, therefore lossy. Whether these properties are correct is not known, but what is proven here is that imperfect metal contact between the assembly parts can result in the high losses as found in the measurements.

5.3.8. PDR Waveguide Conclusion

The waveguide PDR has concluded the radiating front-end shall have an inline (brick) architecture based on the manufacturing practicalities and recommendation from TAS. Two waveguide feed designs have been evaluated: Vivaldi and Dipole. A 4 layer PCB layer stackup has been chosen with the waveguide feed being implemented in the inner layers. Both waveguide feed designs simulated performance resulted in < 0.6 dB loss. The septum design simulations show a loss of 0.1 dB and that a stepped septum design is preferred.

Both waveguide feed designs where manufactured by ACB. The lead time was long at 14 weeks considering the PCB complexity is low.

The waveguide exciter measurements have shown good return loss over all three designs (dipole, Vivaldi Lumped and Wave) showing > 17dB. The return loss measurements also show good agreement simulations. The evidence suggests that the energy is entering the waveguide exciter and not being reflected by the RF via. Unfortunately the waveguide feed loss results for both Vivaldi and Dipole are > 1 dB.

The Dipole, Vivaldi waveguide measurements have been repeated multiple times, each measurement is a new WG construction including the connectors; this was to test measurement repeatability. In summary the WG repeated measurements for all feed types: Dipole, Vivaldi show good grouping (i.e. similar loss). As the majority of the repeated measurements group well one must conclude the dis-assembly and re-assembly of the wave guide isn't the issue. The Dipole and Vivaldi measurements resulted in the lowest total loss of 0.95dB @ 17.3 GHz.

Further investigations identified that imperfect metal contacts within the waveguide (WG) simulation was the cause of the losses. Revisiting the simulation model confirmed this, showing gaps and dielectric properties as the culprits.

The DRIFT team have found a Dutch company (MF Vonkverspaning) that can build a waveguide with no assembly construction lines, i.e. a waveguide made from a single piece of material using a spark erosion method. Therefore to continue the project the DRIFT team identified these next steps in ensuring a successful WG CDR:

- Build another set of test structure WG using MF Vonkverspaning spark erosion method.
- Perform the WG and waveguide feed loss measurement using a port 2 measurement similar to TAS-F's method.
- New waveguide exciters were manufactured by Eurocircuits rather than ACB as manufacturing costs and lead times are much lower. Lead time is 10 days rather than 14 weeks. (NB Eurocircuits cannot produce PCB's with RT3003 Teflon material therefore the inner layers must be Rogers 4000 series, which will introduce 0.1dB additional loss. An acceptable compromise in terms of cost and lead time from ACB).
- Optimise the septum design.
- Upon successful waveguide and waveguide feed loss measurements, finalise the demonstrator design, the full WG + PCB construction and the detailed test plan.

5.4. HPA Critical Design Review (CDR) (WP 3.1)

5.4.1. HPA Critical Design

The HPA topology has been defined during the preliminary design and Figure 5-63 schematically shows the topology. The RF input is 50ohm and the two differential outputs are matched to the waveguide feed, which is also designed to be 50ohm.

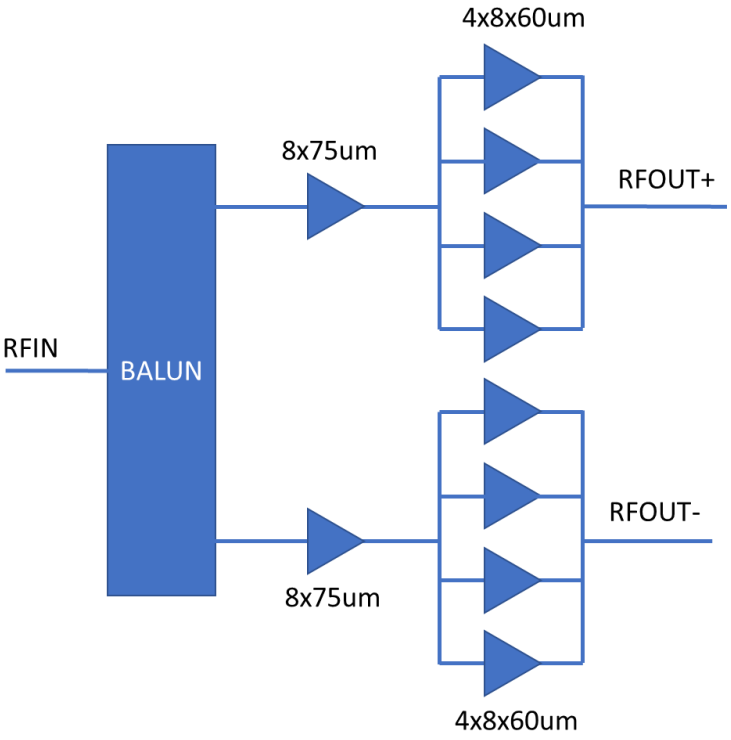


Figure 5-63 : HPA topology.

Figure 5-64 shows the complete layout of the HPA, with a size of 3.1 x 2.8 mm^2 (excluding half the dicing street).

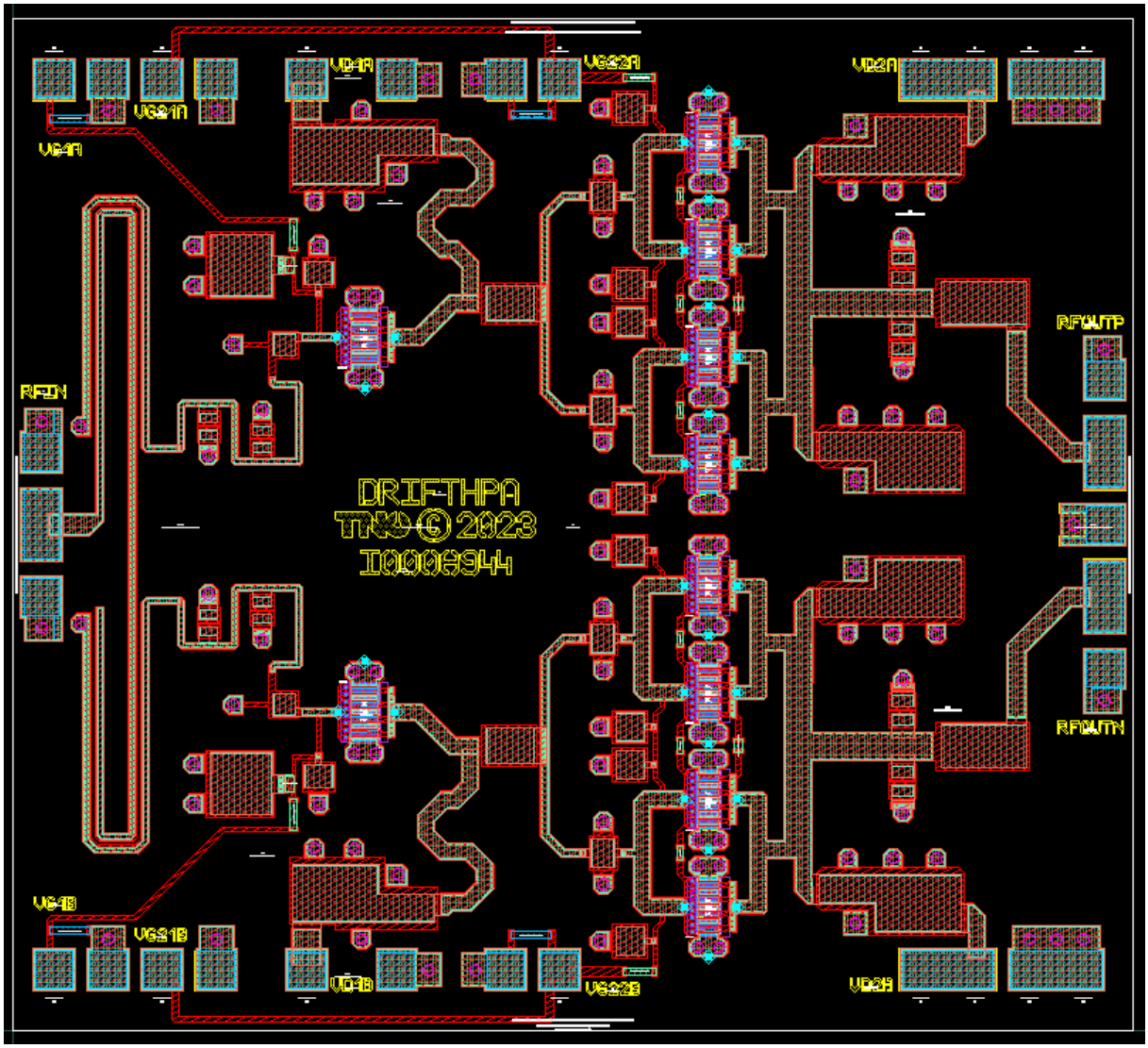


Figure 5-64 : HPA layout.

Figure 5-65 shows the DC and RF probe pad layout. The RF input is a 200um GGS probe and the RF output a 200um GSGSG probe. The two HPAs are biased separately from the north and south side. The gate and drain bias for the amplifier input stage and output stage each has its own bias connection (VG1, VD1 and VG2, VD2). The pads on the north side have the suffix “a” and on the south side “b”, so that each bondpad has a unique label. The gate bias for the output stage is also routed to a bondpad at the left side of the MMIC, next to the gate bias of the input stage (VG21 = VG22). This could enable easier wire bonding and routing in the demonstrator.

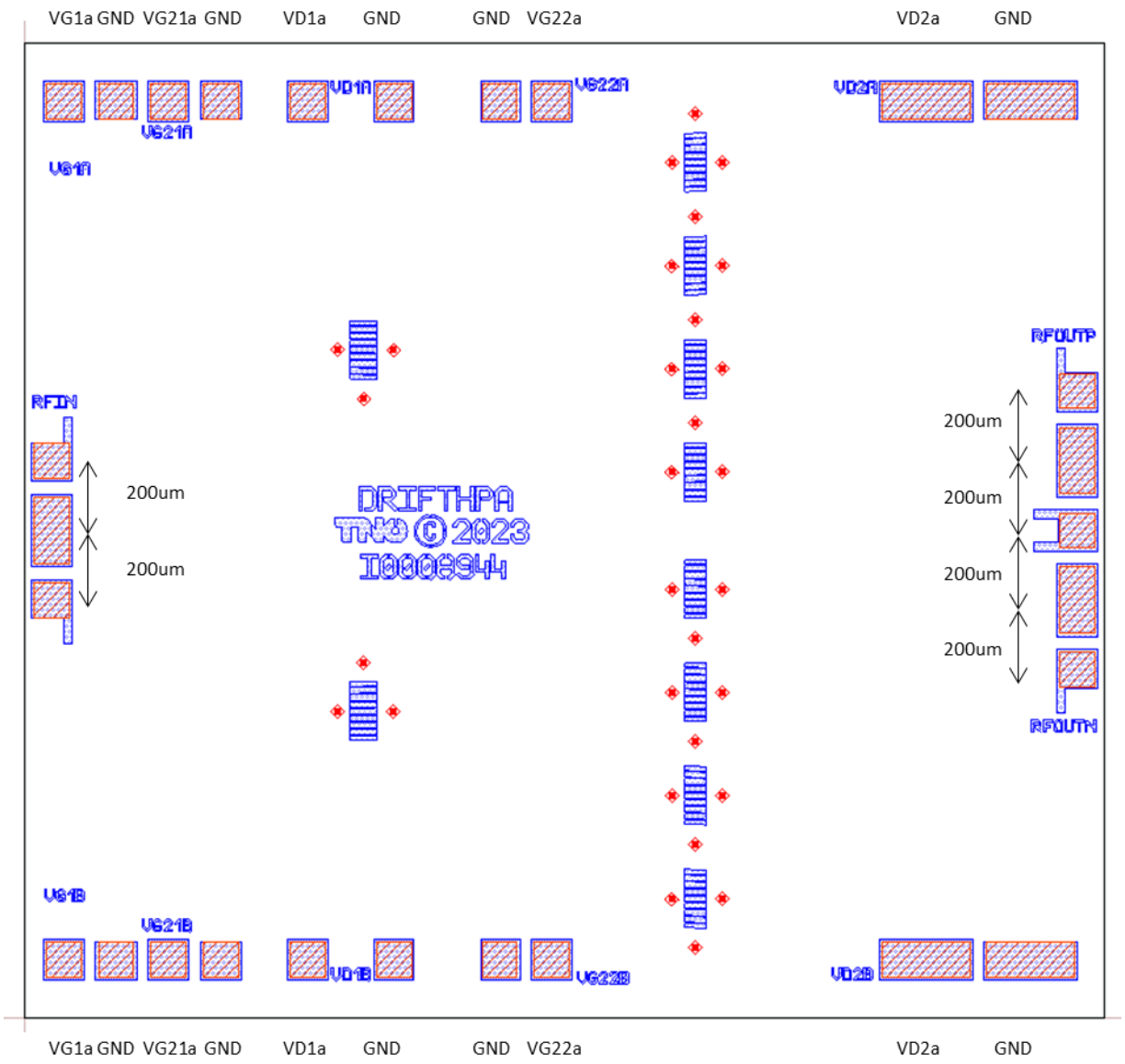


Figure 5-65 : DC and RF probe pad definitions.

Simulation environment

The performance of the HPA has been simulated with the actual differential waveguide feed as load, including the bond wire transitions at the RF output. The HPA performance is calculated for the input reference plane at the PCB and the output reference plane at the MMIC RF output, as shown in Figure 5-23. This means that the input transition is included in the simulation results, but the output transition is not included, although the load presented by this transition is included.

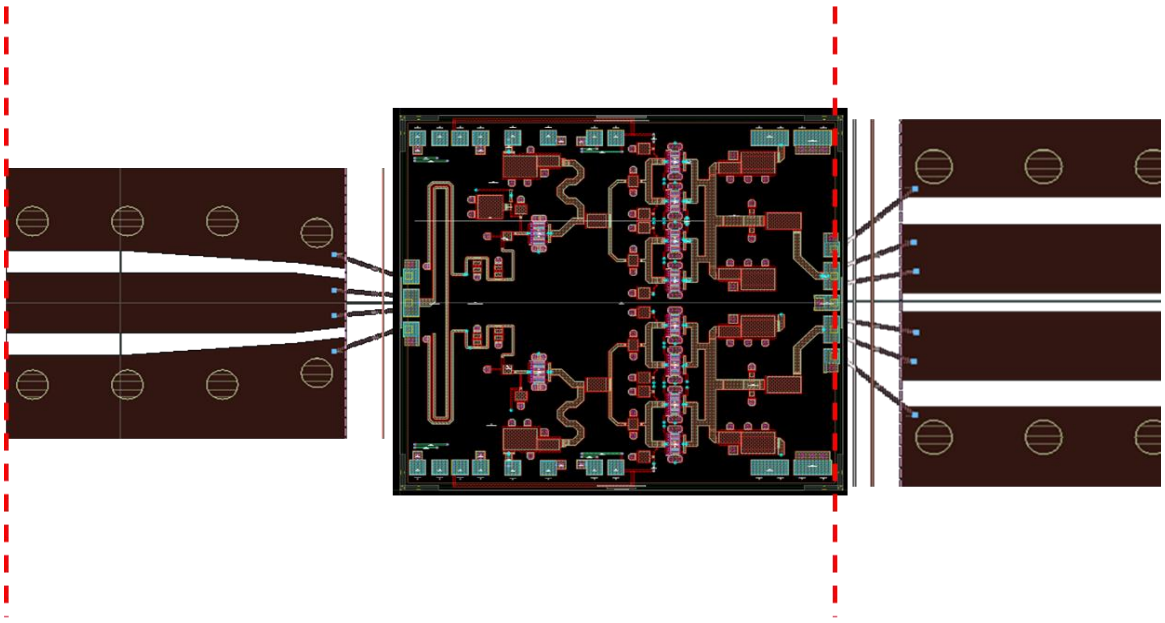


Figure 5-66 : Refence planes (red dotted lines) for the HPA performance simulations.

The nominal design has been made at 80degC and unless otherwise specified the simulations have been performed at:

- Vd = 20 V
- Vg = -3.1 V (Idq=25mA/mm)
- Ta = 80°C (backside MMIC temperature, defined for the PDK transistor models)

Since the threshold voltage of the transistors is temperature dependent, and slightly different gate bias must be used at room temperature, to obtain the same quiescent current density, as shown in Table 5-16.

Table 5-16 : DC bias conditions.

	Ta=20degC	Ta=80degC
Vg	-3.0 V	-3.1 V
Vd	20 V	20 V
Id1	34 mA	32 mA
Id2	110 mA	105 mA
Ig1	0.60 mA	0.62 mA
Ig2	1.21 mA	1.25 mA

The HPA design was optimized for the MMIC mounted in the demonstrator environment, which means that parasitics due to for example bondwires at the RF in- and output are included. To obtain these parasitics 3D EM simulations have been performed of the bondwire interface from MMIC to PCB. The PCB is a 254um thick Rogers3003 substrate with a grounded co-planar waveguide (single ended at the input and differential at the output).

The MMIC will be mounted on a metal pedestal, such that the 70um thick MMIC topside will be level with the 254um thick PCB. A cavity will be made in the PCB to mount the MMIC and a worst-case margin is taken between the edge of the MMIC and pedestal (125um) and the edge of the pedestal and PCB

(300um).

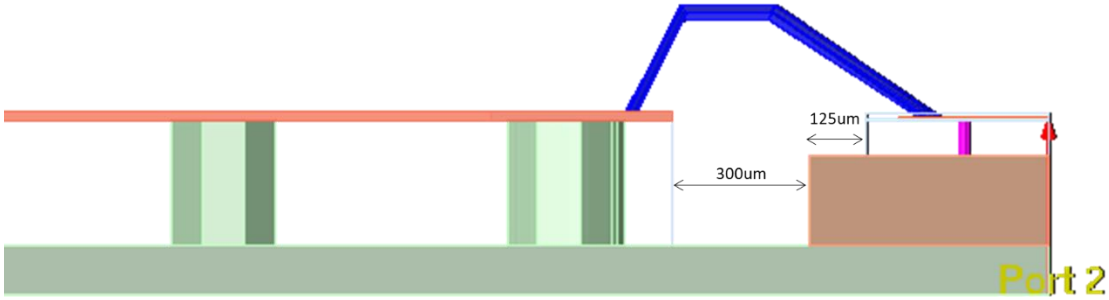


Figure 5-67 : Cross section of the 3D model of the input bondwire transition.

5.4.2. S-parameters

Figure 5-24 and Figure 5-25 show the S-parameters under nominal bias conditions. For these 2-port simulations an ideal balun has been used at the output because the differential waveguide feed simulation data is not available over a wide frequency range. No gain peaks outside the band of interest are visible and the input and output matching are always passive (dB(S11) and dB(S22) < 0).

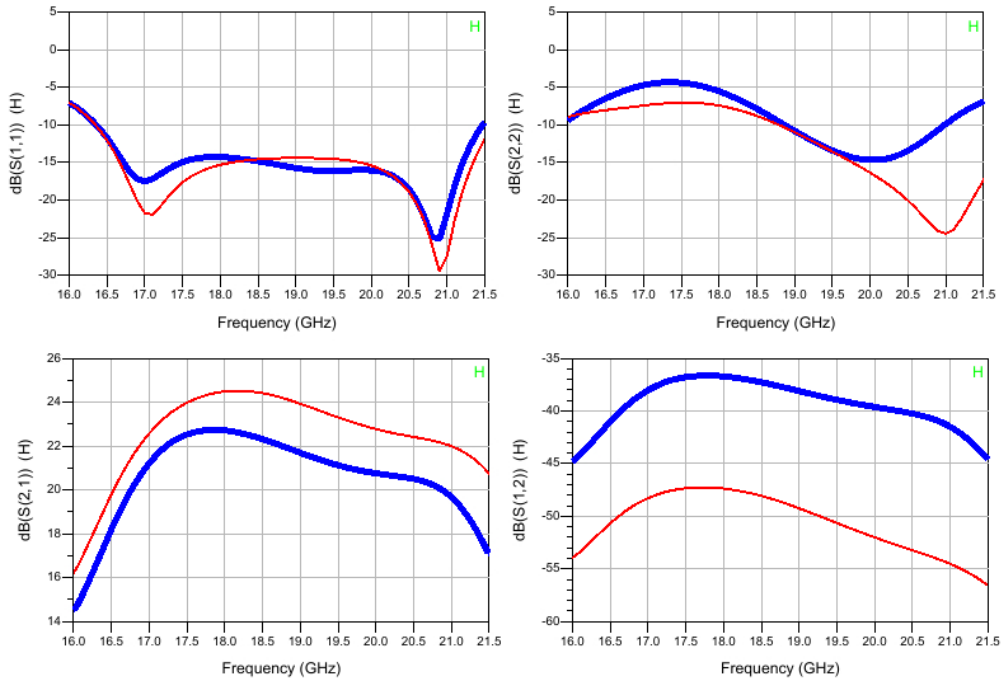


Figure 5-68 : Small-signal S-parameters for the HPA using an ideal balun at the output, Vg=-3.0V (20degC) and Vg=-3.1V (80degC), Vd=20V, Ta=20degC (red) and 80degC (blue).

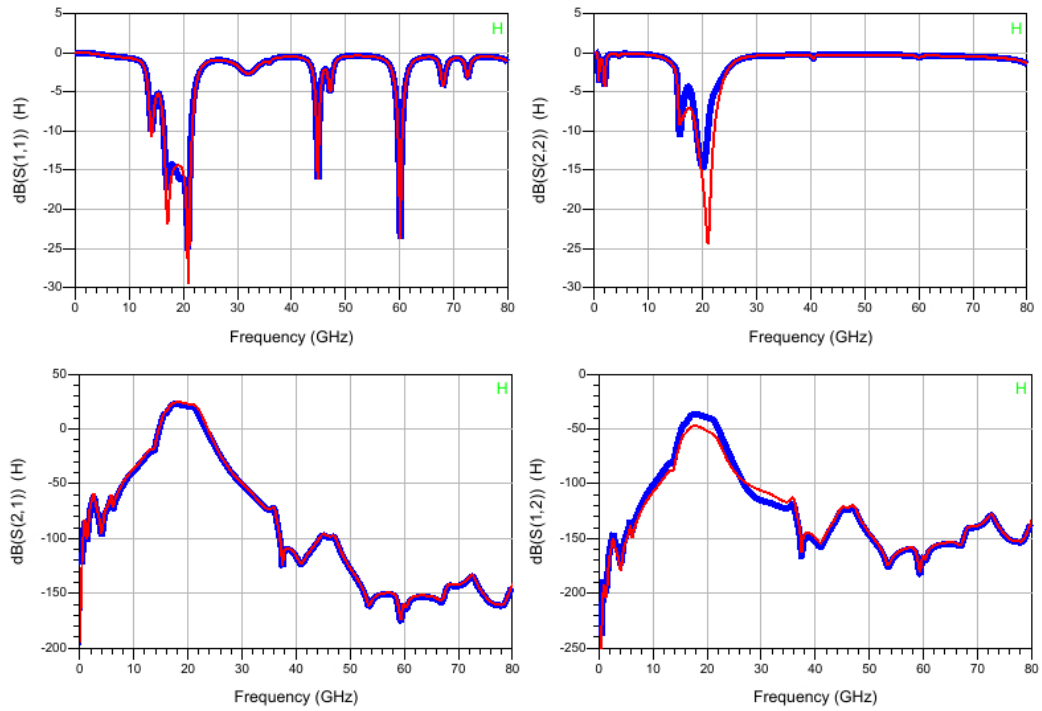
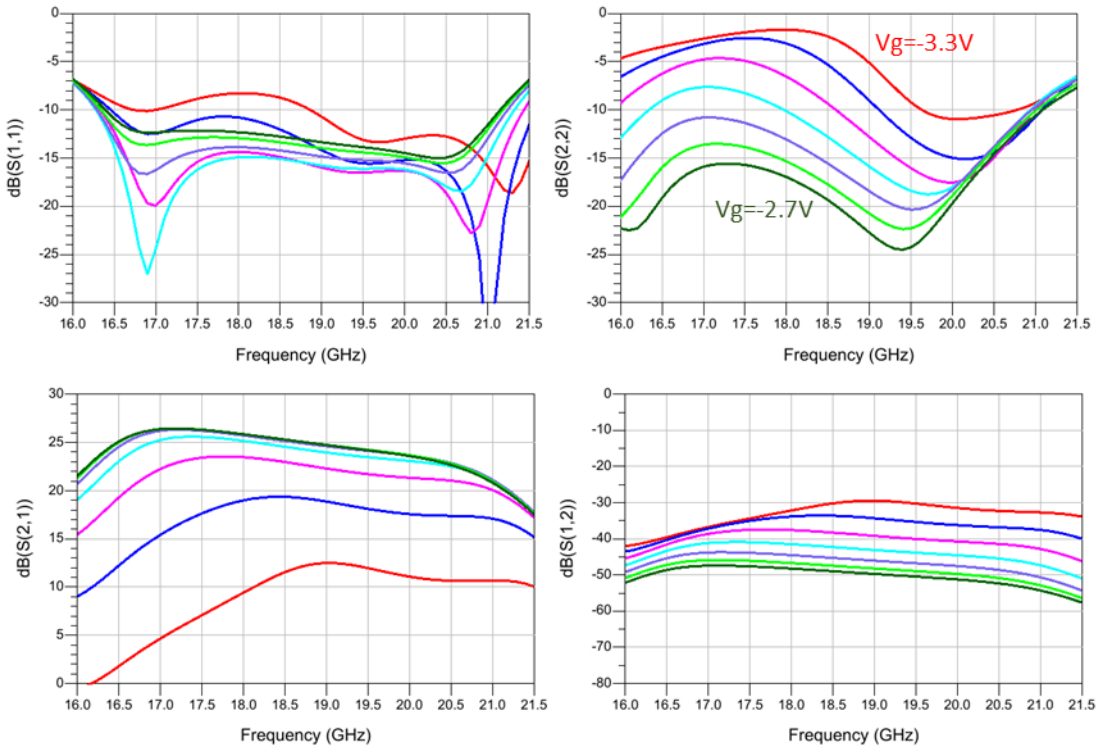


Figure 5-69 : Wide-band S-parameters for the HPA using an ideal balun at the output, Vg=-3.0V (20degC) and Vg=-3.1V (80degC), Vd=20V, Ta=20degC (red) and 80degC (blue).

Figure 5-70 shows the S-parameters as function of gate-bias. The small-signal performance is quite sensitive to gate bias voltage, most likely because no stability network (so no additional loss) is included at the gate of the first stage transistors.



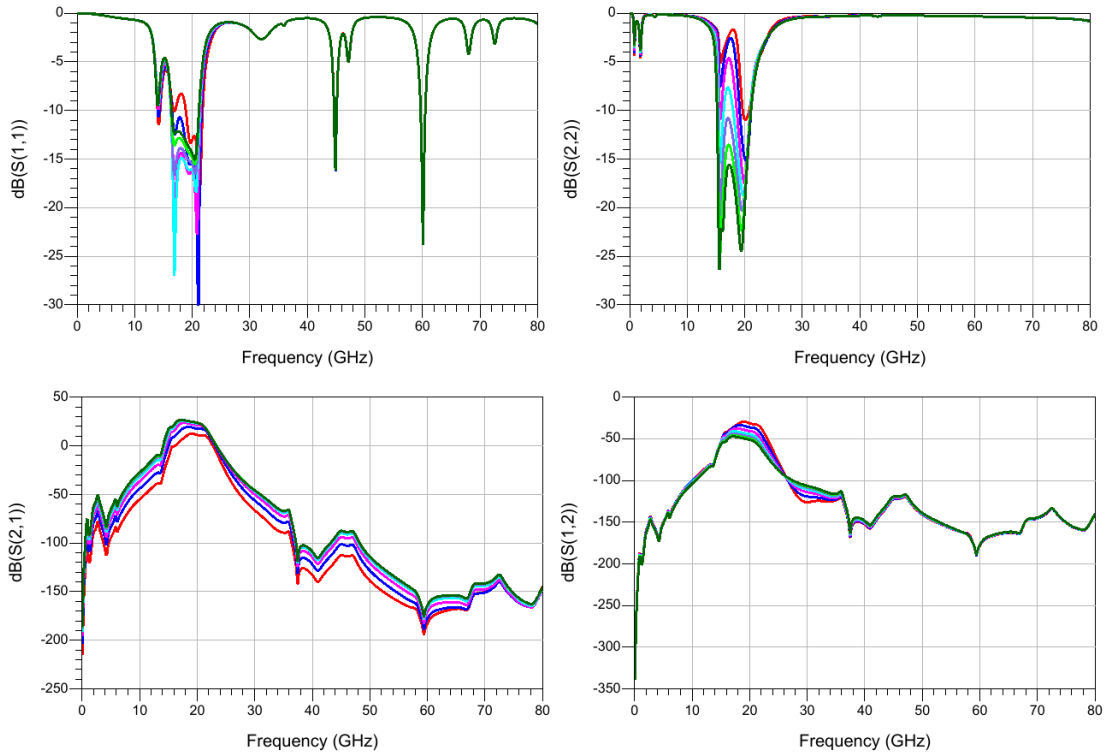


Figure 5-70 : Small-signal narrow- and wide-band S-parameters for the HPA, as function of gate bias voltage (Vg=-3.3 to -2.7V).

5.4.3. LS simulation

Figure 5-26 shows the large signal performance for a source power of 15 to 25 dBm, including the small signal source power point. The saturated output power is larger than 40 dBm with a peak efficiency of 40%.

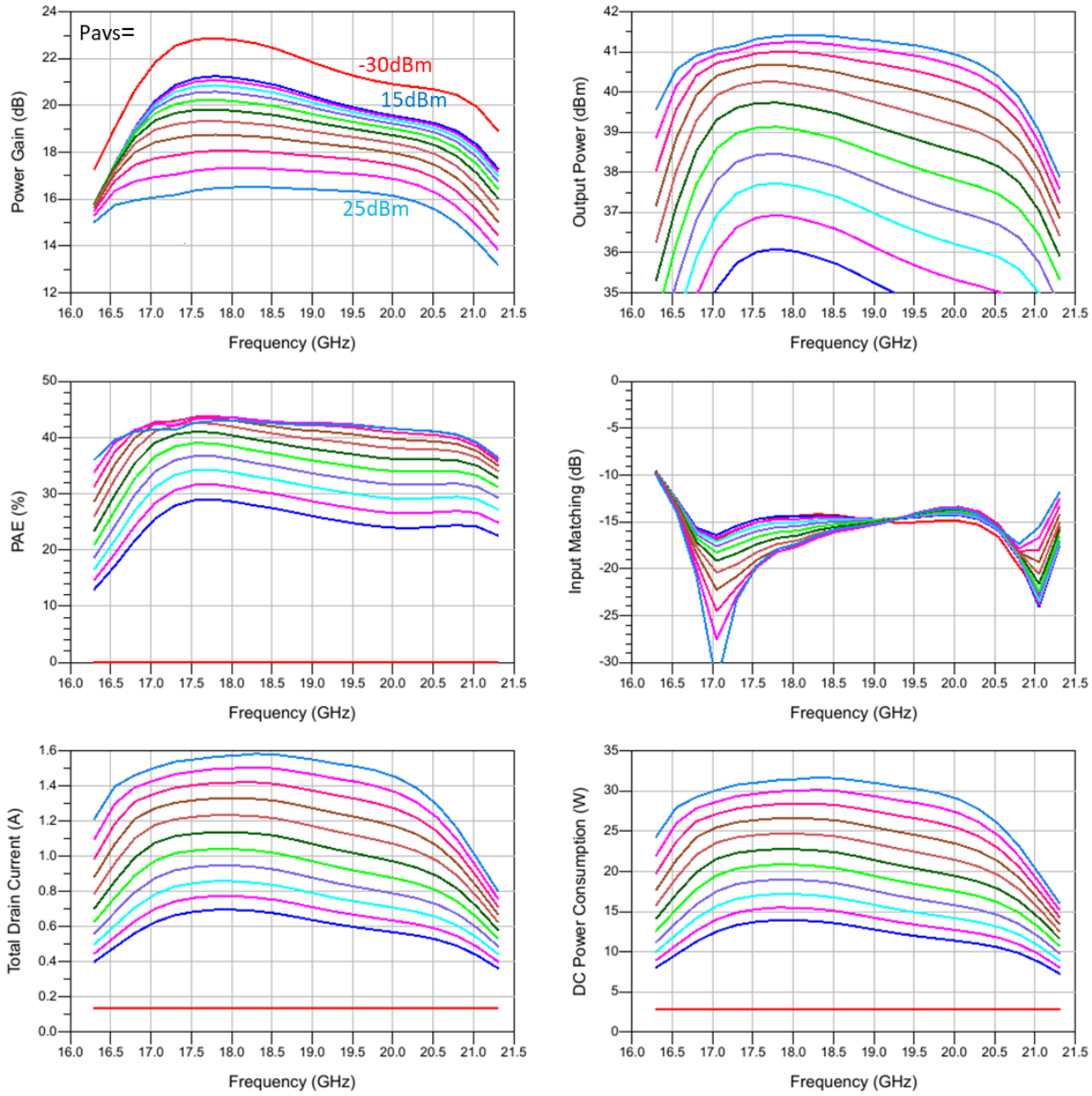


Figure 5-71 : Large-signal performance for Pavs = -30 and 15 – 25 dBm, Vg=-3.1V, Vd=20V, Ta=80degC, using the dipole feed as load.

Figure 5-27 shows power sweep simulations at 17.3, 18.75 and 20.2 GHz. At 17.3 GHz there is a bit more phase compression variation then at 18.75 and 20.2 GHz, which will have some impact on the linearity performance.

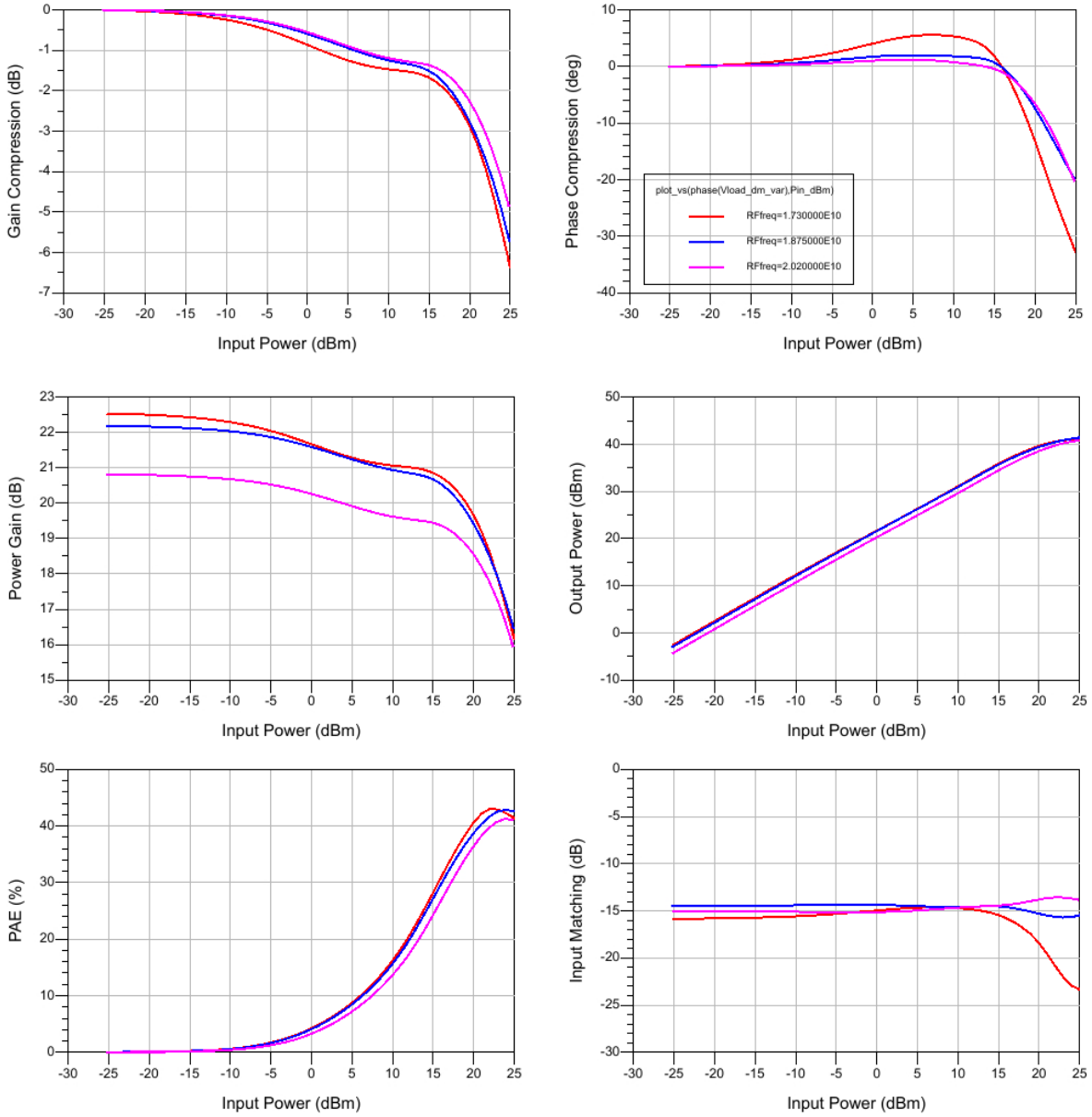


Figure 5-72 : Large-signal power-sweep at 17.3 GHz, 18.75 GHz and 20.2 GHz, Vg=-3.1V, Vd=20V, Ta=80degC.

Figure 5-28 shows power sweep simulation as function of gate bias voltage. In saturation the gate bias voltage does not have much impact on the performance. However, there is a large impact on the AM/AM and AM/PM performance. For the design a gate bias of -3.1 V (blue curve) has been used at 80degC since this results in the least gain and phase compression variation. Figure 5-29 shows a similar sweep but now versus frequency at a fixed source power level, corresponding to the maximum efficiency point.

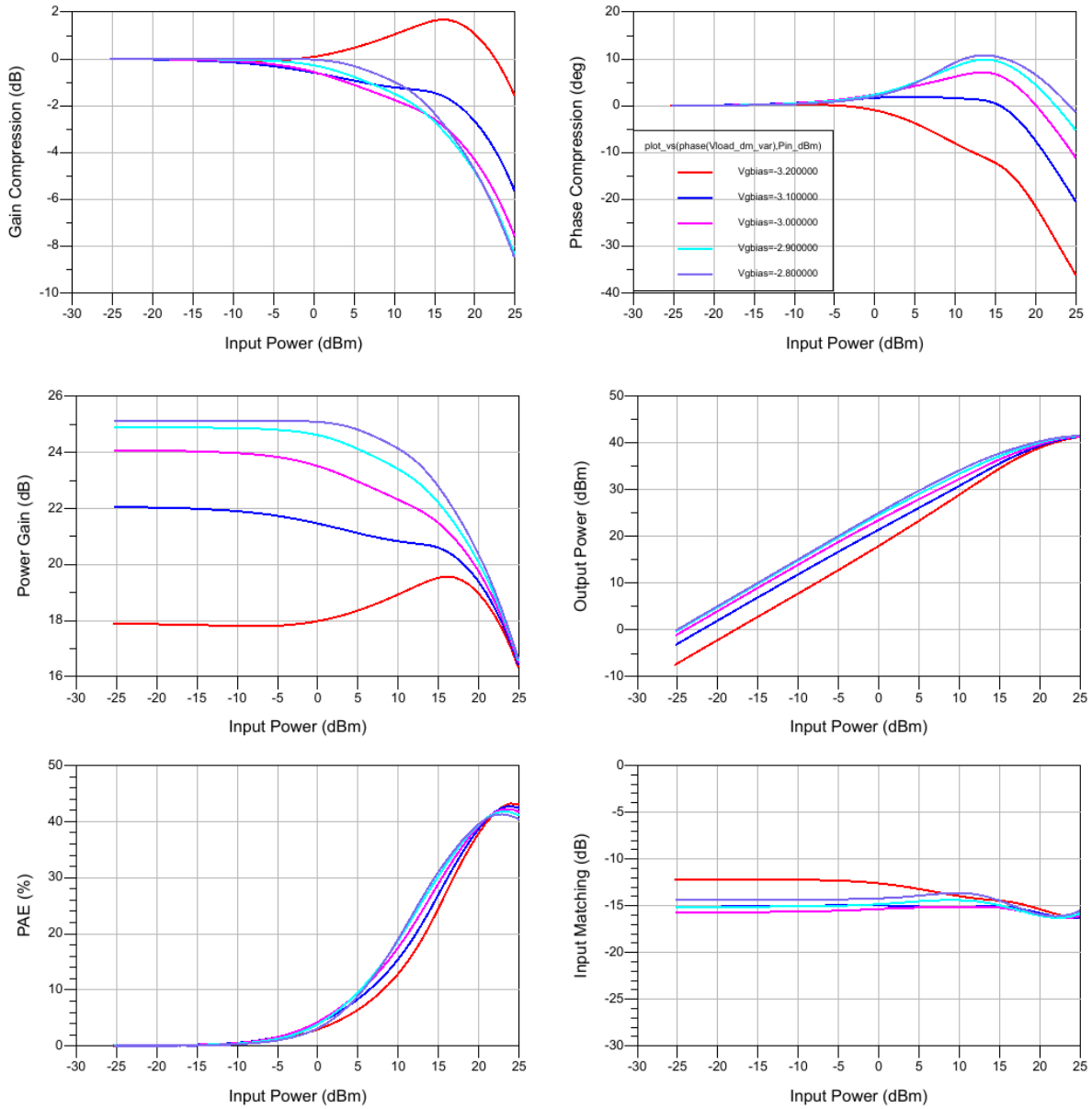


Figure 5-73 : Power sweeps at 18.8 GHz for Vg = -3.2 to -2.8 V, Vd=20V, Ta=80degC.

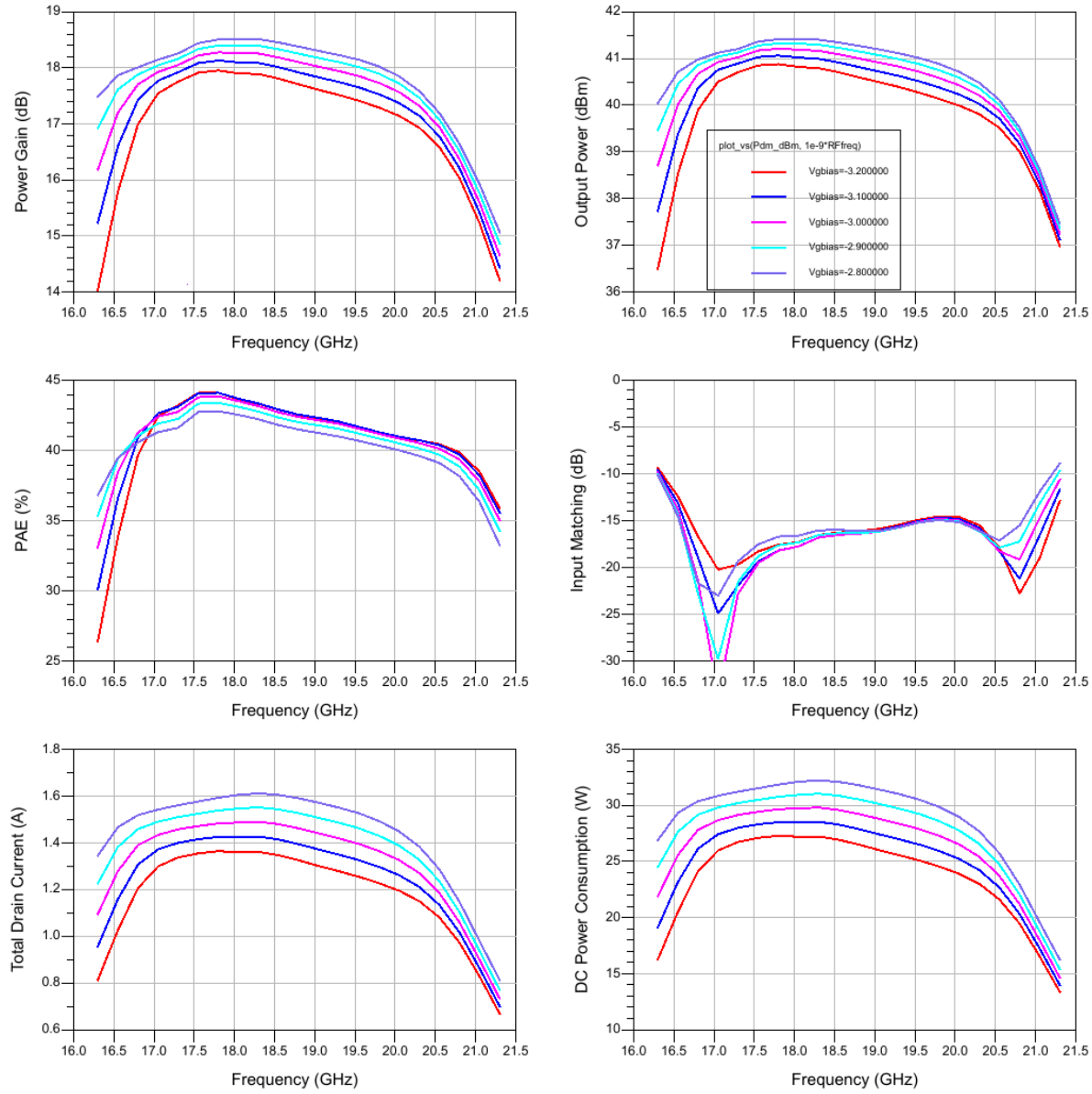


Figure 5-74 : Frequency sweeps at 23 dBm source power for Vg = -3.2 to -2.8 V, Vd=20 V, Ta=80degC.

Figure 5-30 shows the impact of the drain bias on the frequency sweep performance. The drain bias variation causes a minor frequency band shift and of course a variation in gain and output power.

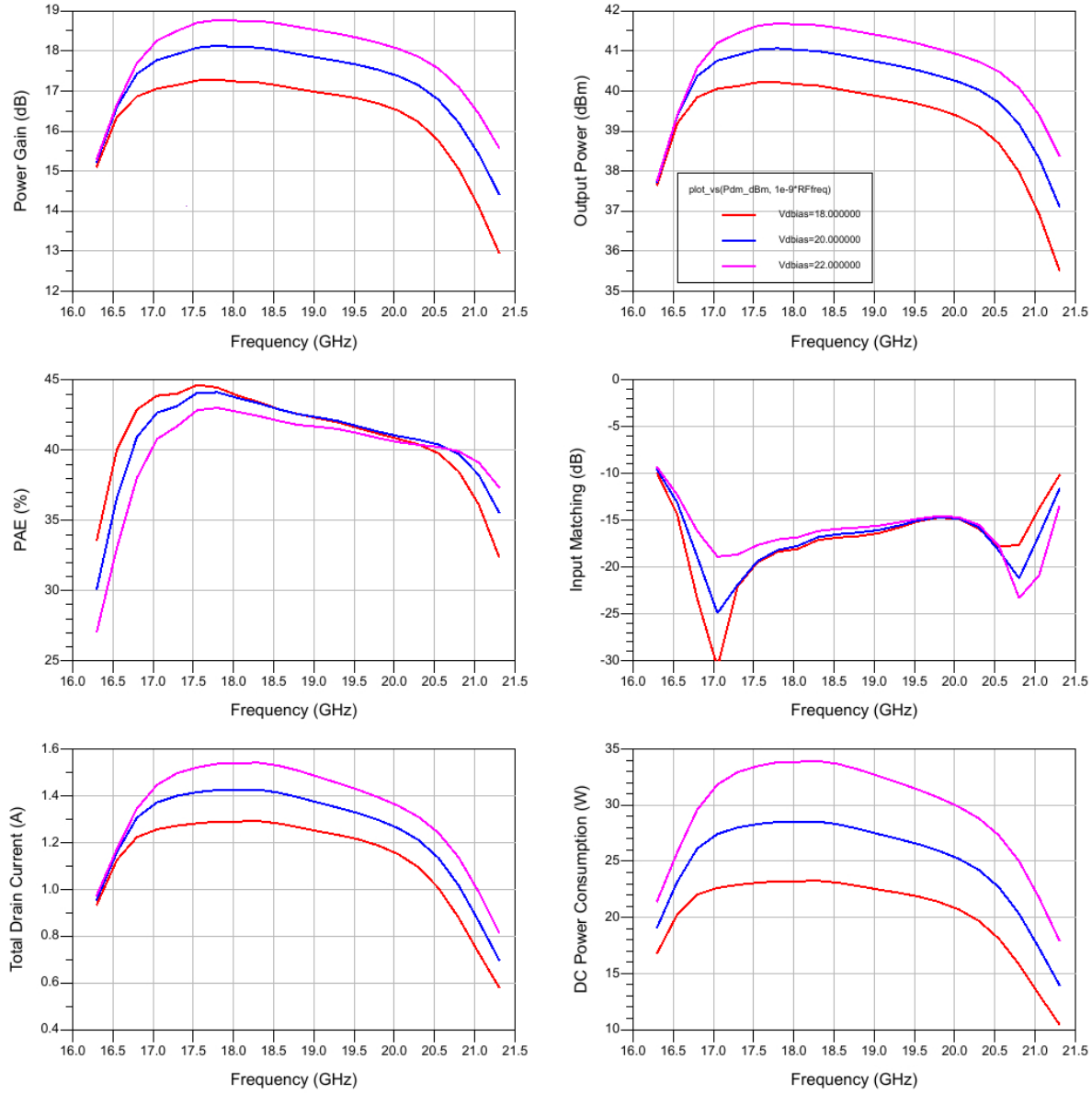


Figure 5-75 : Frequency sweeps at 23 dBm source power for Vd = 18, 20 and 22 V with Vg=-3.1 V.

The process spreading for passive and active components will results in a frequency shift and performance variation. The main parameter that causes performance variation is the spreading of the MIM capacitor. According to the PDK definition this capacitor has a uniform distribution of +/- 9%, which is a worst-case assumption since the real variation will be more gaussian-like. Figure 5-76 shows the effect of +/- 9% MIM capacitor variation on the large signal performance at a fixed source power. The design is centred well in relation to capacitance variation. At 18.8 GHz the effect of the capacitance variation on the gain and phase compression is shown in Figure 5-77. In the centre of the band there is almost no effect on the linearity due to the capacitance variation.

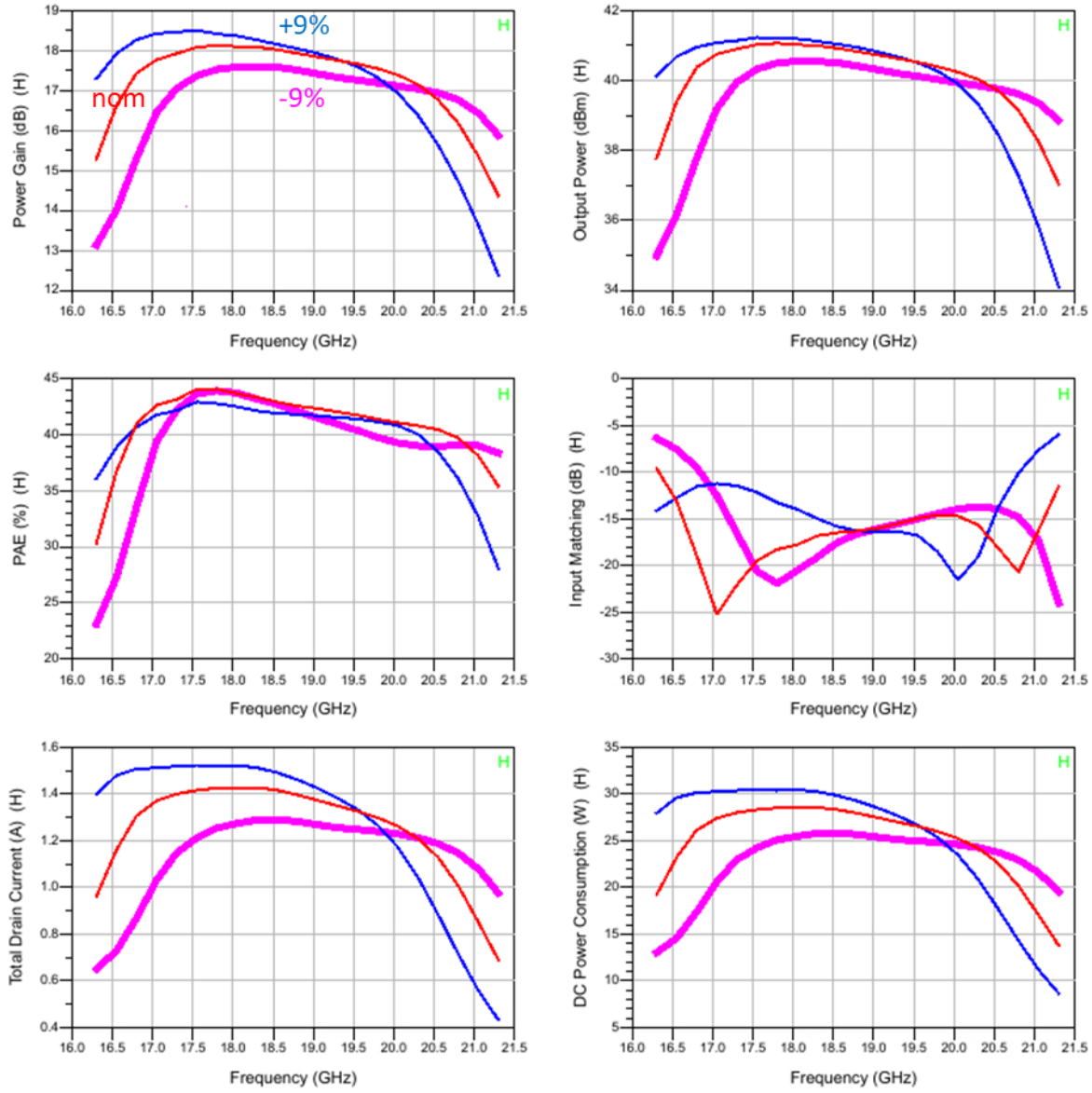


Figure 5-76 : Large-signal performance for 23 dBm source power and a +/- 9% MIM capacitor variation, Vg=-3.1 V, Vd=20 V, Ta=80degC.

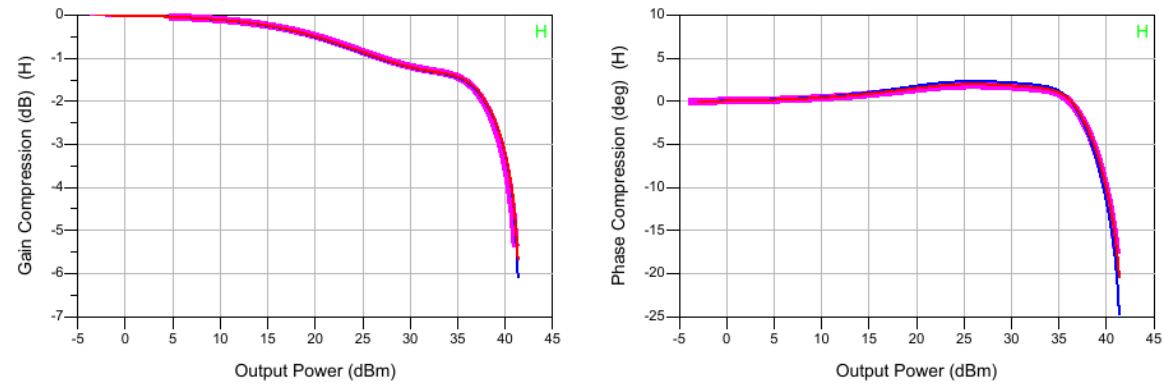


Figure 5-77 : Power sweep at 18.8 GHz with +/- 9% MIM capacitor variation, Vg=-3.1 V, Vd=20 V, Ta=80degC.

Figure 5-78 shows the impact of temperature on the saturated power performance. For this comparison a constant quiescent drain current was used (137mA), which means that at room temperature the gate bias is slightly higher than at 80degC. At room temperature the peak PAE reaches 48%, which is state of the art performance.

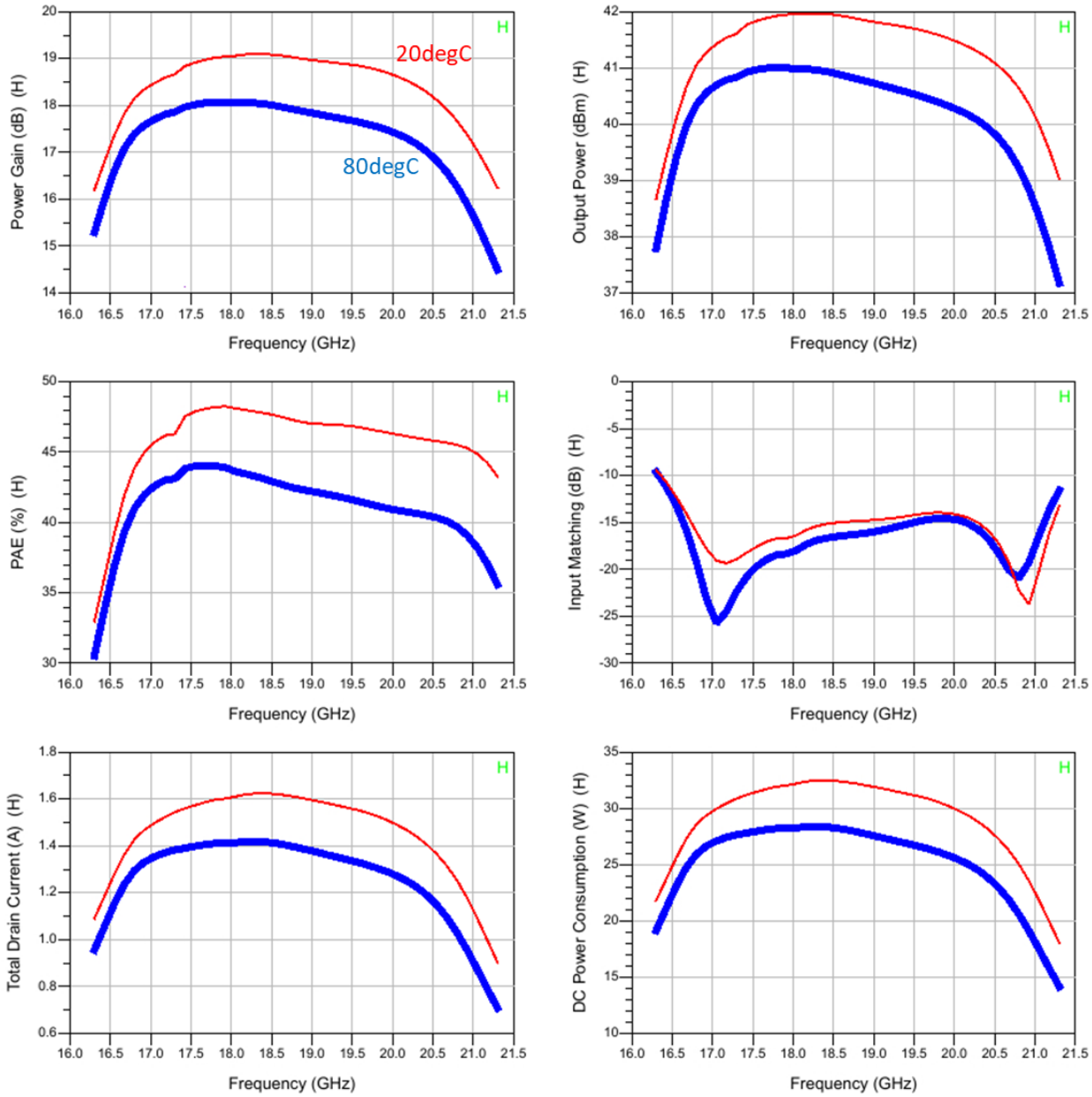


Figure 5-78 : Frequency sweeps at 23 dBm source power at Vg=-3.1 V, Vd=20 V for Ta=20 and 80degC.

The sensitivity to load variation has been simulated using the EM model of the waveguide exciter (Dipole version). Figure 5-79 shows the impact of a varying load with 20, 15 and 10 dB return loss on the simulated output power and PAE at 23 dBm source power. It is clear that the matching of the antenna, as seen by the HPA output should be better than 15 dB to not have too much impact on the power and efficiency performance.

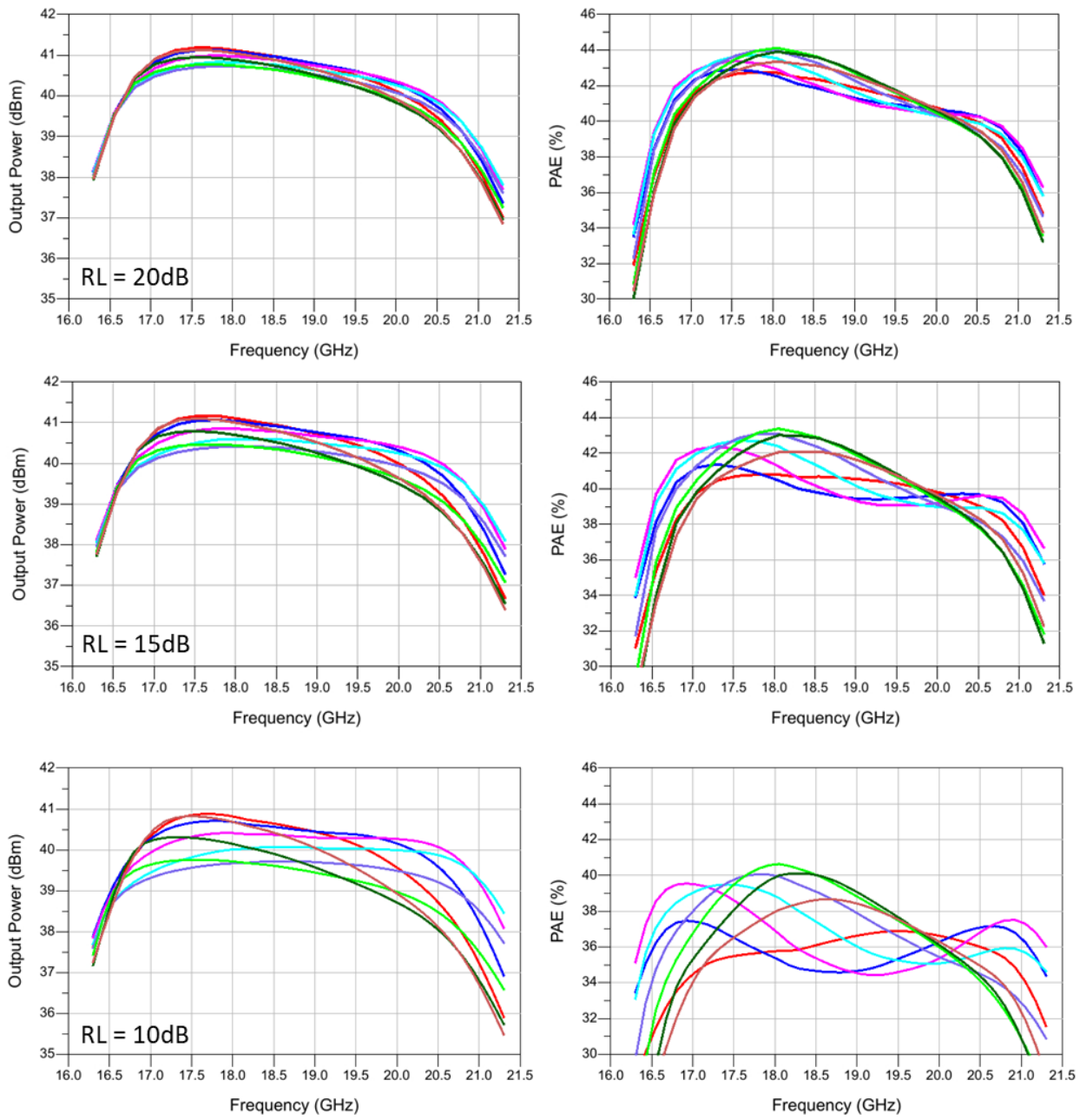


Figure 5-79 : Impact of 20, 15 and 10 dB return loss (with varying phase) at 23 dBm source power, Vg=-3.1V, Vd=20V, Ta=80degC.

5.4.4. Linearity simulations

The performance at 15 dB NPR has been calculated with IMAL, based on simulated power sweep data. The 15 dB NPR performance has been specified at the HPA output reference plane. The obtain the simulation data an ideal balun has been used at the HPA output to convert the differential signal into a single ended signal required for the IMAL calculation Figure 5-80 shows the NPR calculated by IMAL versus efficiency and output power. Figure 5-81 shows the calculated results at 15 dB NPR at 80degC versus frequency. The output power is larger than 37 dBm, expect for a small part at the lower side of the frequency band. It is possible to obtain 37 dBm output power over the full band by slightly increasing the gate bias, but this will cause a small reduction in efficiency. As was already concluded during the preliminary design it is difficult to obtain the 35% efficiency at 15 dB NPR. The calculated efficiency varies from 32.0 to 35.5% over the frequency band. As a result, the DC power consumption is also higher than specified.

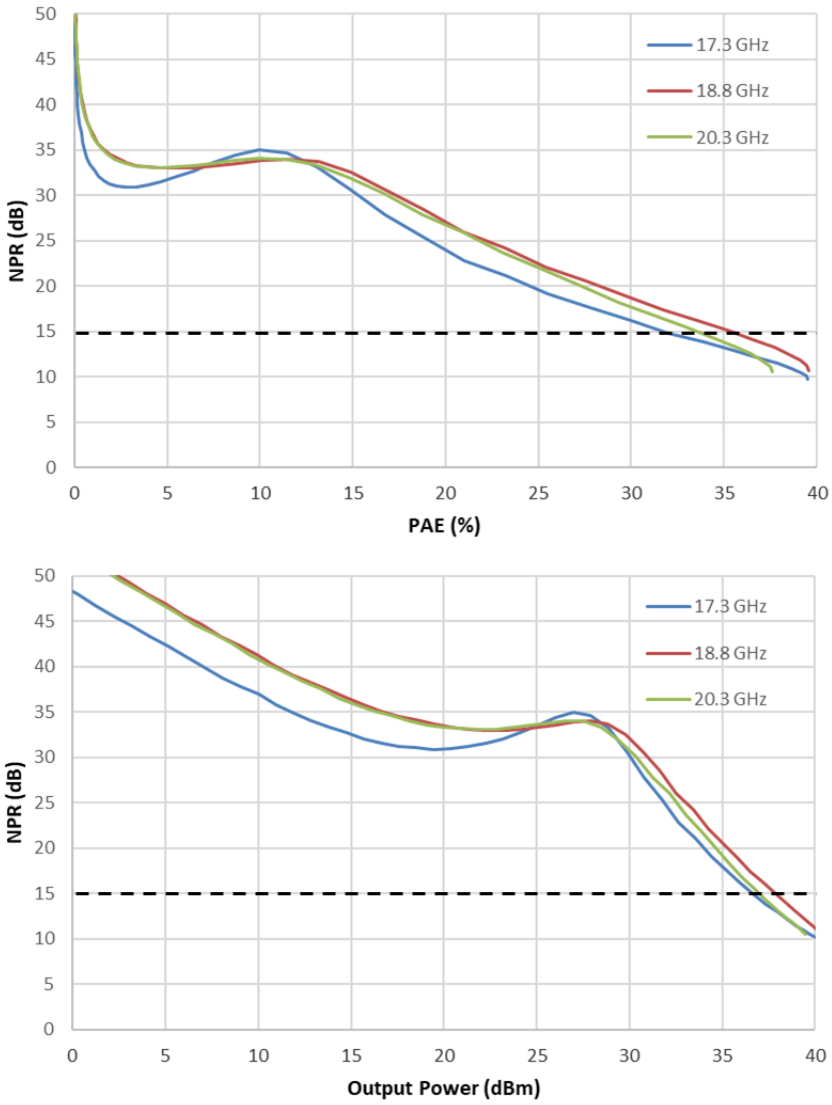


Figure 5-80 : NPR versus efficiency and output power at Vg=-3.1V, Vd=20V, Ta=80degC.

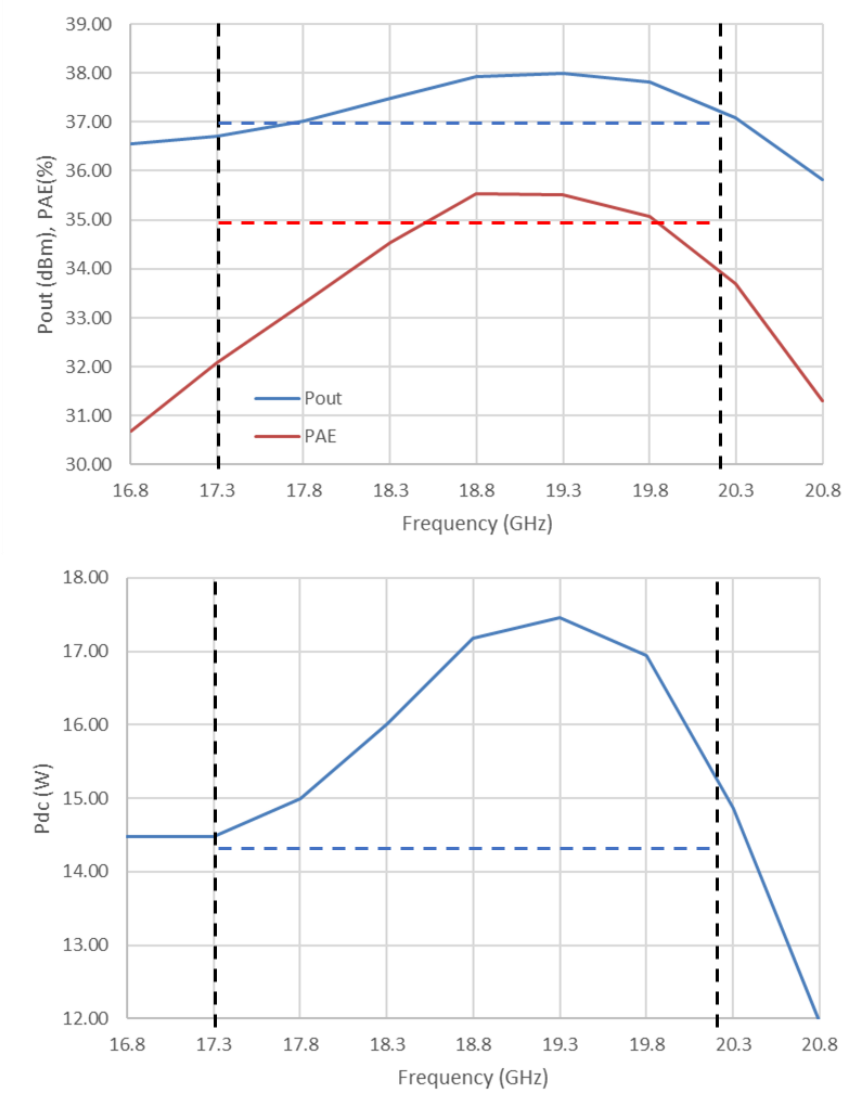


Figure 5-81 : Output power, efficiency and DC power consumption, calculated by IMAL for the 15 dB NPR point at Vg=-3.1V, Vd=20V, Ta=80degC.

Figure 5-82 shows the result of the same IMAL calculation but now for simulated power sweep data at 20degC. In this case both the output power and efficiency specifications are achieved. The DC power consumption is higher than specified because the output power is higher than 37dBm.

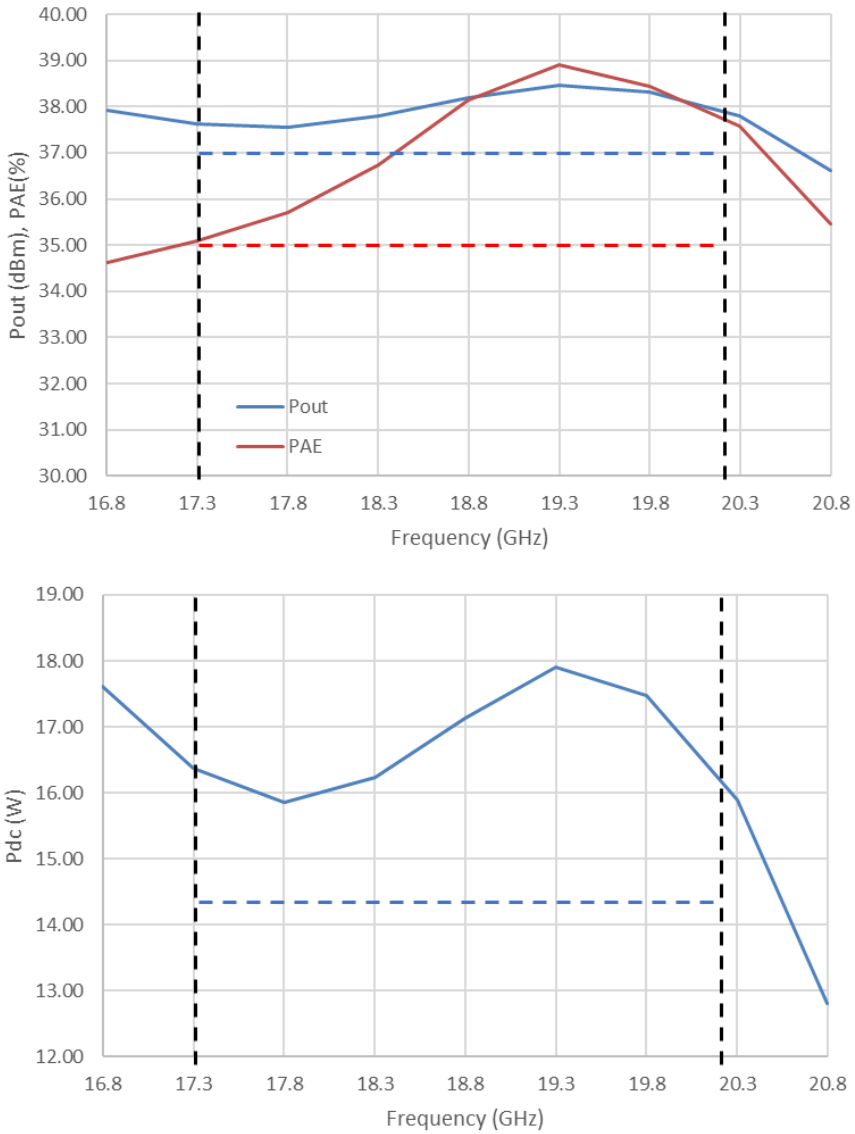


Figure 5-82 : Output power, efficiency and DC power consumption, calculated by IMAL for the 15 dB NPR point at Vg=-3.0V, Vd=20V, Ta=20degC.

Several simulation experiments have been performed with other combinations of gate voltages for the input and output stage, but no combination was found that results in a better efficiency at 15 dB NPR. Of course, this will also be checked during measurements.

5.4.5. Stability simulations

Stability has been checked with four different methods:

- small-signal k-factor for the complete HPA (2 port),
- small- and large signal loop gain analysis (Ohtomo method),
- small- and large signal pole-zero identification.

- Small-signal gain and stability between bias pins

A small-signal stability check has been performed at the input and output, to check unconditional stability for any source and load impedance. The stability factor has been simulated, for the HPA loaded with an ideal balun, versus gate bias at several temperatures. Figure 5-83 shows that the stability factor becomes lower for higher temperatures, which was already seen at transistor level, but in all simulated cases the design is unconditionally stable.

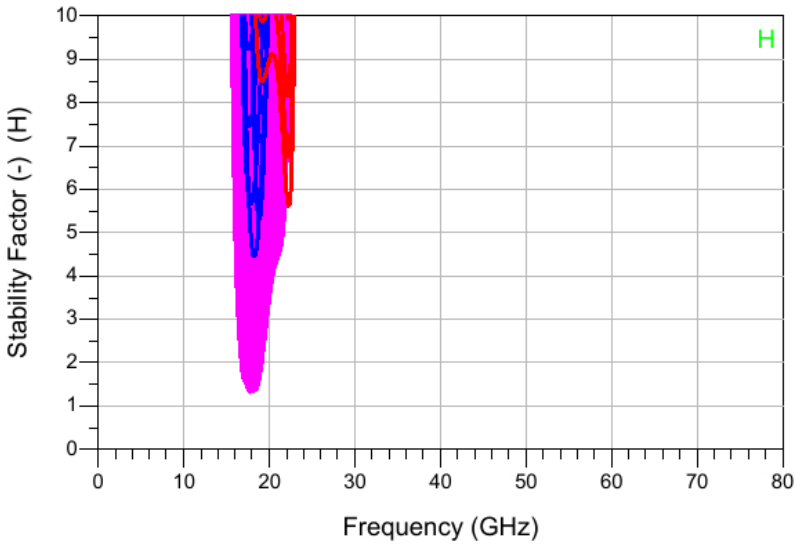


Figure 5-83 : Stability factor for Ta=-40degC (red), 20degC (blue) and 80degC (magenta), at Vg= -4.0 to -2.5V, Vd=20V.

The S-parameter analysis has also been performed over a range of gate and drain bias voltages and the results showed that there is no gain outside the intended band. There is however a positive S22 for drain bias voltages in the range of 2 – 12V and a gate bias voltage larger than -3.5V. Therefore, the design is not unconditionally stable. The output impedance for both individual output ports when the HPA is simulated as 3-port are identical on both outputs. Because of the potential instability at low drain bias, it is required to power-up the HPA in pinch-off conditions, and only increase the gate bias voltage to the nominal value when the nominal drain bias voltage is applied.

Loop gain analysis is performed by measuring the impedance on each gate and drain connection, while other connections are toggled from a thru-mode to an isolator-mode (the Ohtomo method). When these impedance values are plotted on a polar chart, the response must not encircle the +1 point on the real axis, since that will indicate an unstable loop. Figure 5-84 shows the small signal loop gain for all possible loops under nominal bias conditions at low and high temperature. No unstable loops are present.

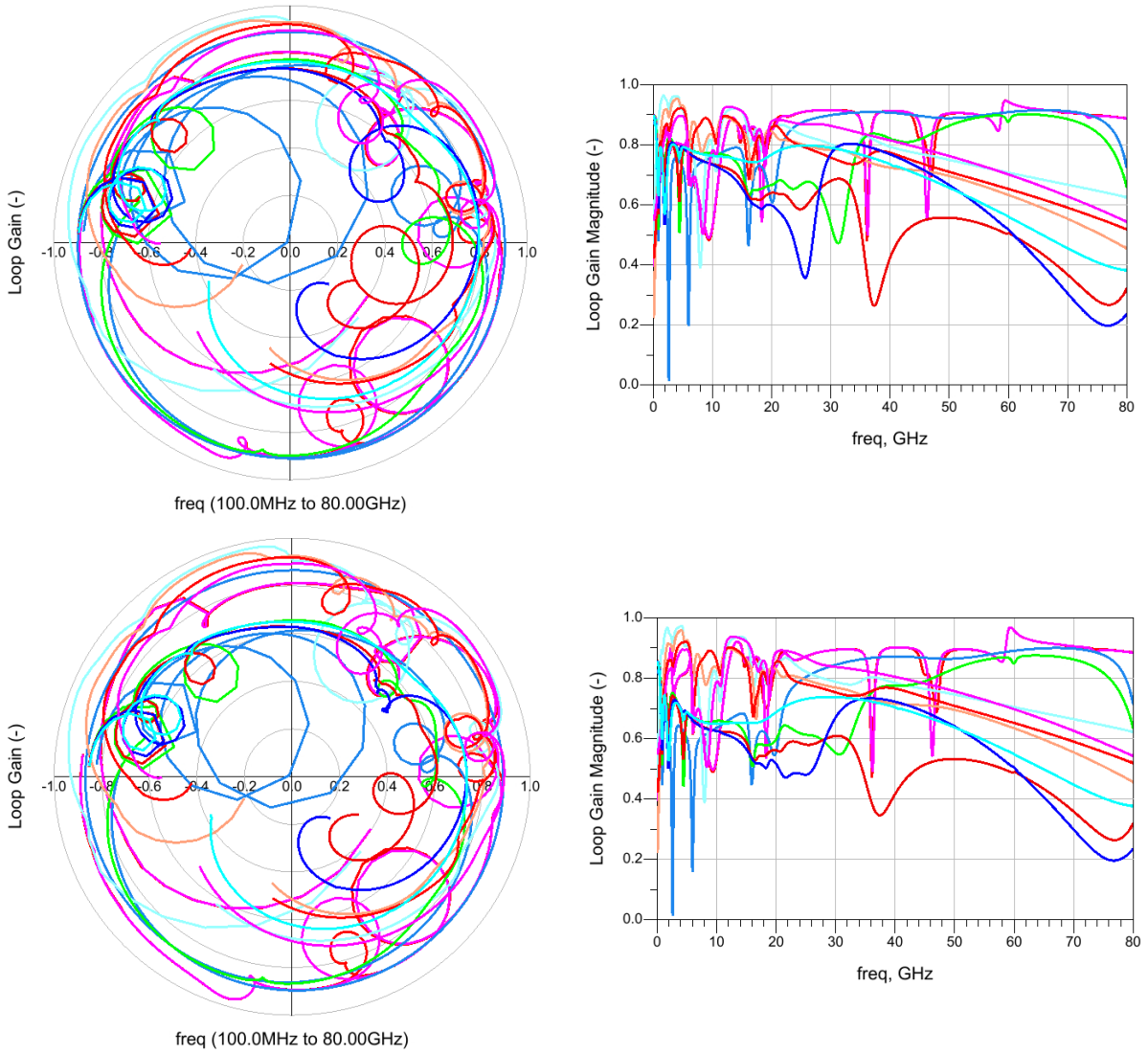


Figure 5-84 : Small signal loop gain simulation for the nominal operation at Vg=-3.1V, Vd=20V for Ta=20degC (top) and Ta=80degC (bottom), with the HPA loaded by 50ohm.

The SS loop gain analysis was repeated for both gate bais sweep at a nominal drain bias and drain bias sweep at a nominal gate bias. The results for the gate bias sweep showed that a loop appears with magnitude larger than 1, but not unstable. This loop occurs at the gate of the first stage. The drain bias sweep resulted in loop gains for Vd = 2 – 22 V at low and high temperature. No unstable loops are present.

The loop gain simulations have been repeated using the waveguide exciter as the load for nominal bias, a gate bias sweep and drain bias sweep. The results showed for a low bias voltage at the nominal gate bias a loop appears, which is very close to the unstable point. Though this was already identified from the S-parameter stability simulations that operation at low drain bias could be an issue, therefore the drain bias should only be activated in pinch-off conditions. For example Vg=-4.0V there are no unstable loops versus drain bias.

The last small signal analysis has been done to check the impact of varying source and load impedances. To check the impact of the load impedance the loads on the two differential outputs have been varied in the same way (i.e. symmetrical), under the nominal operating conditions. The magnitude of the load has been set at 0.33, 0.66 and 0.99 and the phase has been varied from 0° to 315° in 45° steps. The the load variation stability simulations resulted in no unstable loops.

This stability simulation where repeated for a varying load on only one of the differential outputs, while keeping the other output at 50ohm. Again the stability simulation results showed that this asymmetrical load variation does not cause unstable loops.

The large-signal loop gain analysis has been performed for the nominal operating bias and has focused on the loops at the gate of the first and second stage transistors, as the previous analysis has shown that these are the most critical points. First a power sweep has been done in the middle of the frequency band, for a situation with the waveguide feed load (up to 50 GHz) and with a 50ohm load (up to 80 GHz). Figure 5-85 shows that there are no unstable loops and no loops with a magnitude larger than 1.

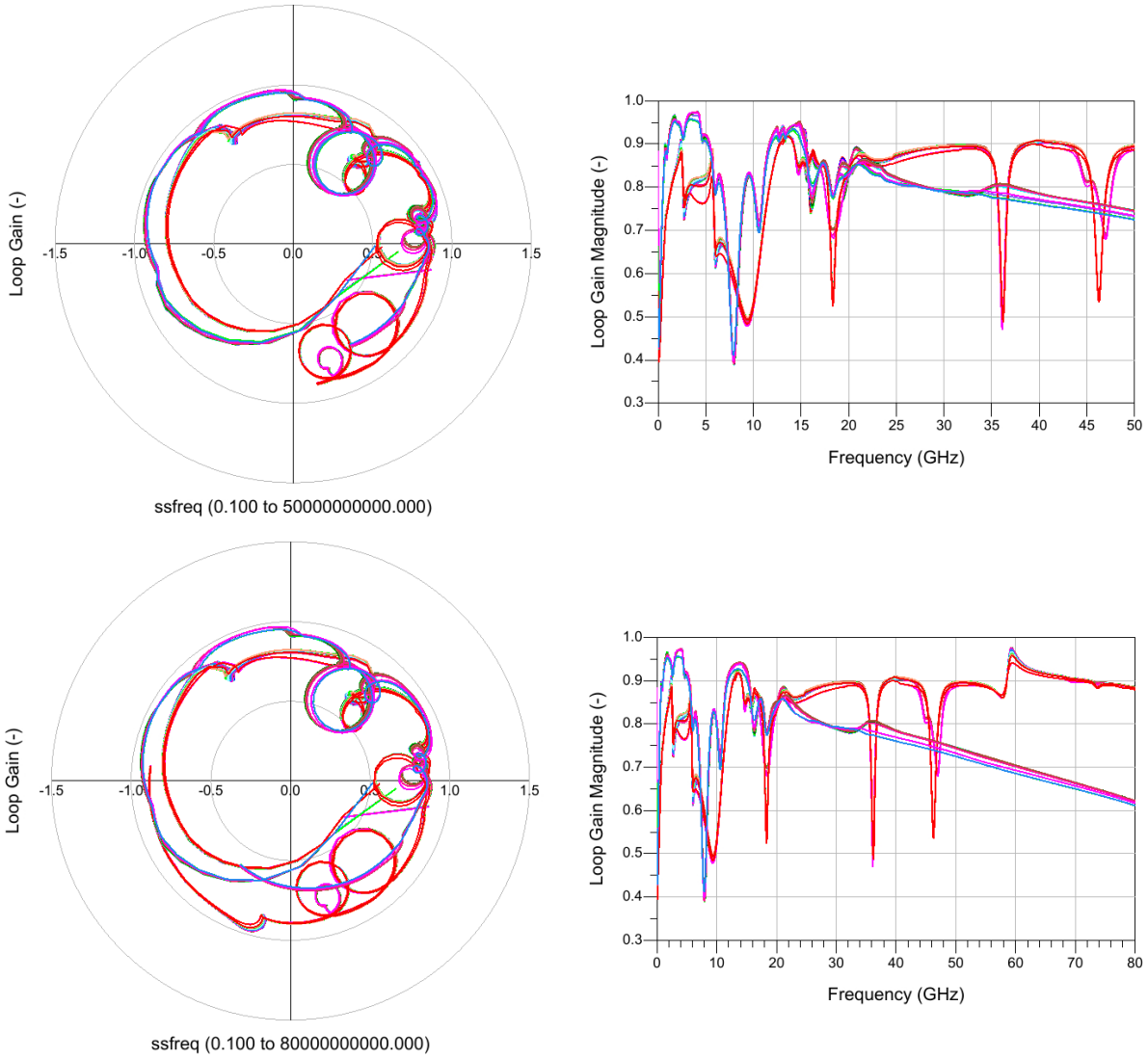


Figure 5-85 : Large signal loop gain analysis for a source power range of -25 to +25 dBm at 18.8 GHz, Vg= -3.1V, Vd=20V, Ta=80degC, waveguide feed output load (top) and 50 ohm load (bottom).

A similar simulation is performed versus RF frequency at a source power of 15 dBm. The results in Figure 5-86 and Figure 5-87 show again no loop with magnitude larger than 1.

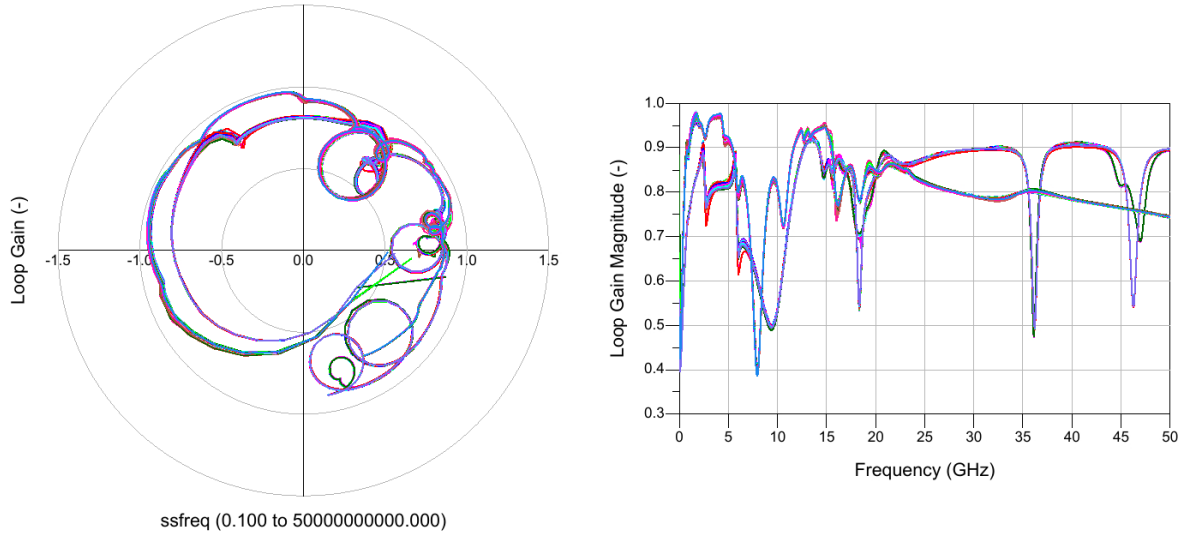


Figure 5-86 : Large signal loop gain analysis for a source power of 15 dBm at 16-21.5 GHz, Vg= -3.1V, Vd=20V, Ta=80degC, waveguide feed output load.

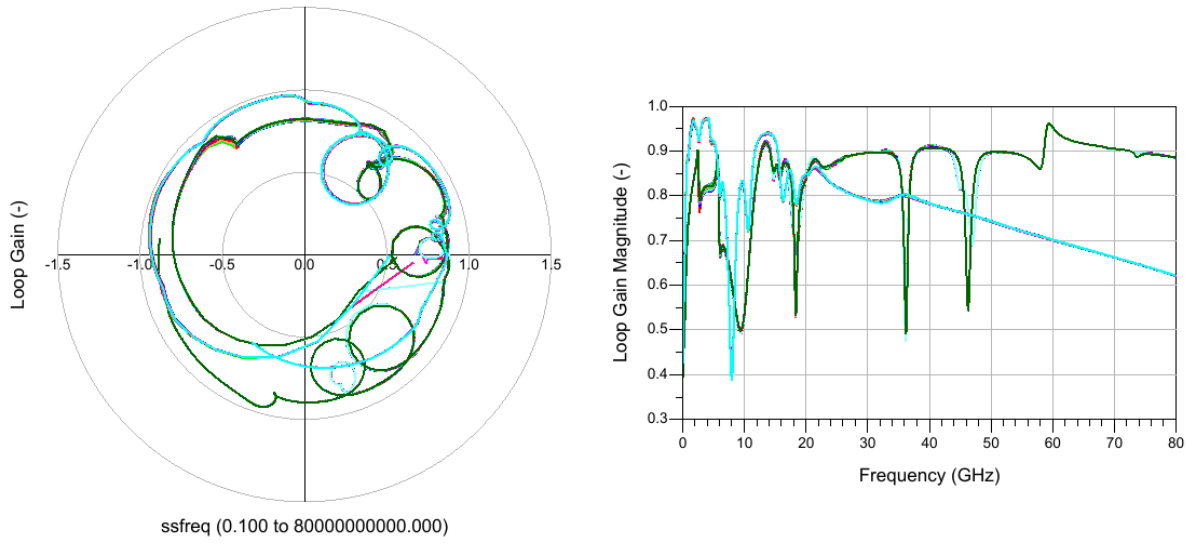


Figure 5-87 : Large signal loop gain analysis for a source power of 15 dBm at 17.3-20.3 GHz, Vg= -3.1V, Vd=20V, Ta=80degC, 50ohm output load.

Figure 5-88 shows the loop gains for a power sweep at 18.8 GHz, under nominal bias at 25degC. No unstable loops are present.

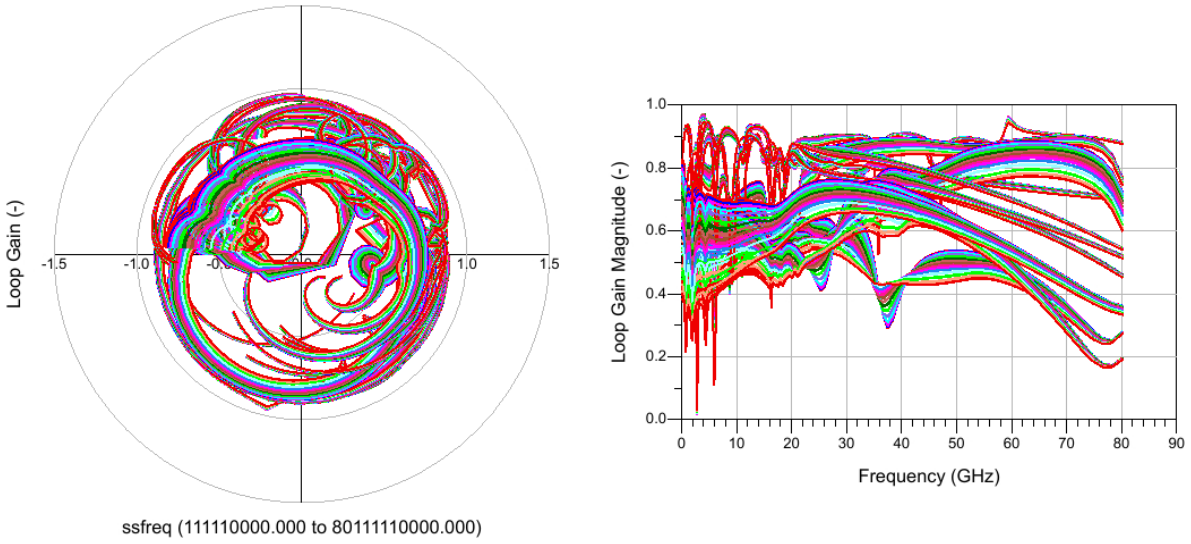


Figure 5-88 : Loop gain analysis for a source power range of +10 to +25 dBm at 18.8 GHz, Vg= -3.1V, Vd=20V, Ta=25degC, 50ohm output load, showing all 20 loops.

For a gate bias voltage higher (more positive) than -3.0V the loop gain on the input stage becomes larger than 1, but at a phase which is far from the unstable region, as shown in Figure 5-89.

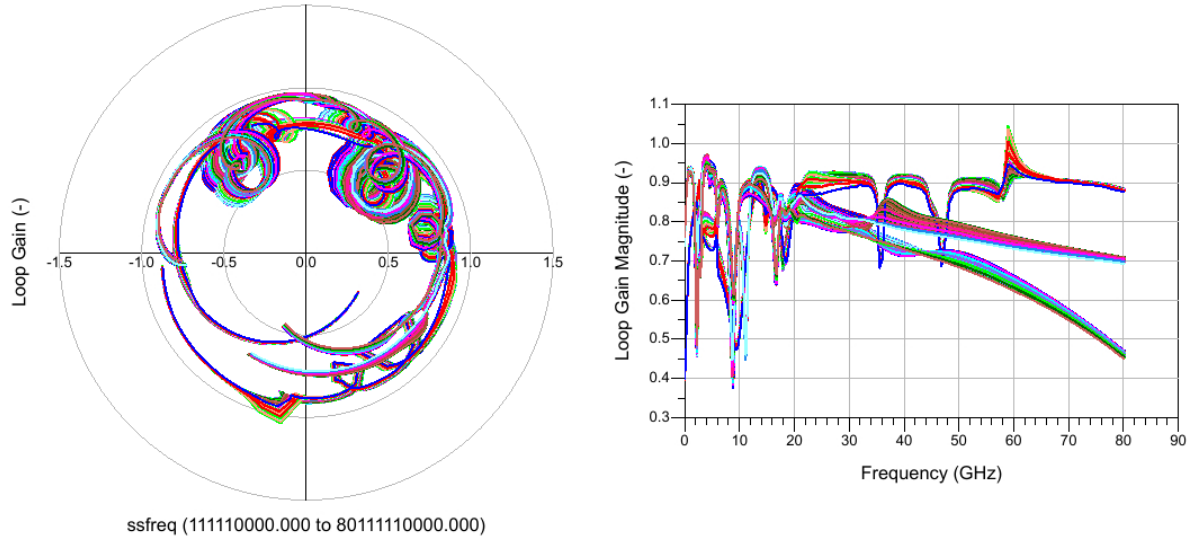


Figure 5-89 : Loop gain analysis for a source power range of -25 to +25 dBm at 18.8 GHz, gate bias range of -3.4 to -2.7V, at Vd=20V, Ta=25degC, 50ohm output load, showing the loops at the gates of the input and output stage.

Figure 5-90 shows a loop gain analysis versus source power and load impedance. Only for an almost shorted load a loop gain appears close to the +1 point, but not unstable yet.

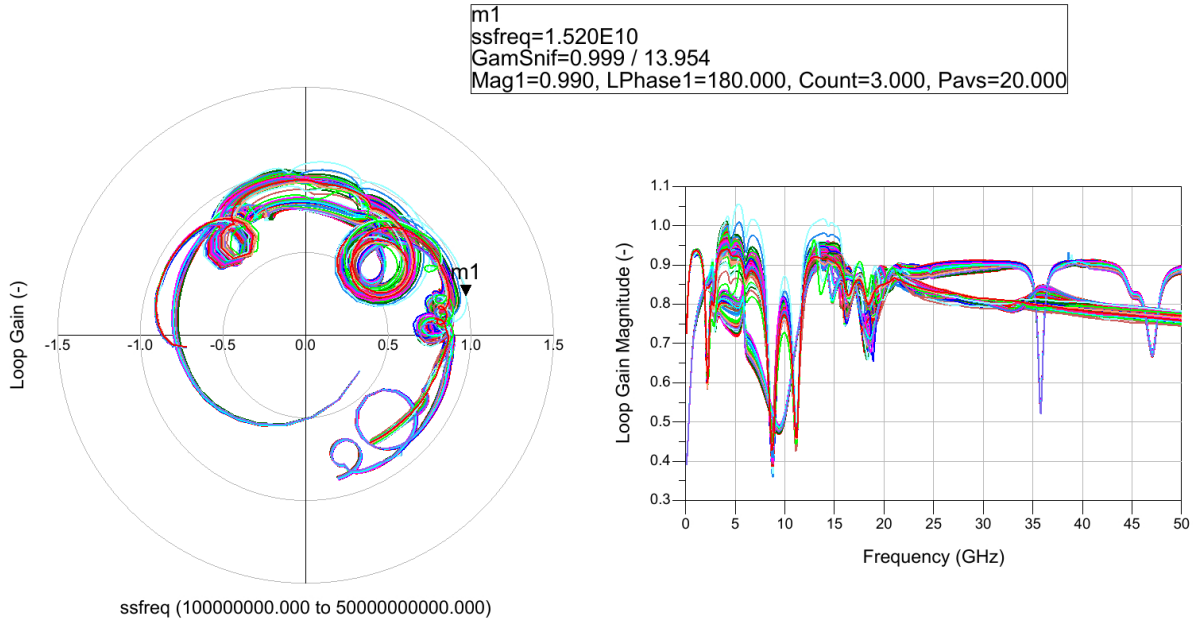


Figure 5-90 : Loop gain analysis for a source power range of -25 to +25 dBm at 18.8 GHz, Vg= -3.1V, Vd=20V, Ta=25degC, output load sweep magnitude 0.33, 0.66 and 0.99 with phase from 0-360deg, showing the loops at the gates of the input and output stage.

Figure 5-91 shows a similar analysis but now for a source impedance sweep. No loops with a gain larger than 1 are present.

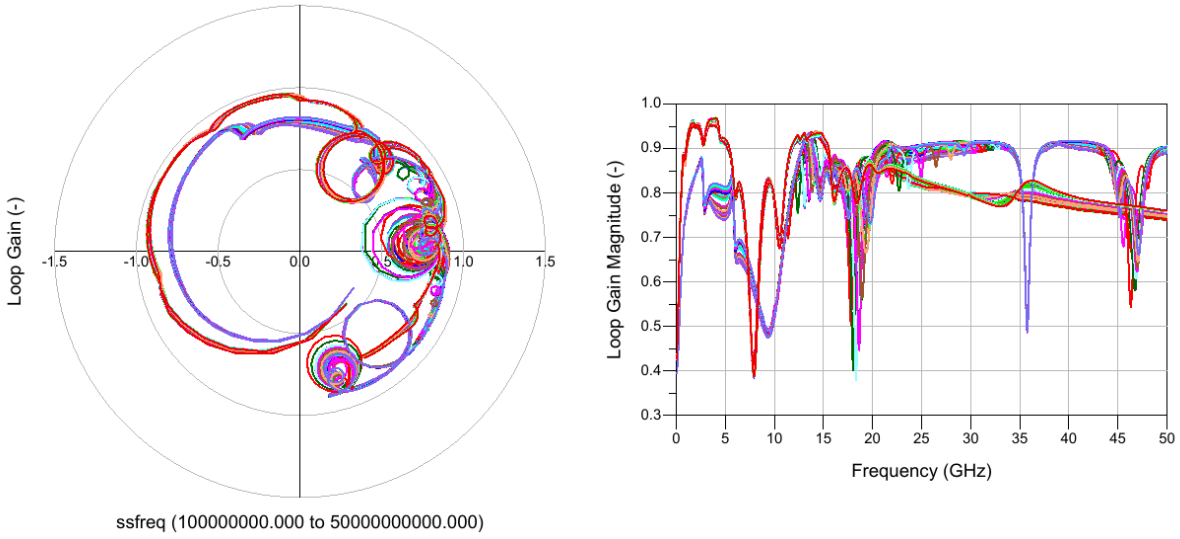


Figure 5-91 : Loop gain analysis for a source power range of -25 to +25 dBm at 18.8 GHz, Vg= -3.1V, Vd=20V, Ta=25degC, source impedance sweep magnitude 0.33, 0.66 and 0.99 with phase from 0-360deg, showing the loops at the gates of the input and output stage.

The STAN tool for pole-zero identification has been used as additional stability check, focusing especially on the critical cases that have been identified in the previous stability analyses. First the small-

signal stability versus drain bias has been checked, for the HPA with the waveguide feed at load. No right-hand poles were found, so no instabilities.

5.4.6. HPA CDR Compliance and Summary

Based on the preliminary design the final design of the DRIFT HPA has been completed. The focus of the design has been on obtaining the maximum PAE by minimizing the losses of the matching networks and in that way obtaining the best efficiency at 15 dB NPR. This has resulted in a design that is not unconditionally stable for all bias conditions, but for the nominal operating mode no instabilities have been found.

The simulation results and compliancy are shown in Table 5-13. These simulation results are obtained with Momentum EM simulations of the matching networks, 3D EM simulation of the MMIC to PCB bondwire interface, HFSS simulations for the waveguide feed and IMAL calculations to obtain the performance at 15 dB NPR.

Table 5-17 : HPA MMIC compliancy with specifications.

Parameter	Specification	Simulation at 20°C	Simulation at 80°C	Compliant?
Frequency range	17.3 – 20.2 GHz			By design
Input Return Loss	> 15 dB	> 14.5 dB	> 14.5 dB	No
Output power @ 15dB NPR	> 37 dBm	> 37.6 dBm	> 36.7 dBm	Yes at 20°C No at 80°C
PAE @ 15 dB NPR	> 35%	> 35.7%	> 32%	Yes at 20°C No at 80°C
DC power consumption	< 14.3 W	< 17.9 W	< 17.5 W	---*
Linear gain	> 20 dB	> 22.5 dB	> 21 dB	Yes
Temperature (MMIC backside)	20°C – 80°C			By design
Maximum junction temperature [1]	160°C	not simulated	< 148°C	Yes

* DC power consumption is for information purposes only and not part of the compliancy matrix.

With respect to the simulated non-compliant performances the following observations can be made:

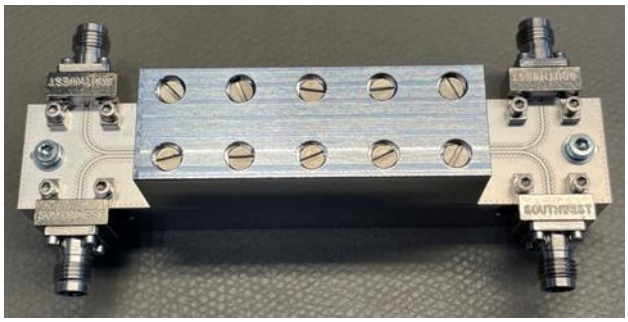
- The input return loss has proven difficult to get better than 15 dB. Design focus has been more on wide bandwidth than on matching in a smaller frequency range
- The output power of >37 dBm can be achieved at 80degC when increasing the gate bias from -3.1 V to -3.0 V, at the cost of a slight reduction of efficiency.
- As was already concluded during the preliminary design, the PAE specification of >35% at 15 dB NPR has been difficult to achieve over the full temperature range.
- The DC power consumption has been defined such that is corresponds exactly to the specified PAE and output power values. So as soon as the output power is slightly higher than specified the DC power consumption will already be too high, even if the PAE was 35%.

5.5. Wave guide and wave guide feed CDR (WP 3.2)

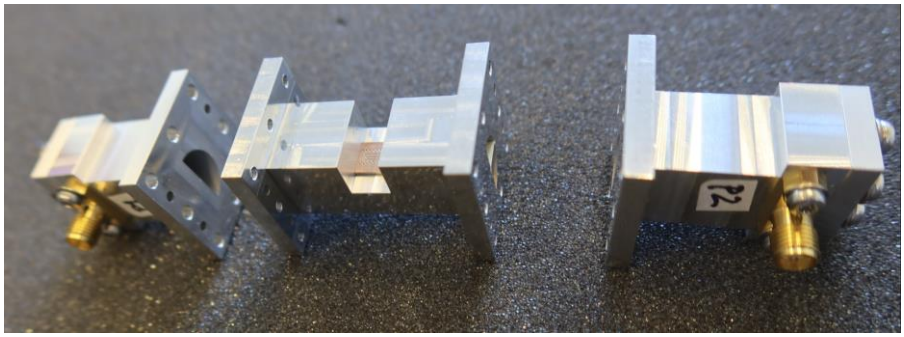
The wave guide and exciter critical design review addresses:

- the alternative wave guide design with MF Vonkverspaning and manufacturing process,
- the wave guide feed manufacturing re-spin with Eurocircuits,
- the septum design and performance
- Wave guide feed measurement results

The first iteration test structures were based on 4 single-ended grounded coplanar waveguide input lines creating a 4-port network from which the differential mode characteristics were composed indirectly. Both (identical in theory) waveguide exciters were facing each other inside a continuous semi-circular waveguide (sCWG). When resorting to standard procedures such a structure could only be built when composing it of several separate parts and using a cold joint and screws construction method, see Figure 5-92(a).



(a)



(b)

Figure 5-92: a) 4-port single-ended PCB-sCWG-PCB setup implemented for the first iteration test campaign, and b) 2-port sCWG-PCB-sCWG setup for the second iteration test campaign.

It was found that one of the aluminium-PCB interfaces introduced high losses. Through simulation this interface could be identified. It has forced an alternative test strategy and the decision was made to create exactly the opposite of the setup in Figure 5-92(a)..

In the setup shown in Figure 5-92(b) only 2-ports are accessible which are in fact single-ended sCWGs. These connect to the a sCWG-PCB-sCWG transition (center part in the figure (b)) and takes out the need of converting the single ended results into differential mode results as was previously the case. Indeed, exciting the waveguide results in its fundamental mode propagating which is picked up by the exciter and transforms it in the differential mode on the parallel line etched on the PCB. It will travel along this line (connected to free space) only to be coupled into the second sCWG through a reverse transformation. Insertion losses of the complete structure become readily available after post processing, i.e. de-embedding the coax-to-sCWG adapters.

5.5.1. Wave guide manufacturing process

For the second iteration test structures, we aimed to exclude mechanical interfacing by creating them from a single piece of aluminum using spark-erosion. This process uses high voltage to erode the metal, providing low surface roughness and precise structural features like sharp corners and uniform gaps. Two types of spark-erosion are used: wire-sparking for uniform features and sink-sparking for features up to a certain position (see Figure 5-93)).

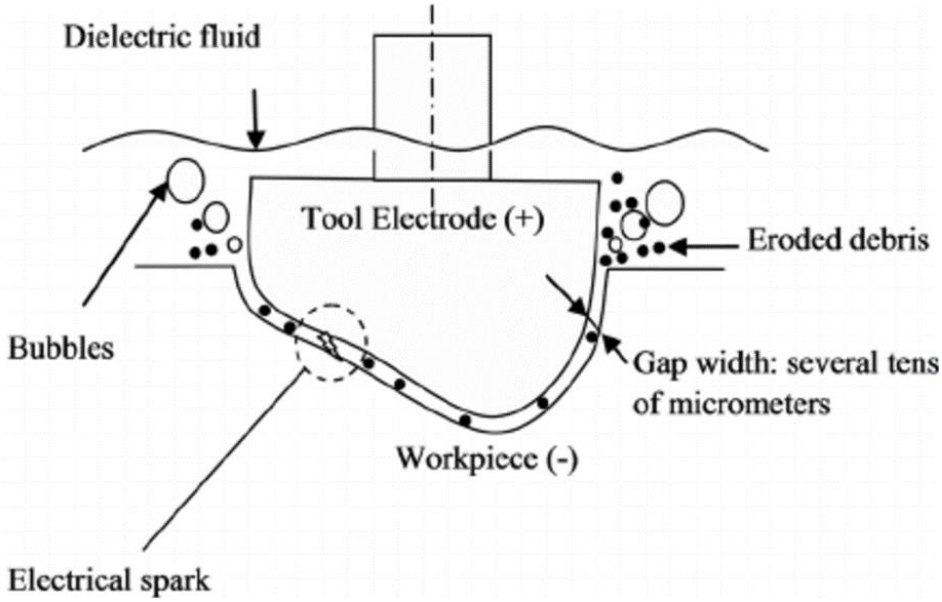
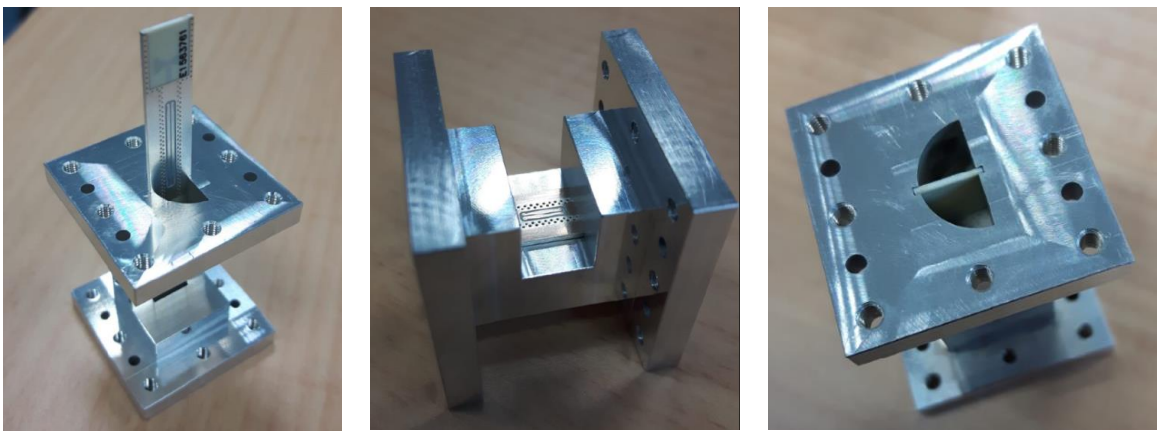


Figure 5-93: Concept of sink-sparking, schematic display

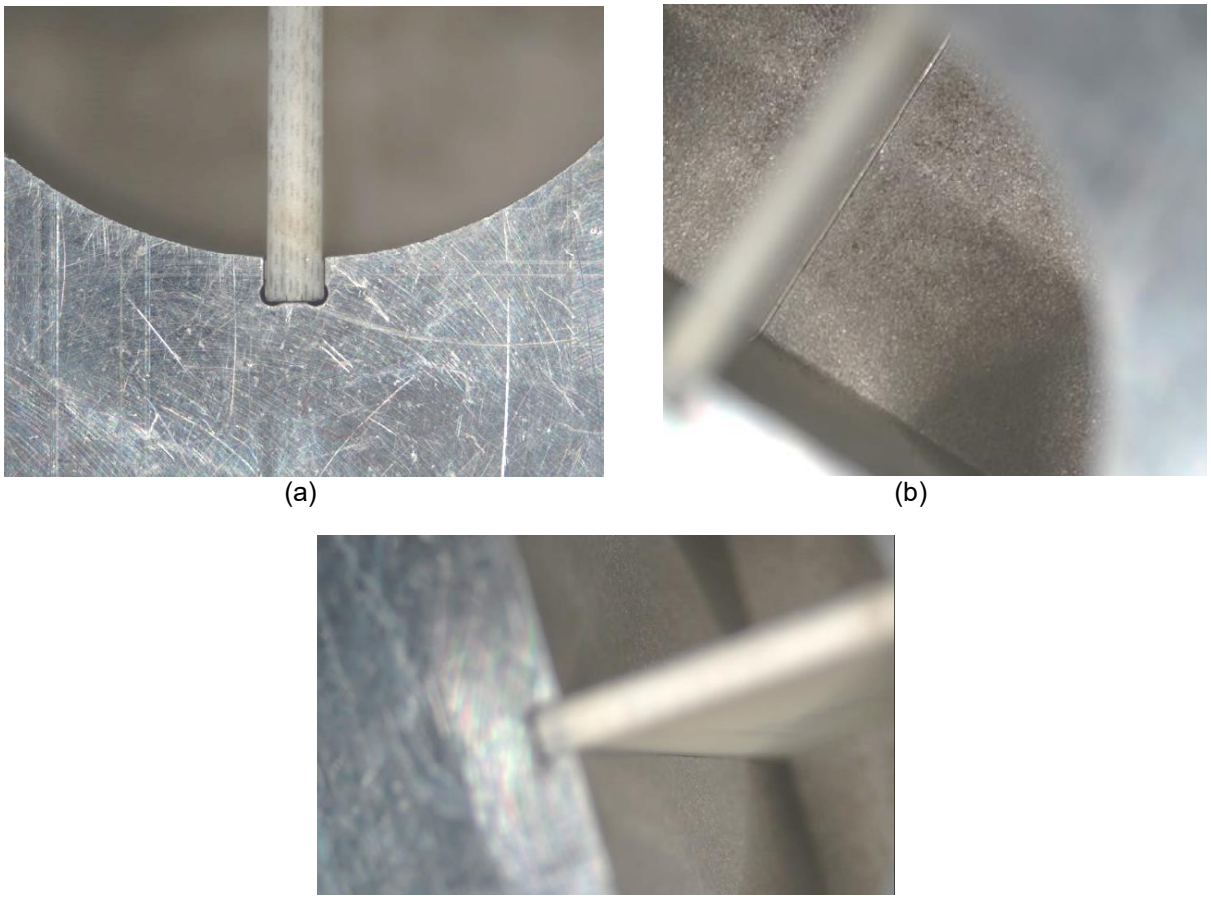
Sink-sparking is more costly depending on the shape of the electrode. Eroding sharp corners is limited with this process as the sparks have the freedom to bend as they emerge in the free space between electrode and object. However, it can be controlled by choosing the radius of the wire electrode accordingly. Bend radius in product can be as small as 0.15mm and is therefore small enough for our needs. In case of using a shaped electrode (sink-sparking), the corners can be sharper as it depends on the applied edge of the electrode itself. This is the case when creating the sCWG through sink-sparking: the corners which it features are significantly sharper than would have been possible resorting to wire-sparking. Several test structures have been manufactured with this process, a long and short version to accommodate each waveguide exciter, and some of them are shown in Figure 5-94 and details in Figure 5-95.

All the test structures are well made, and the treated surfaces have low surface roughness much less than 5um. To fit the PCBs inside the waveguide pieces they had to be sanded (with a very fine grade) beforehand. Subsequently a jig was used to accurately slide them into the waveguides and alcohol was applied to provide lubrication.



(a) (b) (c)

Figure 5-94: Some of the test structures: (a) PCB is slid into the semi-circular waveguide (sCWG) piece. (b) Dipole exciter PCB placed in the sCWG piece with the transmission line visible which is outside the waveguide connected to free space. (c) View into the sCWG.



(a) (b)

(c)

Figure 5-95: Zoom of the test object with the PCB in place. (a) Tight fit of the PCB in the waveguide piece. (b) Focus on the back wall of the sCWG, and (c) on the bottom wall of the sCWG.

Waveguide feed PCB re-spin

To address the need for additional exciter PCBs, production was shifted from ACB to Eurocircuits (EC) due to ACB's long lead times and poor quality. EC, lacking a Teflon-based substrate line, required a switch from RO3003 to RO4350B, introducing a 0.1dB loss. Despite this, the decision was made to validate the concept, as EC have a short lead time of 7 days.

Upon delivery the PCBs have been visually inspected under the microscope, some views are shown in Figure 5-96. It can be seen from the photos how well the vias are placed on the pads of the parallel transmission line (Figure 5-96(b)). Milling out (routing) the individual PCBs from the manufactured multi-layer production panel resulted in rough edges as shown in Figure 5-96(c).

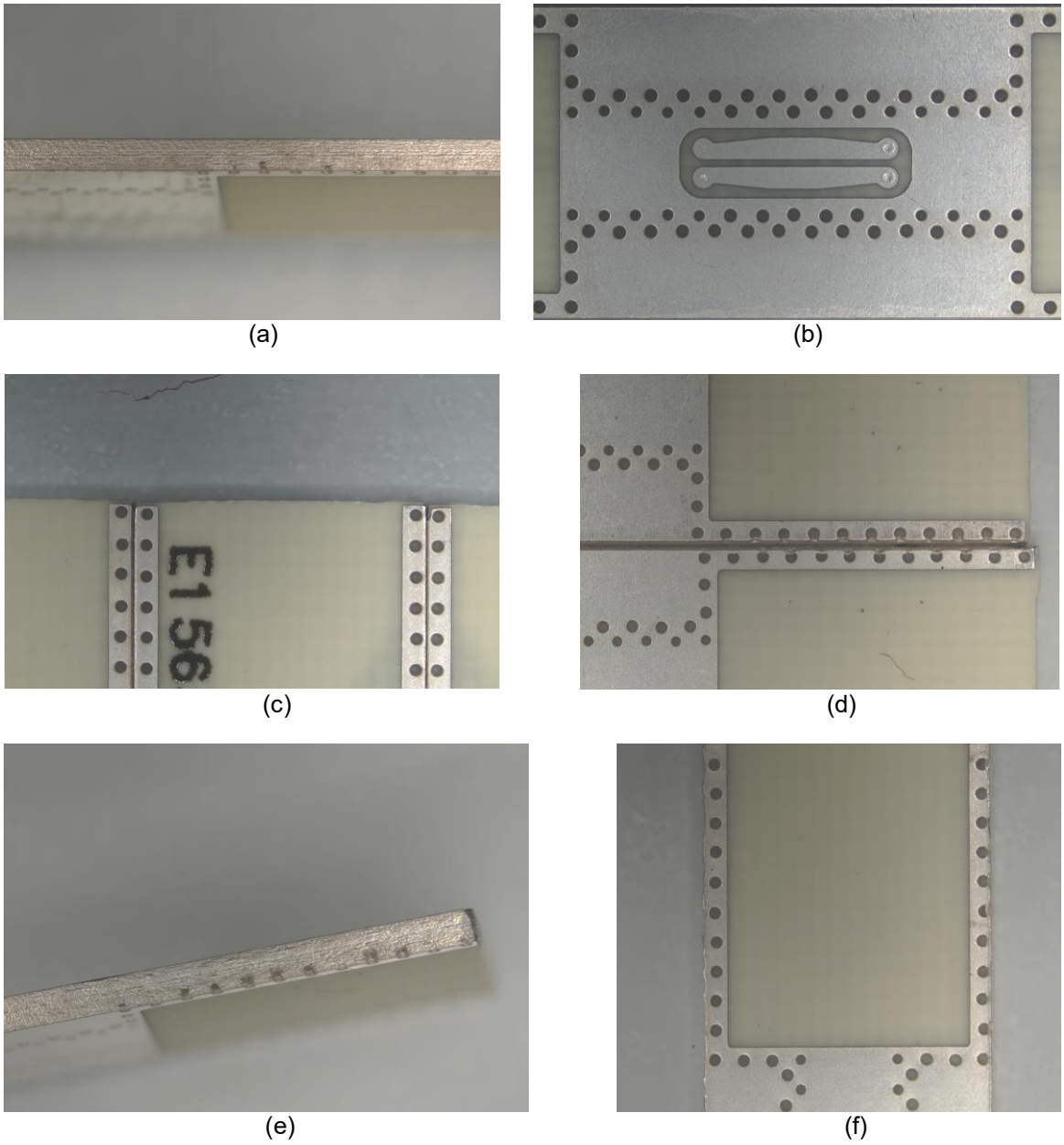


Figure 5-96: PCBs manufactured by Eurocircuits. (a) Silver plated edge, (b) parallel line with vias neatly placed in the pads. (c) View on the milled edges of the PCBs, (d) via placement on the edges in some cases is off centre, and (e) results in open voids on the PCB's edge. (f) Rough metal edges.

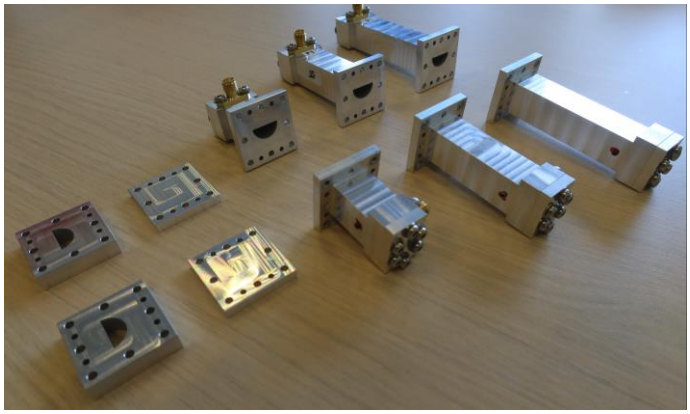
The remaining photos indicate that the positioning of the grounding vias on the narrow copper strips on the PCB edges are sometimes too far to the side. It causes openings on the PCB sides. It seems that this is a combination of tolerance in via placement and routing, this is concluded from Figure 5-96(f) where the vias on the left narrow metal strip are mostly centered while the ones on the right narrow strip are not. Figure 5-96(e) shows that the tool used for routing the individual PCBs is not straight: only half of some vias are cut open, where it is assumed that the plated via holes themselves are straight.

5.5.2. Waveguide feed test setup

As the waveguide testing philosophy has changed, the feeding transmission lines are now sCWGs instead of single ended grounded co-planar strip lines. For these lines specific TRL calibration standards have been designed. These standards are shown in Figure 5-97(a), complemented with shorting plates and two line lengths options ($\lambda_g/4$, and $\lambda_g/2$) where λ_g indicates the guided wave length inside the sCWG. Different length standards have been defined to also assess the losses of

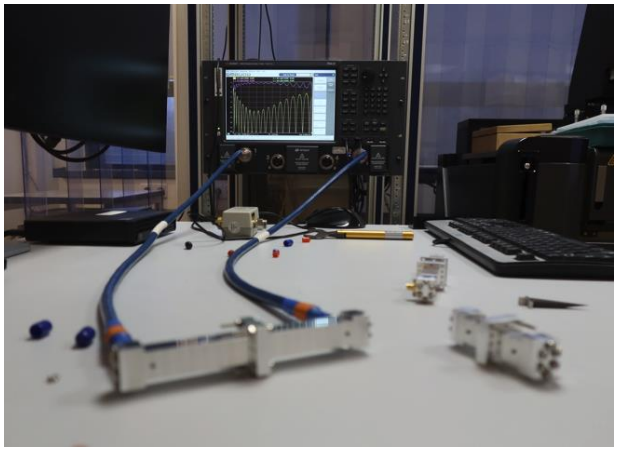
the waveguide. In the same figure (b) and (c) shows the setup when measuring the Vivaldi exciter PCB. In

Table 5-18 a list of the performed tests is presented. Note that the table indicates the test setups always to consist of three separate structures.



(a)

(b)

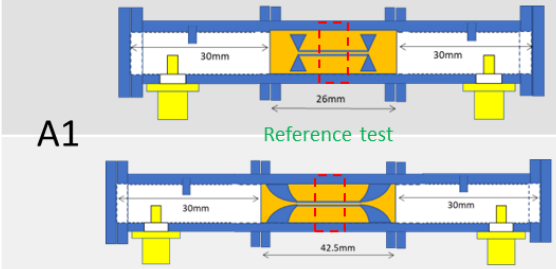
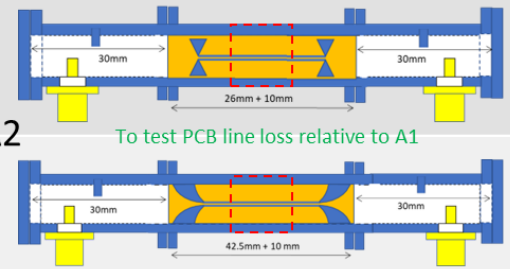
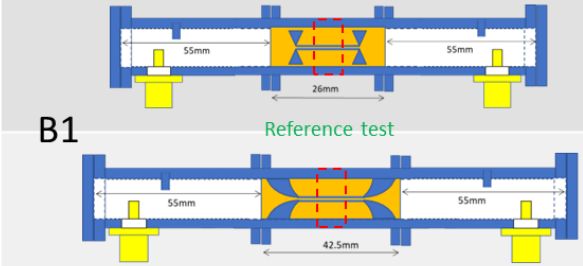
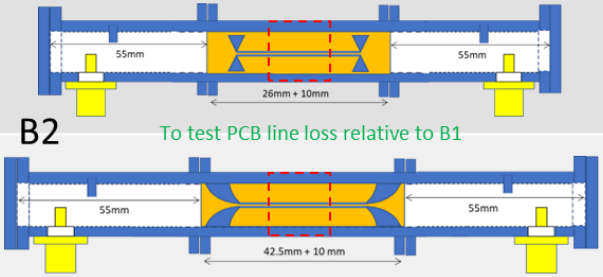
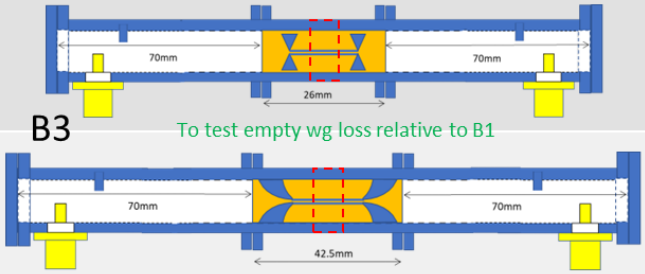


(c)

Figure 5-97: (a) TRL calibration standards, only the 30mm (the shortest set) were intended to act as calibration standards. (b) Testing the structure with the Vivaldi exciter PCB included. (c) Impression of the test setup.

With reference to Figure 5-94, the structure accommodating the PCB has the waveguide part exactly of the length of the PCB.

Table 5-18: Definition of the different test setups to characterise the test structures. Short and long refer to the piece of parallel line between the exciters.

	Short exciter	Long exciter
30mm adapters	 A1 Reference test	 A2 To test PCB line loss relative to A1
55mm adapters	 B1 Reference test	 B2 To test PCB line loss relative to B1
70mm adapters	 B3 To test empty wg loss relative to B1	- -

Note the dashed red box in each schematic representation of a test setup: it represents the part of the waveguide structure containing the PCB where the parallel transmission line connects to free space.

As can be seen in

Table 5-18, two versions of each exciter PCB have been defined:

- Dipole-short
- Vivaldi-short
- Dipole-long
- Vivaldi-long.

Difference between the short and long PCB versions is 10mm in parallel line length, and constitutes to roughly λ_g at mid band. This, with similar reasoning for the extra line lengths for the calibration standards, has been done to measure the losses of this particular line. The losses of the empty sCWG are measured at 0.04dB/λ_g (see Figure 5-98) at mid band.

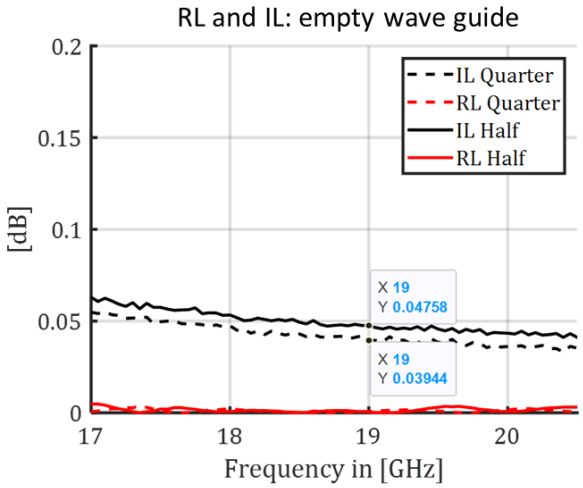
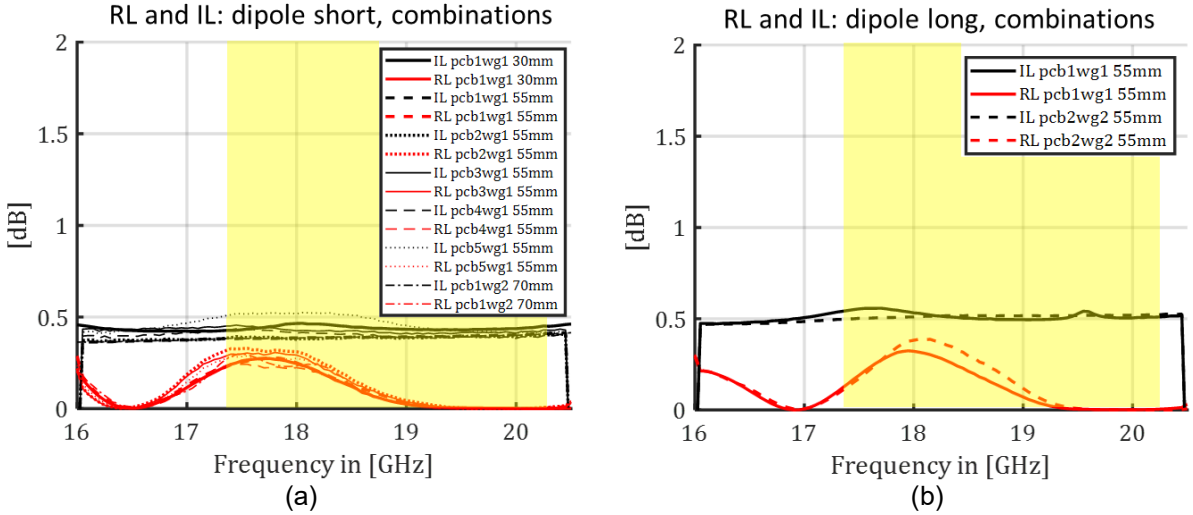


Figure 5-98: Measured losses of the empty $\lambda_g/4$ and $\lambda_g/2$ waveguide sections.

5.5.3. Waveguide feed measured results

All measured S-parameters have been de-embedded to exclude the contribution of the waveguide adapters obscuring the relevant performance. The measurement campaign evaluated not only the wave guide performance but also the repeatability over 5 different PCB for each wave guide feed type and 2 wave guide builds.

During testing the Vivaldi exciter has been more extensively tested than the dipole exciter. This was instigated by its prominent mid band IL increase. Nevertheless, from the measured results involving most of the available PCBs and their related waveguide structures it can be concluded that the dipole exciters produce more stable results and also the lower loss compared to the Vivaldi exciters.



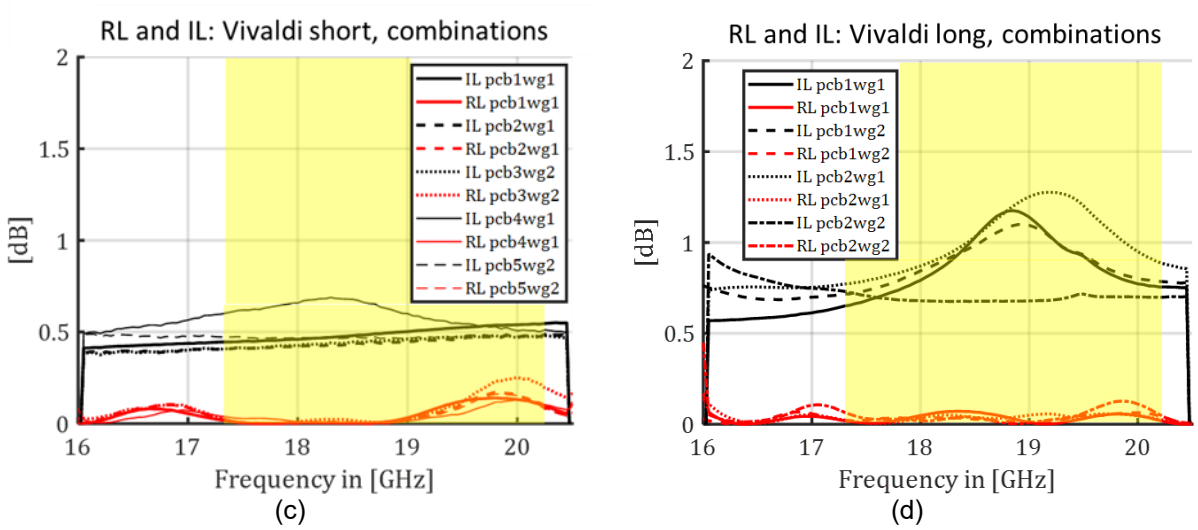


Figure 5-99: Test results of the available PCBs in their related waveguide structures.

In Figure 5-100 a comparison is made for both exciter types between simulated and their best measured loss performance. Both wave guide feed types have resulted in a insertion loss < 0.6 dB and the wave guide manufacturing process of arc ersion has been successful.

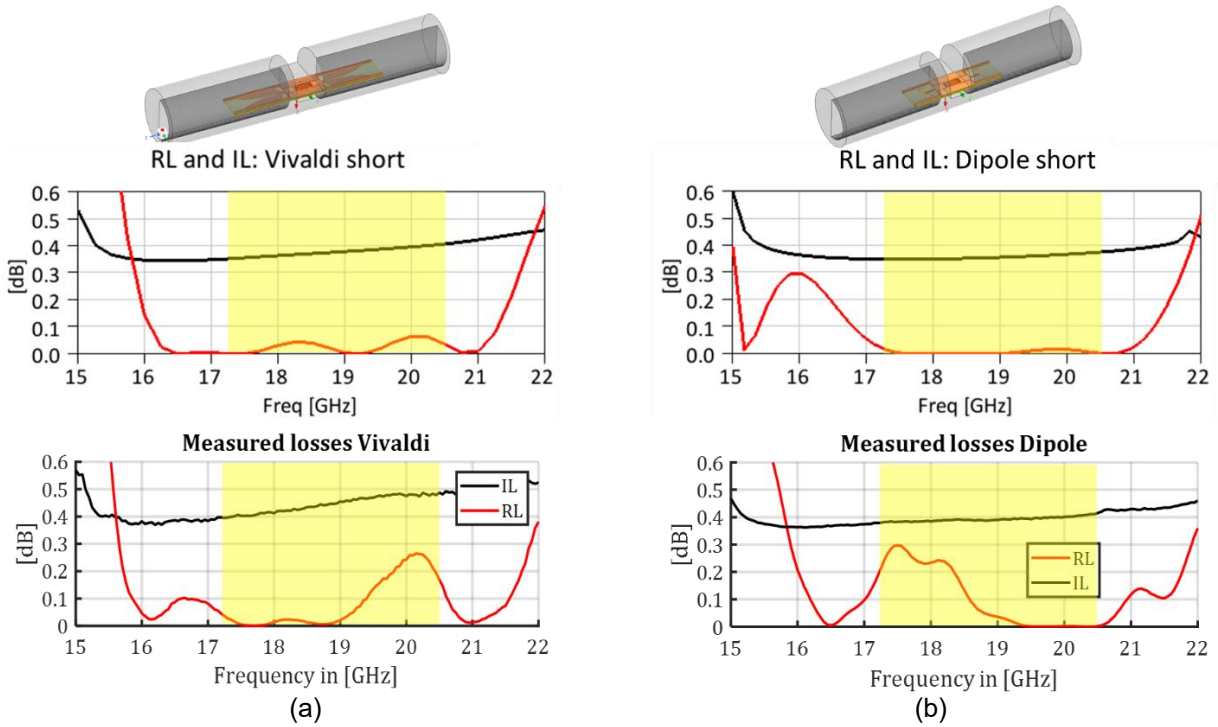


Figure 5-100: Comparison of the simulated and measured insertion loss in case of: (a) Vivaldi exciters, and (b) Dipole exciters.

5.5.4. Waveguide feed polarising septum design

For the demonstrator a complete cascade of the wave guide feed, polarising septum and horn performance evaluation is required which will yield an optimal axial ratio result. At the same time the reflection coefficient seen at the exciter input must be retained at the same level as we have seen it in the simulations involving only the exciter coupling into the empty sCWG. Also the coupling between the two input ports of the front-end radiating module needs to be as small as possible. Two types of septum

have been designed and evaulated, i.e.: exponentially tapered and stepped, see Figure 5-101(a) and (b) respectively.

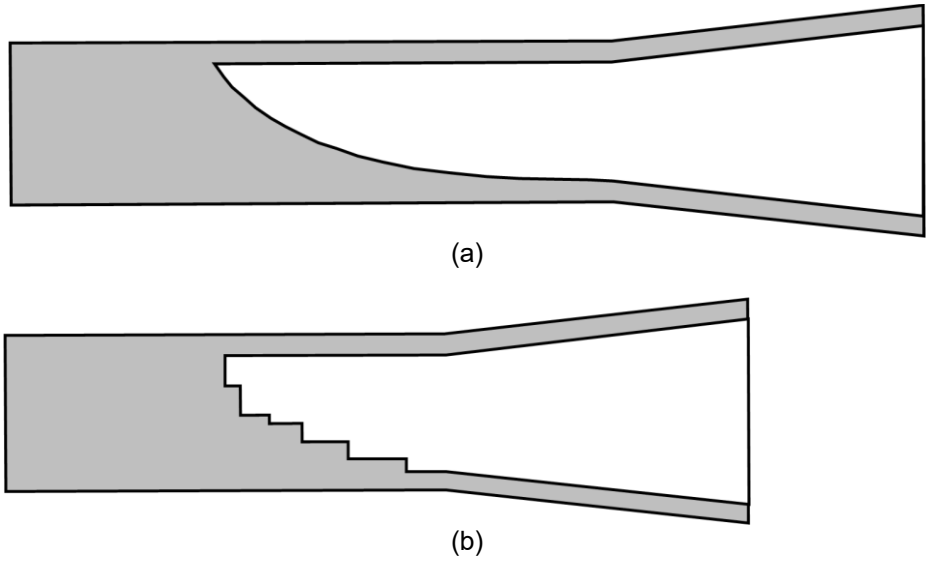


Figure 5-101: Different polarising septum solutions: (a) exponentially tapered 91mm, and (b) stepped 76mm.

5.5.5. Simulated performance of the radiating module

It appeared to be more difficult to generate sufficiently low axial ratio over the frequency band of interest for the exponentially tapered septum than is the case for the stepped septum, see Figure 5-102. Also, the stepped septum achieves this over significantly less length making the total cascade more compact. The stepped septum measures (waveguide + septum + horn) 76mm, whereas the exponential tapered septum results in a total length of 91mm.

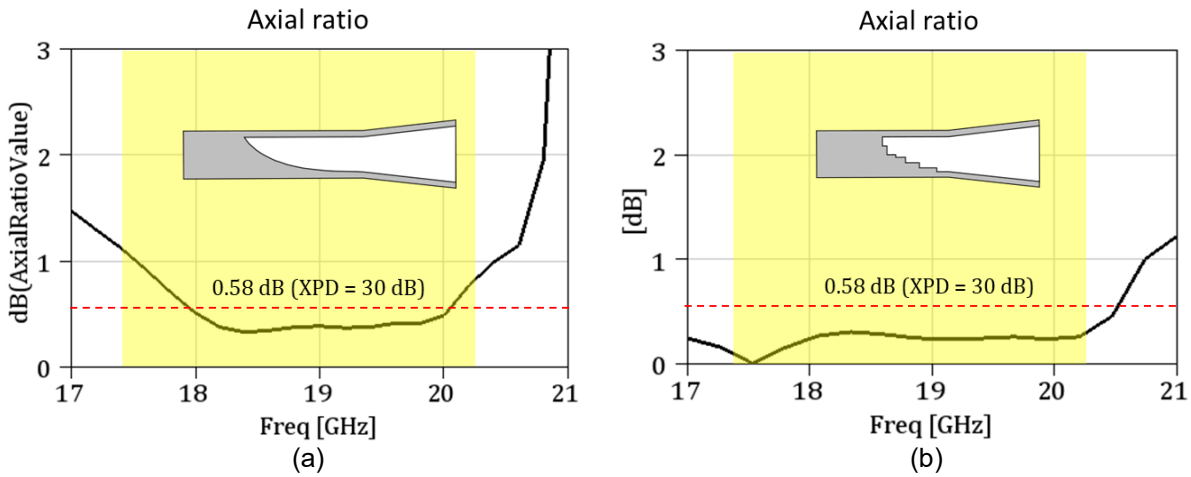


Figure 5-102: Simulated axial ratio for: (a) exponentially tapered septum, and (b) stepped septum.

For the stepped septum solution the axial ratio is well above the specified cross polarisation discrimination (XPD) requirement of 30dB. When observing the reflection and coupling between the two input ports, see Figure 5-103, it can be seen that the input reflection is quite sufficient always remaining well below -15dB in the presence of the septum and horn section. The low coupling between the input ports (mainly lower than -30 dB) contributes to the low axial ratio and the total efficiency in general.

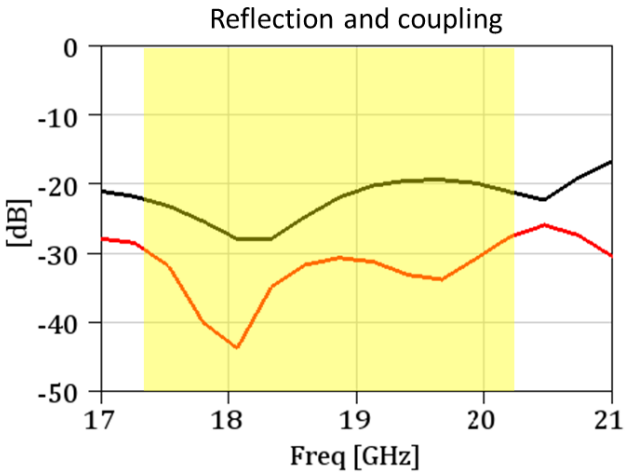


Figure 5-103: Reflection seen at the input of a single exciter (black curve), and coupling between the two exciters (red curve) which is very low.

Spark-erosion can be applied with high accuracy to produce the required structures. In order to assess the sensitivity of the radiating front-end to the production tolerance two integral scaling factors have been introduced in the simulator to work on the septum polariser only. This part of the front-end is considered as most sensitive to the production tolerances. It consists of delicate steps of which the smallest feature measures just about a millimetre. The value range of both scaling factors have been set to represent the tolerances expected in the adopted spark-erosion process, i.e. ±10 um for the smallest feature. One factor works on all the step lengths, the other on all the step heights. Applying the factors in this way does not create the same absolute decrease/increase in height and length for each step. Indeed, it rather induces a more dramatic change where small sizes see less change than large sizes. Care has been taken that the average size change of the steps lines up with the mentioned production tolerance. Implementing it this way in the model was the most convenient. The results of the tolerance study are shown in Figure 5-104.

Apparently taking into account the production tolerances on the septum polariser the simulated performance (axial ratio and scattering parameters) remain within specification.

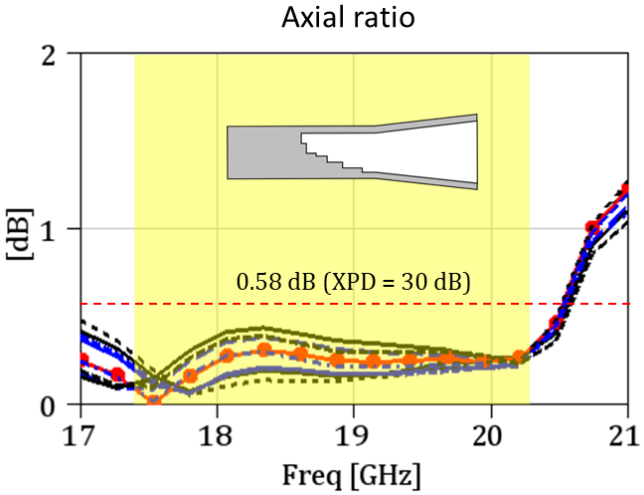


Figure 5-104: Axial ratio of the passive radiating front-end taking into account spark-erosion tolerance. Step sizes have been varied using a single factor to work on all step heights and a single factor to work on all step lengths. Nominal performance is represented by the red solid line with red circles.

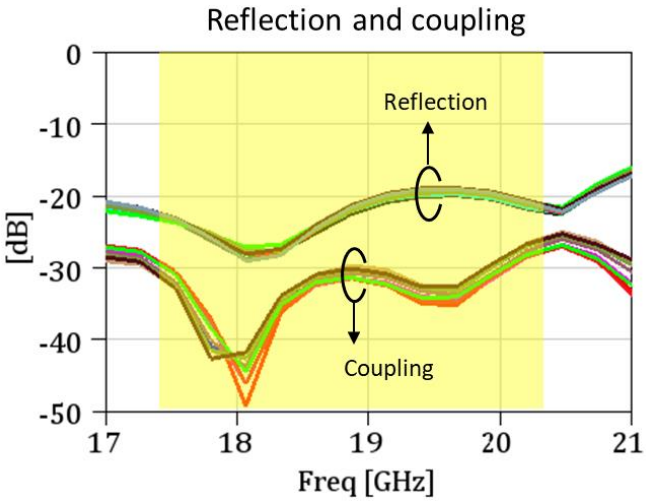


Figure 5-105: Variation in the reflection and coupling due to production tolerance on the polarising septum. Performances are quite clustered indicating tolerance effects are minimal.

Finally, an impression of the test ready demonstrator model including the exciter, septum polariser, horn section and active components is presented in Figure 5-106.

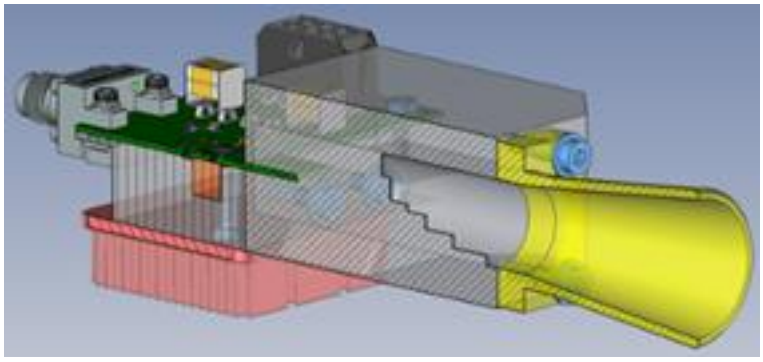


Figure 5-106: Cut-away impression of the designed septum polariser and COTS horn section with dipole exciter for the active demonstrator.

5.5.6. CDR Waveguide Conclusion

An alternative approach to the test procedure has been adopted to validate the loss performance of the designed exciters. This approach resulted in a more straightforward measurement sequence but also an alternative set of test structures. In order to minimise metallic interfaces in the waveguide structure itself the team has resorted to spark-erosion as a manufacturing technique. It is a well-known technique but not often encountered in antenna design. The resulting waveguide structures are made out of one piece and include all the necessary features to accommodate the exciter PCBs.

Insertion losses of both the dipole and Vivaldi exciter are according to simulations and only slightly increase with frequency for the former and more increase for the latter. On average the losses for the dipole are at 0.4dB and those of the Vivaldi at 0.45dB. Especially at the higher frequency end of the band the dipole is favoured with almost 0.1dB less IL (e.g. Figure 5-100). Note that the exciters are built using non-Teflon based material, i.e. RO4350B instead of RO3003. The reasons for this have been discussed in the report and adds 0.1dB of extra loss.

For the demonstrator design the dipole exciter has been chosen, it is significantly shorter than its Vivaldi counterpart, has the most repeatable results, better performance if a poor edge connection is made, has the lowest loss and is therefore selected as the preferred exciter. The argument of less length is a relevant one as it was shown that the shorter the PCB the better and reliable the metallic contact

between it and the waveguide can be made. Obviously this will also result in more lengthy waveguide. The complete cascade of exciter + polarising septum + horn has been optimised in terms of XPD/axial ratio, reflection loss and cross talk between both input ports.

Table 5-19: Compliancy

Parameter	Specification	By simulation	By measurement
Frequency range	17.3 – 20.2 GHz	Yes	Yes
Input return loss	> 15 dB	Yes	Yes*
Polarisation	CP (switchable)	Yes	- NA -
XPD (AR)	> 30 dB (< 0.58 dB)	Yes	- NA -
Beam scan maximum	8.7°	- NA -	- NA -
Hexagonal lattice	d = 51.9 mm	Fits within cell size	- NA-
RF input impedance	50 Ω or co-design	50 Ω	50 Ω
Loss	=<0.6 dB	< 0.6 dB**	< 0.6 dB**

*: through reasoning, refer to paragraph **Error! Reference source not found.**
**: considering the expected additional losses (bonding pads + bond wire (<0.05dB TAS-F), polariser (<0.03dB simulated), horn section (<0.03dB TAS-F)), even when considering RO4350B as substrate material which induces an additional 0.1dB w.r.t. RO3003

5.6. DRIFT Demonstrator (WP 3.3)

This section shall detail the DRIFT demonstrator in full. Figure 5-107 through to Figure 5-109 show the demonstrator from multiple angles. Each angle highlights all demonstrator features such as: waveguide body, horn, septum, PCB, PCB back plate, components, heat sink and fixture screws.

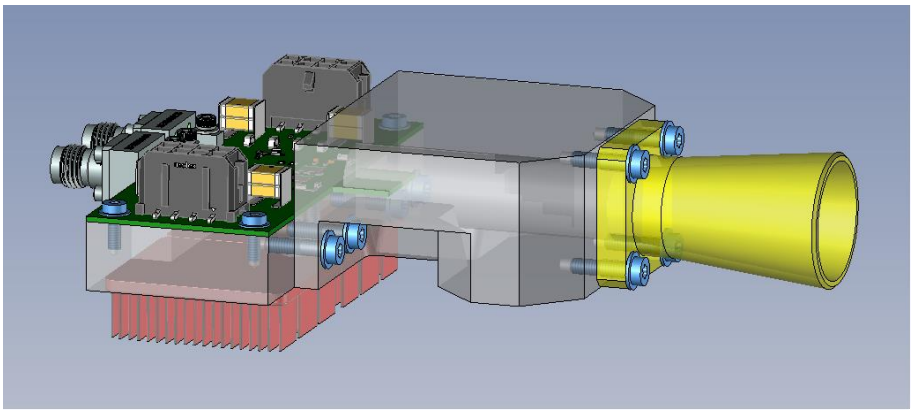


Figure 5-107 DRIFT Demonstrator top side view.

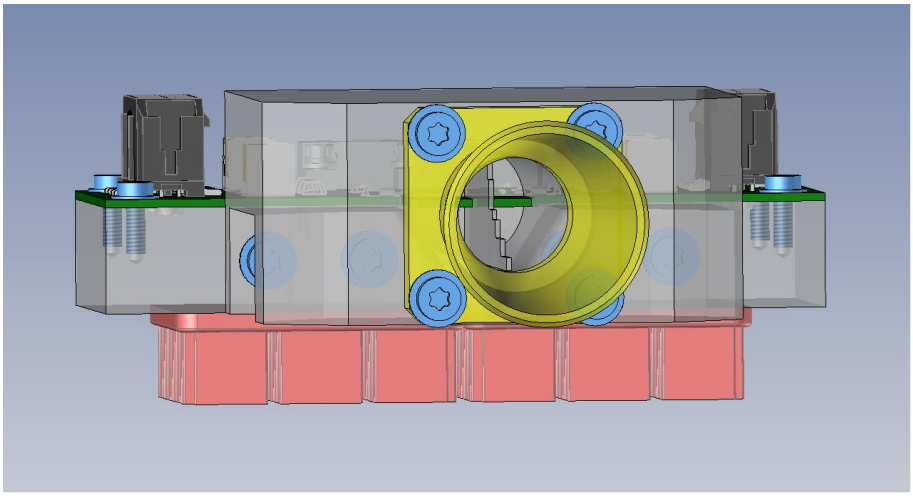


Figure 5-108 DRIFT Demonstrator front view.

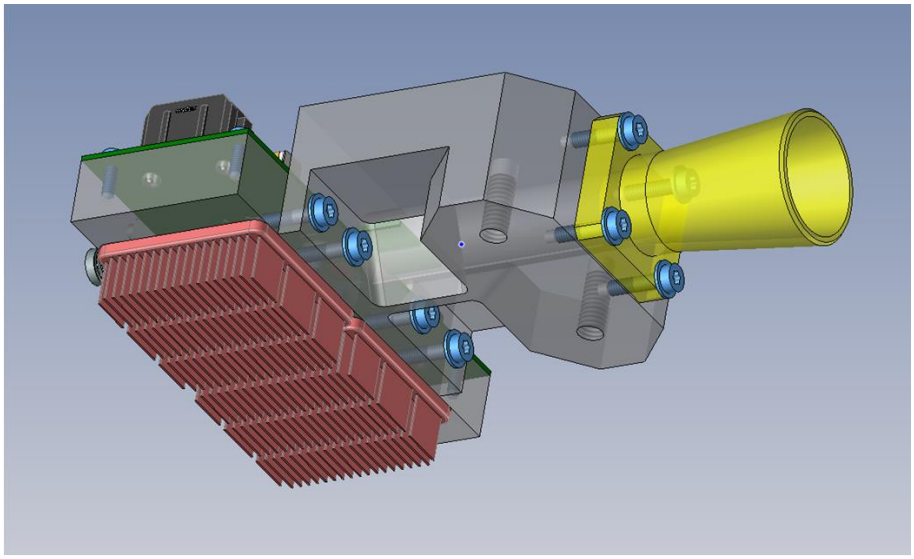


Figure 5-109 DRIFT Demonstrator bottom side view.

The wave guide is manufactured out a single piece of metal using a process called Spark-Erosion performed by the company “MF Vonkverspaning”. Figure 5-110 through to Figure 5-112 shows dissected demonstrator views from multiple angles. These drawings illustrate the stepped septum details, how the wave guide exciter slides into the wave guide and the tungsten heat sink is fitted to below the HPAs.

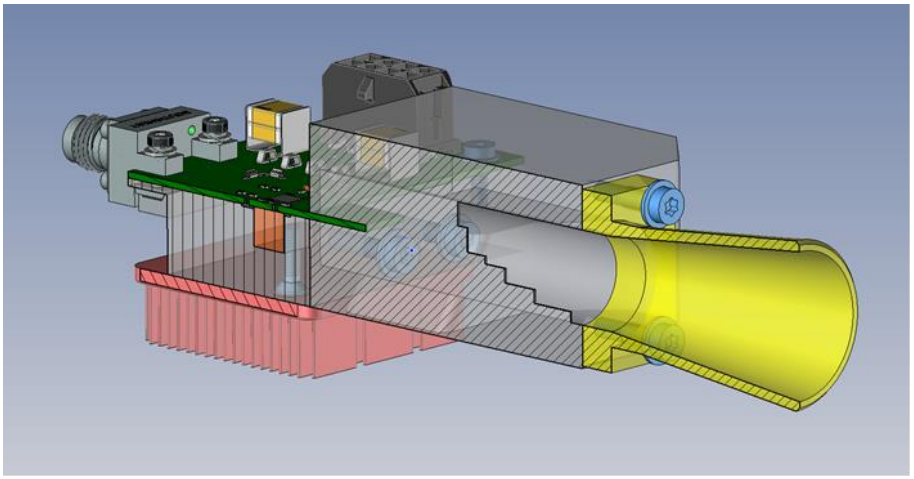


Figure 5-110 DRIFT dissected top side view.

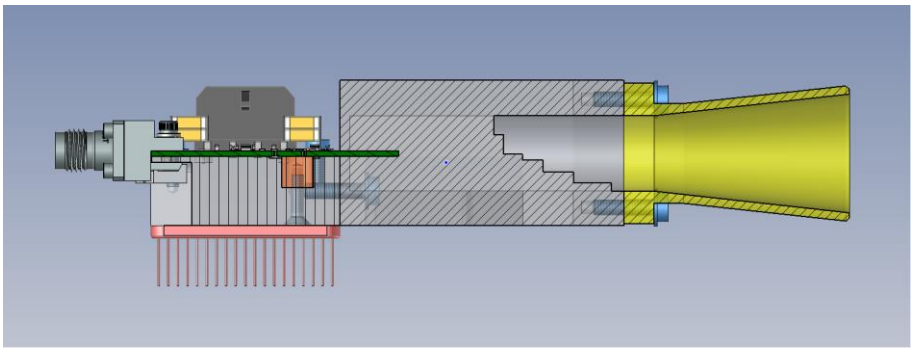


Figure 5-111 DRIFT dissected side view.

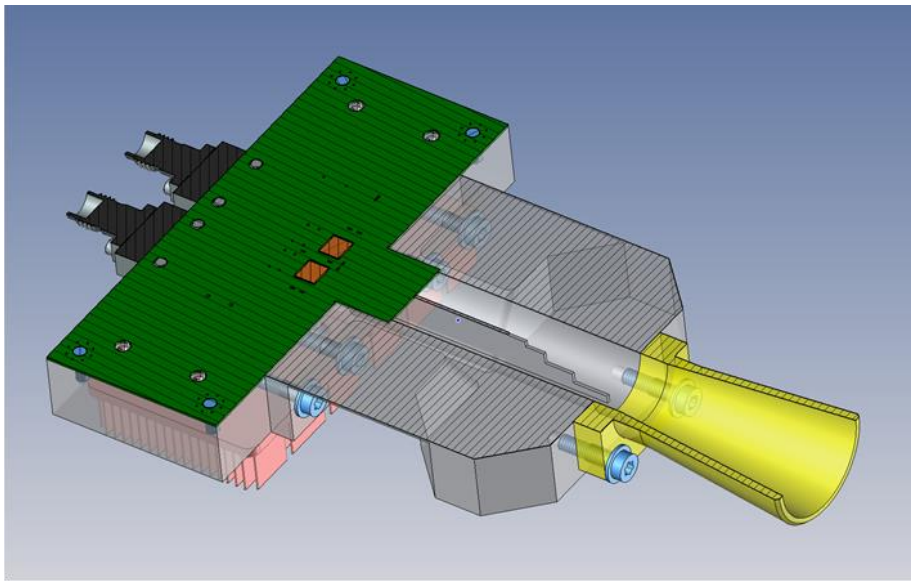


Figure 5-112 DRIFT dissected top side view.

5.6.1. DRIFT Demonstrator PCB

Figure 5-113 shows the DRIFT demonstrator schematics consisting of two differential HPA MMICs designed as per the DRIFT HPA CDR specification. The PCB has 2 HPA fitted per PCB. The additional schematic components are decoupling capacitors and RF connectors and DC test points. The PCB to MMIC connection shall be wire bonded.

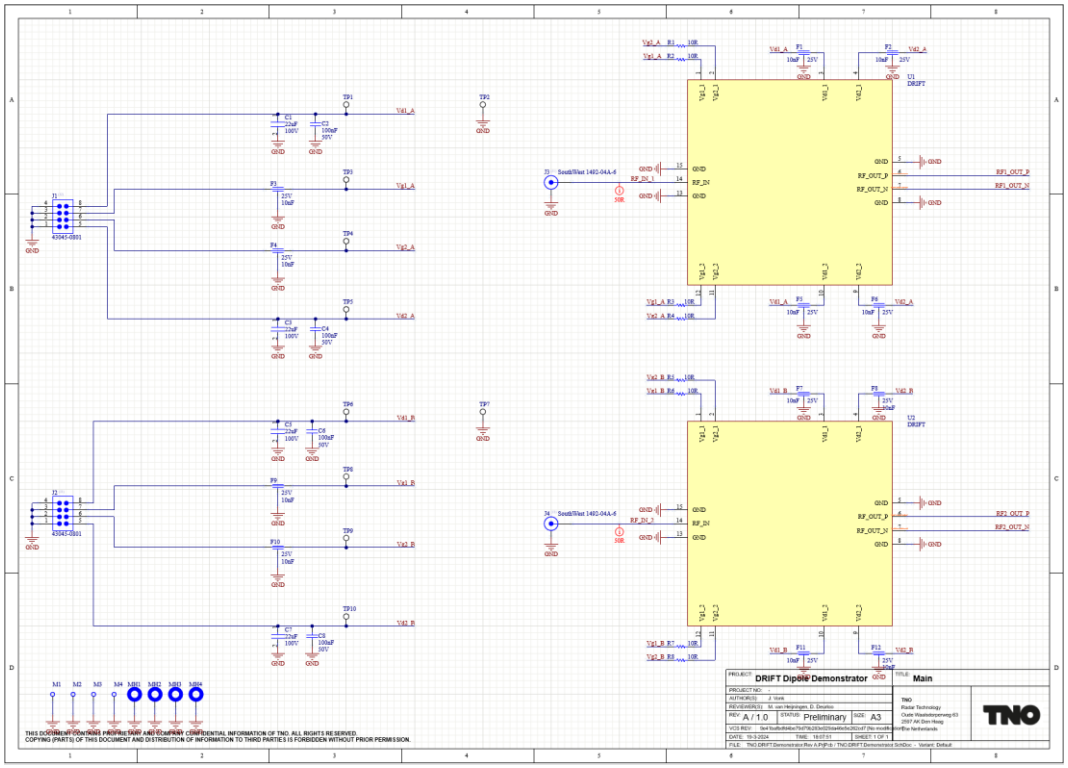


Figure 5-113 DRIFT Demonstrator PCB Schematic

Each PCB has its own independent drain and gate plus provided by its own Molex Microfit connector. The reason for independent connectors is for fault finding (if necessary), de-risking HPA oscillation and to simplify PCB routing.

5.6.2. Technology and Layer Stackup

The DRIFT PCB RF technology chosen is RO4350B and the manufacturer is Eurocircuits based in Belgium. The DRIFT demonstrator PCB uses a 4 layer board and the layer stackup can be seen in Figure 5-114.

#	Name	Material	Type	Weight	Thickness
	Board Layer Sta...	SM-001	Solder Mask		0.0254mm
	Top Surface Fini...	Immersion Silver	Surface Finish		0.02mm
1	L1 (Top)	CF-003	Signal	1/2oz	0.018mm
	Core 1	RO4350B	Core		0.254mm
2	L2	CF-003	Signal	1/2oz	0.018mm
	Prepreg 1	RO4450F	Prepreg		0.101mm
	Prepreg 2	RO4450F	Prepreg		0.101mm
3	L3	CF-003	Signal	1/2oz	0.018mm
	Core 2	RO4350B	Core		0.254mm
4	L4 (Bottom)	CF-003	Signal	1/2oz	0.018mm
	Bottom Surface...	Immersion Silver	Surface Finish		0.02mm
	Board Layer Sta...	SM-001	Solder Mask		0.0254mm

Figure 5-114 DRIFT Demonstrator PCB layer Stackup

Layer 1, depicted in Figure 5-114 as L1 is only used for RF microstrip routing and layer 2 (L2) as ground. Layer 3 is used for routing the DC connections and layer 4 is ground. All PCB design's shall be fitted in a panel and will be manufactured from the same batch.

Connector pinouts

The DRIFT demonstrator has both DC and RF as show in Figure 5-113 as J1 & J2 and J3 & J4 respectively. In addition to the RF and DC connector there are wire to board connections implemented via a gold bondwire.

The 8 pin DC Molex Microfit connector (J1 and J2) pinout is:

- Pin 1: GND (Ground)
- Pin 2: GND (Ground)
- Pin 3: GND (Ground)
- Pin 4: GND (Ground)
- Pin 5: Vd2 (HPA Drain 2)
- Pin 6: Vg2 (HPA Gate 2)
- Pin 7: Vg1 (HPA Gate 1)
- Pin 8: Vd1 (HPA Drain 1)

The DRIFT demonstrator PCB has 2 RF input SouthWest connector J3 and J4 and there pinout is:

- Pin 1: RF
- Pin 2: GND

The DRIFT HPA wire bonding pinout is;

- Pin 1 & 12: Vg1
- Pin 2 & 11: Vg2
- Pin 3 & 10: Vd1
- Pin 4 & 9 : Vd2
- Pin 5, 8, 13 & 15: GND
- Pin 6 & 7: RFout
- Pin 14: RFin

5.6.3. DRIFT Demonstrators PCB 3D View

The waveguide feed critical design review evaluated 2 wave guide exciters: Vivaldi and Dipole; concluding that the Dipole is the preferred option. As the DRIFT demonstrator PCB is the same irrespective of the wave guide exciter both designs shall be shown. The DRIFT demonstrator PCB with dipole and Vivaldi wave guide exciter can be seen in Figure 5-115 and Figure 5-116 respectively.

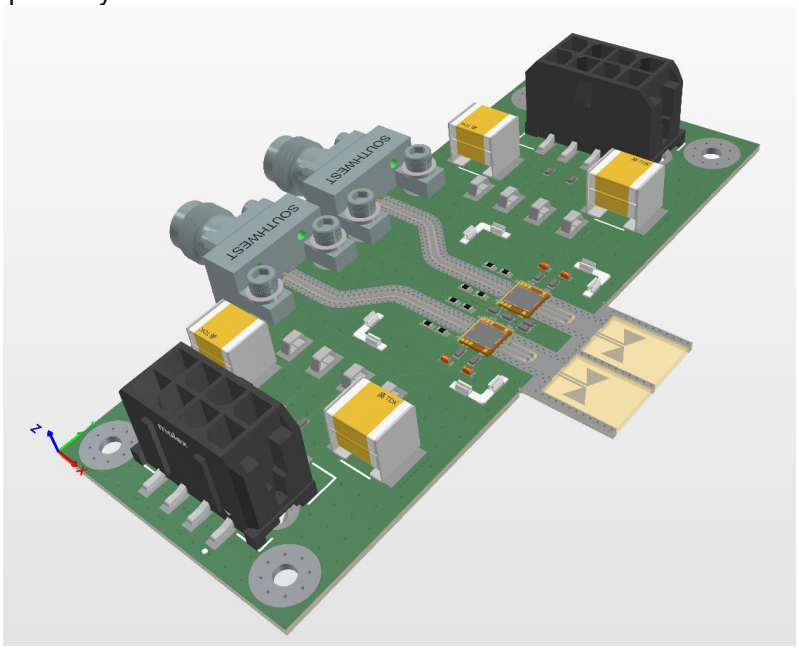


Figure 5-115 DRIFT Demonstrator PCB with Dipole.

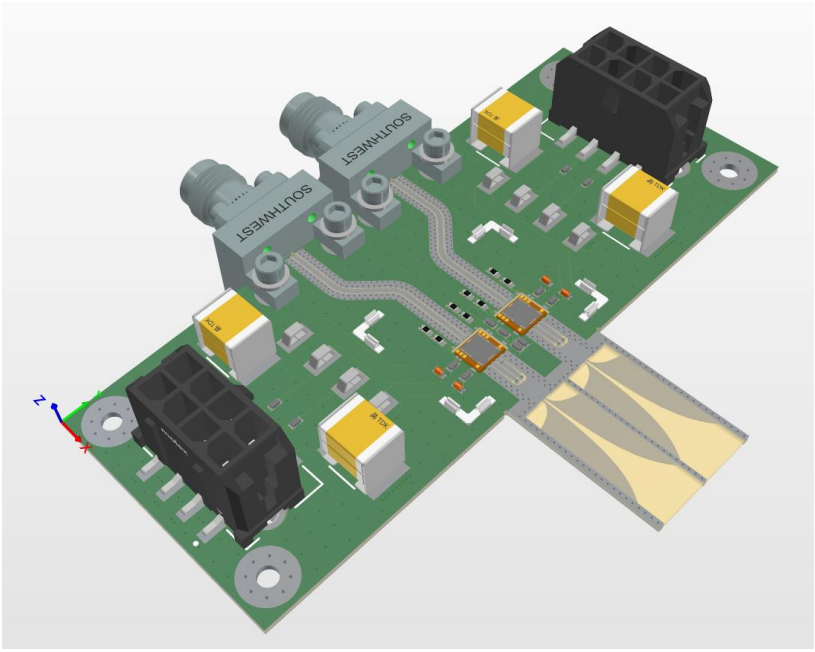


Figure 5-116 DRIFT Demonstrator PCB with Vivaldi.

The PCB dimensions: 30mm and 75mm respectively. There are 4 screw fixing holes on the outer edges which will be used to secure the PCB to the metal back plate. The PCB also has lid fixtures to project the exposed MMIC die and bond wire.

5.6.4. Assembly and Wire Bonding

DRIFT PCB will be assembled in multiple stages. The PCB passive components shall be assembled at TNO and back plate fitting. The PCB fitted to the back plate will then be sent to CICT to assembly the MMIC to the Cu-Mo Carrier. The Cu-Mo carrier-MMIC assembly will then be mounted to the demonstrator back plate on Cu-Wu slug which is placed inside the PCB back-plate which will align with HPA PCB cavity. Each mounting step shall use conductive epoxy with good thermal conductivity such as silver. The final step is MMIC to PCB wirebonding, each wirebond is illustrated in Figure 5-117.

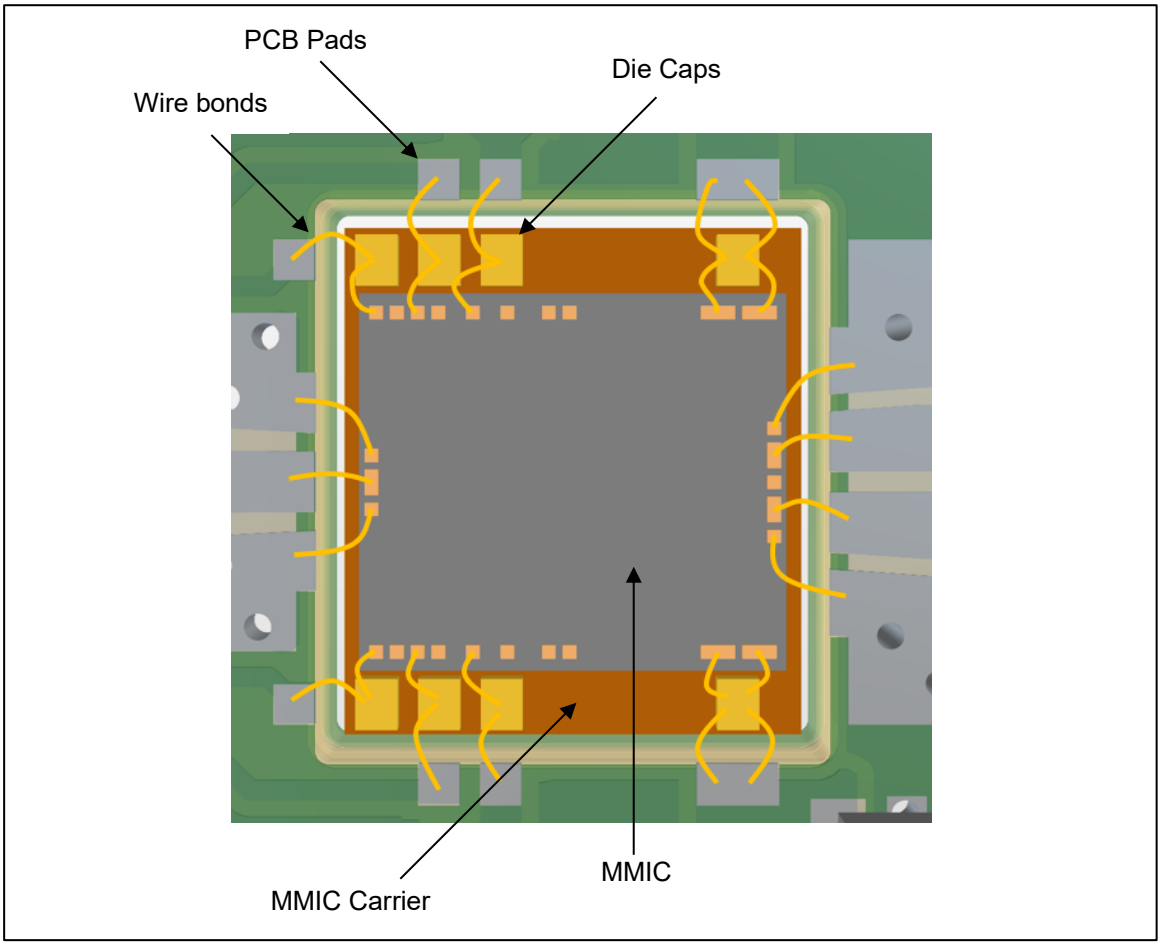


Figure 5-117 Detailed view of HPA MMIC assembly and wirebonding.

5.6.5. Assembly Sequence & Test Mounts

This sections details the order, in which the demonstrator is assembled and illustrates the test mounting fixtures. Figure 5-118 shows an exploded view of the total assembly which each individual part marked in the following order:

1. Demonstrator PCB
2. MMIC Mounting Module
3. PCB Mounting structure
4. Heatsink
5. Waveguide Structure
6. Horn waveguide

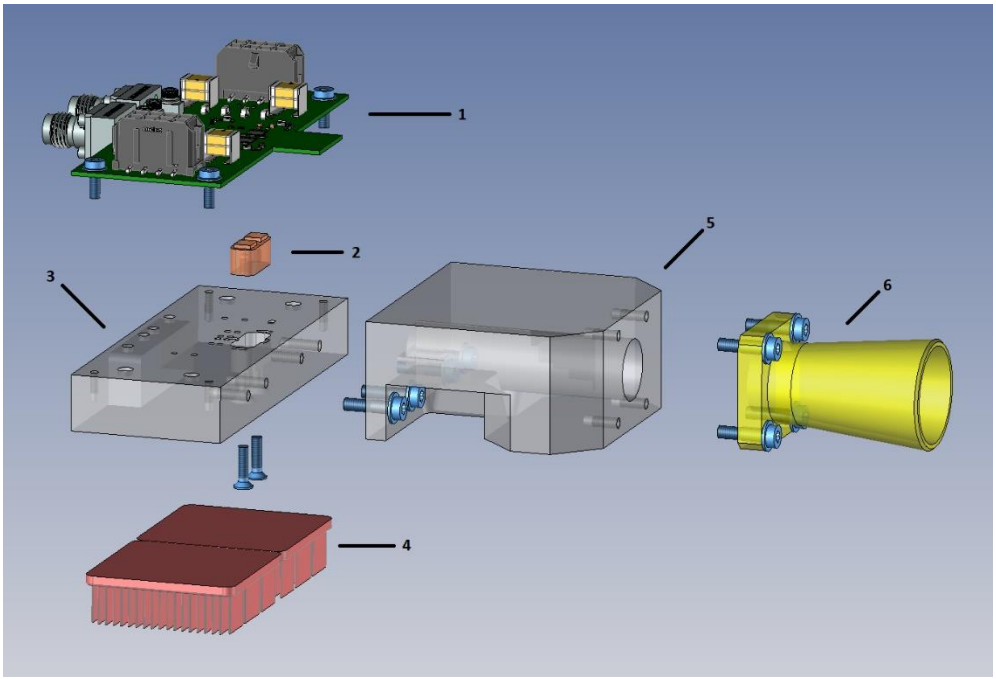


Figure 5-118 DRIFT Demonstrator Exploded View.

The assembly sequence is as follows: First, the HPA MMIC will be mounted on top of the MMIC Module (2) and which after will be integrated in the PCB Mounting structure (3). Then the Demonstrator PCB (1) shall be mounted atop of the PCB mounting structure (3). At this stage, the assembly has to be wirebonded from the MMIC to the PCB before continuing further assembly. Once the wire bonding process is complete, the Horn waveguide (6) can be bolted to the Waveguide Structure (5) and all together be bolted to the PCB Mounting Structure (3). The Heatsinks (6) will be attached to the PCB Mounting Structure using it's pre-applied glue layer and can be applied when all other parts are bolted.

5.7. DRIFT Test Plan

On-wafer small-signal screening of the HPA will be performed by UMS, directly after processing. UMS will only measure small-signal S-parameters at the default bias condition. As UMS cannot perform a true differential output measurement, a 2-port measurement will be performed for each output power with the other port loaded by 50ohm. These measurements will give an indication of the yield and process spreading over the wafer.

After wafer dicing the MMIC samples will be shipped to TNO. A selection of samples (3 to 5 pieces) will be soldered on CuMo carriers for more detailed S-parameter and large signal measurements. The testing will be carried out in the MMIC measurement facility of TNO, shown in Figure 5-119. The HPA MMIC-on-carrier will be measured on a wafer probe station with temperature controlled chuck. The following test equipment will be used:

- Controllable DC supplies
- Multimeters
- Keysight 4-port PNA-X (26.5 or 50 GHz model, depending on availability)
- Keysight spectrum analyzer
- LeCroy scope for monitoring (and correcting) current and voltage levels
- K-band RF Driver amplifier (R&S SAM100 2-20 GHz, 20W)
- K-band balun (TBD)

Figure 5-119 : MMIC test facility at TNO.

The measurement equipment will be controlled using Python scripts running on a Windows PC. The measurements sweeps will be automated and data will be collected in “hdf5” file format for later post-processing in Python or Matlab. For the measurement setup different configurations are possible and will be used:

- Small-signal 3-port measurement
- Large-signal 3-port measurement
- Large-signal 2-port measurement with external balun

For the small-signal measurements the standard measurement ports of the PNA-X can be used, as shown in Figure 5-120. The damage level for each port is 30 dBm, so care must be taken not to exceed this limit. Using the differential measurement option of the PNA-X the true differential output signal can be measured.

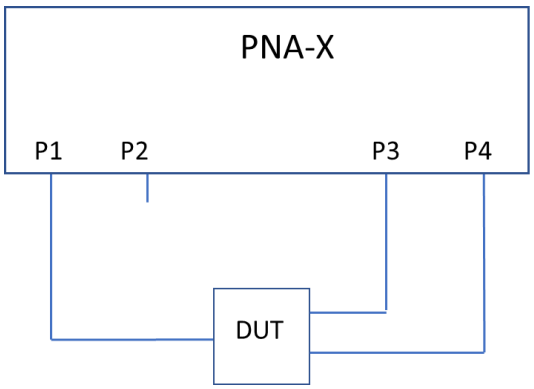


Figure 5-120 : Small-signal 3-port measurement setup, using the internal couplers in the PNA-X (limited to maximum 30 dBm output power per port).

For the large signal characterization external couplers are required. The setup will look as shown in Figure 5-121. To characterize the differential output signal at least 2 measurement sweeps are needed. Forward and reflected waves (amplitude and phase) will be measured for each port.

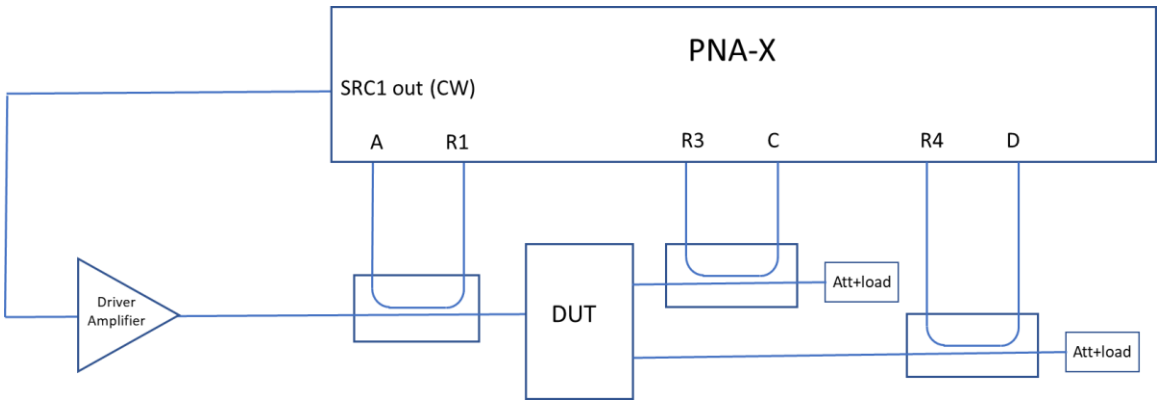


Figure 5-121 : Large-signal 3-port measurement setup.

Alternatively an external balun can be used at the output of the HPA and standard 2-port large-signal measurements can be performed. For characterizing the linearity of the differential output signal such a balun will be included. The setup will look similar to the one shown in Figure 5-122.

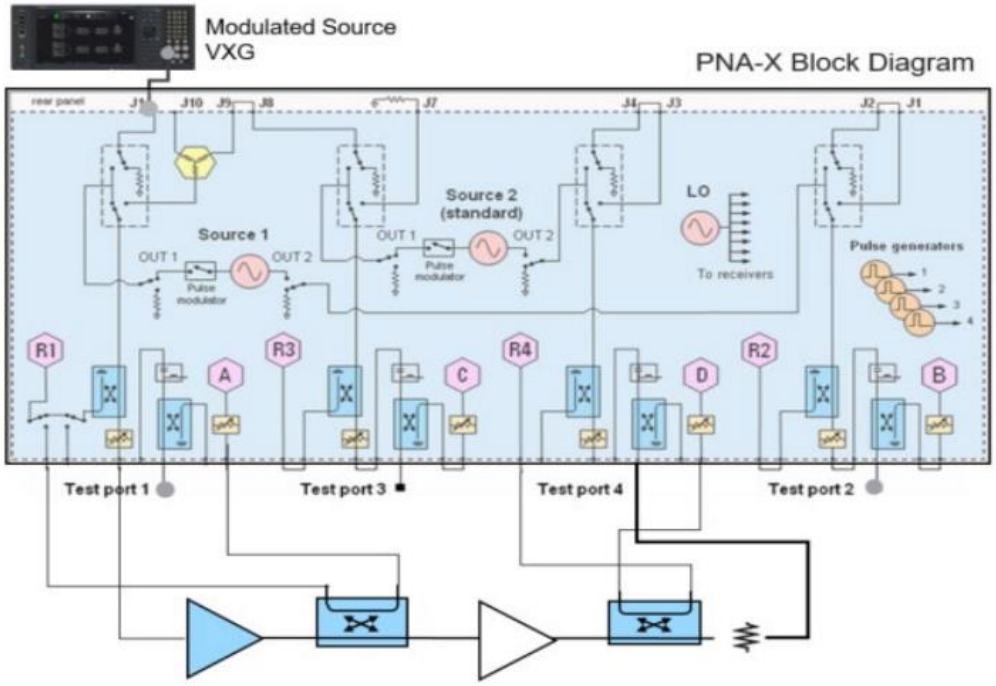


Figure 5-122 : Example of a measurement setup for non-linearity characterization.

For the 2-tone linearity measurement the 2nd source inside the PNA-X can be used to generate a 2-tone signal. For the NPR measurements shall be derived from the power sweep measurements using the IMAL tool.

5.7.1. Device under test

After the MMIC wafer processing, diced samples will be delivered to TNO. A few (3 to 5) samples will be mounted on CuMo metal carriers using AuSn or Silver Sintering die attached (TBD), for good thermal contact. The metal carrier will be placed on the temperature controlled chuck of the probe station.

The MMIC will be contacted using probes: a GSG and GSGSG at the RF in- and output (FormFactor Infinity probes), and a DC probe (GGB multi-contact wedge probe) at the north and south side. The DC probes will contain decoupling capacitors at the tip of the needles, to mimic the effect of die capacitors,

which will be used in the PCB assembly. Additional low-frequency decoupling will be implemented on a DC-probe card, connected to the DC probes.

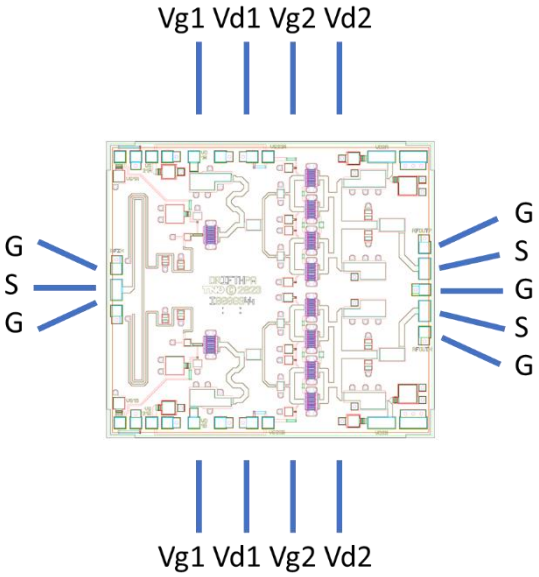


Figure 5-123 : On-chip probing.

5.7.2. Calibration

The reference plane for the measurements will be at the probe-tip. Therefore calibration structures will be measured on a dedicated calibration substrate (short, open, load and straight thru). The calibration will consist of a small-signal calibration followed by a power calibration.

Calibration will be performed over the full frequency range of the network analyzer (e.g. 1 – 26 GHz).

5.7.3. HPA Measurements

The following measurements are foreseen:

- DC verification
- Stability verification
- Small-signal S-parameters
- Large-signal measurements
- Linearity measurements

Goal of these measurements is to establish the compliancy of the realized MMIC to the specifications. The measurements are described in the following paragraphs.

DC and stability verification

The first test will consist of check the DC current consumption. The RF input is loaded with 50ohm and the RF output is connected to a spectrum analyzer. The control of the gate bias (pinch off capability) will be checked, starting at low drain bias. Next the quiescent drain current will be checked at the nominal operating point (Vd = 20 V) to know which gate bias voltage to use in the following measurements. The nominal drain current is 130 mA, correspond to 25 mA/mm current density. The stability will be checked by monitoring the RF output on the spectrum analyzer and monitoring the gate and drain current and voltage levels on an oscilloscope.

Small-signal S-parameters measurements

Small-signal S-parameters will be measured for the following conditions.

Table 5-20 : S-parameter measurement range.

Frequency range	1 – 26 GHz (or higher for the 50 GHz PNA-X) step 0.1 GHz
Mode	CW
Tchuck	20°C and 80°C
Vd	15 – 25 V, step 1 V
Vg	Nominal Vg and +/- 0.1 V +/-0.2 V

Large-signal measurements

Large-signal measurements will be performed for the following conditions.

Table 5-21 : Large-signal measurement range.

Frequency range	16.3 – 21.2 GHz, step 0.1 GHz
Mode	CW
Tchuck	20°C and 80°C
Vd	18, 20 and 22 V
Vg	Nominal Vg and +/- 0.1 V +/-0.2 V
Source power	-20 dBm and 10-25 dBm, 1 dB step

Linearity measurements

NPR calculations will be derived from the large signal power sweep measurements via the use of the IMAL tool.

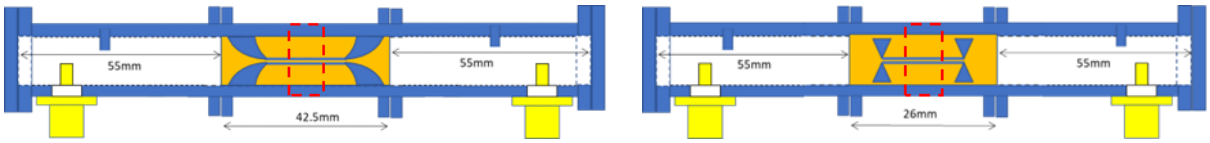
5.8. Waveguide feed test plan

The passive radiating module contains the following parts:

- Semi-circular wave guide
- Semi-circular wave guide exciter PCB
- Polarising septum in a circular wave guide
- Circular wave guide
- Radiating horn section (COTS).

5.8.1. Waveguide Feed Testing

A back-to-back test waveguide feed test has been chosen the setup is depicted in Figure 5-124.



(a) (b)

Figure 5-124: Alternative test for measuring the losses of the exciter options. The red dashed box in the centre indicates the piece of parallel line where it is outside the wave guide and connects to free space.

A consequence of the altered test philosophy is the need for a separate set of calibration standards. An overview of waveguide based TRL calibration standards is presented in Figure 5-125

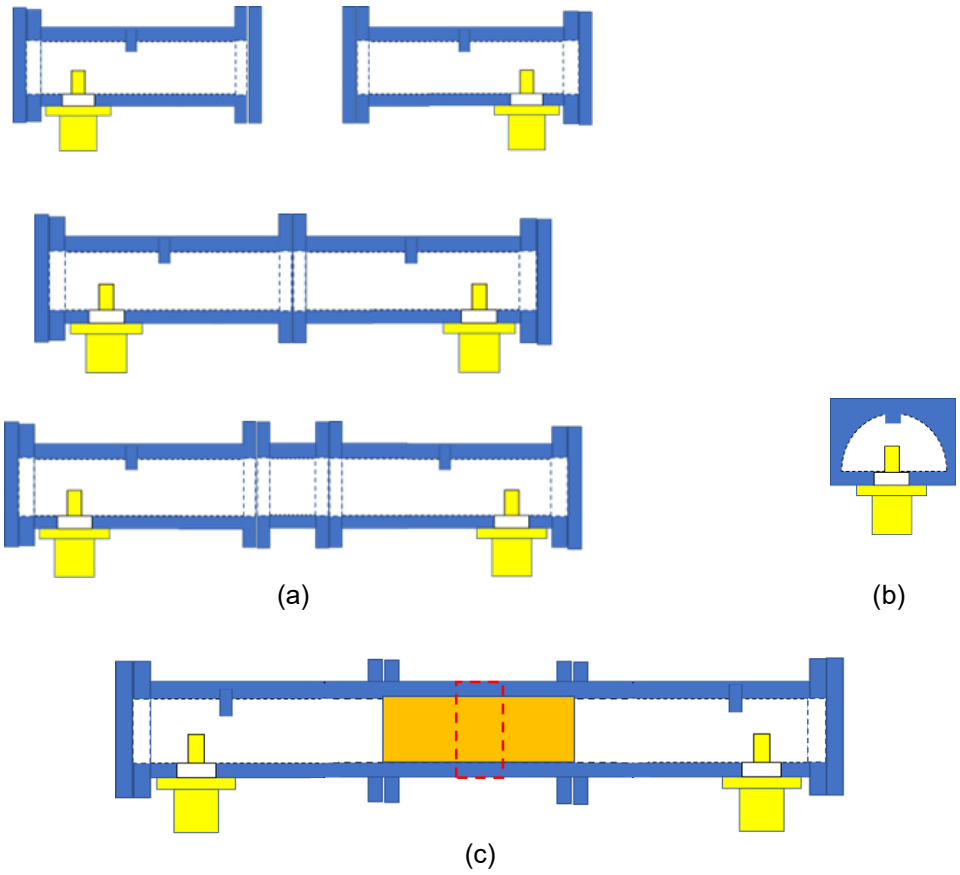


Figure 5-125: (a) Calibration standards based on semi-circular wave guides, from top to bottom: reflect, through and line. (b) Frontal view of the semi-circular wave guide including a tuning stub. (c) Anticipated test setup with the coax-to-semi-circular wave guide transitions in place and the test structure in between. The orange part represents a PCB and the red dashed box indicates the position in the centre where the parallel line is connected to free space.

The coax-to-semi-circular wave guide adapter is a component designed specifically for this test, a CAD-model impression is shown in Figure 5-126.

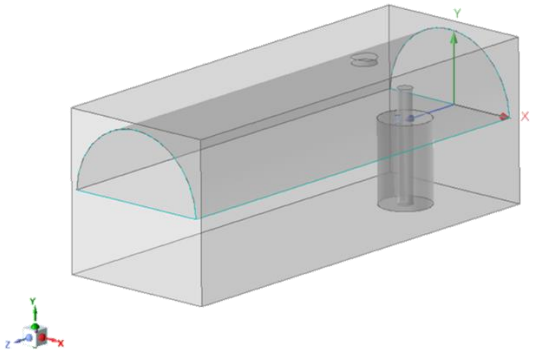


Figure 5-126: CAD-model of the transition from coaxial cable to the semi-circular wave guide.

Several adapter lengths have been manufactured to be able to determine the loss of the empty wave guide. For the exciter PCBs two types have been manufactured, with the only difference being the line length in order to determine the loss of the parallel line. The guided wave lengths of the different transmission lines are indicated in Table 5-22.

Table 5-22: Guided wave lengths of the different transmission lines

	$17.3\ GHz$	$18.9\ GHz$	$20.5\ GHz$
WG	$\lambda_g = 34$ [mm]	$\lambda_g = 25.3$ [mm]	$\lambda_g = 21.2$ [mm]
$PCB\ diff.m.$	$\lambda_g = 11.4$ [mm]	$\lambda_g = 10.3$ [mm]	$\lambda_g = 9.6$ [mm]

Based on averaged values of these the manufactured lengths are based, i.e.:

- Extra parallel line length: 10mm
- Quarter wave length piece (2x) for the calibration standards: 6.7mm
- Extra empty semi-circular wave guide length: 25mm, and 40mm.

Table 5-23: Adapter lengths

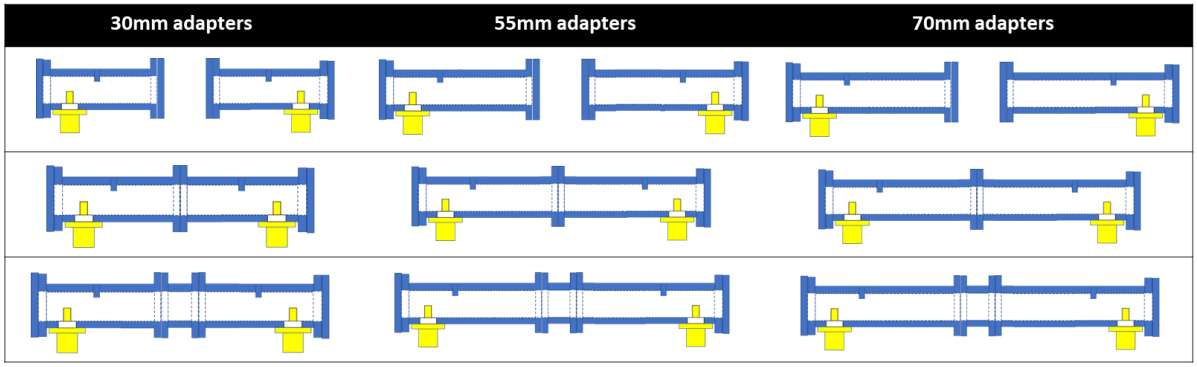
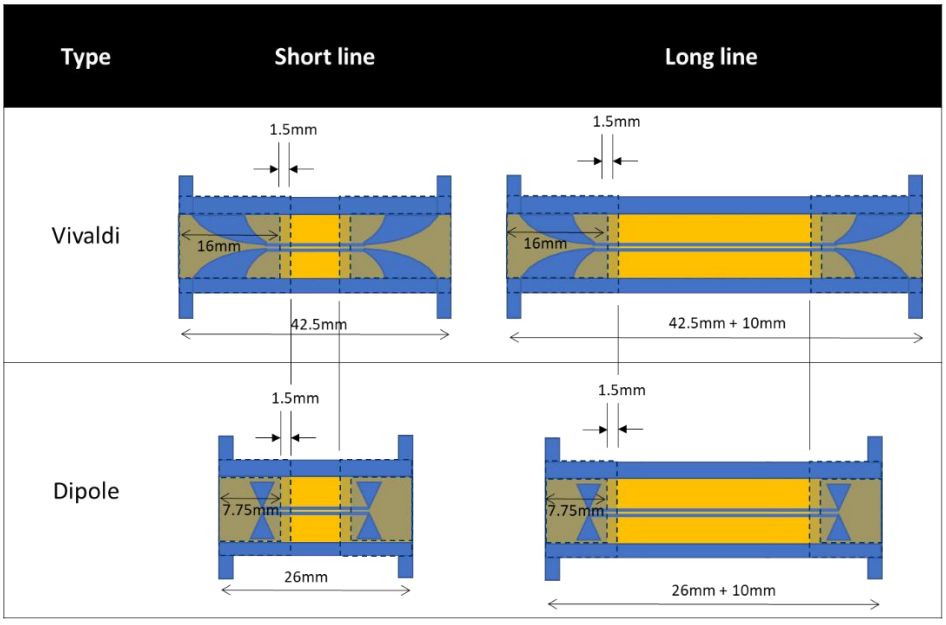
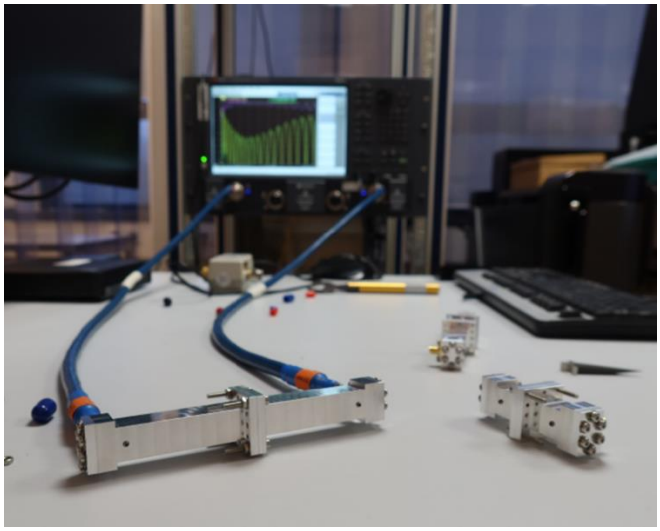
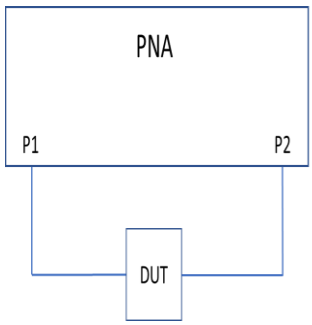


Table 5-24: Parallel line length difference implemented on PCB for both exciter types. The indicated 1.5mm represents the thickness of the back wall of the wave guide



In Figure 5-127 the related test setup, using the same equipment as mentioned in the previous paragraph, is shown.





(a) (b)

Figure 5-127: Scattering parameter test setup as implemented for the 2nd iteration of the waveguide exciter characterisation. (b) Utilising a 2-port network analyser.

The following test equipment will be used:

- Keysight 4-port PNA-X (26.5 or 50 GHz model, depending on availability)

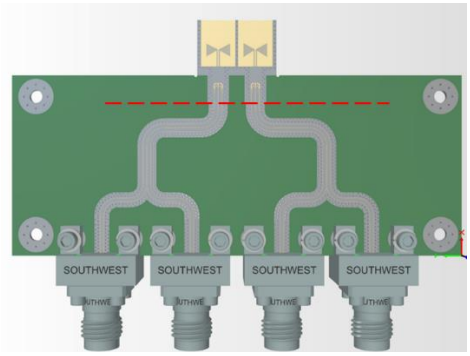
The calibration standards are a through, reflect and line. These are shown in Figure 5-125a and Table 5-23.

5.8.2. Passive antenna demonstrator test plan

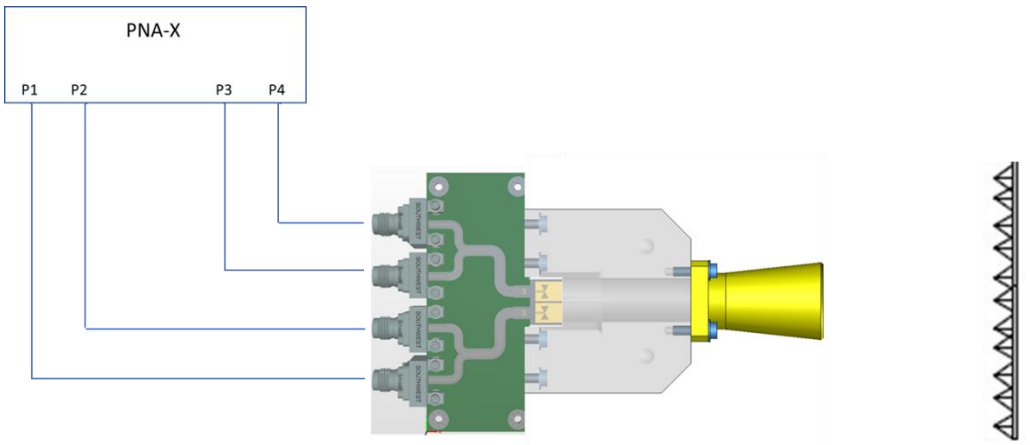
With the availability of a horn antenna the radiating front-end module can be completed and manufactured. Described in this paragraph are test related to the passive demonstrator and thus excludes the HPA and its peripheral components. Each of the exciters can be directly driven or terminated in a 50 Ohm load. Since the 4-port PNA-X can be set up to drive two of its ports in differential mode it is the preferred option to pursue over e.g. K-band baluns.

The goal is to measure the scattering parameters. To perform this test the availability of a dedicated PCB is required. It will be of the same size of the active panel and can be mounted on a support structure similar to that of the active panel. As both exciters must be directly accessible to the PNA-X the board design will be quite different. Indeed, both parallel lines must be split up into their basic two single-ended coplanar wave guides and connected to a Southwest connector. The panel to support such a measurement is sketched in Figure 5-128a and the test setup in Figure 5-128b.

Also the definition of calibration standards is required in order to extract the performance of the test object at the reference frame.



(a)



(b)

Figure 5-128: (a) Example of the routing for the passive demonstrator test. It will involve 4 Southwest connectors. The dashed red line represents the reference plane. (b) Test setup to measure the scattering parameters of the passive demonstrator.

Besides the scattering parameters, the radiation performance is also of interest. While driving one single exciter at the time, the polarization performance across the band (AR or XPD) can be measured. These tests are planned in the near-field test facility of TNO and it requires strategic placement of some absorber tiles prior to test. Note that this test does not involve any probing of the field other than at one single orientation, i.e. broadside maximum, see Figure 5-129 for the anticipated setup. This test has the sole purpose to investigate the reflection experienced at the differential input of each exciter, the cross-talk between them, and the polarization performance across the band.

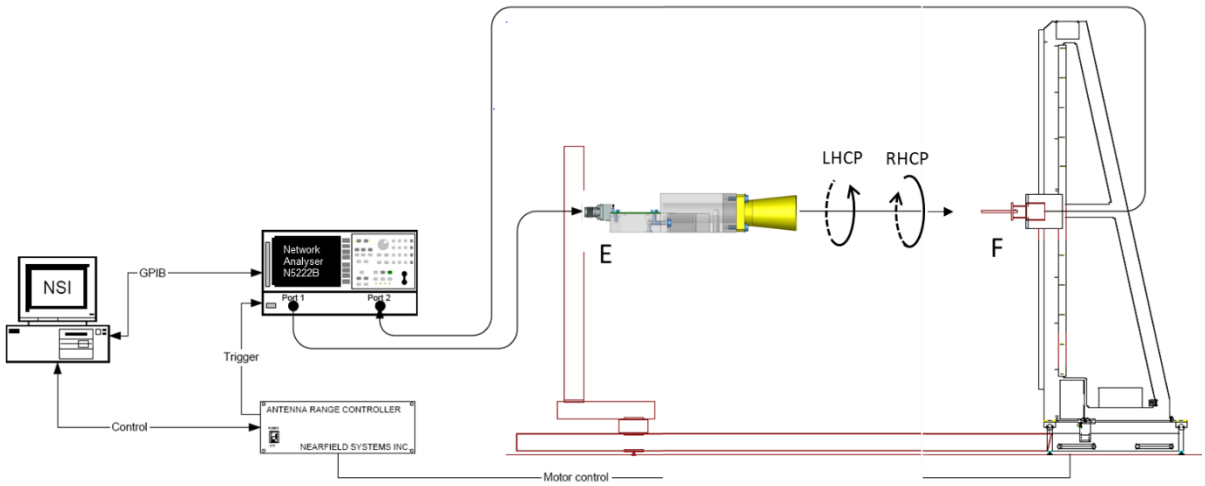


Figure 5-129 : Schematic of the polarisation test. Two lines run from the PNA-X to the receiving horn, however it is TBD whether a single or dual polarised horn will be used.

Axial ratio will be derived from measuring the received signal in two orthogonal planes. These planes have to coincide with the principal planes of the demonstrator. One plane lines up with the orientation of the polarising septum, and the other with the orientation of the exciter PCBs. During the measurements the polarisation of the receiving horn needs to be aligned accordingly. This horn can be linearly or dual-linearly polarised. In case of the former two measurements are required to extract the wanted information, in case of the latter the information can be extracted in a single measurement (using the 4-port PNA-X). For this particular demonstrator the principal planes are chosen such that one lines up with the earth-horizontal and the other the earth-vertical.

If the different input ports are labelled A, B, C, and D as shown in Figure 5-130, the following table can be defined for generating the different polarisation senses:

Table 5-25: Indication of the input settings to generate circular polarised radiation

Pol. sense	A	B	C	D
LHCP	0°	180°	50Ω	50Ω
RHCP	50Ω	50Ω	0°	180°

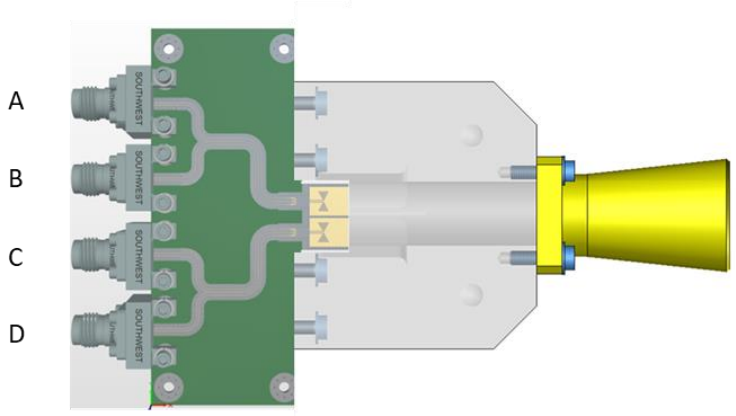


Figure 5-130: Labelling the input ports of the passive demonstrator.

For generating subsequently LHCP and RHCP: the active ports A and B, or C and D, will be connected to a K-band balun as indicated in Figure 5-131. The input of this balun will be labelled E (see Figure 5-129).

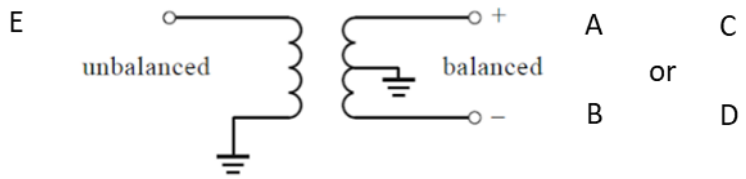


Figure 5-131: Balun outputs connected to either the input port combination A and B, or C and D, for generating the polarisation senses.

To determine the gain of the passive radiating front-end module the latter must be replaced by a standard gain horn (SGH) in the schematic measurement chain shown in Figure 5-129. Subsequently the exact same measurements needs to be repeated. As the gain of the SGH is known as a function of the frequency, the gain of the passive radiating front-end module can then readily be derived.

6. DRIFT Test Results

6.1. Test Readiness Review (TRR)

6.1.1. HPA Test Results

After the MMIC wafer processing, diced and sorted samples have been delivered to TNO. Four MMICs have been mounted on a CuMo carrier using Silver sintering for good thermal contact. A picture of an MMIC, mounted on the CuMo carrier, can be seen in Figure 6-2. The metal carrier is placed on the temperature controlled chuck of the probe station.

On the probe card a gate series and shunt resistor has been applied for both Vg1 and Vg2, which have been connected to a single power supply. The drain bias is decoupled with a feed-through capacitor of 100nF and for amplifier stage 1 and stage 2 separate power supply outputs have been used, as shown in Figure 6-1 .

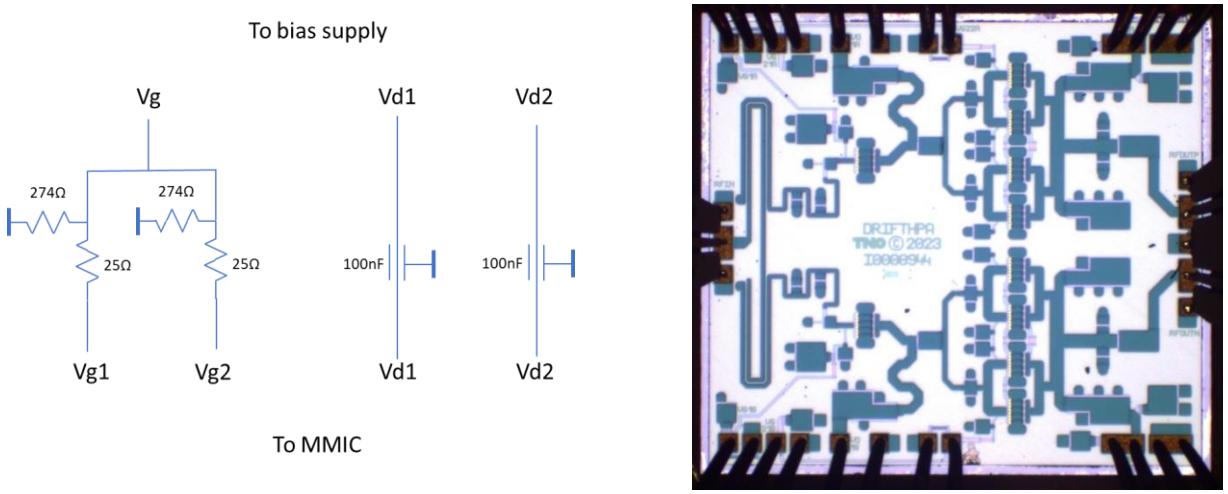


Figure 6-1 Decoupling on the DC probe card and Drift HPA on-wafer measurement

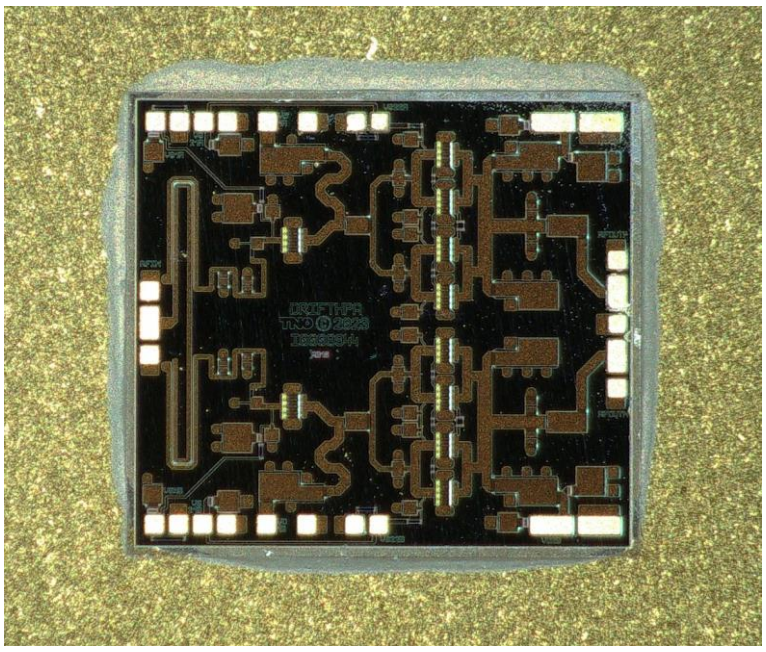


Figure 6-2 : MMIC mounted with silver sintering on CuMo carrier.

6.1.2. Calibration

The reference plane for the 3-port measurements is at the probe-tip. Therefore calibration structures have been measured on a dedicated calibration substrate (short, open, load and straight thru). The calibration consists of a small-signal calibration, optionally followed by a power calibration. Calibration has been performed over the full frequency range of the network analyser (e.g. 1 – 50 GHz).

6.1.3. Small-signal

The reference plane for this calibration is at the probe tip. A standard PNA-X smart cal is performed using a CSR-8 calibration substrate (SOLT), using the following settings:

- 1 – 50 GHz, 500pt
- IF 100Hz
- -10dBm all ports
- No receiver attenuation

3-Port large-signal

A similar calibration is performed as for the small signal case, but now also including a source power calibration. A standard PNA-X smart cal is performed using a CSR-8 calibration substrate (SOLT), using the following settings:

- 1 – 44 GHz, 100MHz step, 431pt
- IF 50Hz
- 0 dBm all ports
- No receiver attenuation
- Power cal at -10 dBm, using adapter removal with 2.4mm SOL

The performance after calibration looks reasonable, with less than 0.1 dB error and matching better than 40 dB, as shown by Figure 6-3.

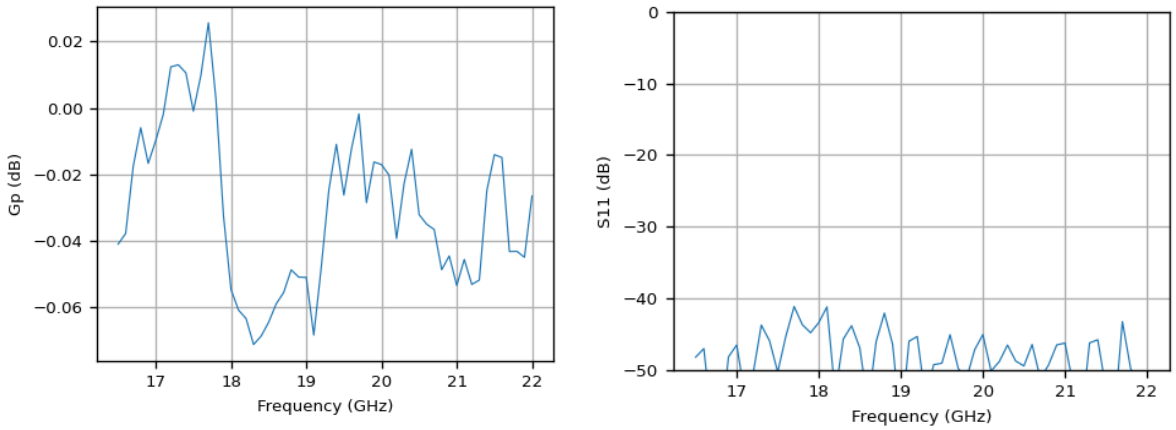


Figure 6-3 : Measured power gain and S11 of the THRU port 1 -> 2, without driver amp at -10dBm source power, directly after calibration, using the "match corrected" method.

This performance is only achievable when the DUT is measured in the same environment as has been used for the calibration, i.e. same load and source impedance. When performing large signal measurements, the calibration method of the PNA-X has to change to "actual waves" to account for mismatch at the source and load side. This however has an impact on the measurement accuracy. The error on the gain has now increased to 0.16 dB and the matching is reduced to 16 dB. This will limit the accuracy of the large signal measurements, as shown by Figure 6-4.

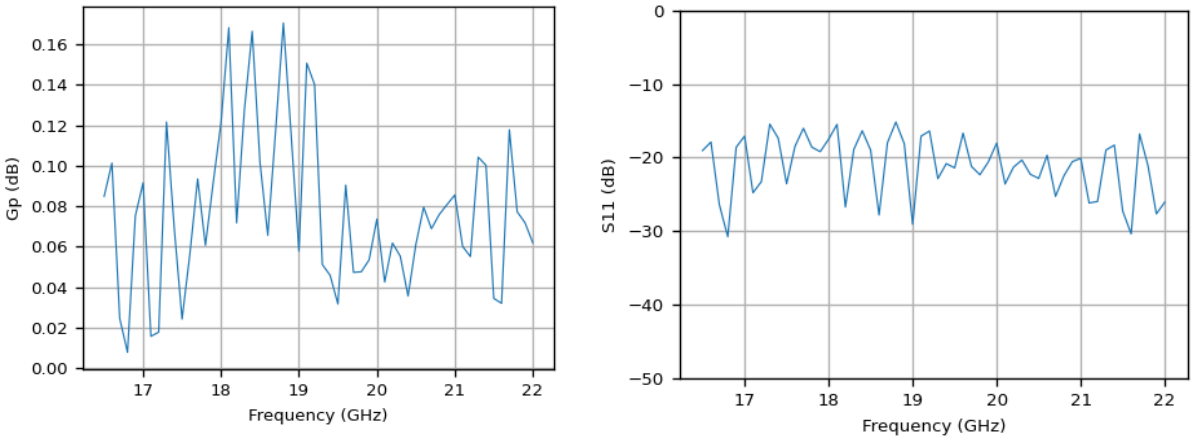


Figure 6-4 : Measured power gain and S11 of the THRU port 1 -> 2, without driver amp at -10dBm source power, directly after calibration, using the "actual waves" method.

When including the driver amplifier the accuracy is still similar, as shown in Figure 6-5.

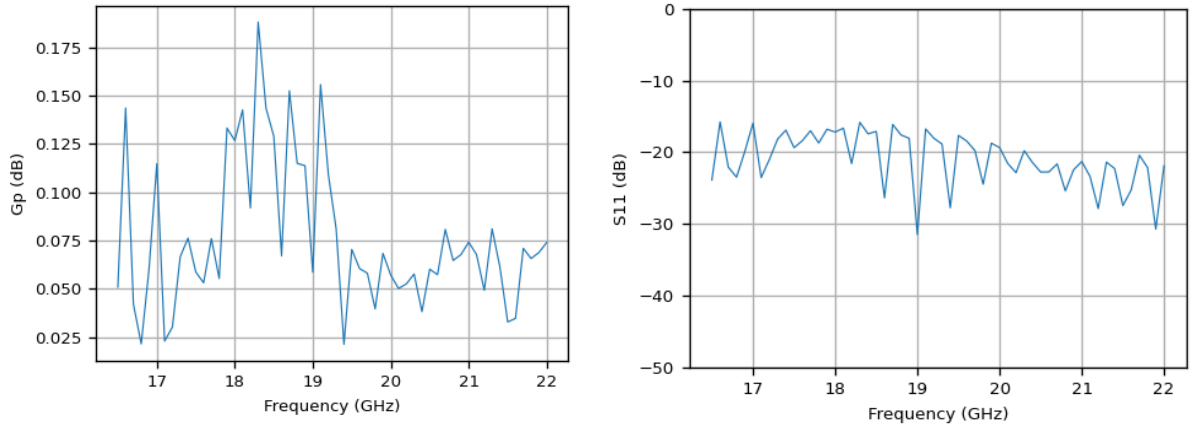


Figure 6-5 : Measured power gain and S11 of the THRU port 1 -> 2, with driver amp at 0dBm source power, directly after calibration, using the "actual waves" method.

6.1.4. Small Signal UMS on-wafer screening

UMS has performed small-signal on-wafer S-parameters for screening and sorting purposes. The S-parameters have been measured as 2-port in 2 separate measurements, one for each output port while the other output port is terminated in 50ohm. The measurements have been performed at the nominal bias point of 20V drain bias and -3.1V gate bias. In total 33 samples have been measured. Figure 6-6 shows the measurement data on all samples. Eight samples are clearly non-functional. Figure 6-7 shows a detail of the measurement data for the functional samples with 2 additional outliers removed.

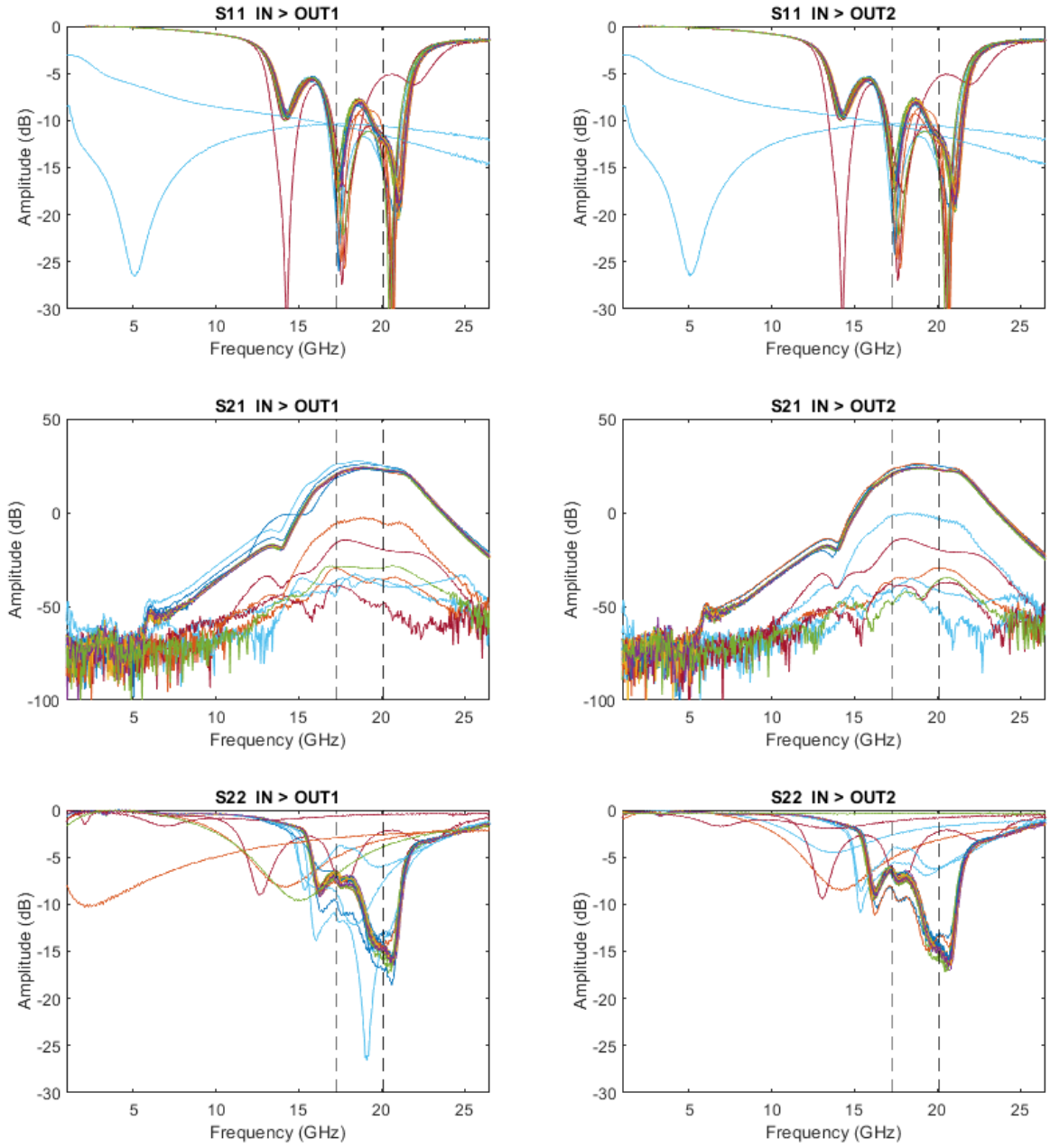


Figure 6-6On-wafer S-parameter measurement data for all samples on the wafer.

After removal of the non-functional and outlier samples the remaining samples show a very uniform behaviour. It can already be observed that the operating frequency range has shifted a bit upwards. Based on this screening data the diced functional and non-functional samples have been delivered to TNO.

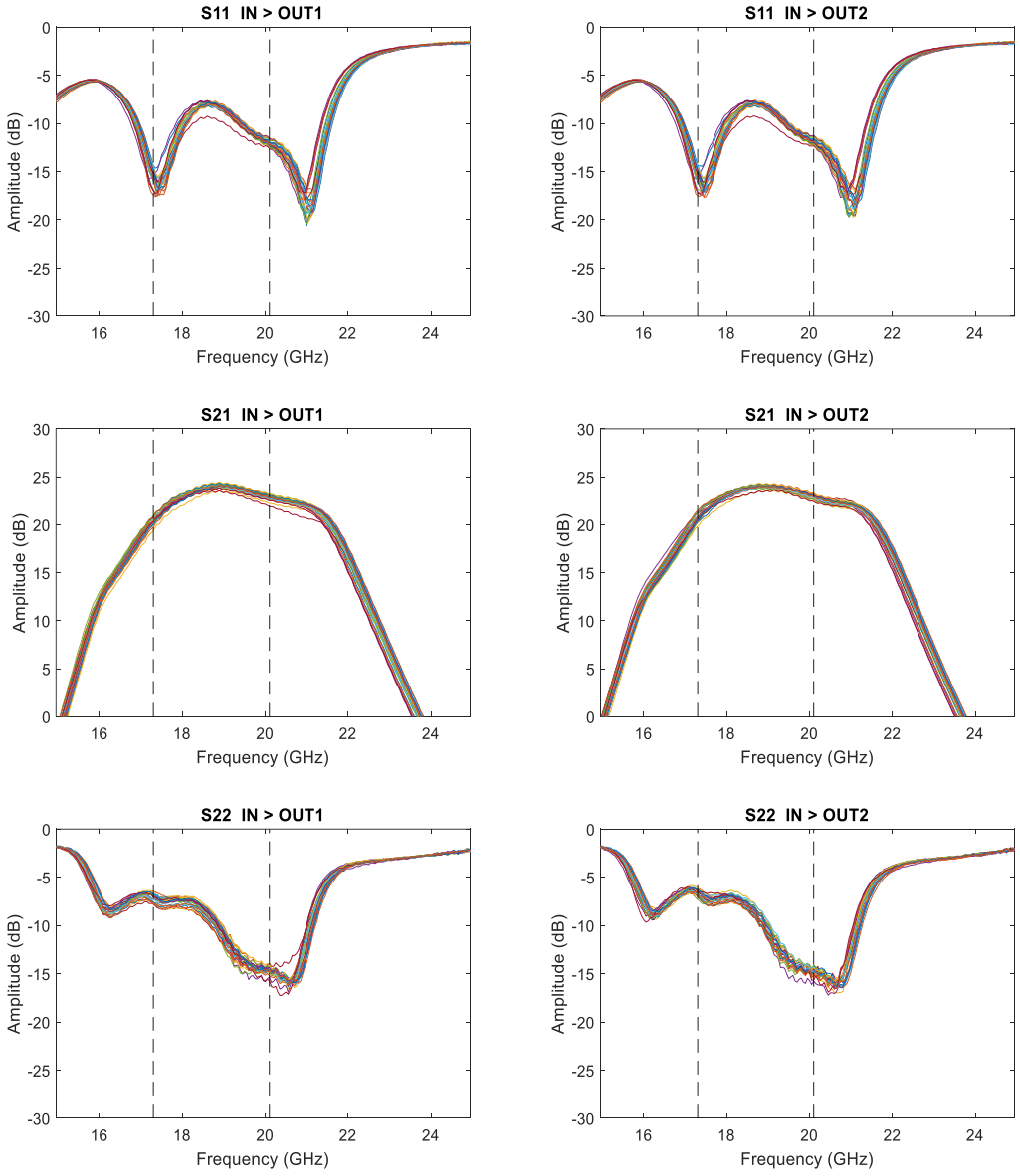


Figure 6-7 : On-wafer S-parameter measurement data for the functional samples on the wafer with 2 additional outliers removed.

6.1.5. TNO on-carrier measurements

The measurement results for the 3 mounted samples at the nominal bias conditions are shown in Figure 6-8. One sample (R1C1-red) is deviating, the other 2 samples (R2C1-blue and R2C2-pink) show very similar responses. Note that the spike in S11 around 14.5 GHz is caused by a small calibration issue. The 3-port measurement setup is described in section **Error! Reference source not found.**. Please note in Figure 6-8 the y-axis labels: dB(4,4) corresponds to the HPA input return loss, dB(5,4) & dB(6,4) to the SS gain of each differential arm and dB(5,5) & dB(6,6) to the HPA output return loss of each differential arm.

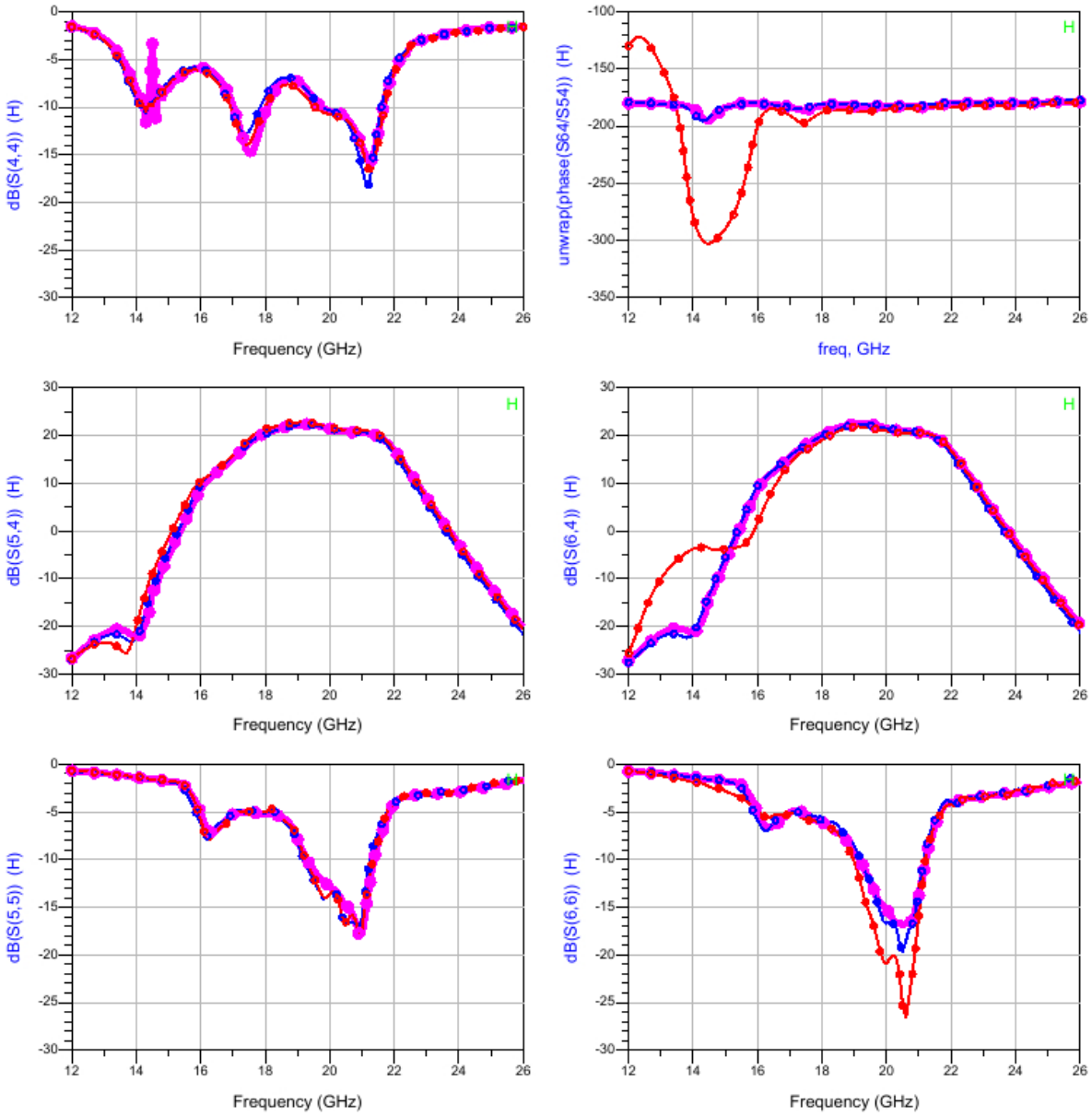


Figure 6-8 : S-parameter measurements of the 3 mounted samples at Vd=20V, Id~140mA, Ta=25degC.

Figure 6-9 shows a comparison between the measured and simulated S-parameters. In general the measurements show good agreement with simulation. The most notable differences are: the measurements show an upward frequency shift of about 0.5 GHz and input return loss has a spike response in the middle of the band compared to the simulation. The SS gain result of each differential

arm is higher than simulated, which is > 20dB and meets specification. The plot (Figure 6-9) in the top right corner shows the phase difference between the 2 RF outputs, which is very close to 180 degree.

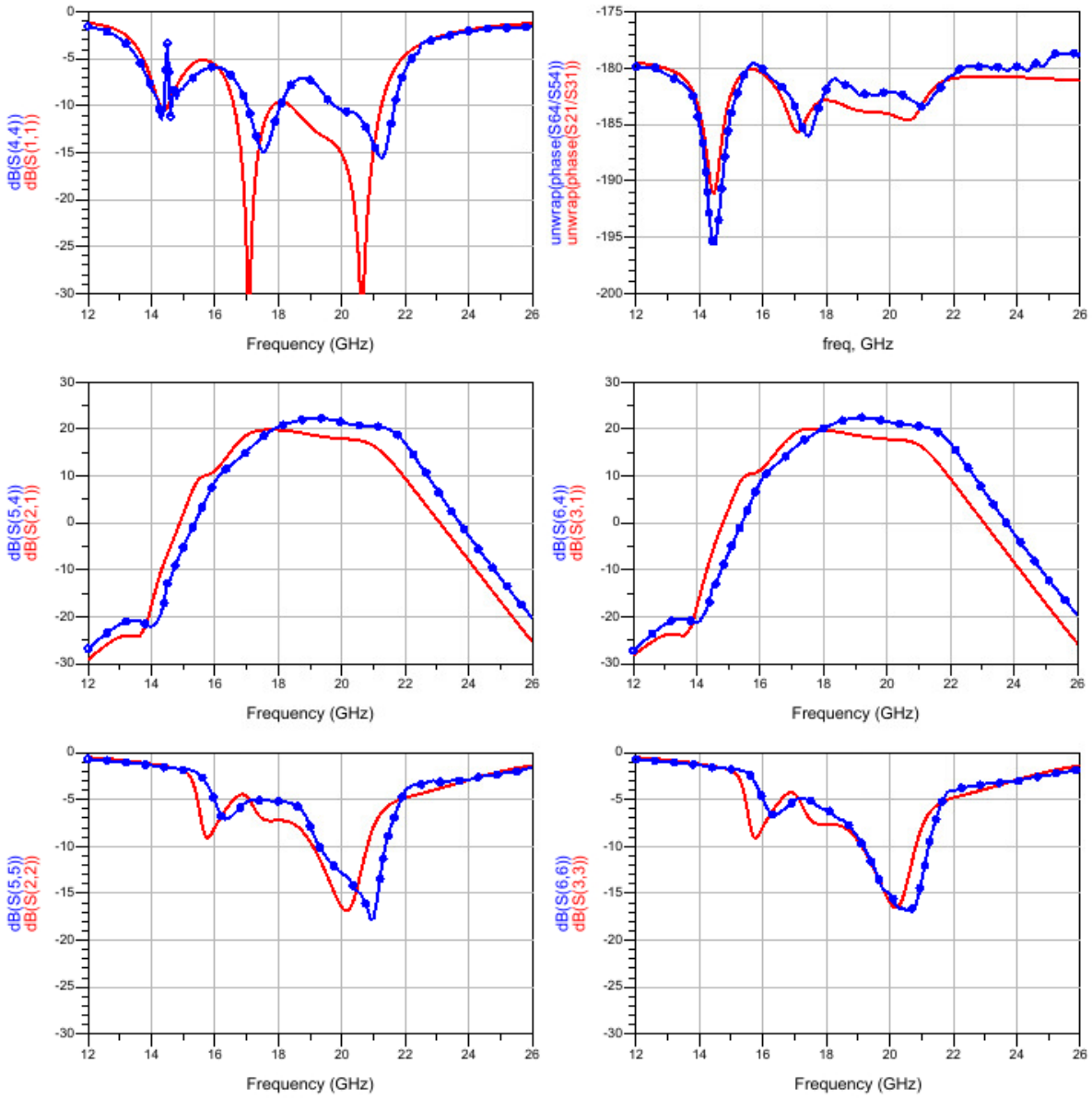


Figure 6-9 : Comparison of simulation (red) and measurement (dotted blue, sample R2C2) at Vd=20V, Idq~140mA, Ta=25degC.

The impact of +/-0.1V gate bias variation on the measured S-parameters is shown in Figure 6-10. For more positive gate bias the gain increases by approximately 0.5dB and the small-signal output matching improves. A more positive gate bias (higher quiescent drain current) also helps to improve the gain at the low side of the operational bandwidth.

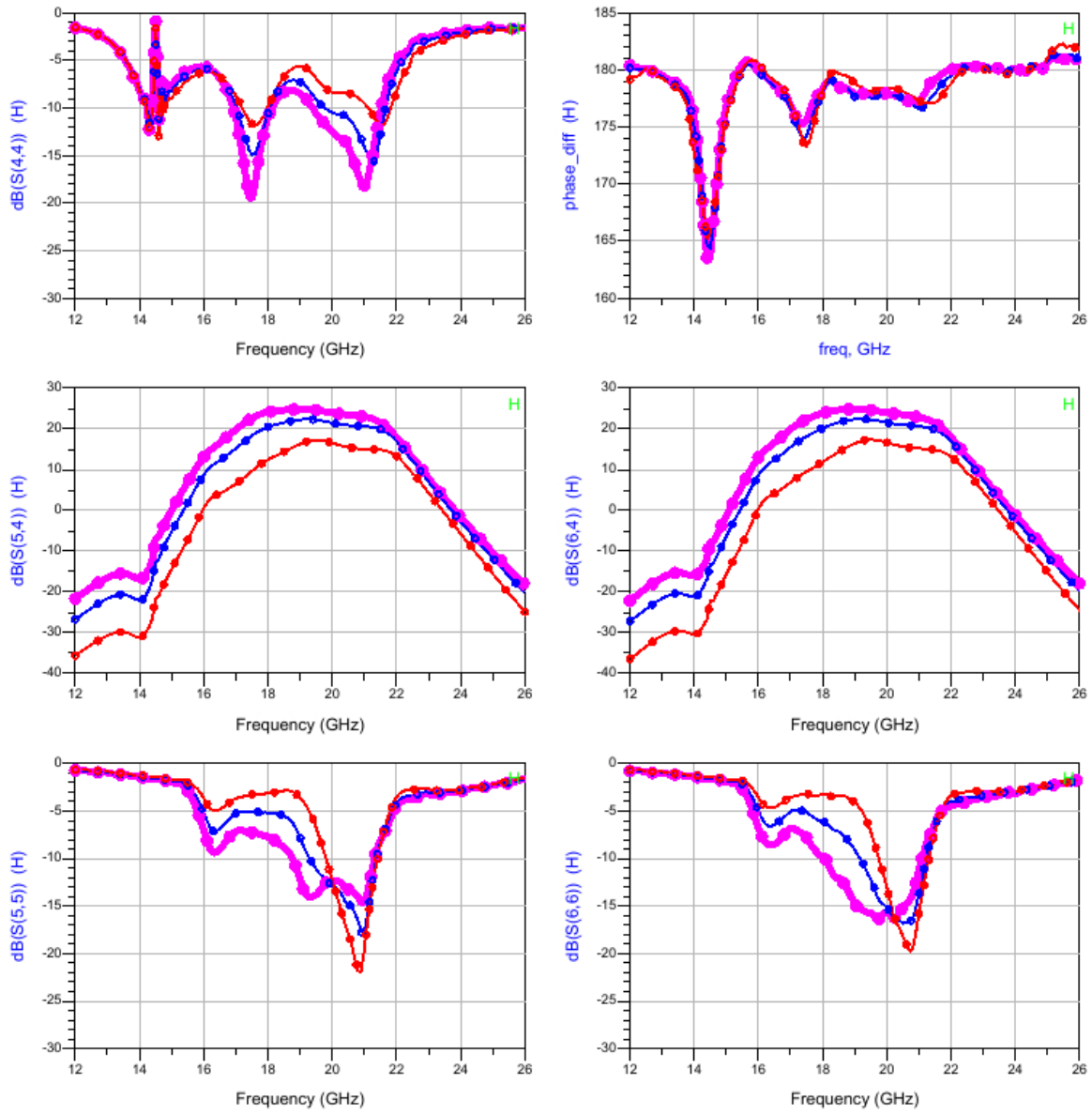


Figure 6-10 S-parameter measurements on sample R2C2 at Vd=20V and the nominal gate bias and +/-0.1V gate voltage variation, Ta=25degC.

The impact of temperature on the measured S-parameters is shown in Figure 6-11. The gate bias is kept at a constant voltage corresponding to the nominal bias condition at room temperature. As shown by the measured temperature results there is ±0.5 dB variation in gain.

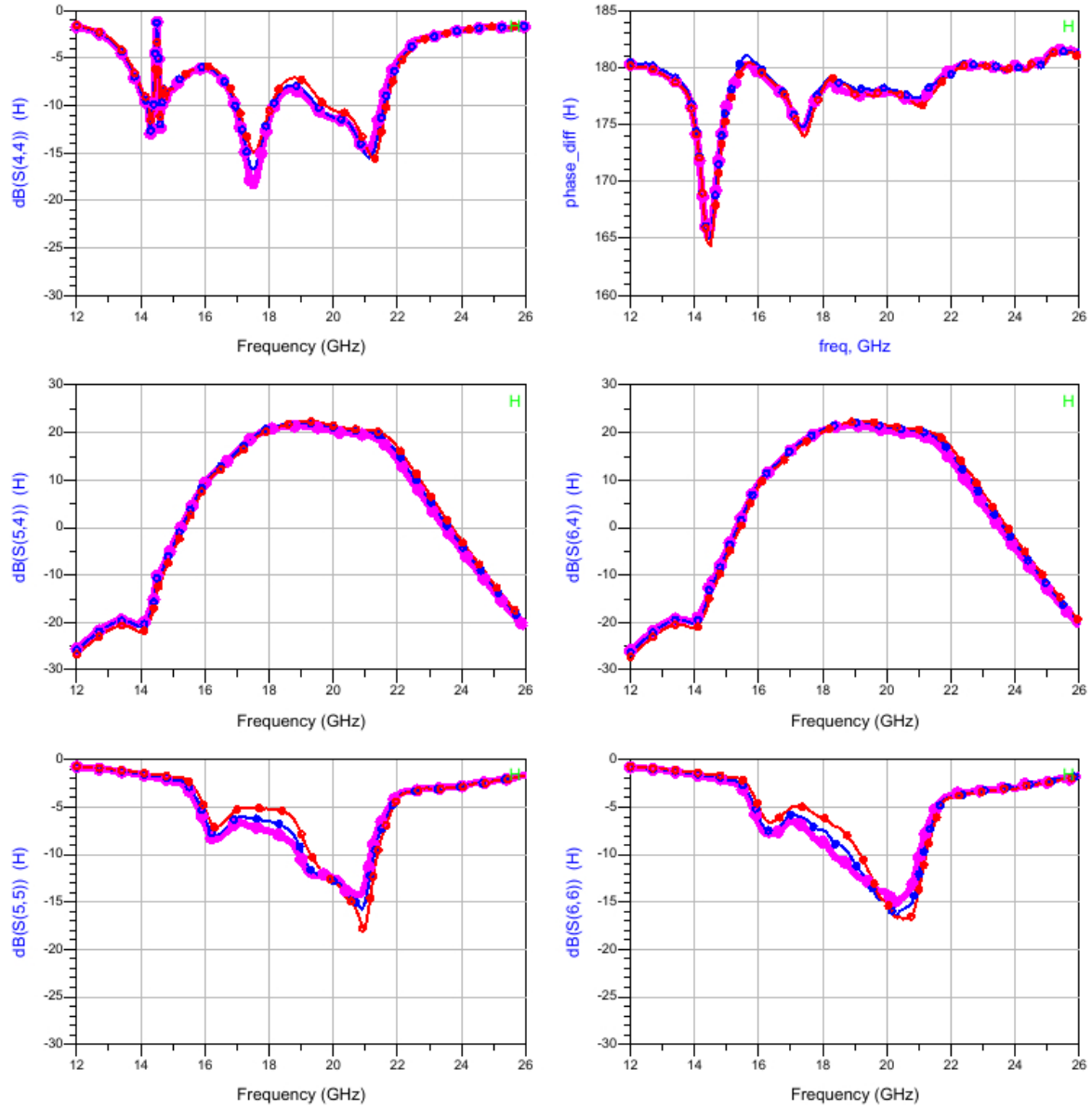


Figure 6-11 S-parameter measurements on sample R2C2 at Vd=20V, Vg=-3.23V for Ta=25degC (red), 50degC (blue) and 75degC (magenta).

6.1.6. Large signal MMIC measurement results

3-port large signal measurements have been performed and the complex output wave from both HPA outputs has been recorded. The combined performance of the differential output has been calculated by vectorial combination of both individual output signals. The results of a CW power-frequency sweep measurement, using a frequency step of 0.5 GHz, under nominal bias conditions is shown in Figure 6-12.

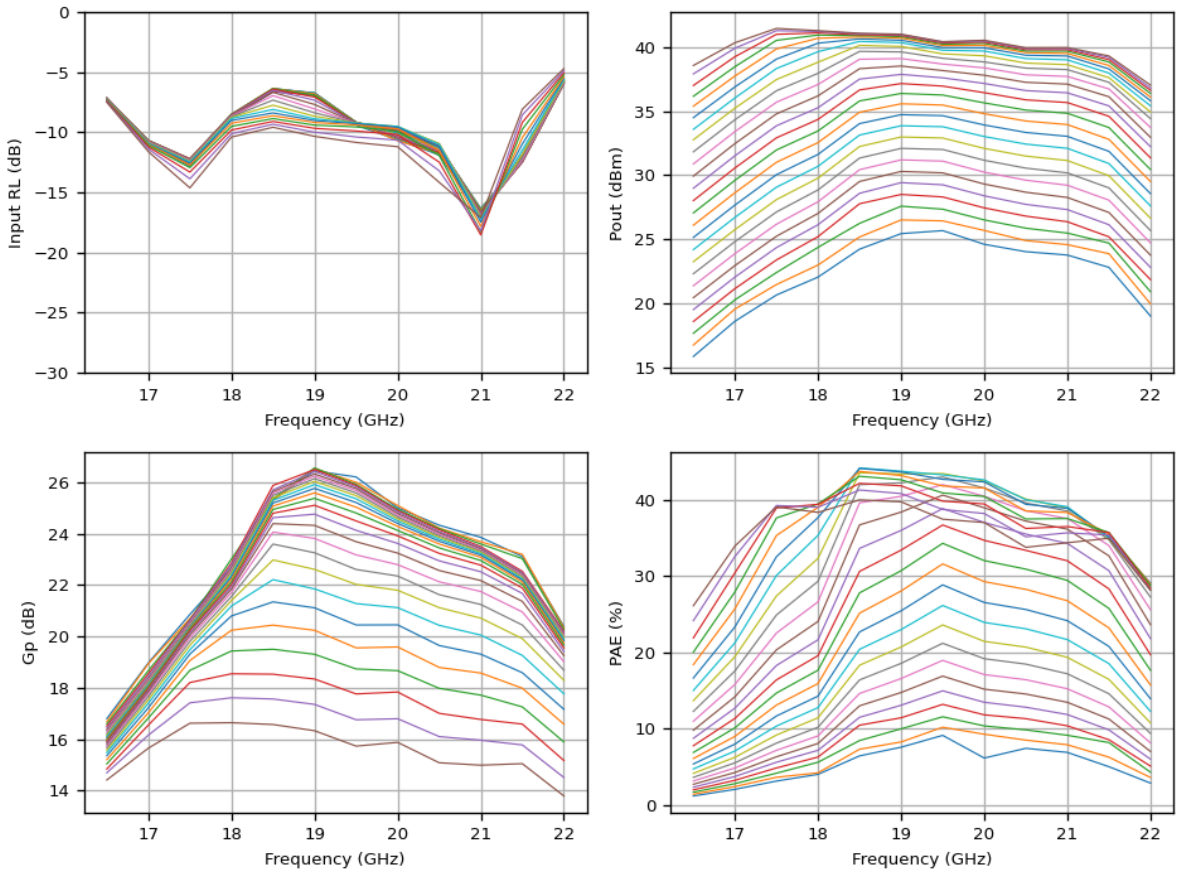


Figure 6-12 Measured CW power-frequency sweep for a source power of 0-25 dBm (1dB step), at the nominal gate bias at 20V, 25degC, sample R2C1.

At the low side of the frequency band the gain is lower than expected and the targeted PAE level is not achieved. The saturated output power is higher than 40 dBm from 17-21 GHz.

Figure 6-13 shows a power sweep for the two individual HPA outputs at 19 GHz. The gain for the two paths is slightly different because the non-perfect power splitting in the input balun and the output power of the two paths is also slightly different, mainly because of the not-perfect loading of each output in the on-wafer measurement setup.

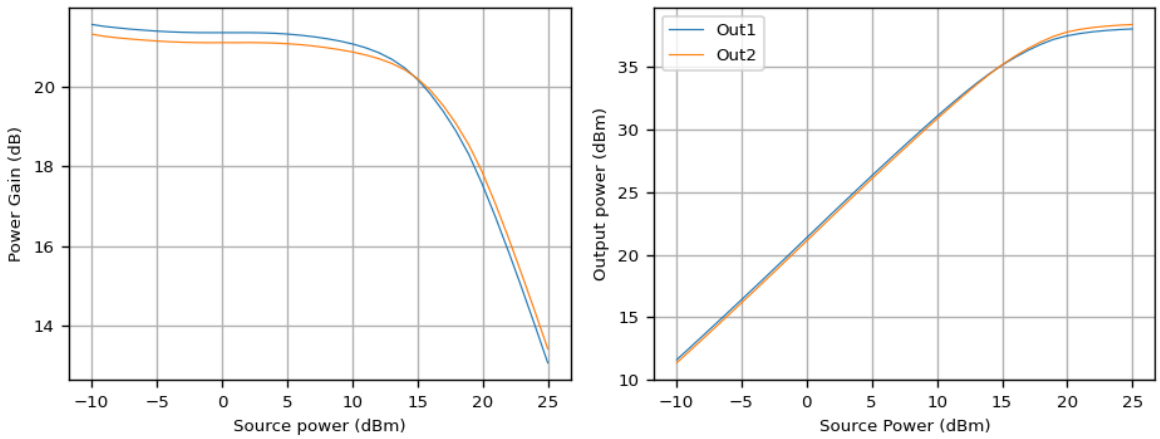


Figure 6-13 : Measured CW power sweep at 19 GHz showing the power gain and output for the two individual outputs, at the nominal gate bias at 20V, 25degC, sample R2C1

Frequency sweeps have been performed at 20dBm source power for the nominal gate bias voltage (-3.15V corresponding to 140mA drain current) and +/-0.1V and +/-0.2V. As shown in Figure 6-14. the gain and output power at the low side of the band can be improved by using a higher quiescent current density, but this will lower the PAE above 19 GHz. This measurement, and the following measurements, have been performed using a frequency step of 10 MHz. Due to this smaller frequency step the ripple on the measured data is more clearly visible. This ripple was already seen after calibration on measurements of a THRU test structure, see for example Figure 6-4, and is caused by the actual loading of the HPA by the measurement setup, which is not exactly 50 Ohm.

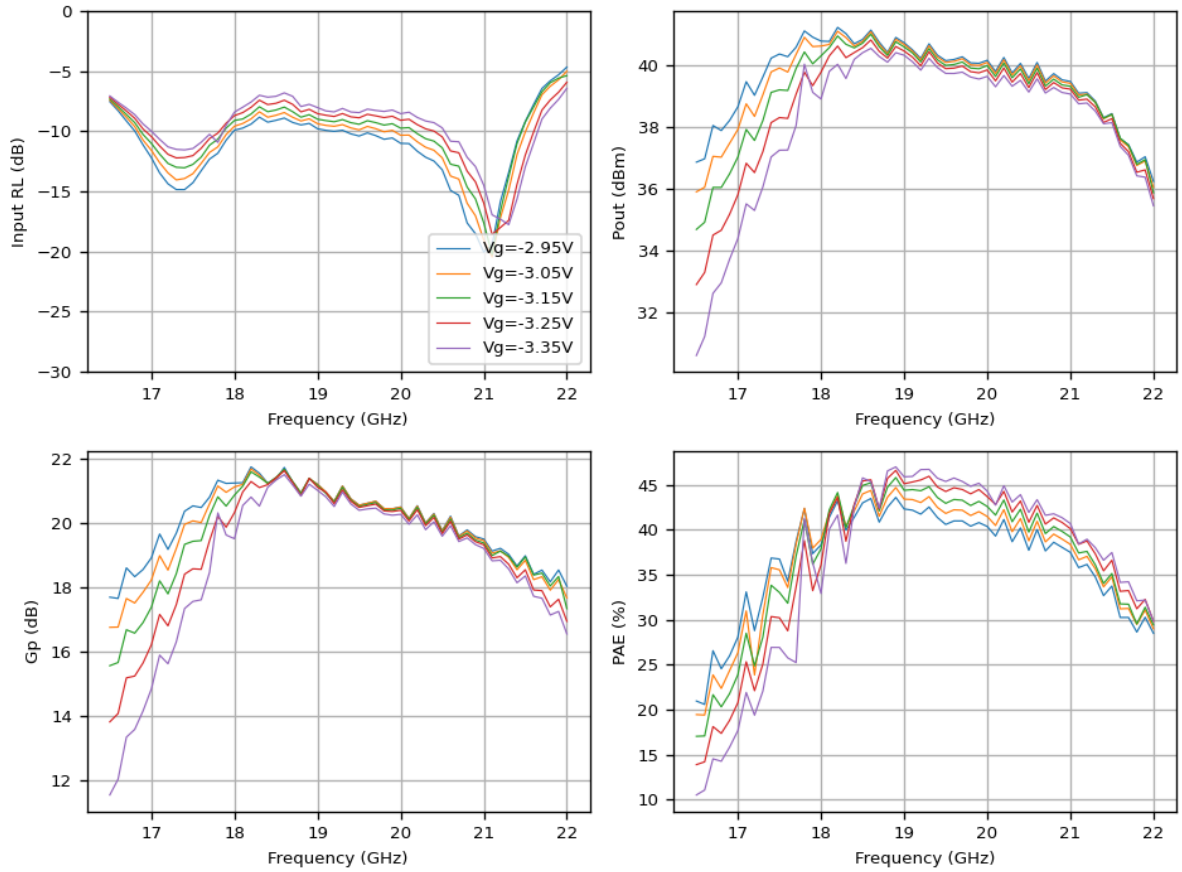


Figure 6-14 : Measured frequency sweep for a source power of 20 dBm, versus gate bias voltage at 20V, 25degC, sample R2C1.

A similar experiment has been done, but now for a drain bias sweep from 18-22V, see Figure 6-15. A lower drain bias results in a better efficiency, but of course a lower output power.

The measurement at the nominal bias point has been repeated on the other 2 function samples. Figure 6-16 shows that the performance of the 3 samples is very comparable.

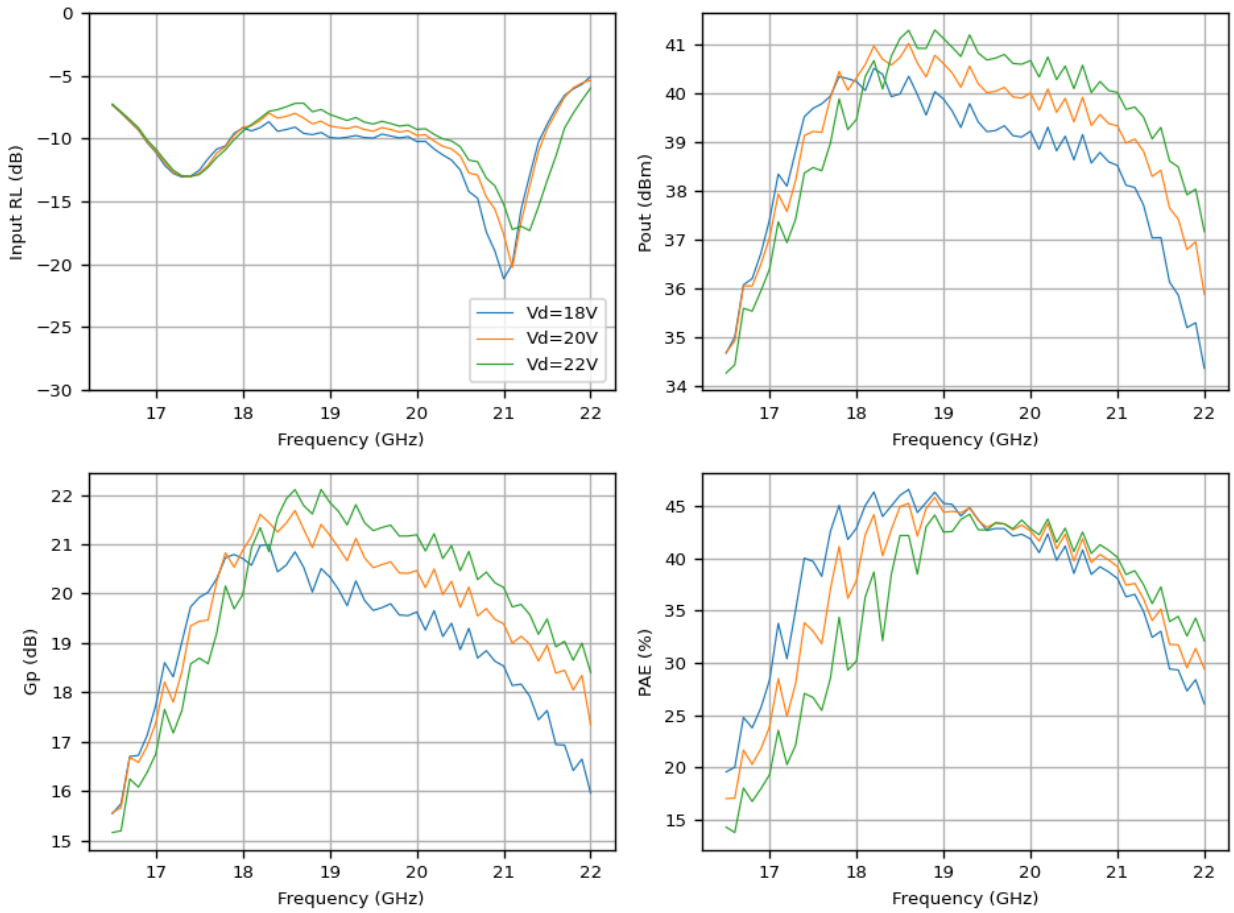


Figure 6-15 : Measured frequency sweep for a source power of 20 dBm, versus drain bias voltage at the nominal gate bias, 25degC, sample R2C1.

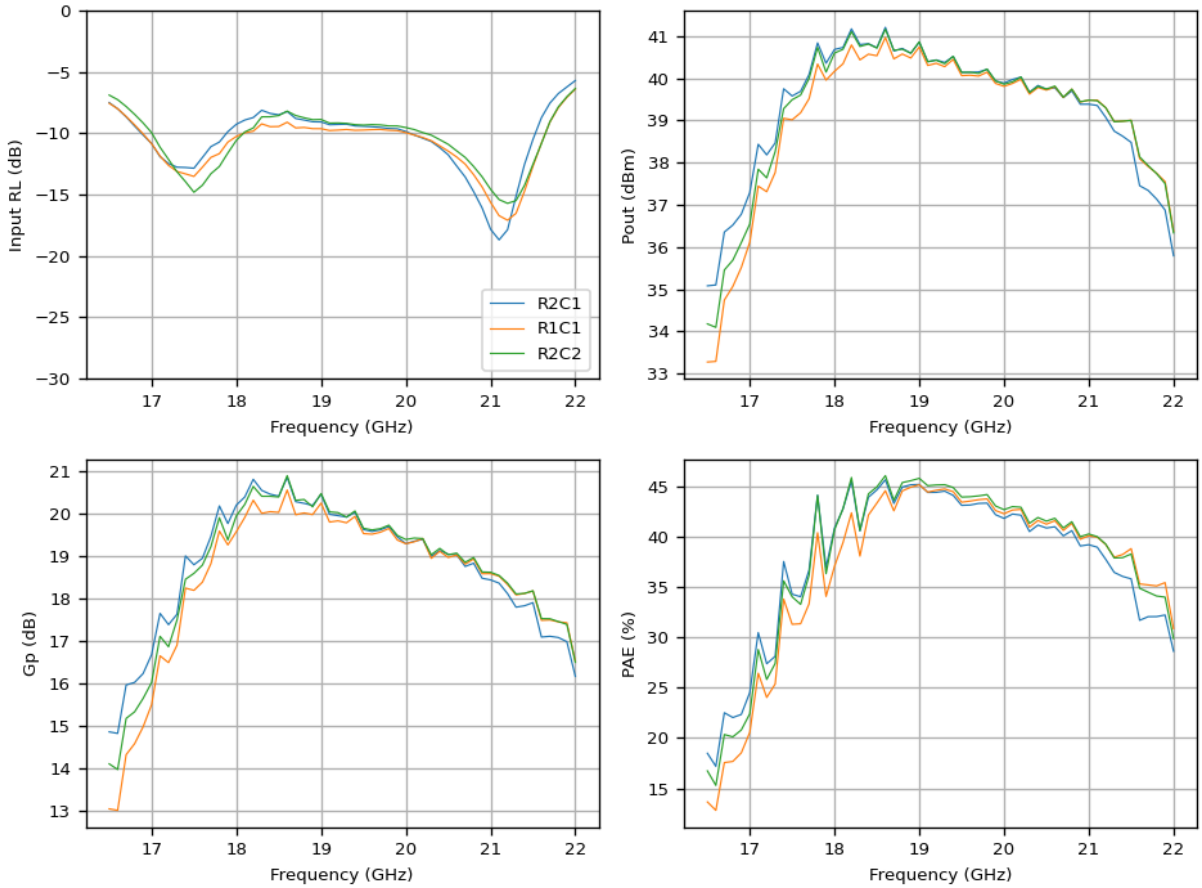


Figure 6-16 : Frequency sweep for all samples at a source power of 21 dBm, at the nominal quiescent bias current of 140 mA and 20V, 25degC.

Figure 6-17 shows a comparison between the measured performance under nominal bias conditions at 20 dBm source power versus the large-signal simulation results. As seen before, the performance at the low side of the frequency band is lagging behind. In the middle of the band the performance is as expected.

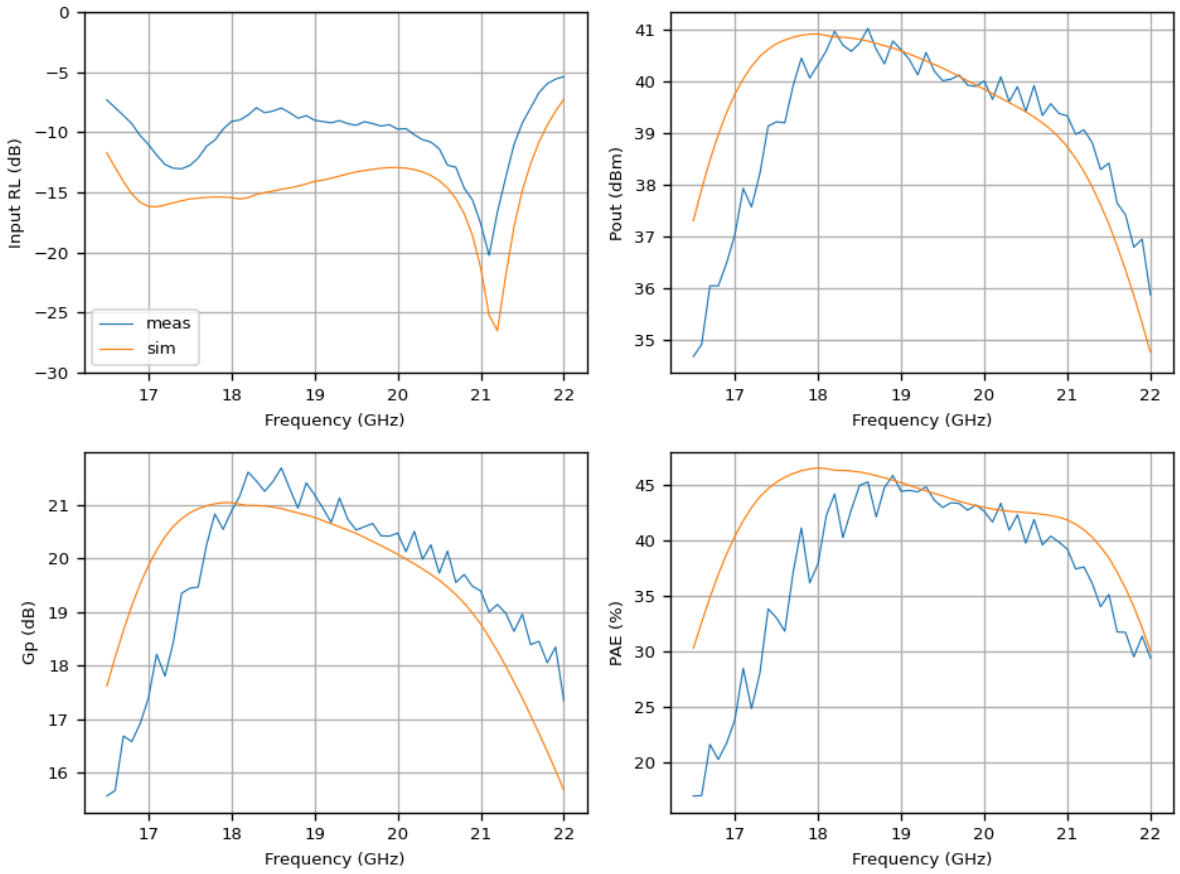


Figure 6-17 : Comparison of the measured and simulated CW frequency sweep for a source power of 20 dBm, at the nominal quiescent bias current of 140 mA and 20V, 25degC, sample R2C1.

Power-frequency sweep measurement at 80degC

The specified maximum MMIC backside temperature is 80degC. Therefore measurements have been performed at a wafer chuck temperature of 80degC. The actual MMIC backside temperature will be slightly higher due to the thermal resistance of the CuMo carrier and silver sinter die attach. A comparison between the room temperature performance and measurement at 80degC is shown in Figure 6-18. Gain, output power and efficiency performance is slightly reduced due to the increased temperature.

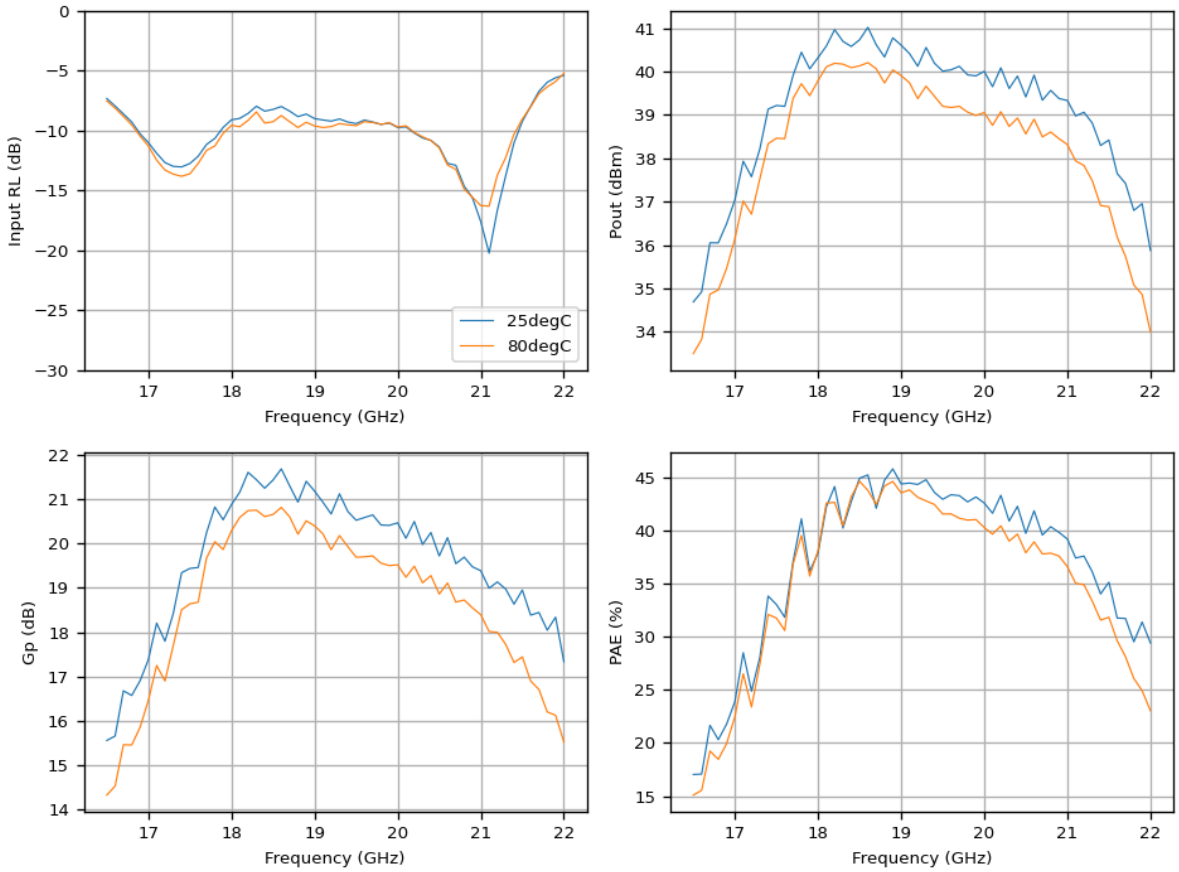


Figure 6-18 : Comparison of measured frequency sweep at 25degC and 80degC, at 20dBm source power for the nominal gate bias (-3.15V) at 20V, 25degC, sample R2C1.

Measurement of the 2nd harmonic

Figure 6-19 shows the fundamental and 2nd harmonic output power of each individual output including the calculated harmonic suppression for each output. Figure 6-20 shows the combined differential output performance. The 2nd harmonic rejection is around 50 dBc, while for the individual outputs this value is approximately ranging from 30 to 45 dBc.

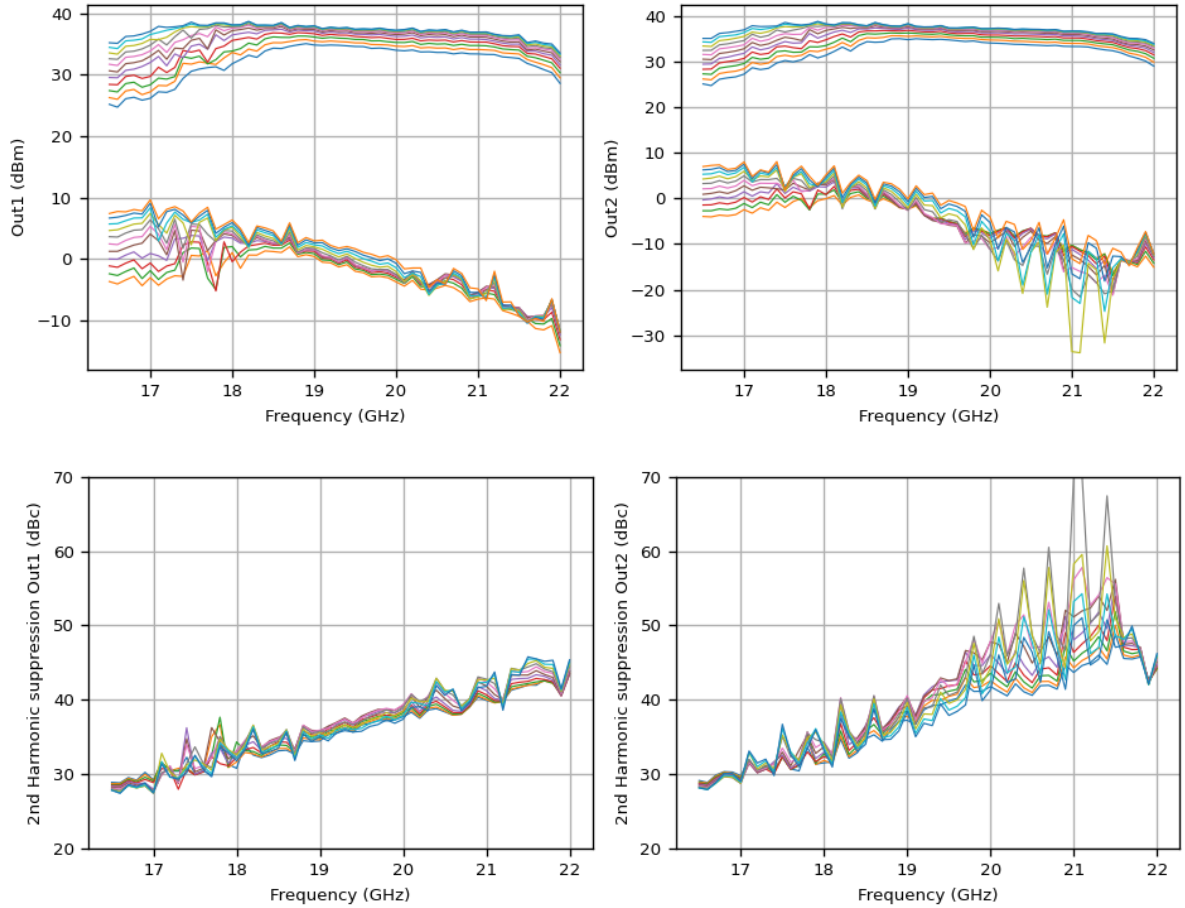


Figure 6-19 : CW power-frequency sweep for a source power of 15-25 dBm (1 dB step), at the nominal quiescent bias current of 140 mA and 20V, 25degC, sample R2C1, showing the fundamental and 2nd harmonic of the 2 outputs.

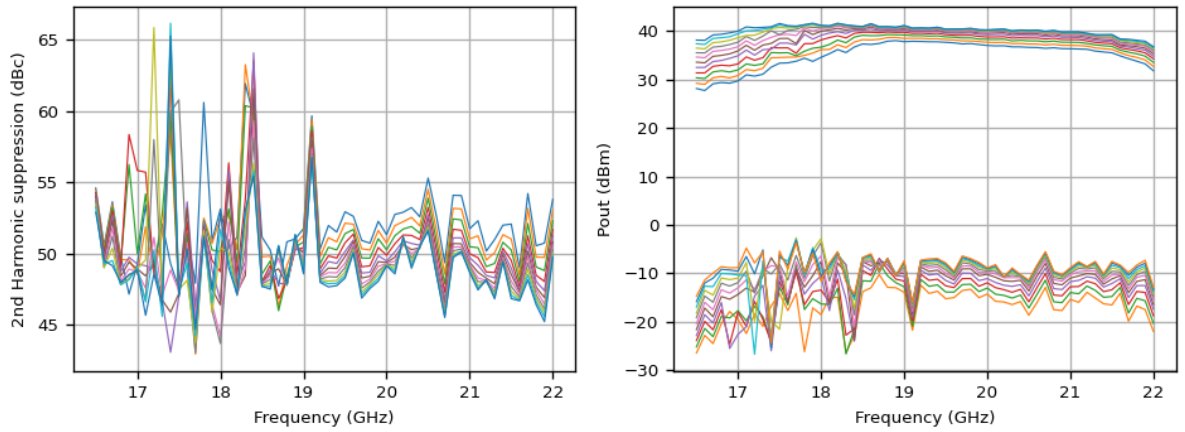


Figure 6-20 CW power-frequency sweep for a source power of 15-25 dBm (1 dB step), at the nominal quiescent bias current of 140 mA and 20V, 25degC, sample R2C1, showing the 2nd harmonic suppression and differential output power of the fundamental and 2nd harmonic.

Power sweep measurements

To check the linearity performance, power sweeps have been performed at 19 GHz for different gate bias values, the measurements are shown in Figure 6-21 and simulations are shown in Figure 6-22. Also the phase compression of the insertion phase is shown. Depending on the gate bias setting the gain compression and phase compression will change. The measurement results show the same behaviour as obtained from simulations.

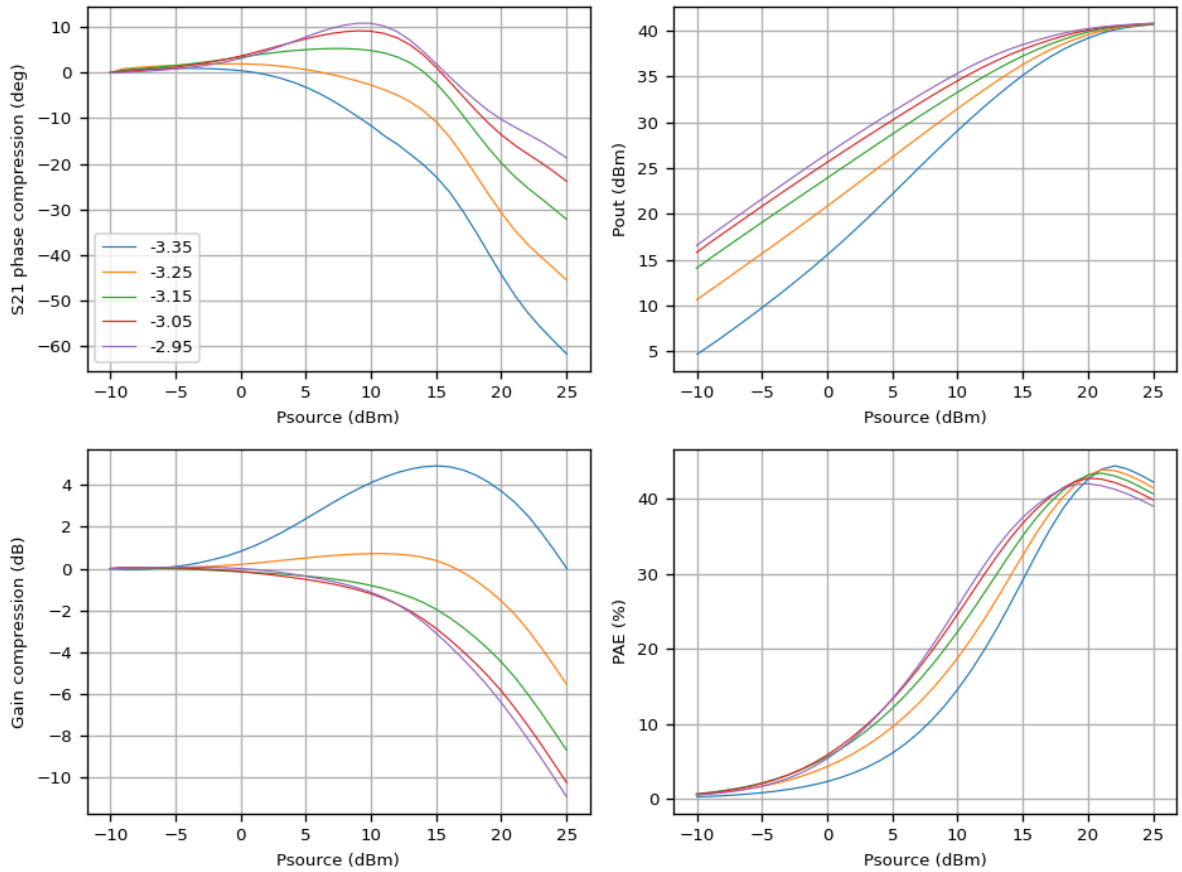


Figure 6-21 Power sweep measurements at 19 GHz versus gate bias at 20V, 80degC, sample R2C1.

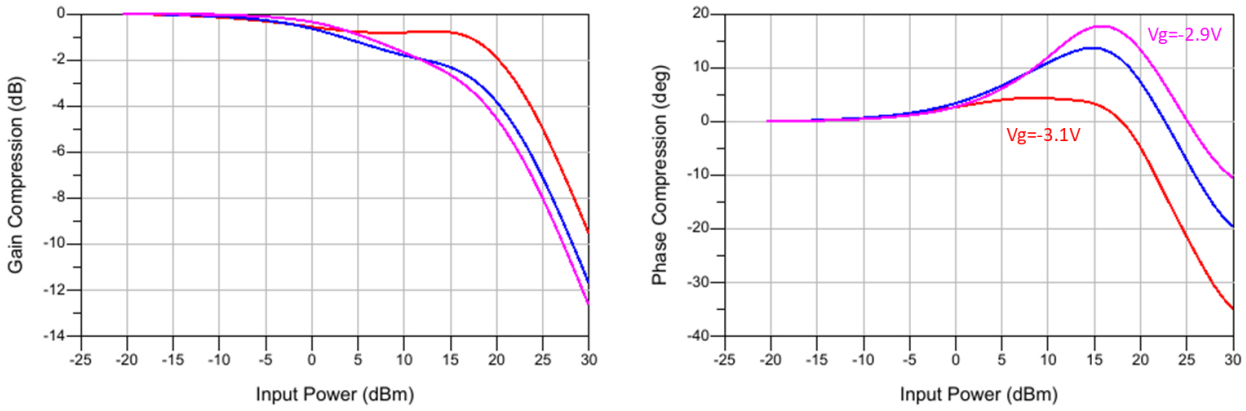


Figure 6-22 : Simulated power sweep at 18.8 GHz, Vd=20V, Ta=80°C, for Vg=-3.1 to -2.9 V.

A number of measurements have been performed with different gate biases for stage1 and stage2, to see the effect on the phase and gain compression and the results can be seen in Figure 6-23. Changing Vg1 has little effect on the phase compression, but a large impact on the gain compression.

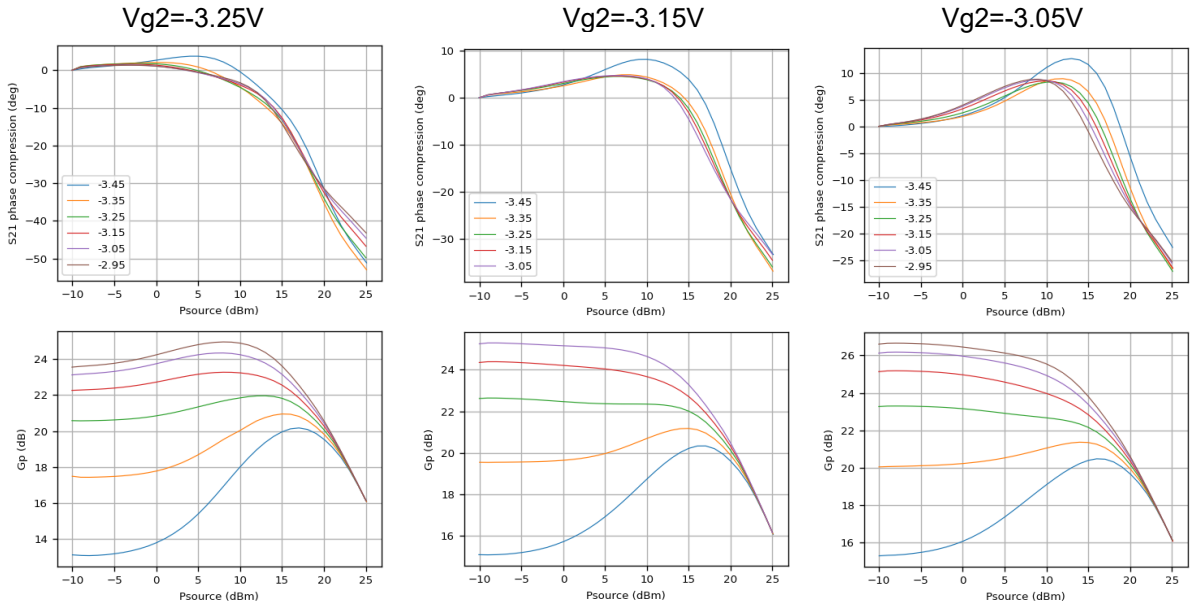


Figure 6-23 : Power sweeps at 19 GHz for different Vg1, Vg2 combinations at Vd=20V, 80degC, sample R2C1.

A bias point at Vg1=-3.29V and Vg2=-3.05V has been selected to perform power sweep measurement for the NPR calculations. Figure 6-24 shows the final power sweep measurements at the selected bias point, at three different frequencies, as input for the IMAL calculations.

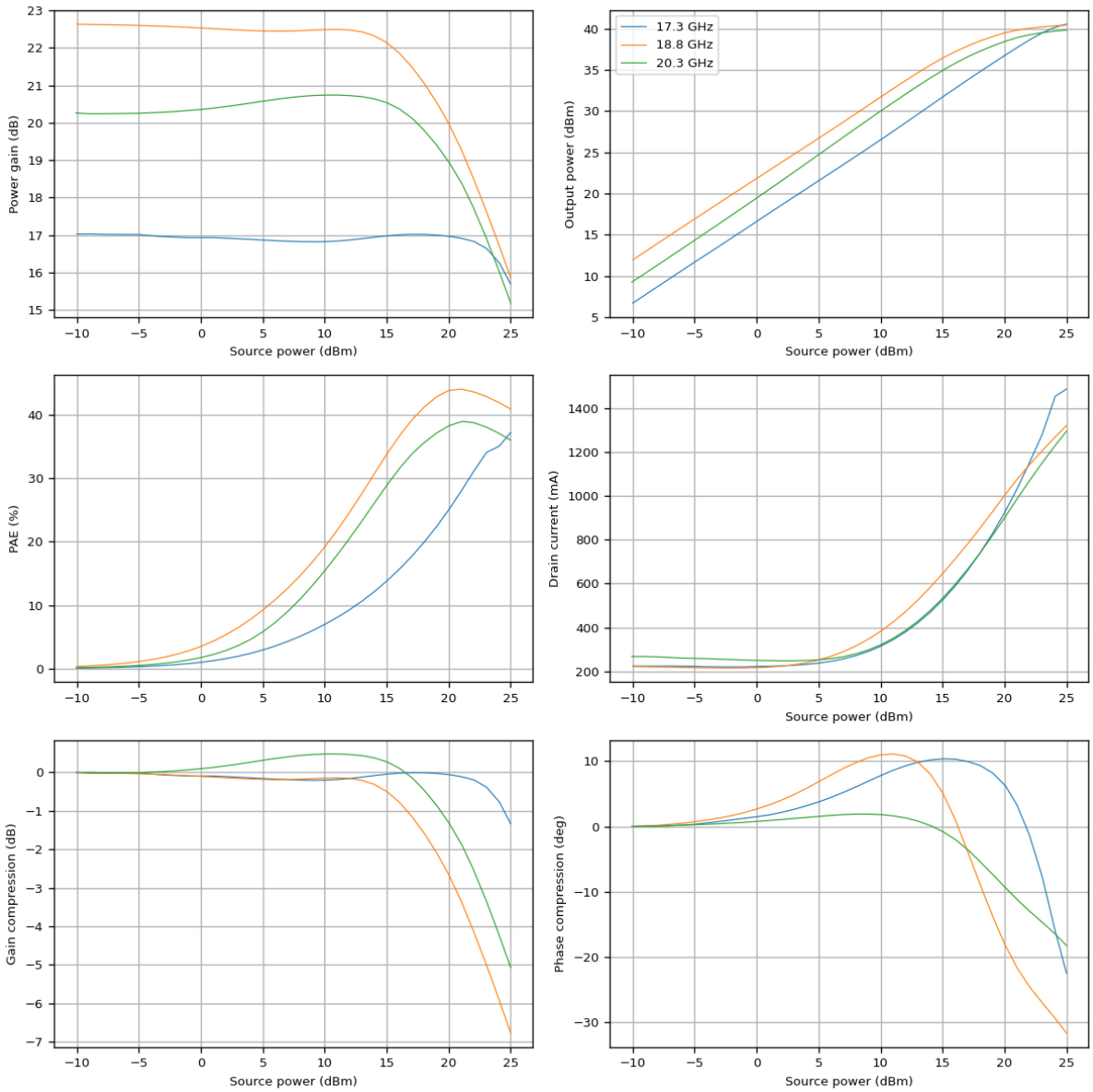


Figure 6-24 : Power sweep measurements at 80°C, at three frequencies, showing also the gain and phase compression for the combined differential output, as input for the IMAL calculations.

6.1.7. Linearity IMAL calculations 80degC

The measured differential output power, gain, phase and DC power dissipation have been used as input for IMAL calculations to obtain the performance at 15dB NPR, at 80degC. The results are shown in Figure 6-25 and summarized in Table 1. The figure also show the NPR calculated for each individual output of the differential HPA. In case there is some unbalance between the two outputs, the NPR of the combined differential output is the average of the two individual NPR levels. There is no NPR improvement due to combining the differential output signals.

The NPR performance based on simulated data is shown in Table 5-12 for comparison. As expected from the measurement results the performance at the low side of the band is lower than simulated, but for the middle and high part of the band the PAE performance shows good agreement, although the output power is lower than expected by approximately 1 dBm.

Table 1 : IMAL results at 15 dB NPR from measured power sweeps at 17.3, 18.8 and 20.3 GHz, for Vd=20V, Vg1=-3.29V, Vg2=-3.05V, Ta=80°C.

Frequency (GHz)	Pout (dBm)	PAE (%)	Pdc (W)
17.3	35.2	22.8	14.2
18.8	35.1	30.4	10.6
20.3	36.5	33.0	9.0

Table 2 : IMAL results at 15 dB NPR from ADS power sweep simulations at 17.3, 18.8 and 20.3 GHz, for Vd=20V, Vg=-3.1V, Ta=80°C.

Frequency (GHz)	Pout (dBm)	PAE (%)	Pdc (W)
17.3	37.74	34.99	16.7
18.8	37.68	32.32	17.9
20.3	37.50	32.86	16.6

Figure 6-25 : IMAL calculations based on power sweep measurements at 3 frequencies.

6.1.8. HPA measurements compliancy and conclusions

A differential output K-band (17.3 - 20.2 GHz) power amplifier has been designed in the GH15 GaN MMIC technology of UMS. After processing UMS has performed on-wafer small-signal S-parameter measurements of the HPAs. 23 out of 33 samples (~70%) were functional. The diced samples have been shipped to TNO and four samples have been mounted on a metal carrier for large signal measurements. These measurements have shown that the design has shifted upward in frequency, resulting in reduced performance at the lower side of the targeted frequency band. Above 18.5 GHz the measured output power and efficiency are according to simulation, but over the full frequency band the performance is lower than specified, as shown in Table 5-13. The performance at 15 dB NPR has been calculated using the IMAL software, based on power sweep measurement data, as agreed with ESA. The differential operation of the HPA has a clear advantage in lowering the 2nd harmonic output level, but does not help to improve the linearity.

Table 3 : Measured HPA MMIC performance compliancy with specifications and comparison with simulation.

Parameter	Specification	Simulation at 80°C	Measurement at 80°C	Compliant
Frequency range	17.3 – 20.2 GHz			By design
Input Return Loss	> 15 dB	> 14.5 dB	> 9 dB	No
Output power @ 15dB NPR	> 35 dBm	> 36.7 dBm	> 35.1	Yes
PAE @ 15 dB NPR	> 35%	> 32%	> 22.8 > 30.4 from 18.8-20.3 GHz	No **
DC power consumption	< 14.3 W	< 17.5 W	< 14.2	---*
Linear gain	> 20 dB	> 21 dB	> 20 dB	Yes
2nd Harmonics	-30 dBc	-50 dBc	-50 dBc	Yes
Temperature (MMIC backside)	20°C – 80°C			By design
Maximum junction temperature [1]	160°C	< 148°C	Not measured	

* DC power consumption is for information purposes only and not part of the compliancy matrix.
** Though the ambitious spec PAE@15dB NPR remained at 35% it has been reported at every stage the actual performance will be approximately 32%.

6.2. DRIFT Demonstrator Assembly and Integration

This section shall detail the DRIFT assembly and integration demonstrator in full. Figure 6-26 shows a CAD side view of the DRIFT demonstrator, for illustration purposes. In Figure 6-27 you can the assembled demonstrator for comparison.

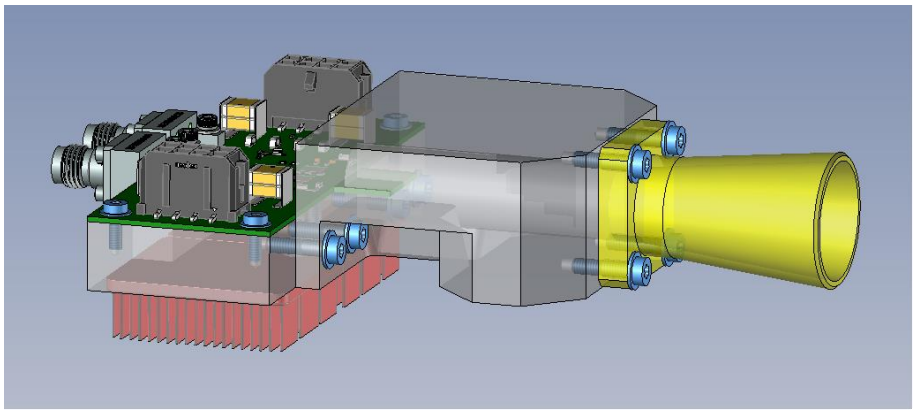


Figure 6-26DRIFT Demonstrator CAD top side view.

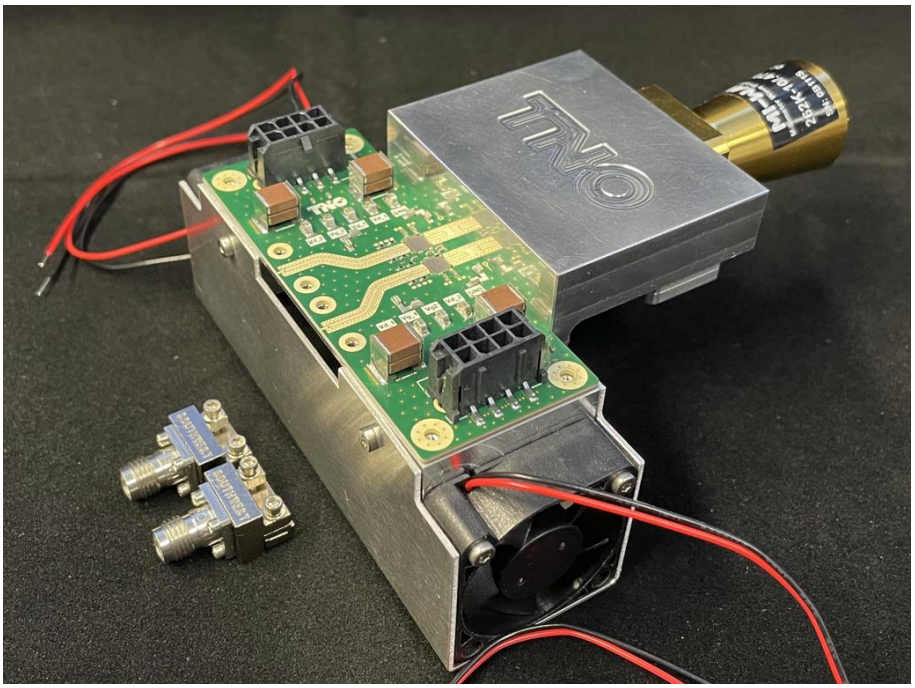


Figure 6-27 DRIFT Demonstrator Assembled and Integrated.

Please note in Figure 6-27 the heatsinks are inside the fan housing and can't be seen in this image. In addition Figure 6-27 clear shows all the demonstrator features such as: Assembled Demonstrator PCB, PCB mounting structure complete with heatsink fans, the waveguide structure and horn waveguide.

6.2.1. DRIFT Demonstrator PCB and PCB Mounting Structure

In Figure 6-28 the DRIFT PCB's can be seen, these where manufactured at Eurocircuits based in Belgium. The RF PCB technology is RO4350B on a 4 layer stackup. Layer 1, the top layer, is only used for RF microstrip routing and layer 2 as ground. Layer 3 is used for routing the DC connections and layer 4 is ground. All PCB designs are manufactured in a panel and will be manufactured from the same batch. The exposed metal for the passive components and bonding pads have been finished in Ag. The PCB has 4 mounting holes located in each corn for mounting to the PCB mounting structure

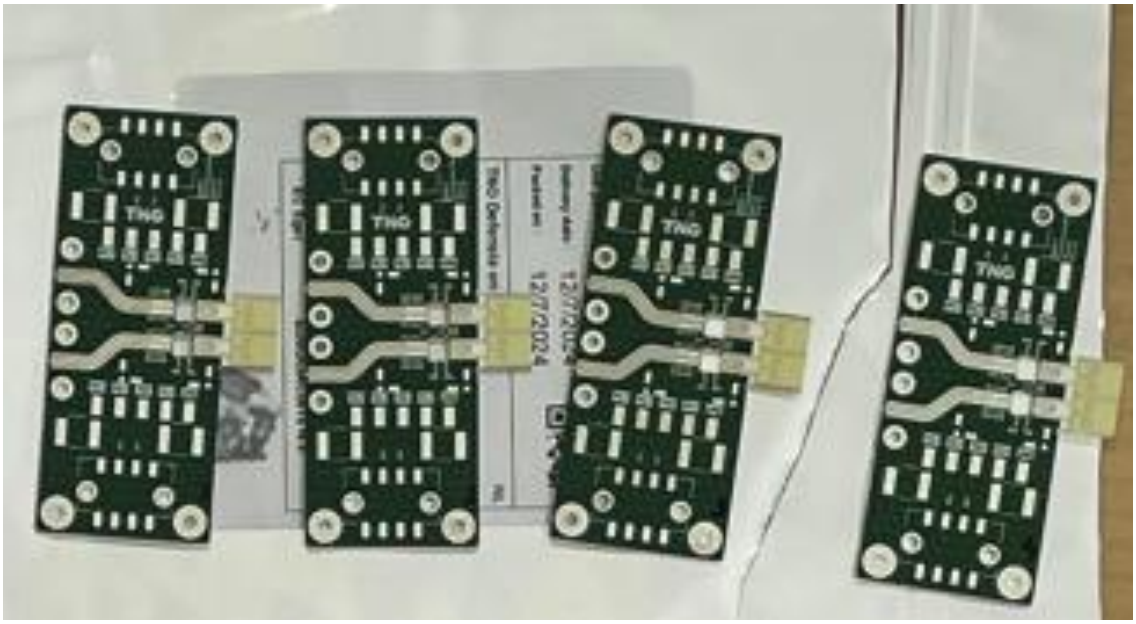


Figure 6-28 The DRIFT manufactured PCB boards.

In Figure 6-29 shows the DRIFT PCB mounting structure with an assembled MMIC mount module.

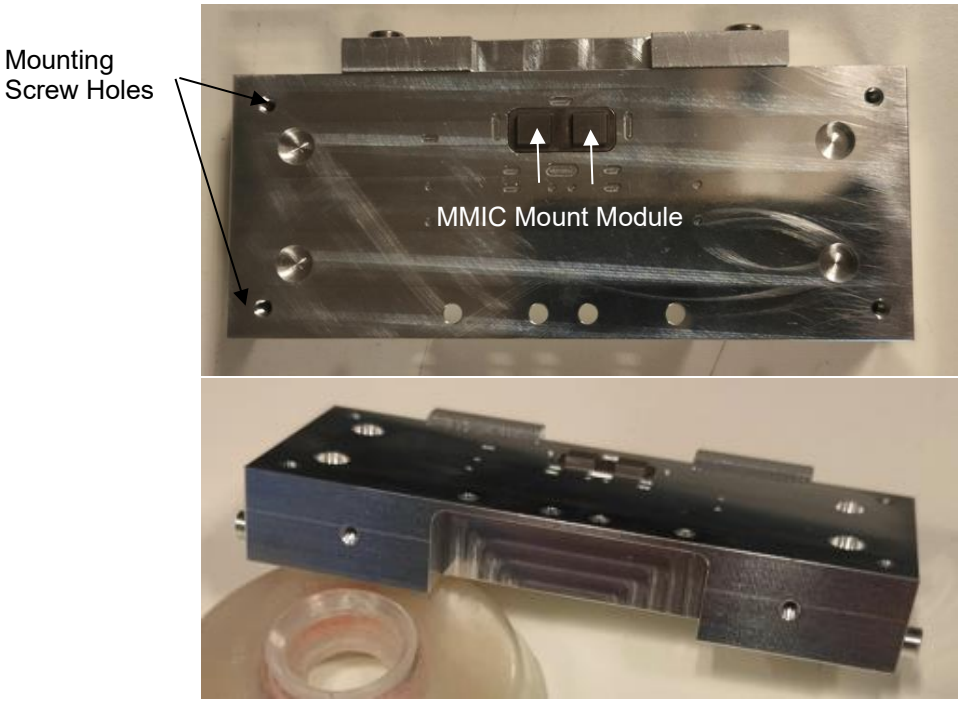


Figure 6-29 DRIFT PCB mounted structure with assembled MMIC mount module.

The PCB mounted structure is milled out of a single piece of Aluminium and the MMIC mount module is made out of piece of CuW and it protrudes the PCB mounting structure. The MMIC mount module is the platform for the MMIC dies and these algin with the PCB cavities.

Figure 6-30 Fully assembly PCB mounted structure with MMIC mount module and heatsink housing, fans and heatsink.

Figure 6-30 shows the fully assembly PCB mounted structure with MMIC mount module and heatsink housing, fans and heatsink. Please note the heatsinks are inside the heatsink fan housing. The heat sink fans and housing the attached to the PCB mount structure with screws. The heatsink uses thermally conductive adhesive to be stook on the back side of the PCB mounted structure.

6.2.2. PCB Assembled

The DRIFT demonstrator PCB has been assembled at TNO by hand as all the components are passive components and no smaller than 402. The components included are: DC connector, Capacitors, feedline filter and DC probe connectors. The DRIFT assembled demonstrator PCB can be seen in Figure 6-31. The solder used is lead free solder.

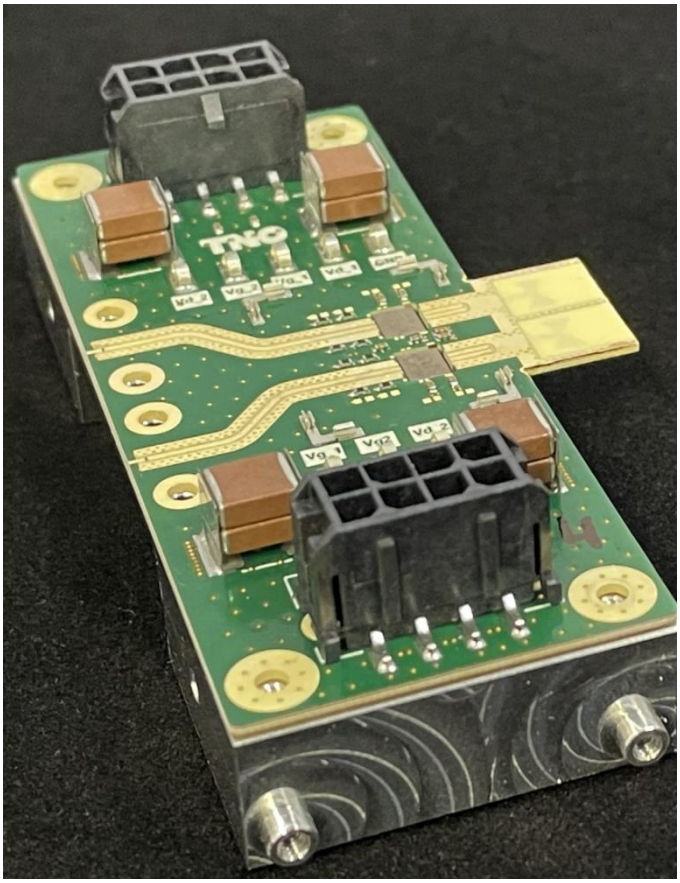


Figure 6-31 DRIFT Assembled Demonstrator PCB.

6.2.3. PCB MMIC and Die-Cap Attach

Figure 6-32 details the DRIFT MMIC and Die Attach and wire bonding. The MMICs and Die-Caps are attached to the MMIC mounting module using Ag epoxy. As you can see there 2 MMICs and 16 Die-Caps in total for a DRIFT demonstrator assembly. The RF input and output connections are double bonded to lower the bondwire inductance.

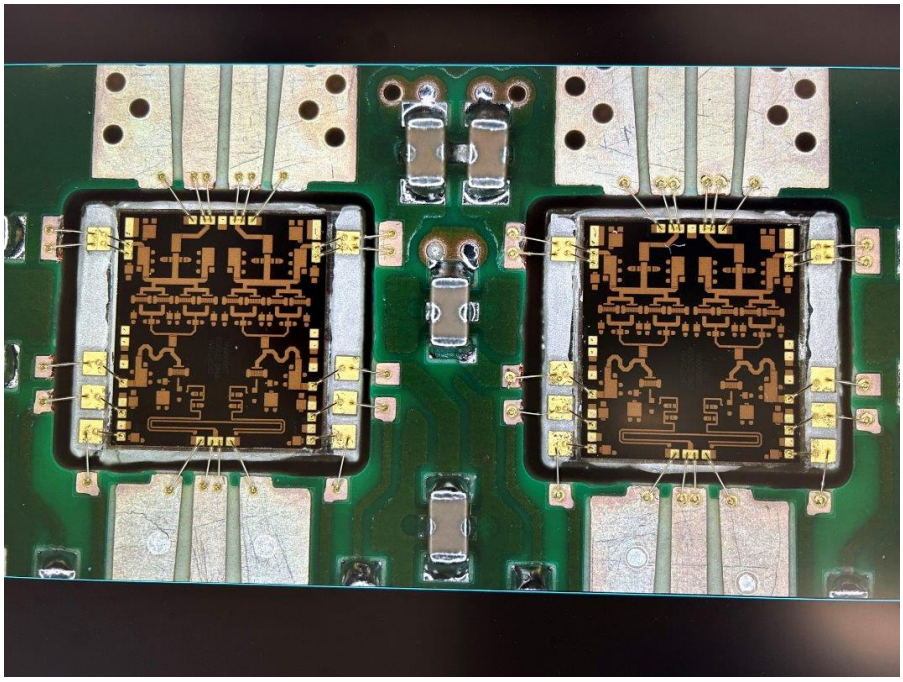


Figure 6-32 DRIFT MMIC and Die-Cap attach and wire bonding.

Each DC connection has a single bondwire from the PCB to the Die-Cap and then Die-Cap to MMIC. Apart from the HPA's 2nd stage (I.e. the HPA's output stage) where they are double bonded because of the increased current load.

Figure 6-33 DRIFT Demonstrator.

Figure 6-33 shows the full DRIFT demonstrator which consists of: assembled PCB with MMIC and Die-Caps attached and wire bonded, PCB mounting structure, MMIC mounting module, waveguide, horn and RF southwest connectors.

6.2.4. Waveguide

The DRIFT waveguide is manufactured using spark erosion to remove the aluminum to form the waveguide design. To create the septum and the waveguide exciter openings special spark erosion tools have been made, which can be seen in Figure 6-34.

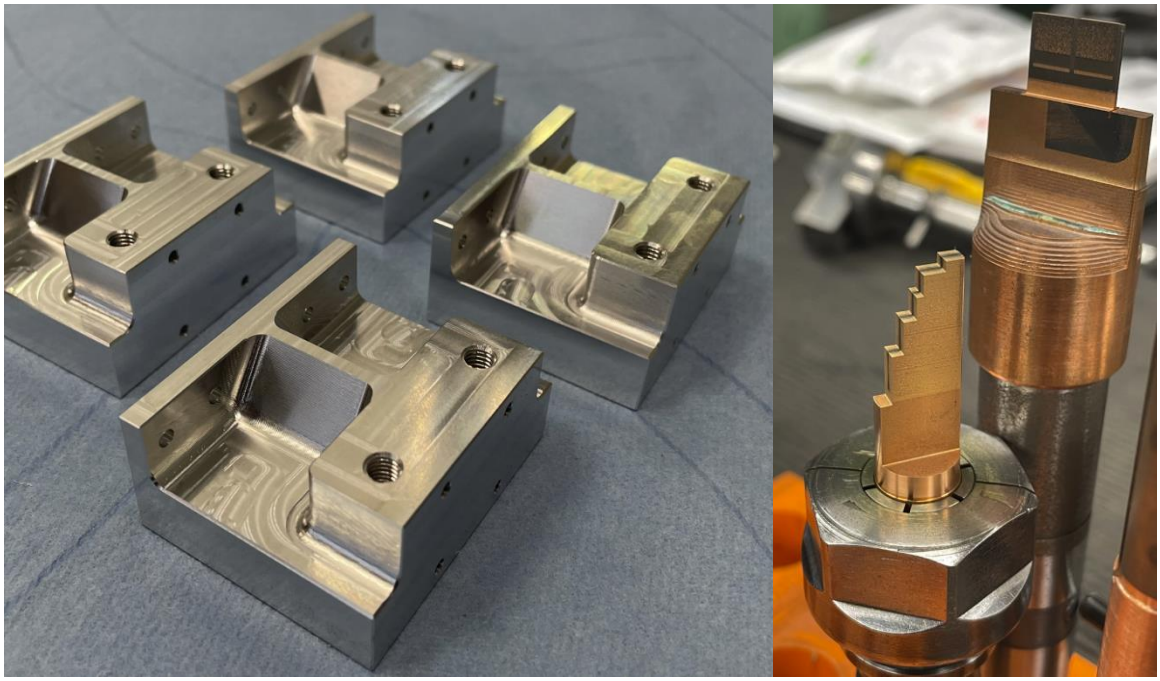


Figure 6-34 DRIFT waveguide initial structures (left), and tooling structures (electrodes) (right) to erode the septum and waveguide exciter from the initial structures.

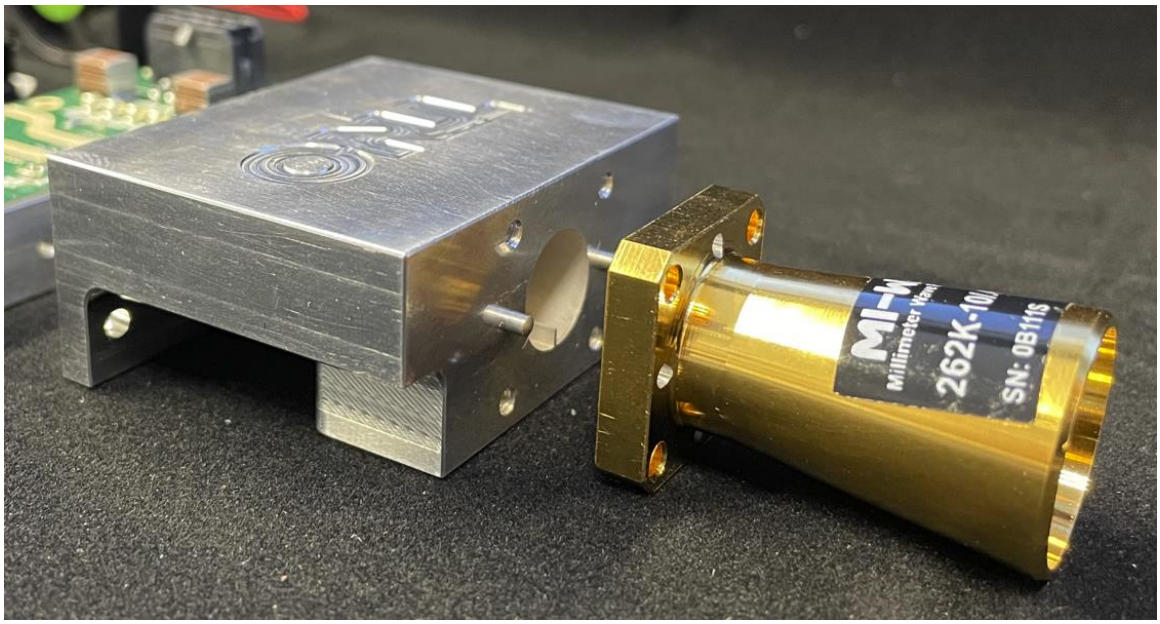


Figure 6-35 DRIFT waveguide viewed from the horn connection side.

Figure 6-35 shows a side/front view of the waveguide, manufactured using the spark erosion method. As you can clearly see there are 4 mounting screws and 2 alignment pins used for the horn assembly.

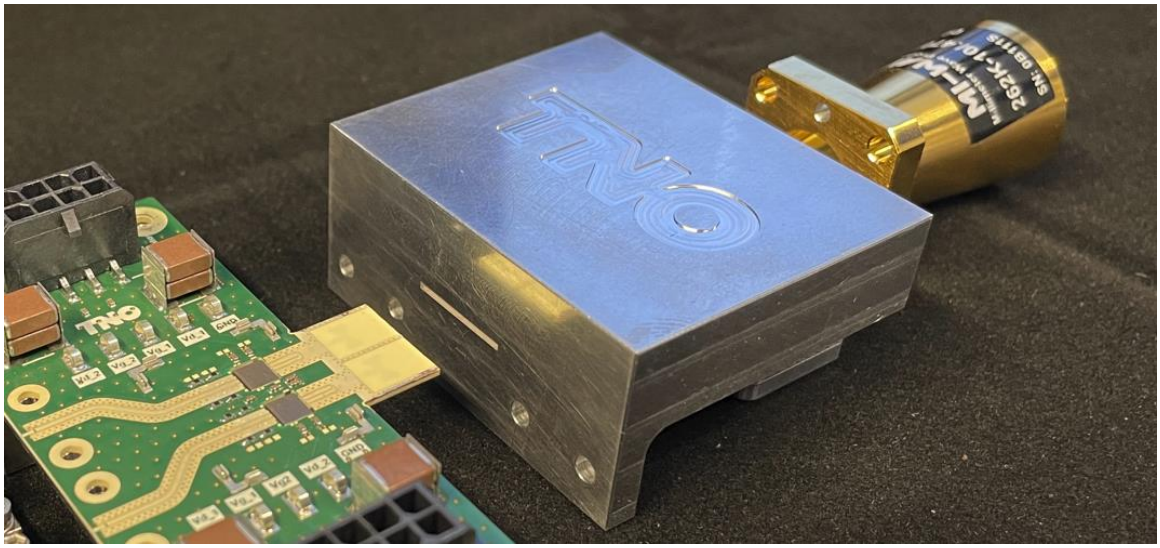


Figure 6-36 DRIFT waveguide viewed from the waveguide exciter side.

Figure 6-36 shows the waveguide as seen from the waveguide exciter. The demonstrator PCB is connected to the waveguide by pushing the PCB antennas into the waveguide slot and then secured by 4 mounting screws that fastens the waveguide to the PCB mounting structure.

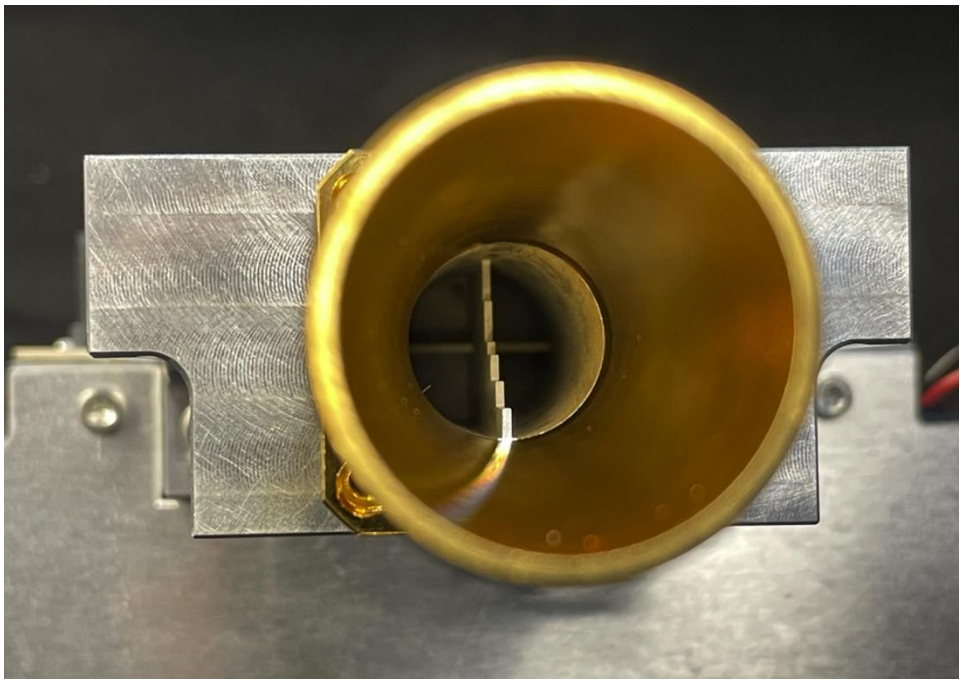


Figure 6-37 DRIFT waveguide front view looking into the waveguide and septum.

Figure 6-37 shows the front view of the waveguide looking into the septum. At the very back of the waveguide perpendicular to the septum you can see the waveguide exciter.

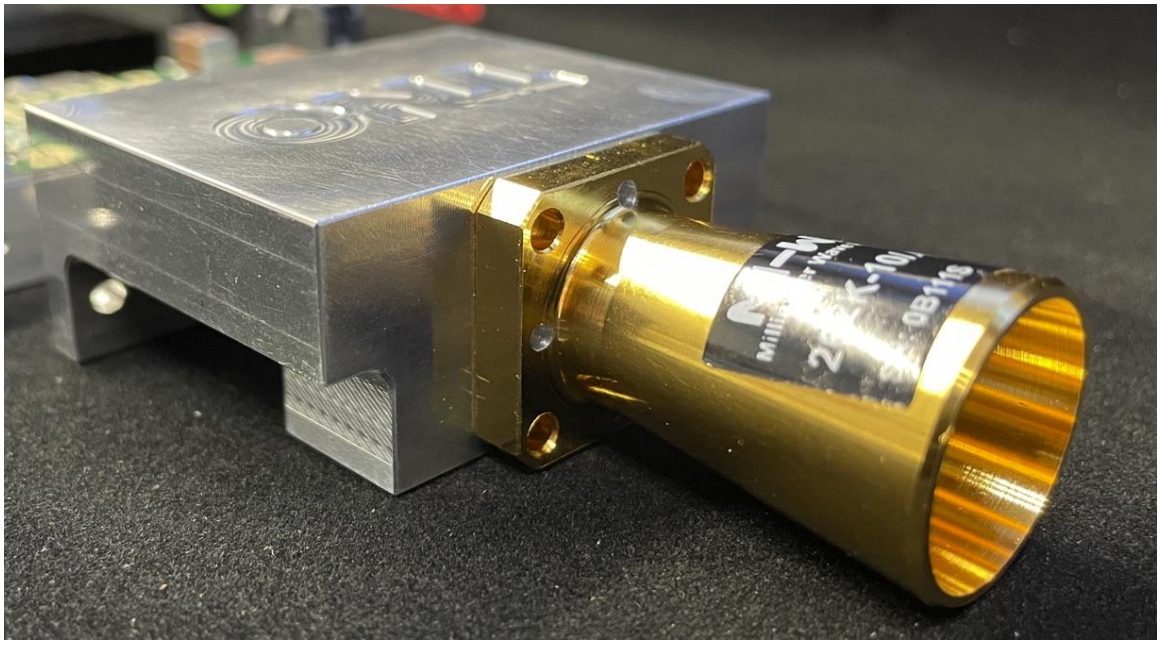


Figure 6-38 DRIFT waveguide and horn assembled.

Figure 6-38 shows the waveguide and the horn assembled via the 4 fixing screws and using the 2 alignment pins.

6.2.5. Fully assembled demonstrator

Figure 6-39 shows the DRIFT demonstrator as laid out by its component parts. The assembled PCB is connected to the PCB mounting structure and the waveguide and horn are also assembled. The heatsink, heatsink fans and housing are to the left of the assembled PCB and the southwest connectors in the middle.

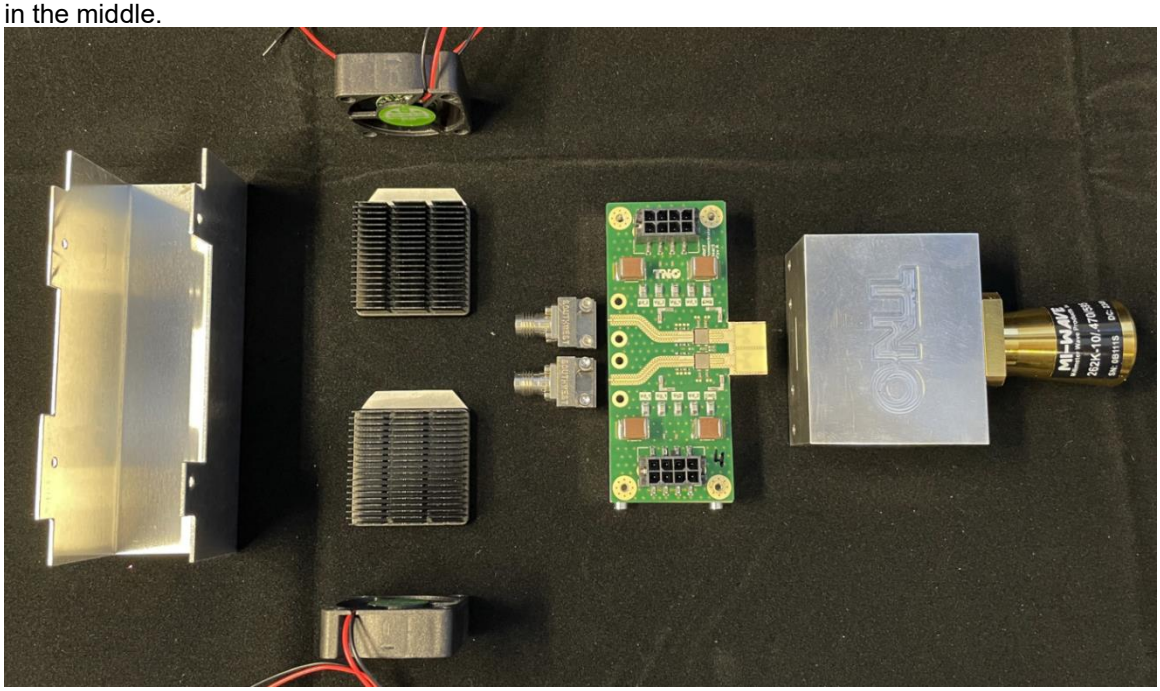


Figure 6-39 DRIFT full demonstrator layed out as component parts.

6.3. Passive Antenna Demonstrator Assembly

In this section the assembly of the passive antenna demonstrator structure is detailed. The component parts are (as seen in Figure 6-40):

1. Southwest RF connectors
2. PCB mounting structure
3. Passive waveguide exciter PCB
4. Waveguide
5. Horn

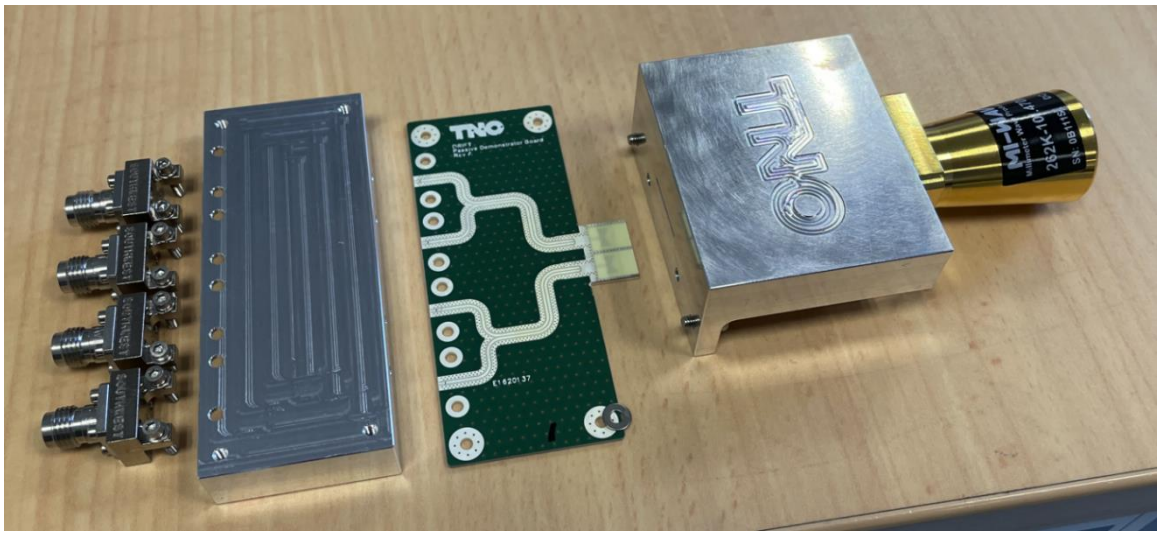


Figure 6-40 DRIFT passive antenna demonstrator components

The passive waveguide exciter PCB is mounted to the PCB mounting structure to provide structural base for the test setup. The PCB is fixed to the mounting structure via 4 mounting screws and the 4 southwest RF connectors. The waveguide exciter is then slotted into the waveguide itself and fixed to each other by 4 mounting screws and guided by 2 alignment pins as seen in Figure 6-41.

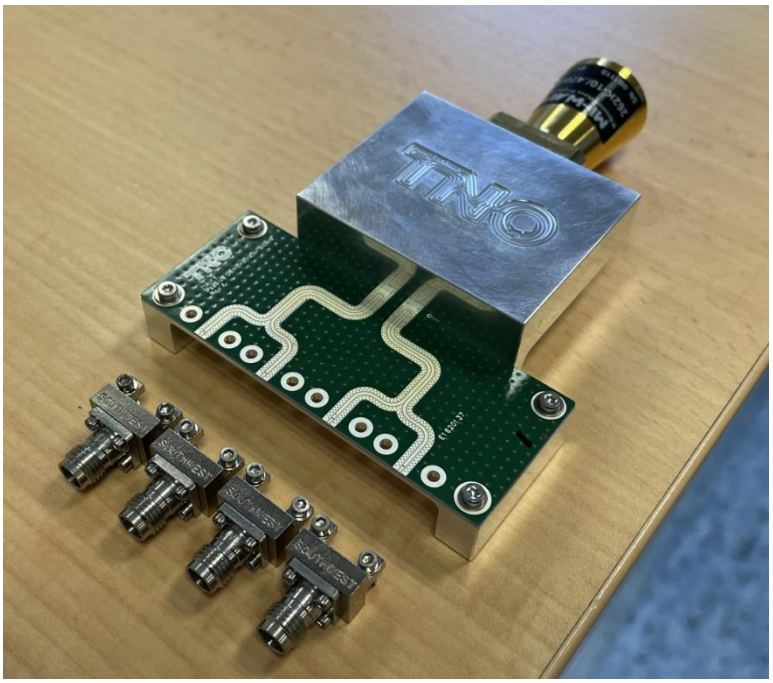


Figure 6-41 DRIFT assembled passive antenna demonstrator.

Figure 6-42 shows a zoomed view of the waveguide exciters slotted into the waveguide and how flush the PCB is to the wall of the waveguide.

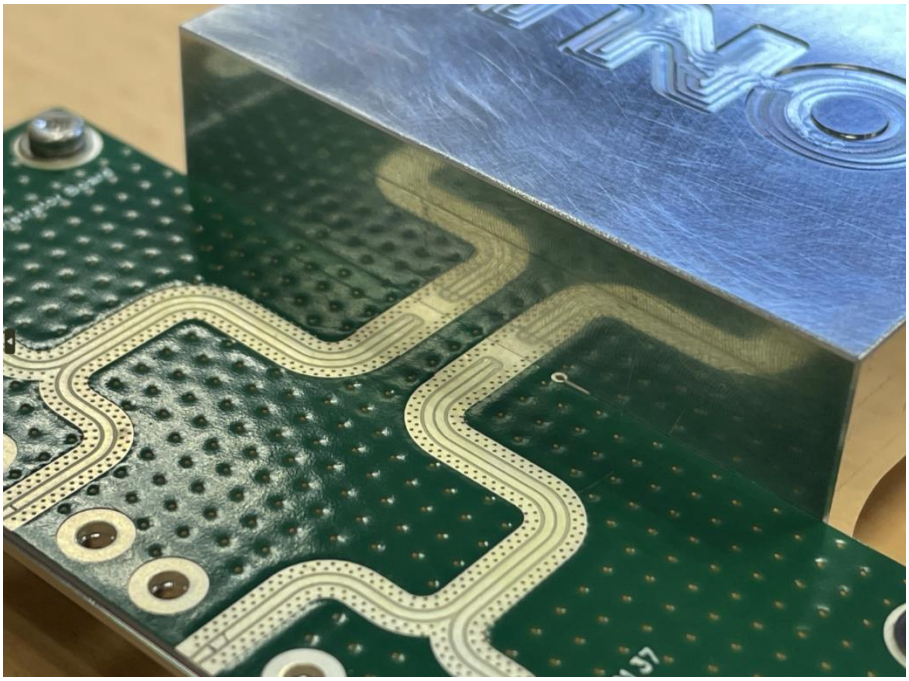


Figure 6-42 close up view of the waveguide exciters slotted into the waveguide.

The passive antenna demonstrator is mounted onto the test mount which consists of a metal support at the rear and on the front the absorbing material. In the rear the southwest RF connectors are exposed and a balun connected to one side and 50 ohm loads to the other as seen in Figure 6-43.

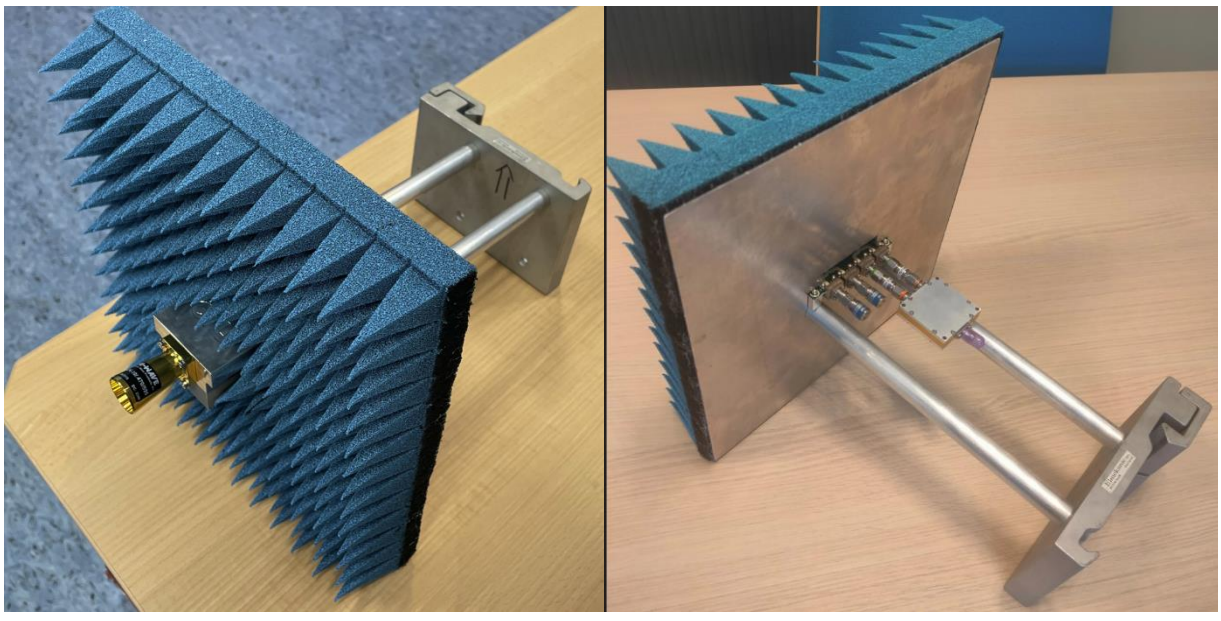


Figure 6-43 DRIFT fully assembled passive antenna demonstrator.

6.4. Test Review Board (TRB)

The final measurements to be performed relate to the passive antenna demonstrator. It is required to test the polarisation performance and validate it against simulation.

6.4.1. Axial Ratio measurement

In order to proof the developed concept the actual passive radiating frontend must be build and tested. Indeed the test structure includes two dipole exciters that feed the waveguide, the septum polariser and the horn antenna. Each dipole is fed on the PCB through two coaxial connectors (2.4mm Southwest). In Figure 5-128 the setup is shown in which the structure is measured with use of a 4-port network analyser.

In Figure 6-44 the results of the measurement are shown. It can be seen that the isolation between the two input ports is quite high. Together with the low level of reflection, and the presented low loss nature of the transition earlier in the report this indicates that the structure is very efficient in radiating the power given at its input. Note that the measured and simulated cross-talk performances are very comparable.

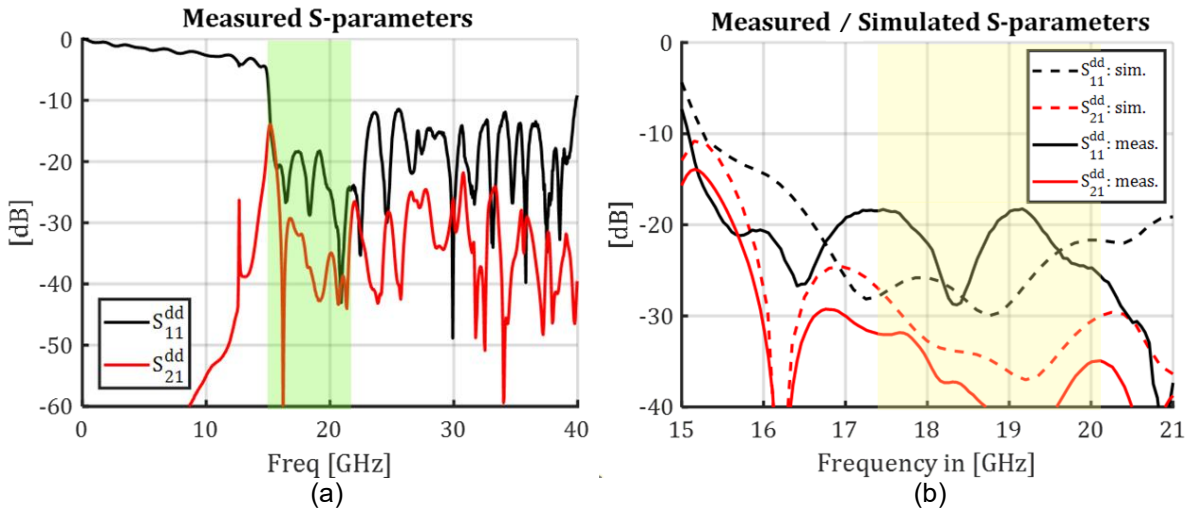


Figure 6-44: Measured reflection seen at a single differential input port and cross-talk between the two input ports. (a) Full band results with the green shade indicating the frequency band of interest, and (b) zooming in on that spectral range.

To assess the efficiency of the complete passive frontend measurement of the gain is quite suitable. These measurements however have not been performed due to time and budgetary constraints. An effort is made to determine its value by simulation. Results of this are shown in Figure 6-45. The graph presents gain levels for different structural portions of the frontend. As can be expected the gain will reduce when more material is added. The study starts with the horn section only and its gain is evaluated through the calculation of the total radiated power and referencing it to the power given at the input. To determine the loss in the horn itself it is referenced to its PEC (perfect electric conducting, i.e. lossless) version. For the horn only a loss is estimated to be 0.05dB. With this knowledge the losses of the exciter + septum polariser can be estimated and they are shown in Figure 6-46. Note that at 18GHzthe loss of the septum + horn exceed that of the horn alone and it reflects the fact that commercial simulation tools in general have difficulty in calculating the losses in highly conductive structures.

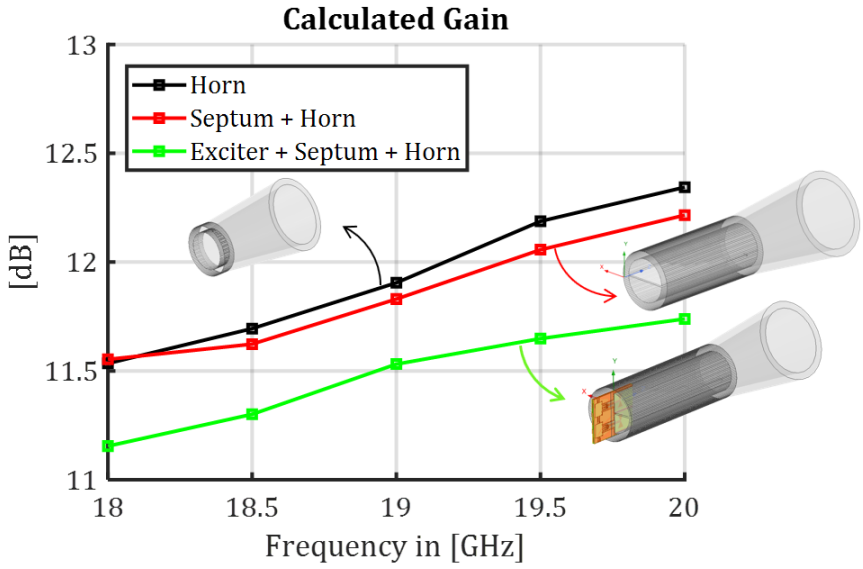
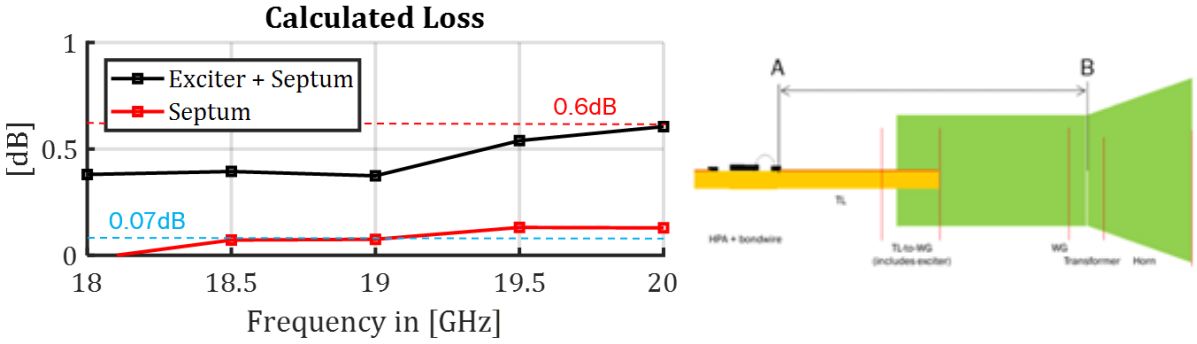


Figure 6-45: Calculated gain levels for the different structural portions of the passive frontend.

The calculated losses in Figure 6-46a refer to the portion A-B of the structure in Figure 6-46b. With the loss of the horn section being L_h = 0.05dB, the loss of the bonding pads + bond wire being L_{bw} = 0.03dB the total maximum loss of the passive radiating frontend by calculation is 0.03 + 0.6 + 0.05 = 0.68dB. Note that these are losses based on RO4350B, and if RO3003 were used this would be 0.58dB. Loss based on measurement for the dipole transition is 0.4dB (see Figure 5-100**Error! Reference source not found.**b), complementing this with L_{bw}, L_h and the maximum simulated loss for the septum polariser (see Figure 6-46a) Ls = 0.12dB a total maximum loss of L_{bw} + 0.4 + L_s + L_h = 0.6dB is calculated. In case of RO3003 this would be 0.5dB of loss. For both cases the loss is compliant with specification.



(b)

Figure 6-46: (a) Losses calculated from the results shown in Figure 6-45. (b) Losses in the graph relate to the part from A to B.

6.4.2. Waveguide performance: Polarisation

For the validation of the Axial Ratio (AR) the passive radiating frontend has been measured with respect to its polarisation capability. The test structure was measured in the nearfield test facility of TNO. To validate the axial ratio two measurement procedures were performed, i.e.: one in the Near Field (NF) and one in the Far Field (FF). During the NF measurement both the co- and cross-polarised (meaning both orthogonal linear polarisations) radiation is measured and recorded. From these results the processing software (NSI-MI), which is part of the test facility, can derive the circular polarisation performance. To make sure that the processed AR from the NF-data is correct also a FF measurement is performed which should produce the same result. In case of the FF measurement the linearly polarised probe antenna is placed in the far-field of the horn antenna and on the centre line of the horn (thus in its radiation beam maximum). In this position the probe is rotated about its own axis (which thus is lined up with that of the horn antenna) to find the maximum and subsequently the minimum of the

radiated field. This corresponds to the major and minor axes respectively as shown in the diagram of Figure 6-49.

The results found from the measurement can be seen in Figure 6-49b, and clearly reports an AR performance < 0.58 dB over the whole frequency band of interest. Furthermore, the AR values readily produced by the NF measurement processing software excellently line up with those calculated using FF measurement data. Although the trend of the measurements does not fully follow those of simulation, the magnitude is excellent. As it is the purpose of the radiating frontend to efficiently generate circular polarisation using two linearly polarised exciters the AR should be very pure. At the same time it must be able to create the two orthogonal senses of the polarisation. To prove this the FF data has been further scrutinised.

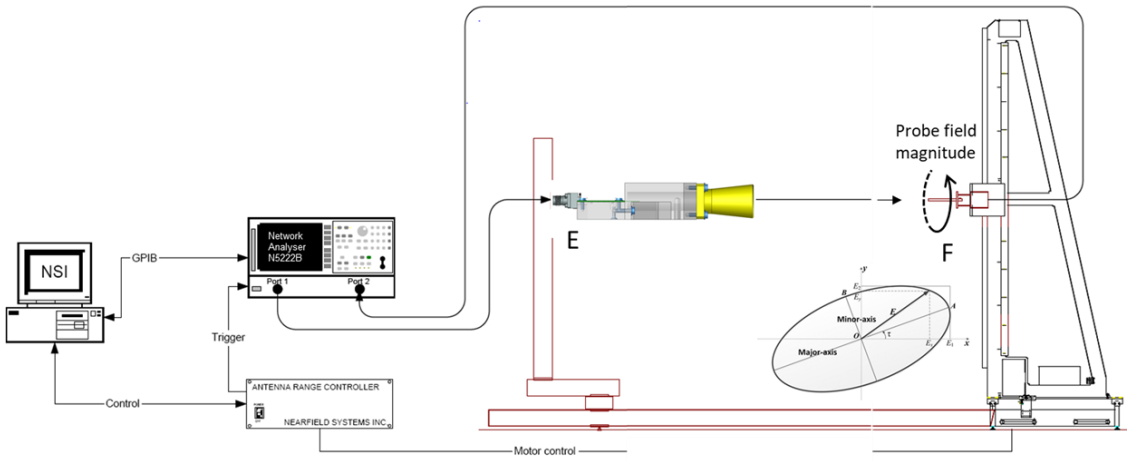


Figure 6-47: Passive radiating frontend for validating the AR performance schematically shown in a near-field test setup.

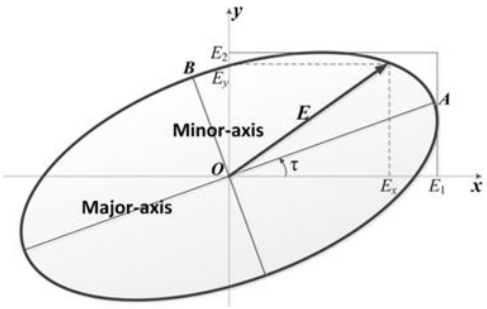
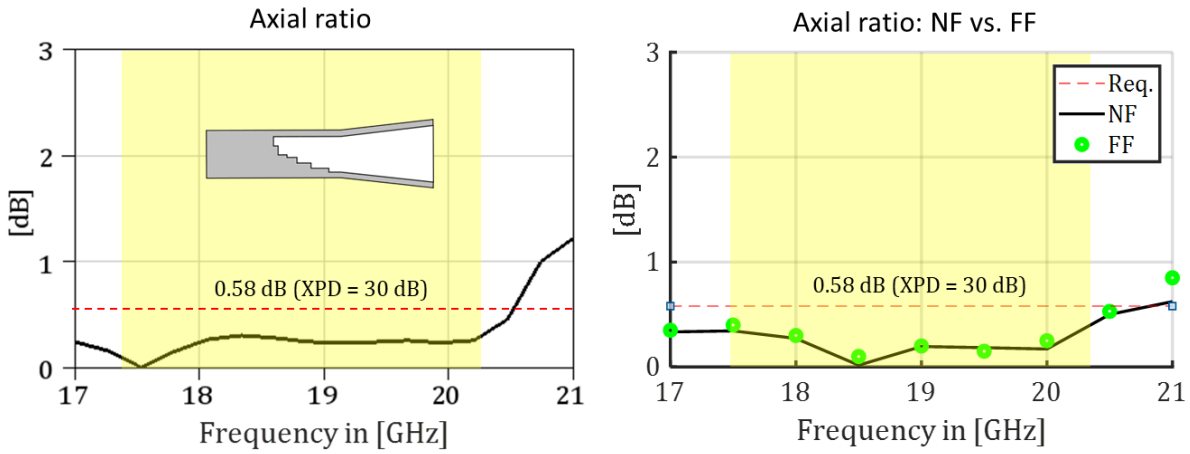


Figure 6-48: Polarisation ellipse, minor and major axis [21].



(a) (b)

Figure 6-49: (a) DRIFT simulated AR. (b) DRIFT NF and FF AR measurement results.

From the NF measurement data also the sense of the polarisation can be determined. Since the test results for the AR indicate that the polarisation is nearly circular, it is allowed to prove the sense by simply extracting the phase difference between the horizontal and vertical electric field components. For the cases where only one exciter is active while the other is terminated, these differences have been plotted in Figure 6-50a and b.

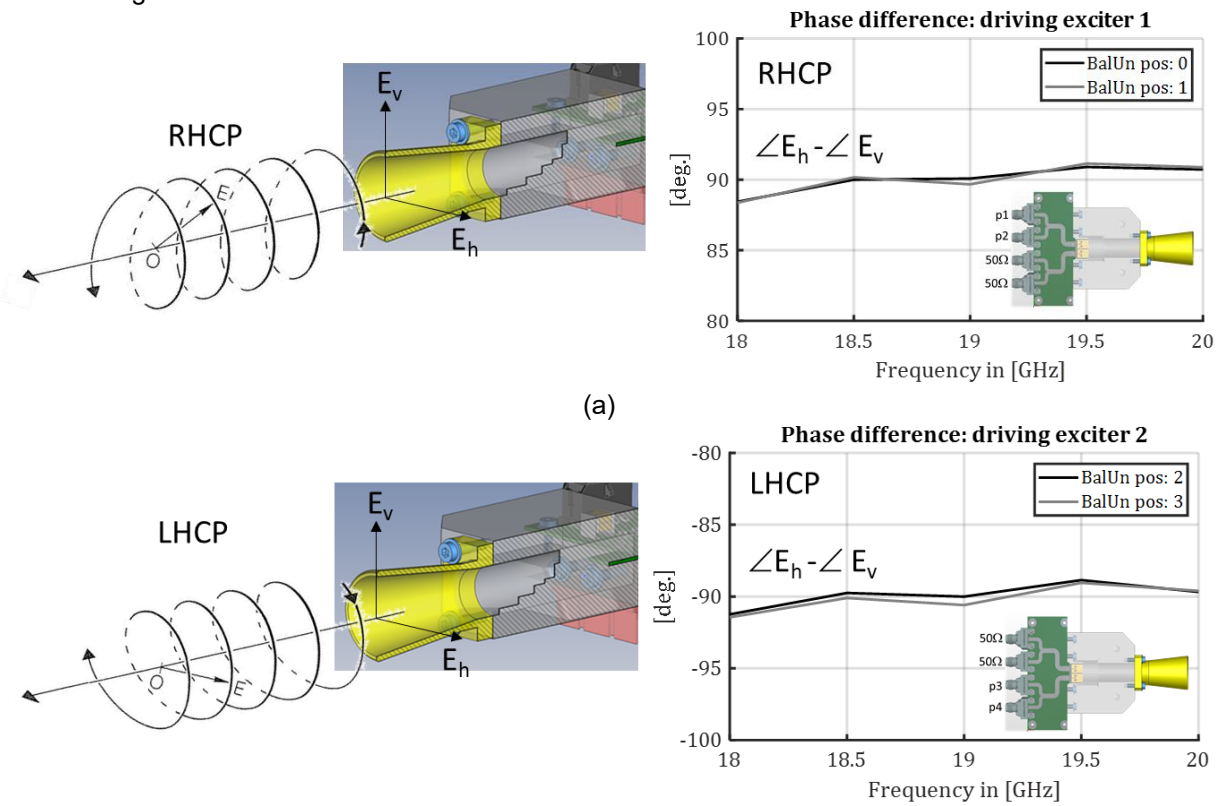


Figure 6-50: Measured phase differences between the horizontal (E_h), and vertical (E_v) electric field components measured under far-field conditions. Note that, under the condition of exciting only a single dipole while the other is terminated in 50Ω, the structure will generate either a +90deg. phase difference (exciter 1) between these principal electric field components or a -90deg. phase difference (exciter 2) between the principal electric field components.

As is the purpose of the excitation concept, each exciter will generate an outward propagating field polarised opposite to that generated by the other. Accompanying each phase difference plot in Figure 6-50 is a graphical representation showing the rotation of the propagating resultant electric field towards broadside away from the horn aperture. Note that the legend indicates explicitly which of the two exciters has been terminated and which is active. The 'BalUn pos' value in the legend indicates how the BalUn is connected to the pair of input connectors, and essentially means a change in polarity. In fact, the graphs show the invariance of the polarisation sense to this connection position.

For the graphs in Figure 6-50 only the in-band phase differences are shown. Only for one case a more extended frequency range has been measured, namely from 17 to 21GHz. Strictly speaking the open-ended waveguide probe with which the measurements have been performed is specified starting from 18GHz. This does however not mean it is useless at frequencies slightly below, especially if the performance to be tested regards the polarisation character. The related result is shown in Figure 6-51.

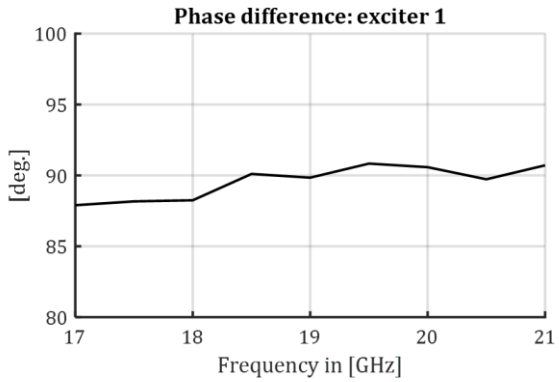


Figure 6-51: Phase difference measured across a more extended frequency range.

6.4.3. DRIFT Compliance Matrix

The differential HPA, waveguide feed and waveguide have all been measured and test results are summarised in the compliance matrix seen in Table 6.4. There are a number of non-compliance's, which are PAE at 15 dB NPR and the output power variation. All other specification points have been achieved and demonstrated by measurement.

The difficulty to meet the PAE at 15 dB NPR requirement has been communicated at the start of the project but was always maintained as an ambitious target to strive for. Compounding the PAE's non-compliance is the 600 MHz positive frequency shift, which shows the PAE at the 17.3 GHz at 22.8 %.

In addition, the HPA saturation performance is good, with an output power > 41 dBm, small signal gain > 20 dB and PAE > 41 %. Considering the operational frequency and device bandwidth this is an impressive result.

Table 6.4 DRIFT compliance matrix

ID	Parameter	Specification	Simulation at 80°C	Measurement at 80°C	Compliant
1.1	Frequency range	17.3 – 20.2 GHz			Yes; by design and measurement
1.2	HPA Output power @ 15dB NPR	> 35 dBm	> 36.7 dBm	> 35.1	Yes NPR measurement
1.3	PAE @ 15 dB NPR	> 35%	> 32%	> 22.8 > 30.4 from 18.8-20.3 GHz	No By HPA power sweep measurements**
1.4	Linear gain	> 20 dB	> 21 dB	> 20 dB	Yes; by SS and LS HPA measurements
1.5	Conducted NPR	15 dB	15 dB	15 dB	Yes; by measurement setup
1.6	Output Power Variation	0.5 dBpp	1 dBpp	1 dBpp	No By SS and LS HPA measurements
1.7	Antenna Gain	TBC dBi	11 dBi	N/A	Exciter + Septum + Horn simulation
1.8	Antenna Polarisation	Dual-circular pol.	Dual-circular pol.	Dual-circular pol.	By design – Septum By waveguide feed axial ratio measurement
1.9	Axial Ratio	< 0.58 dB		< 0.4 dB	Yes By waveguide feed axial ratio measurement
2.0	2nd Harmonics	-30 dBc	-50 dBc	-50 dBc	Yes By HPA LS Measurement
2.1	3rd Harmonics	N/A	N/A	N/A	Outside the range of the measurement equipment
2.2	Input and output Interface	Input TBD / WG Output	Input RF connector / Output WG	Input RF connector / Output WG	Yes By design
2.3	Temperature (MMIC backside)	20°C – 80°C			HPA measurements
2.4	Mass	< 300 g	N/A	189 g	Yes, by weighting

* DC power consumption is for information purposes only and not part of the compliancy matrix.
** Though the ambitious spec PAE@15dB NPR remained at 35% it has been reported at every stage the actual performance will be approximately 32%.
*** Weight of the waveguide is 81.1 g and the horn 12 g

7. DRIFT Conclusion

The DRIFT project has to the best of their ability, achieved its objectives of delivering a differential radiating front-end and in the process addressed some key challenges in the development of HPA high-efficiency and waveguide feed technology. Through innovative advancements in High Power Amplifier (HPA) design, waveguide transitions, and antenna elements, the project demonstrated the potential of differential architectures for Direct Radiating Array (DRA) antennas.

The DRIFT project has demonstrated a differential GaN HPA K-band (17.3 - 20.2 GHz) design optimised for efficiency, and linearity. The HPA measurements demonstrated a frequency shift of approximately 600 MHz, which has skewed the overall HPA bandwidth performance. The HPA resulted in a high PAE of 31 %, achieved > 35 dBm output power at 15 dB NPR and a linear gain > 20 dB at 80 degrees MMIC backside temperature. In addition the HPA realised a saturated output power > 41 dBm, PAE > 41% and linear gain > 20dB which is an impressive result. For an initial differential HPA design on UMS GH15-11, this is a good achievement. The differential operation of the HPA has a clear advantage in lowering the 2nd harmonic output level resulting in a 2nd harmonic suppression of > 50 dBc, but unfortunately this was not seen in the NPR (linearity) performance.

Additionally, the waveguide feed development had 2 setbacks: initial manufacturer poor performance and waveguide design too lossy. Though the waveguide feed had to be re-designs for an alternative manufacturer and a new waveguide manufacturing approach required. The DRIFT team have demonstrated two different waveguide feed designs with low loss < 0.6dB. The spark erosion manufacturing technique has shown that complex structures with tight tolerances can be made using this method. The waveguide and waveguide feed demonstration of both right- and left-hand circular polarisation show an axial ration < 0.58 dB, meeting the project's specification. The project has demonstrated the design and implementation of a septum polariser using spark erosion for waveguide polarisation is a viable option.

The successful validation of these components at TRL 4 marks an important step forward in advancing active DRA systems for Very High Throughput Satellites (VHTS). Looking ahead, the findings of this project pave the way for further development and scalability of differential front-end architectures. Future work may focus on increasing integration levels, addressing thermal management challenges, and transitioning to higher TRL levels to support full system deployment.

In conclusion, the DRIFT project provides a solid foundation for next-generation SATCOM technologies, demonstrating the feasibility of designing a differential radiating front-end. The benefits from an efficiency perspective are on par to that of single ended HPA design but the 2nd harmonic suppression of > 50 dBc is a clear advantage. The waveguide design and polariser demonstrated good isolation between right and left hand polarisation with an axial ratio < 0.58 dB. Spark erosion has the potential to make complex structures for high-performance satellite communications architectures.